Bits to Scalers - 2011

At the November 2010 Collaboration Meeting, the spin pwg discussed input bits for scalers for run-11. Best knowledge, at the time, was based on 8 functional 24-bit scalerboards.

Present best knowledge is 6 such boards, and further compromises thus need to be made, at least initially. Two 30 bit boards are on track to become available late February 2011.

Common sense dictates that reconfiguration of the RAT mapping during run-11 is kept to an absolute minimum.

For conventional reasons, the 24-bit scalerboards will be named 5, 6, 7, 8, 11, and 12 here. The 7-bit bunch-crossing counter will occupy bits 17-23 in each 24-bit board:

BX202IN	0	SCALERXX	17
BX202IN	1	SCALERXX	18
BX202IN	2	SCALERXX	19
BX202IN	3	SCALERXX	20
BX202IN	4	SCALERXX	21
BX202IN	5	SCALERXX	22
BX202IN	6	SCALERXX	23

A 24th scalerboard input will be served by run control.

Boards 11 and 12 will continue to serve monitoring of individual tiles in BBC-east and BBC-west, respectively:

BBCEIN	0	SCALERB0	0
BBCEIN	1	SCALERB0	1
BBCEIN	2	SCALERB0	2
BBCEIN	3	SCALERB0	3
BBCEIN	4	SCALERB0	4
BBCEIN	5	SCALERB0	5
BBCEIN	6	SCALERB0	6
BBCEIN	7	SCALERB0	7
BBCEIN	8	SCALERB0	8
BBCEIN	9	SCALERB0	9
BBCEIN	10	SCALERB0	10
BBCEIN	11	SCALERB0	11
BBCEIN	12	SCALERB0	12
BBCEIN	13	SCALERB0	13
BBCEIN	15	SCALERB0	14

BBCEIN	15	SCALERB0	15	
VT201IN	0	SCALERB0	16	) BBC small-tile TAC diff. in window

and

BBCWIN	0	SCALERC0	0	
BBCWIN	1	SCALERC0	1	
BBCWIN	2	SCALERC0	2	
BBCWIN	3	SCALERC0	3	
BBCWIN	4	SCALERC0	4	
BBCWIN	5	SCALERC0	5	
BBCWIN	6	SCALERC0	6	
BBCWIN	7	SCALERC0	7	
BBCWIN	8	SCALERC0	8	
BBCWIN	9	SCALERC0	9	
BBCWIN	10	SCALERC0	10	
BBCWIN	11	SCALERC0	11	
BBCWIN	12	SCALERC0	12	
BBCWIN	13	SCALERC0	13	
BBCWIN	15	SCALERC0	14	
BBCWIN	15	SCALERC0	15	
VT201IN	0	SCALERC0	16	

respectively. These boards will both sample 10 minute intervals for each run.

Boards 5 and 6 serve luminosity measurement purposes. They will have identical inputs. Board 5 integrates for the duration of each run. Board 6 will sample 10 minute intervals.

VT201IN	1	SCALER50	0	)
VT201IN	2	SCALER50	1	) BBC small-tile TAC diff.
VT201IN	3	SCALER50	2	)
VT201IN	4	SCALER50	3	)
VT201IN	7	SCALER50	4	)
VT201IN	8	SCALER50	5	) ZDC TAC difference
VT201IN	9	SCALER50	6	)
VT201IN	10	SCALER50	7	)
ZD101IN	10	SCALER50	8	) ZDC ADC-sum-E > th0
ZD101IN	11	SCALER50	9	) ZDC ADC-sum-W > th0
BB101IN	14	SCALER50	10	) BBC small ADC sum-E > th0
BB101IN	15	SCALER50	11	) BBC small ADC sum-W > th0

VT201IN	XX	SCALER50	12	to be defined from trigger list
VT201IN	XX	SCALER50	13	to be defined from trigger list + live
VT201IN	11	SCALER50	14	) VPD TAC in window
VT201IN	6	SCALER50	15	) ZDC TAC in window
VT201IN	0	SCALER50	16	) BBC small-tile TAC in window

Boards 7 and 8 will serve local polarimetry with the ZDC East and West, respectively.
Board 7:

'Z-SMD-E-H'	0	SCALER70	0	)
'Z-SMD-E-H'	1	SCALER70	1	)
'Z-SMD-E-H'	2	SCALER70	2	) ZDC-SMD highest slat (H,V)
'Z-SMD-E-V'	0	SCALER70	3	)
'Z-SMD-E-V'	1	SCALER70	4	)
'Z-SMD-E-V'	2	SCALER70	5	)
ZD101IN	0	SCALER70	6	)
ZD101IN	1	SCALER70	7	) ZDC Truncated ADC-sum-E
ZD101IN	2	SCALER70	8	)
ZD101IN	12	SCALER70	9	) ZDC Front-ADC-E > th0
ZD101IN	13	SCALER70	10	) ZDC Back-ADC-E > th0
ZD101IN	6	SCALER70	11	) ZDC Good-TAC-E
BBCEIN	3	SCALER70	12	)
BBCEIN	4	SCALER70	13	) BBC-E individual inner small tiles
BBCEIN	11	SCALER70	14	)
BBCEIN	12	SCALER70	15	)
VT201IN	0	SCALER70	16	) BBC small-tile TAC in window

and board 8:

'Z-SMD-W-H'	0	SCALER80	0	)
'Z-SMD-W-H'	1	SCALER80	1	)
'Z-SMD-W-H'	2	SCALER80	2	) ZDC-SMD highest slat (H,V)
'Z-SMD-W-V'	0	SCALER80	3	)
'Z-SMD-W-V'	1	SCALER80	4	)
'Z-SMD-W-V'	2	SCALER80	5	)
ZD101IN	3	SCALER80	6	)

ZD101IN	4	SCALER80	7	) ZDC Truncated ADC-sum-W
ZD101IN	5	SCALER80	8	)
ZD101IN	14	SCALER80	9	) ZDC Front-ADC-W > th0
ZD101IN	15	SCALER80	10	) ZDC Back-ADC-W > th0
ZD101IN	7	SCALER80	11	) ZDC Good-TAC-W
BBCWIN	3	SCALER80	12	)
BBCWIN	4	SCALER80	13	) BBC-W individual inner small tiles
BBCWIN	11	SCALER80	14	)
BBCWIN	12	SCALER80	15	)
VT201IN	0	SCALER80	16	) BBC small-tile TAC in window

These boards will integrate for the duration of each run.

Notes on boards 7 and 8: the above lists for ZDC-polarimetry are intended, initially, for commissioning and, subsequently, for faster optimization of the analyzing power than is possible with dedicated ZDC-trigger runs. On success, a number of bits may be freed up. It is even conceivable that a full board will be freed-up. These bits will then be allocated to luminosity measurements (in particular live-time, and 1-arm vs. 2-arm luminosity measurements).

Notes on boards 11 and 12: if run-9 observations of small BBC analyzing power at 500 GeV are confirmed, selected individual tiles from boards 11 and 12 can be interchanged so that both boards contain inputs from BBC-E and BBC-W.

Notes on boards 5 and 6: the inputs to boards 5 and 6 closely resemble the inputs used in runs 6 and 9 (200 GeV). High BBC multiplicities may make it beneficial to consider the VPD as an additional luminosity monitor. In this case VP101 bits 14 and 15 would need to be routed for corrections.

Would a scaler-board fail during the initial transverse running period, board 6 will become the spare. This will be revisited for the start of the longitudinal running period, or if/when board 7 or 8 are freed up following ZDC-polarimetry commissioning.

Oleksandr Grebenyuk or Ernst Sichtermann will be available at BNL to assist with commissioning until February 10 and February 14-22, afterwards as needed.

Commissioning of boards 7, 8 and 11, 12 presently has higher priority than 5 and 6.

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