Algorithms for TOF and MTD DSM Tree
RHIC 2015 p+p Run

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Change Log:

Date	Description
January 20, 2015	First version for the 2015 proton-proton run. The TF201 algorithm has been modified to make room in the output bitlist for trigger bits from the PP2PP system. The 6 TOFsector bits have been combined in pairs. Also the definition of the 2 MTD bits has been changed from encoding an integer to encoding 2 separate hit counts.
January 22, 2015	Added in the description of the PP101 algorithm with the PP2PP trigger logic.
March 18, 2015	The MT101 algorithm has been modified to add in a new cosmic ray bit with timing constraints. In the TF201 algorithm the 5th TOF multiplicity threshold has been dropped to make room for this new MTD bit.

Layer 0 DSM Boards: MIX_TF001:006

The TOF layer-0 DSM boards each receive 20 5-bit multiplicity values from the TOF trays. The connections are made such that each layer-0 DSM receives TOF data from one 2-hour pie-slice of the detector. Each 5-bit number is actually a count of how many TOF trays, in a group of 24, were hit. Values greater than 24 are therefore unphysical and are ignored. The values are summed to calculate the total multiplicity. The summing is performed in stages. The result of one of the intermediate stages is 4 numbers, each of which covers ¼ of the 2-hour pie-slice: 2 segments on the East side of the barrel and 2 on the West side. Each of those 4 numbers is compared to two thresholds. The 4 bits associated with the 1st threshold are passed to Layer-1 for use by the Ultra-Peripheral Collisions (UPC) program. The 4 bits associated with the 2nd threshold are passed to the TF202 DSM for use in the DAQ10k readout system. In parallel two signals (the RHIC clock and the run/stop signal) are passed through to the test header. This is being done to help debug a synchronization problem in the TOF layer-0 DSM boards.
NOTE: In order to avoid doing too many sums in parallel, this algorithm takes an extra tick of the RHIC clock, which corresponds to 4 extra ticks of the 4xRHIC clock that is used by the FPGA. This allows many sums to be performed in series, which is easier to implement.

RBT File: mix_tf001_2014_c.rbt

Users: TF001:TF006

Inputs: Ch 0:6 = TOF trays
Ch 7 = Unused

On each DSM channel:
(0:14) 3 5-bit TOF multiplicity values
(15) Unused
NOTE: Ch 6 receives just 2 input multiplicity values so it uses only bits 0:9

LUT: 1-to-1. Noisy, dead and non-instrumented channels are also zeroed out here

Registers:
R0: TOF_upc_th (8)
R1: TOF_DAQ10k_th (8)

Action

1st Latch inputs

2nd Zero out any channel with a value greater than 24

3rd Sum TOF channels 0:2, 3:4, 5:7, 8:9, 10:12, 13:14, 15:17 and 18:19

4th Combine these sums in pairs to make the sums of channels 0:4, 5:9, 10:14 and 15:19.
NOTE: Each of these sums covers 1 unit in η and $\pi/6$ (i.e. 1/12 of the barrel = 1 hour) in ϕ. The cabling of the TOF data into the DSM boards is such that the ordering is the same for all 6 TOF layer-0 DSM boards. WHEN VIEWED FROM THE EAST:

- Sum 0:4 = West, low hour
- Sum 5:9 = West, high hour
- Sum 10:14 = East, low hour

- Sum 15:19 = East, high hour

5th Combine these sums in pairs to make the sums of channels 0:9 and 10:19.
Compare each of the 4 sums to the UPC threshold in register 0. The logic looks for sum(channels 0:4) > reg0, etc…
Compare each of the 4 sums to the DAQ10k threshold in register 1. The logic looks for sum(channel 0:4) > reg1, etc…

6th Combine these two sums to make the final sums of channels 0:19.
Also delay the UPC and DAQ10k threshold bits to the 8th step.

7th Delay the final sum

8th Latch Outputs

Output to TF101:

(0:9)	TOF multiplicity
(10:13)	UPC threshold bits
(14:15)	Unused

Output to TF202:

(16:19)	DAQ10k threshold bits
(20:31)	Unused

Output to Test Header:

(0)	Run/Stop signal from Operation Control FPGA
(2:14)	Unused
(15)	RHIC clock

1. Layer 1 DSM Board: MIX_TF101

The TOF layer-1 DSM board receives a 10-bit multiplicity value and 4 UPC threshold bits from each of the six TOF layer-0 DSM boards. Each input multiplicity is compared to a threshold. In parallel with this, the values are also summed to calculate the total multiplicity. For the UPC program, the 24 input bits are masked so the UPC group can constrain which topologies they will trigger on. The masked bits are then searched to look for interesting combinations. The cabling is such that:

TF001 covers sectors that start at 9 o'clock and 10 o'clock when viewed from the East
TF002 covers sectors that start at 11 o'clock and 12 o'clock
TF003 covers sectors that start at 1 o'clock and 2 o'clock
TF004 covers sectors that start at 3 o'clock and 4 o'clock
TF005 covers sectors that start at 5 o'clock and 6 o'clock
TF006 covers sectors that start at 7 o'clock and 8 o'clock

NOTE: In order to avoid doing too many sums in parallel, this algorithm takes an extra tick of the RHIC clock, which corresponds to 4 extra ticks of the 4xRHIC clock that is used by the FPGA. This allows many sums to be performed in series, which is easier to implement.

RBT File: mix_tf101_2014_b.rbt

Users: TF101

Inputs: Ch 0:5 = TF001:TF006
Ch 6:7 = Unused

On each DSM channel:
(0:9) TOF multiplicity
(10:13) UPC threshold bits
(14:15) Unused

LUT: 1-to-1

Registers:
R0: TOF-sector-th (10)
R1: TOF_upc_East_mask (12)
R2: TOF_upc_West_mask (12)

Action

1st Latch inputs

2nd Sum channels 0:1, 2:3 and 4:5
Compare each of the 6 input multiplicity values to the threshold specified in register 0.
Mask out the UPC bits using the values masks specified in register 1 (East) and register 2 (West). A “1” in the mask enables a UPC bit, “0” will disable that bit. BOTH masks are coded such that:

bit(0) enables/disables the sector that starts at 12 o’clock AS VIEWED FROM THE EAST
bit(1) enables/disables the sector that starts at 1 o’clock AS VIEWED FROM THE EAST
…
bit(11) enables/disables the sector that starts at 11 o’clock AS VIEWED FROM THE EAST

3rd Combine the first two sums to make the sums of channels 0:3.
Delay the sum of channels 4 and 5 to the 4th step.
Delay the 6 threshold bits to the 8th step.
Combine (OR) the East and West UPC bits for each ϕ value and then look for all possible combinations separated by 4 hours, i.e.

1 o’clock = East 1 o’clock OR West 1 o’clock
2 o’clock = East 2 o’clock OR West 2 o’clock
…
12 o’clock = East 12 o’clock OR West 12 o’clock

TOF_UPC = 12 o’clock AND 4 o’clock OR
1 o’clock AND 5 o’clock OR
…
11 o’clock AND 3 o’clock

4th Combine the two remaining sums to make the final total multiplicity sum of channels 0:5.
Delay the TOF_UPC bit to the 8th step.

5th Delay the final sum to the 8th step.

6/7th	No logic
8th	Latch Outputs

Output to TF201:

(0:12)	TOF total multiplicity
(13:15)	Unused
(16:21)	6 sector threshold bits
(22)	TOF_UPC bit
(23:31)	Unused

2. Layer 0 QT Board: MXQ_MT001:002

All four MTD QT boards in the MXQ crate are using the same algorithm. That algorithm forms TAC pair sums and then finds the two largest sums to pass on to the DSM tree. In 2013 the algorithm was modified to include a slewing correction. Please see the documentation provided by Chris Perkins for a detailed description of this algorithm at http://www.star.bnl.gov/public/trg/TSL/Software/qt_v6_c_doc.pdf

3. Layer 0 QT Board: MXQ_VP003:004

The two VPD QT boards in the MXQ crate are running the same algorithm as the other two VPD QT boards which are in the BBQ crate. The algorithm has been changed in 2014 to add a slewing correction to the original logic. Please see the documentation provided by Chris Perkins for a detailed description of the new algorithm at http://www.star.bnl.gov/public/trg/TSL/Software/qt_v6_d_doc.pdf

The original logic looked for good hits and then selected the largest good TAC (i.e. the TAC value from the fastest good hit) to pass on to the DSM tree. It also calculated the sum of the good ADC values and passed that on too. Please see the documentation provided by Chris Perkins for a detailed description of this old algorithm at http://www.star.bnl.gov/public/trg/TSL/Software/qt_v5_6_doc.pdf The slewing logic is the same logic that was added to the MTD QT boards in 2013, and is documented in http://www.star.bnl.gov/public/trg/TSL/Software/qt_v6_c_doc.pdf

4. Layer 1 DSM Board: MIX_MT101

The MT101 DSM receives its data through a TDSMI, so there are 10 12-bit input channels. The algorithm receives the 2 best TAC sums from each of the 4 MTD QT boards, and the ID of those sums. It also receives the fastest (largest) TAC values from the QT boards covering the East and West sides of the VPD (MXQ_VP003/4). Note that the cables carrying the VPD ADC sums are not connected to MT101 so that data is not received. There are two separate logic streams flowing through the algorithm:
Muons: The VPD TAC sum is calculated. Then the algorithm finds the difference between each MTD TAC sum and that VPD TAC sum. All 8 TAC differences are checked to determine if they are inside a window. Those that are inside the window are counted, and the count is sent on to TF201.
Cosmic Rays: A bit is set if at least two of the MTD TAC sums are non-zero. That bit is sent to TF201 for use as a simple cosmic ray trigger. In addition the MTD TAC sums are also sorted to find the two largest non-zero values. The difference between those 2 largest TAC sums is calculated, and that difference is checked to determine if it is inside a window. That bit is also sent to TF201 for use as a more restrictive cosmic ray trigger. In parallel the ID values of those two channels are sent on to MT201 for the DAQ10k readout scheme.

A test mode has been added to allow the timing through the DAQ10k readout scheme to be tested. When the algorithm is in normal data mode it operates as described above. In test mode the algorithm sets a user-specified pair of ID values (for MT201) at the same time as setting the muon count (for TF201) to two. This test data is driven out at a user-specified rate, with zeros in between.

NOTE: This algorithm takes an extra tick of the RHIC clock to implement all the logic.

RBT File: mix_mt101_2015_a.rbt

Users: MT101

Inputs: Ch0:1 = MT001 = MTD
Ch2:3 = MT002 = MTD
Ch4:5 = MT003 = MTD
Ch6:7 = MT004 = MTD
Ch8 = VP003 = VPD East
Ch9 = VP004 = VPD West

From the MTD QT boards:
Bits 0:9 = Best MTDE+MTDW TAC sum (value=0 means not enough good hits)
Bits 10:11 = ID of best TAC sum
Bits 12:21 = 2nd best MTDE+MTDW TAC sum (value=0 means not enough good hits)
Bits 22:23 = ID of 2nd best TAC sum

From VP003/4 QT boards:
Bits 0:11 = Max TAC (value=0 implies no good hits)

LUT: 1:1

Registers:
R0: MTD-VPD-TACdiff-Min (11)
R1: MTD-VPD-TACdiff-Max (11)
R2: MTD-InputCh-Bitmask (8)
Bit x = 0 turns off ChX, Bit x = 1 turn on ChX
R3: MTD-DAQ10k-Mode (1)
0 = Normal mode, 1 = Test mode
R4: MTD-DAQ10k-Test-Pattern (12)
Bits 0:3 = Channel number of 1st test ID, values from 1-8
Bits 4:5 = 1st test ID, values from 0-3
Bits 6:9 = Channel number of 2nd test ID, values from 1-8
Bits 10:11 = 2nd test ID, values from 0-3
R5: MTD-DAQ10k-Test-Rate (12)
R6: MTD-Cosmic-Tdiff-Min (10)
R7: MTD-Cosmic-Tdiff-Max (10)

Action:

1st Latch input

2nd Define Good_VPD_E = VPDE-TAC > 0
Define Good_VPD_W = VPDW-TAC > 0
Calculate 13-bit VPD-sum = VPDE TAC + VPDW TAC

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        Truncate VPD-sum to 10-bits by dropping 3 LSB
        For each MTD ChX:
            Zero out MTD-TAC-X if R2(x) = 0

3rd     Define Good_VPD = Good_VPD_E and Good_VPD_W.
        For each MTD ChX:
            Define: Good_ChX = MTD-TAC-X > 0
            Calculate: MTD-VPD-TACdiffX = 1024 + MTD-TAC-X – VPD-sum
        Split the MTD-TAC-X values into 2 groups (A = ch0:ch3 and B = ch4:ch7)
        For each group:
            Make the comparisons necessary to find the 2 largest values in each group, e.g. in group A look for ch0>ch1, ch0>ch2, ch0>ch3, ch1>ch2, ch1>ch3 and ch2>ch3

4th     Count the Good_ChX bits = cosmic_count
        Within each group use the results of the comparisons to find the 2 largest values, e.g. in group A:
            Ch0 is largest if ch0>ch1 and ch0>ch2 and ch0>ch3
            …
            Ch3 is largest if (not ch0>ch3) and (not ch1>ch3) and (not ch2>ch3)
            NOTE 1: If all channels have the same MTD-TAC-X value then this logic will select Ch3 as the largest.
            NOTE 2: If the largest MTD-TAC-X value is zero (i.e. no good hits) then no channel is selected and the output of this stage is also zero.
        For each MTD ChX:
            Compare the TACdiffX value to the min and max values specified in R0 and R1
                TACdiffX-min = MTD-VPD-TACdiffX > R0
                TACdiffX-max = MTD-VPD-TACdiffX < R1
            Zero out TACdiffX-min/max if EITHER Good_VPD or Good_ChX is FALSE.
            Combine the min and max values to determine if the TAC difference is inside the window:
                TACdiff-in-window-X = TACdiffX-min and TACdiffX-max

5th     Set the Cosmic-Ray bit to 1 if cosmic_count > 1
        Count how many TACdiff-in-window bits are true = num-muons
        Compare the largest MTD-TAC-X values from groups A and B to find the overall largest value.
        NOTE 1: If both channels have the same MTD-TAC-X value then this logic will select the one from group B as the largest.
        NOTE 2: If the largest MTD-TAC-X value is zero (i.e. no good hits) then no channel is selected and the output of this stage is also zero.
        Compare the remaining values to find the 2nd largest value. Same NOTES apply.

6th     Calculate MTD-Largest-Tdiff = largest MTD-TAC-X – 2nd largest MTD-TAC-X.
        Zero out the result if either TAC-X value is zero.
        NOTE: The result of this subtraction is guaranteed to be positive so there is no need for the offset of 1024 that is used in the MTD-VPD subtraction logic.
        Create the “test” data:
            When the DSM is not in RUN mode initialize a 12-bit prescale counter to the value in R5
            Once the DSM is in RUN mode decrement the prescale counter by 1 every tick of the RHIC clock. When the counter reaches 1 reset it to the original value from R5.
        If the counter value is 1 then:
            Set Cosmic-Ray-test = 1, num-muons-test = 2 and MTD-ID-test = value from R4
        Else (i.e. counter value has not yet reached 1)
            Set all test data to zero.

7th     Compare the Largest-Tdiff value to the min and max values specified in R6 and R7
            Tdiff-min = MTD-Largest-Tdiff > R6
            Tdiff-max = MTD-Largest-Tdiff < R7
        Combine the min and max values to determine if the TAC difference is inside the
        window. This is the timed-cosmic bit
            Tcosmic = Tdiff-min and Tdiff-max
        If the algorithm is in "normal" mode (R3 = 0) then
            Select the MID IDs, Cosmic-Ray and num-muons values calculated from real data
        Else (i.e. the algorithm is in "test" mode)
            Select the test values of MTD IDs, Cosmic-Ray and num-muons

8th     Latch output
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Output to TF201:

(0:3)	num_muons
(4:11)	"MTD-VPD TAC difference in window" bits
(12)	Unused
(13)	Good_VPD
(14)	Cosmic-Ray
(15)	Timed-Cosmic-Ray

Output to MT201

(16:19)	Channel number (1:8) of second-best good MTD value
(20:21)	MTD-ID value from that channel
(22:25)	Channel number (1:8) of best good MTD value
(26:27)	MTD-ID value from that channel
(28:31)	Unused

5. Layer 0 QT Board: MXQ_PP001

Please see the documentation provided by Chris Perkins for a description of the algorithm.

6. Layer 1 PP2PP DSM Board: MIX_PP101

The PP101 DSM board receives 16 "good hit" bits from the PP001 QT board. Those bits are combined to make "good detector" bits, which are themselves combined to make the trigger and scaler bits. All the bits are passed on to TF201, which separates the trigger bits from the scaler bits and sends them to the appropriate place. A mask register is available to turn each "good hit" bit on or off in case of problems.

RBT File: mix_pp101_2015_a.rbt

Users: PP101

Inputs Ch 0 = PP001
Ch 1:7 = Unused

From: The PP2PP QT board
(0) E2U1 = Roman Pot East-2 (Back) Up 1
(1) E2U2 = Roman Pot East-2 (Back) Up 2
(2) E2D1 = Roman Pot East-2 (Back) Down 1
(3) E2D2 = Roman Pot East-2 (Back) Down 2
(4) W2U1 = Roman Pot West-2 (Back) Up 1
(5) W2U2 = Roman Pot West-2 (Back) Up 2
(6) W2D1 = Roman Pot West-2 (Back) Down 1
(7) W2D2 = Roman Pot West-2 (Back) Down 2
(8) E1D1 = Roman Pot East-1 (Front) Down 1
(9) E1D2 = Roman Pot East-1 (Front) Down 2
(10) E1U1 = Roman Pot East-1 (Front) Up 1
(11) E1U2 = Roman Pot East-1 (Front) Up 2
(12) W1D1 = Roman Pot West-1 (Front) Down 1
(13) W1D2 = Roman Pot West-1 (Front) Down 2
(14) W1U1 = Roman Pot West-1 (Front) Up 1
(15) W1U2 = Roman Pot West-1 (Front) Up 2

LUT: 1-to-1

Registers:
R0: RPmask (16)
NOTE: The bits are arranged in the SAME ORDER as the input data coming from PP001
Bit 0 = E2U1 on(1) or off (0)
Bit 1 = E2U2 on(1) or off (0)
…
Bit 15 = W1U2 on(1) or off (0)

Action

1st Latch inputs

2nd Combine the 2 hits from the same counter, and then combine the 2 counters on each side, to make the detector bits. Mask each hit with Reg0 before it is used.
E2U = (E2U1 and Reg0(0)) or (E2U2 and Reg0(1))
E2D = (E2D1 and Reg0(2)) or (E2D2 and Reg0(3))
W2U = (W2U1 and Reg0(4)) or (W2U2 and Reg0(5))
W2D = (W2D1 and Reg0(6)) or (W2D2 and Reg0(7))
Same for E1D, E1U, W1D, W1U

EU = E1U or E2U
ED = E1D or E2D
WU = W1U or W2U
WD = W1D or W2D

3rd Delay a copy of the detector bits (EU, ED, WU and WD) to the 4th step.
Combine the detector bits to make the trigger bits
EA (Elastic Trigger A) = EU and WD
EB (Elastic Trigger B) = ED and WU
IU (Inelastic Trigger Up) = EU and WU
ID (Inelastic Trigger Down) = ED and WD

ET (Elastic Trigger) = EA or EB
IT (Inelastic Trigger) = IU or ID
EOR (East OR) = EU or ED
WOR (West OR) = WU or WD

4th Latch Outputs

Output to TF201:

(0:3)	ET, IT, EOR, WOR
(4:7)	EU, ED, WU, WD
(8:15)	Unused

7. Layer 2 TOF DSM Board: L1-TF201

All the information from the TOF, MTD and Roman Pot (RP) detectors is brought into the TOF layer 2 DSM. The MTD Cosmic Ray bits, the TOF_UPC topology bit and the RP bits are simply passed through to the TCU. The TOF multiplicity is compared to four thresholds. The 6 TOF sector threshold bits are combined in pairs to make cosmic ray bits. The count of MTD muons is used to set one bit meaning "at least one muon" and a second bit meaning "at least two muons"

RBT File: l1_tf201_2015_b.rbt

Users: TF201

Inputs: Ch 0 = MT101
Ch 1 = Unused
Ch 2:3 = TF101
Ch 4:5 = PP101
Ch 6:7 = Unused

From MTD Layer 1 DSM - MT101

(0:3)	Num_muons
(3:13)	Unused
(14)	Cosmic-Ray
(15)	Timed-Cosmic-Ray

From TOF Layer 1 DSM - TF101 on Ch. 2

(0:12)	TOF total multiplicity
(13:15)	Unused

From TOF Layer 1 DSM - TF101 on Ch. 3

(0:5)	TOF sector threshold bits
(6)	TOF UPC topology bit
(7:15)	Unused

From PP2PP Layer 1 DSM – PP101 on Ch. 4

(0:3)	RP_ET, RP_IT, RP_EOR and RP_WOR
(4:7)	RP_EU, RP_ED, RP_WU and RP_WD
(8:15)	Unused

LUT: 1-to-1

Registers:

R0: TOFmult0 (13)
R1: TOFmult1 (13)
R2: TOFmult2 (13)
R3: TOFmult3 (13)

Action

1st Latch inputs

2nd Delay the MTD Cosmic Ray bits, the TOF_UPC topology bit and the RP bits to the 4th step.
Combine the TOF sector bits from opposite sides of the barrel: i.e.
TOFsector0_3 = TOFsector(0) and TOFsector(3)
TOFsector1_4 = TOFsector(1) and TOFsector(4)
TOFsector2_5 = TOFsector(2) and TOFsector(5)
Compare the TOF total multiplicity to the thresholds specified in registers 0 to 3.
Set the MTD threshold bits:
If Num_muons >= 1 then MTD_th1 = 1
If Num_muons >= 2 then MTD_th2 = 1

3rd Delay the TOF multiplicity bits, the TOF sector bits and the MTD bits to the 4th step.

4th Latch Outputs

Output to TCU:

Bit	Name	Description
Bit 0	MTD_th1	At least one muon in the MTD
Bit 1	MTD_th2	At least two muons in the MTD
Bit 2	RP_ET	Roman Pot Elastic Trigger
Bit 3	TOF_UPC	TOF UPC topology bit
Bit 4	TOFmult0	TOF total multiplicity > th0
Bit 5	TOFmult1	TOF total multiplicity > th1
Bit 6	TOFmult2	TOF total multiplicity > th2
Bit 7	TOFmult3	TOF total multiplicity > th3
Bit 8	MTD-T-Cosmic	MTD timed cosmic ray trigger
Bit 9	TOFsector0_3	TOF sectors 0 and 3 multiplicity > th
Bit 10	TOFsector1_4	TOF sectors 1 and 4 multiplicity > th
Bit 11	TOFsector2_5	TOF sectors 2 and 5 multiplicity > th
Bit 12	RP_IT	Roman Pot Inelastic Trigger
Bit 13	RP_EOR	Roman Pot East Trigger
Bit 14	RP_WOR	Roman Pot West Trigger
Bit 15	MTD-Cosmic	MTD cosmic ray trigger

Output to Scalers:

Bit	Description
Bit 0	TOF sectors 0 and 3multiplicity > th
Bit 1	TOF sectors 1 and 4 multiplicity > th
Bit 2	TOF sectors 2 and 5 multiplicity > th
Bit 3	Roman Pot East Up hit
Bit 4	Roman Pot East Down hit
Bit 5	Roman Pot West Up hit
Bit 6	Roman Pot West Down hit
Bit 7	TOF UPC topology bit
Bit 8	MTD cosmic ray trigger
Bit 9	At least one muon in the MTD
Bit 10	At least two muons in the MTD
Bit 11	TOF total multiplicity > th0
Bit 12	TOF total multiplicity > th1
Bit 13	TOF total multiplicity > th2
Bit 14	TOF total multiplicity > th3
Bit 15	MTD timed cosmic ray trigger