D Flip-Flop using 6 NAND gates

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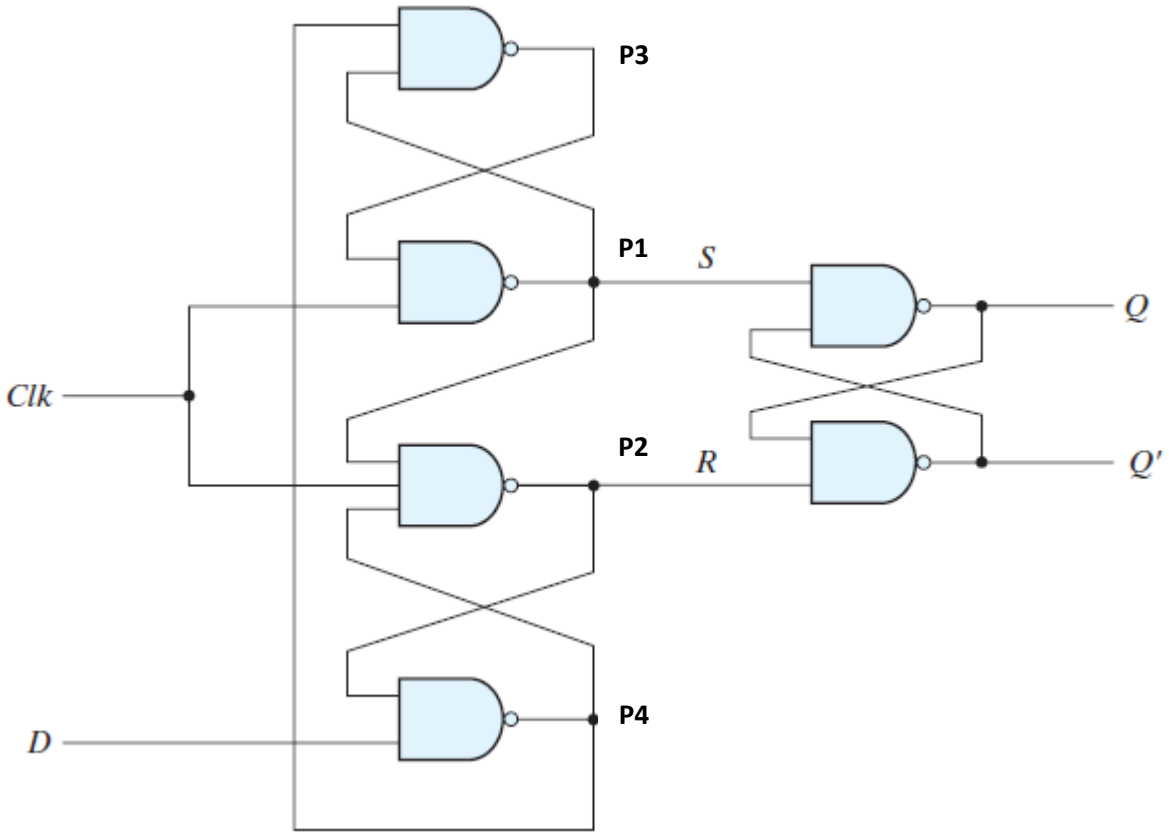
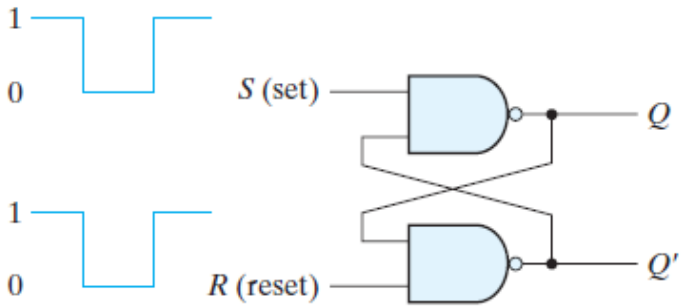


Above circuit is efficient design (with fewer transistors) of positive edge D flip-flop. In this report, I will introduce the working principals and the Timing Diagrams (in both ModelSim and MultiSim) of this circuit. Firstly, I would say that, this scheme consists of 3 S'R' latches.



(a) Logic diagram

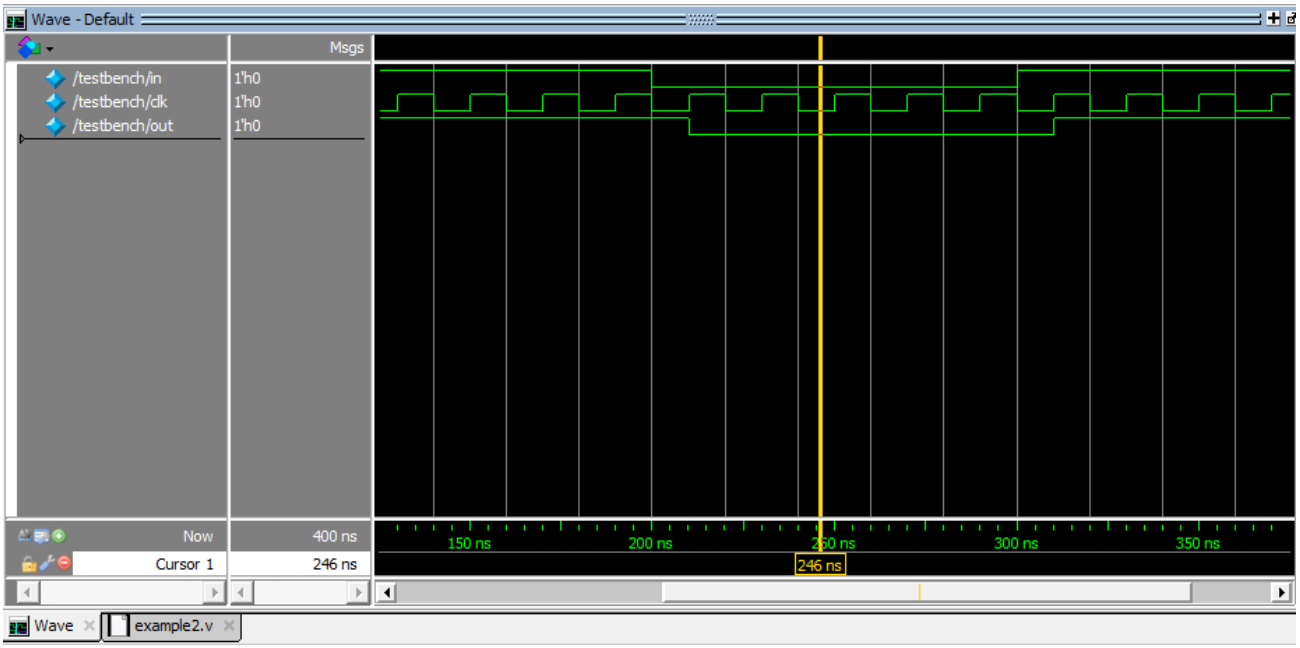
S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	(forbidden)

(b) Function table

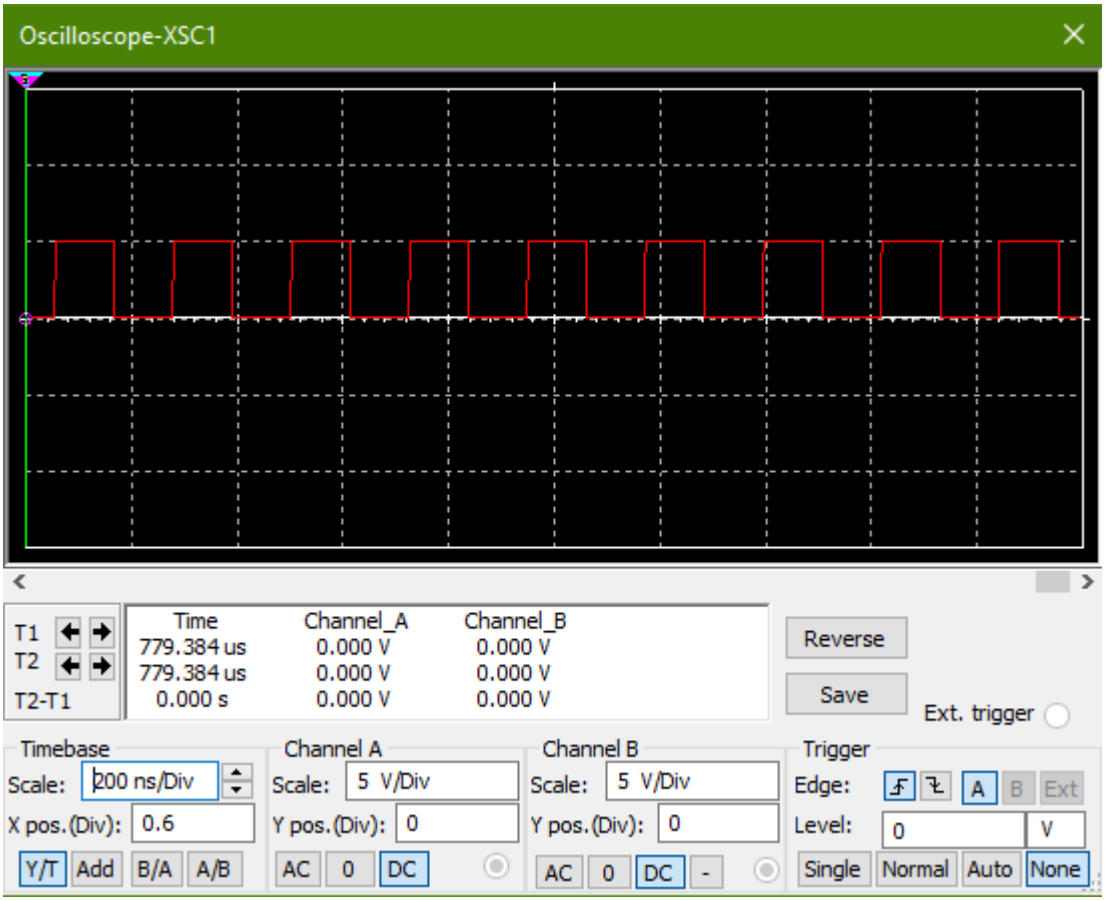
Let’s explain “how the above circuit works?” (look at the first picture):

- When Clk=0, P1 and P2 are high (P1=P2=1). That is why it is keeping the values of Q and Q' intact (look at the table of S’R’ latch).
- Now when Clk=1 (at positive edge), the values of P4 (complement of D) and P3 (equal D) passes through P1 and P2.
    - Now P1=P4=D' and P2=P3=D which means Q=D and Q'=D' (look at the table of S’R’ latch).
        - When D=0, P2=0 which will keep the value of P4=1 regardless of the value of D.
        - When D=1, P1=0 which will keep the value of P2=1 regardless of the value of D.
        - This implies that the above circuit ignores the changes in D when Clk=1 after positive edge of the clock.

Let’s look at the timing diagrams of positive edge D flip-flop in ModelSim & MultiSim:



The figure above is the timing diagram of this circuit in ModelSim Software. As seen from the graph, the value of “out” updates (according to value of “in”) only in the positive edges of “clk”.



Above diagram is the oscilloscope output of this circuit in MultiSim Software.