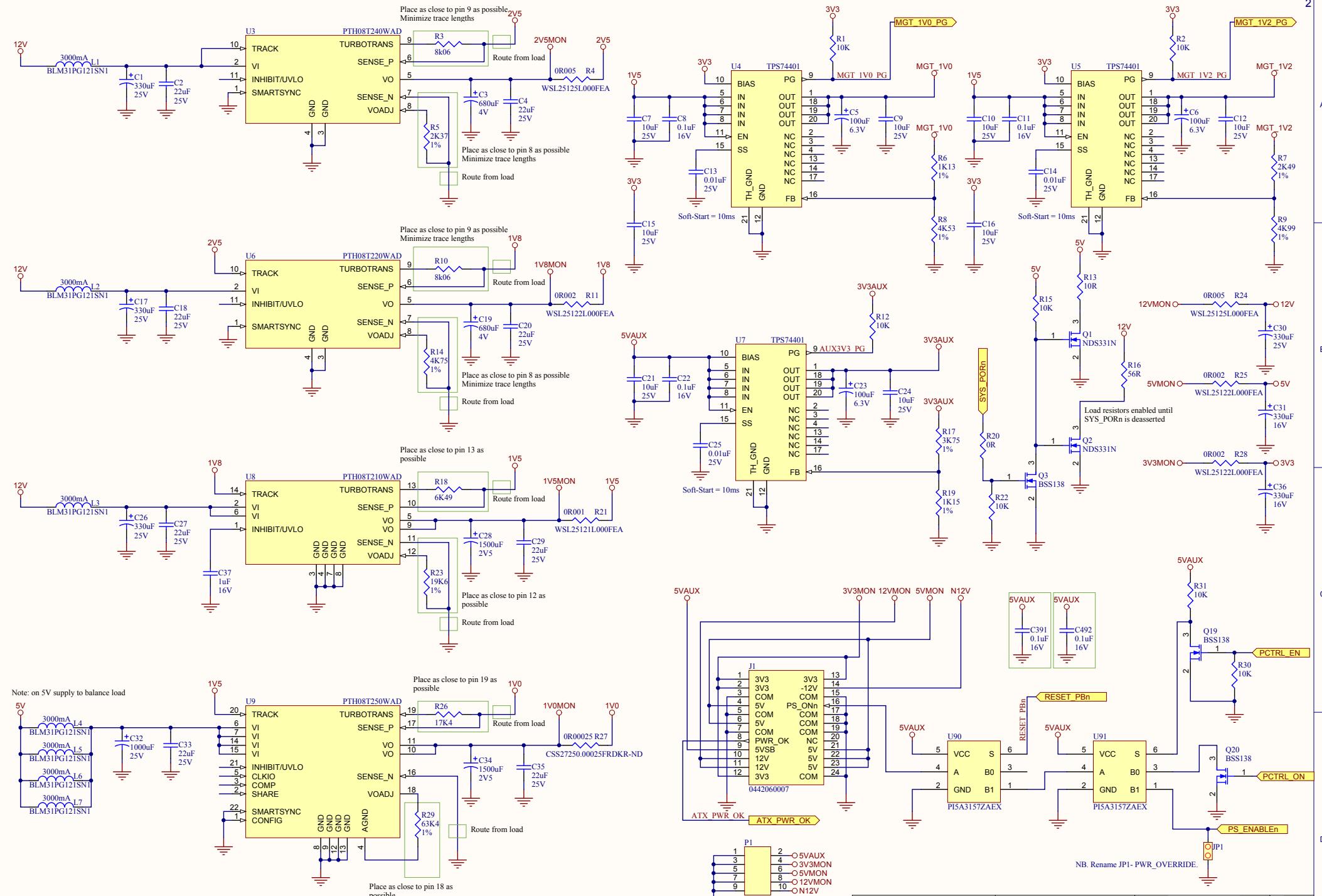


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Note: on 5V supply to balance load

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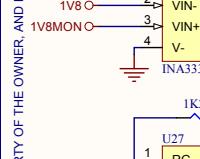
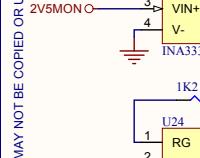
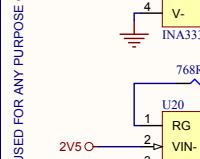
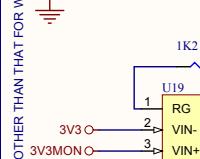
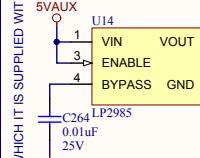
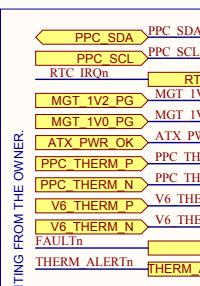
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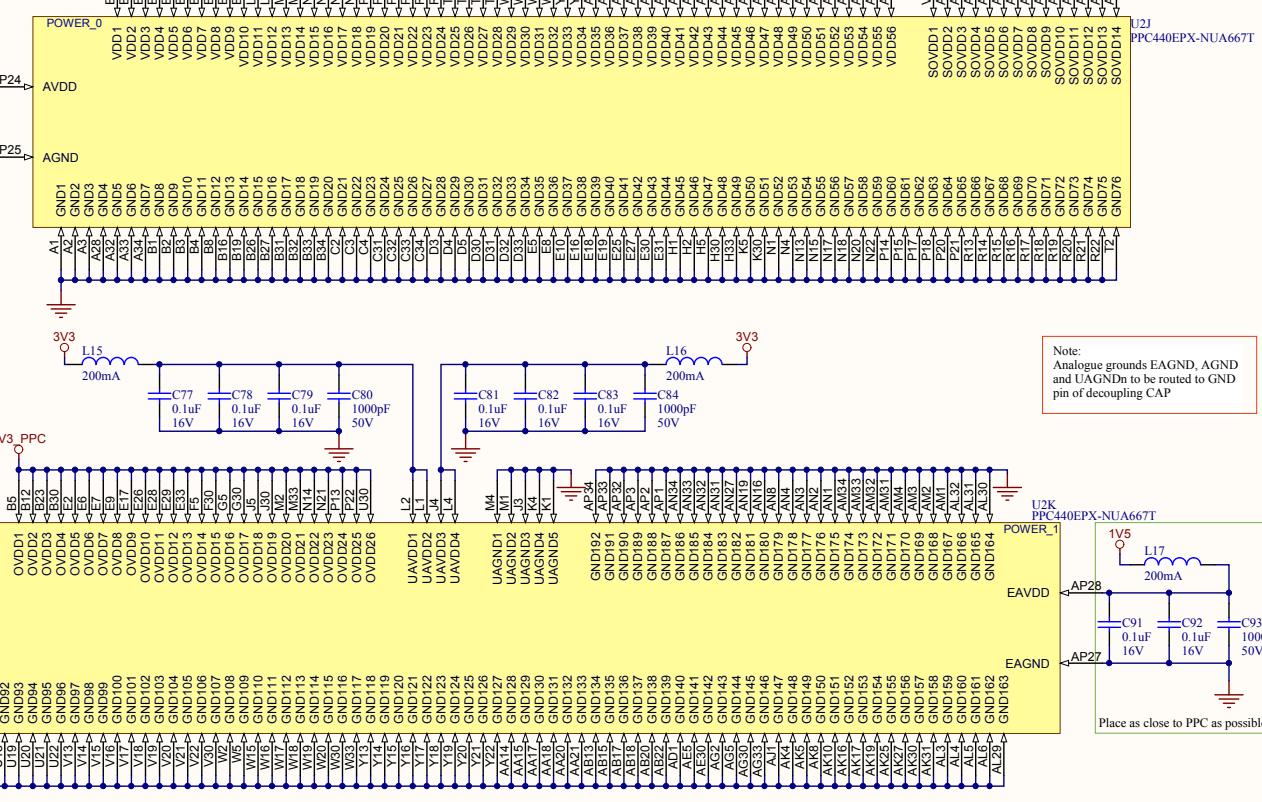
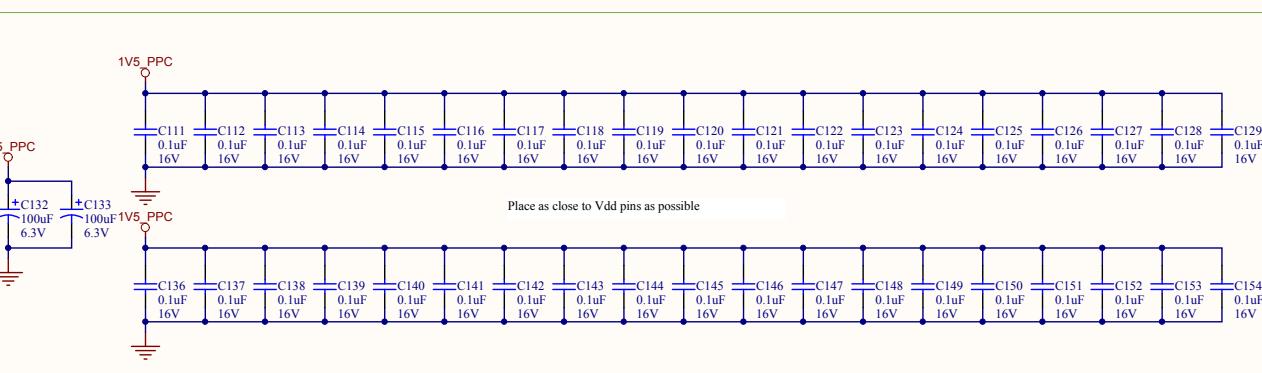
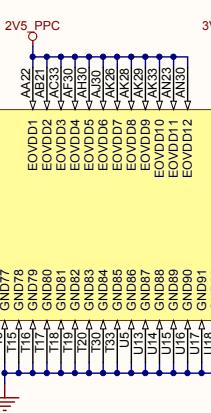
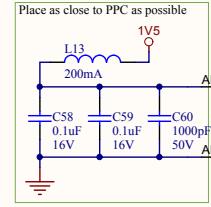
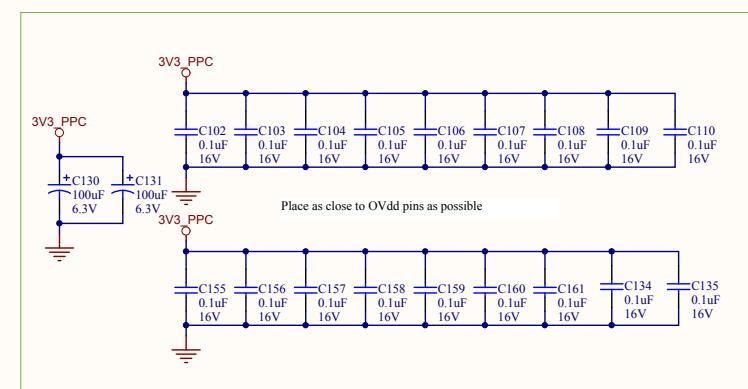
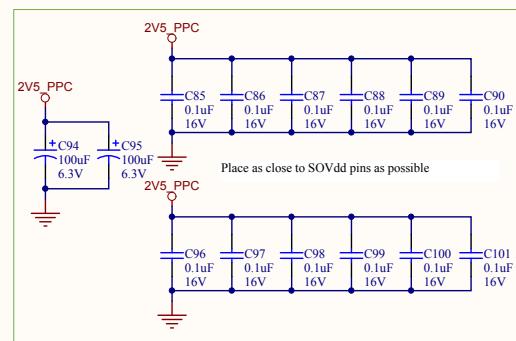
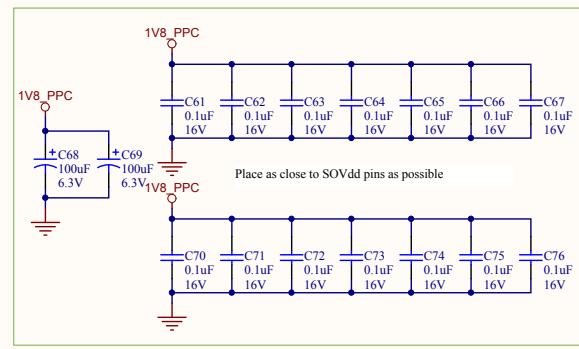
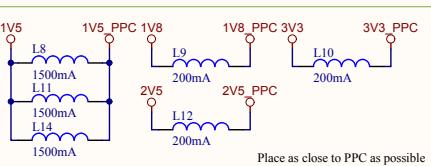
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DRAWN BY:	Philip Gibbs
ENGINEER:	David Geurts

Supply.SchDoc	CIRCUIT DIA
cbDoc	ROACH
APPROVED:	Board Power
George	

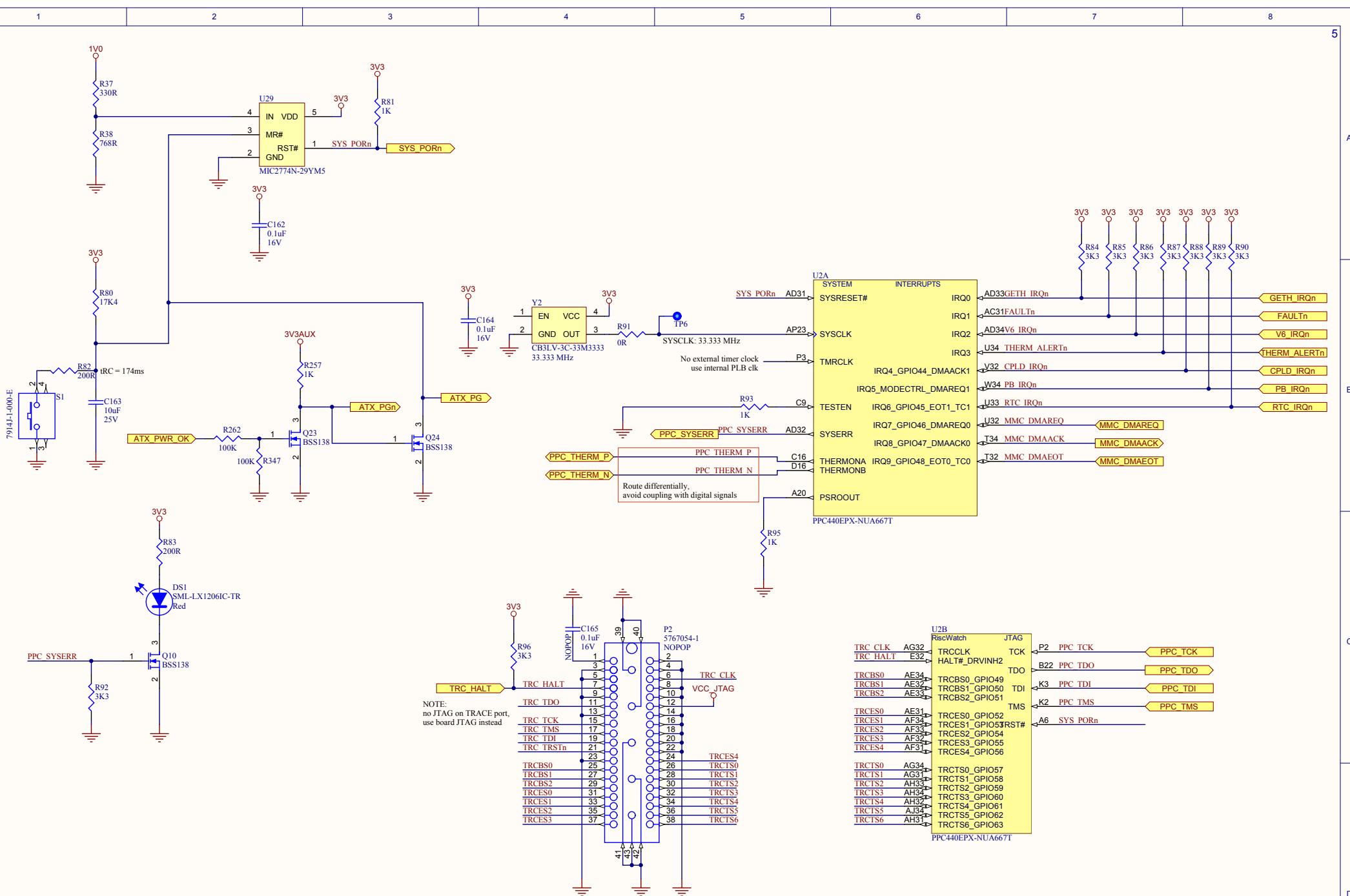
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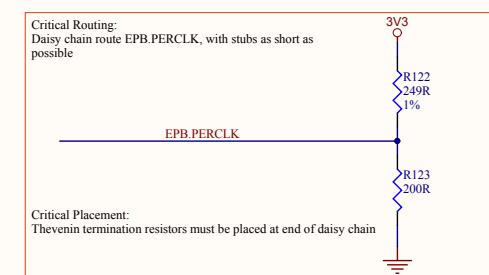
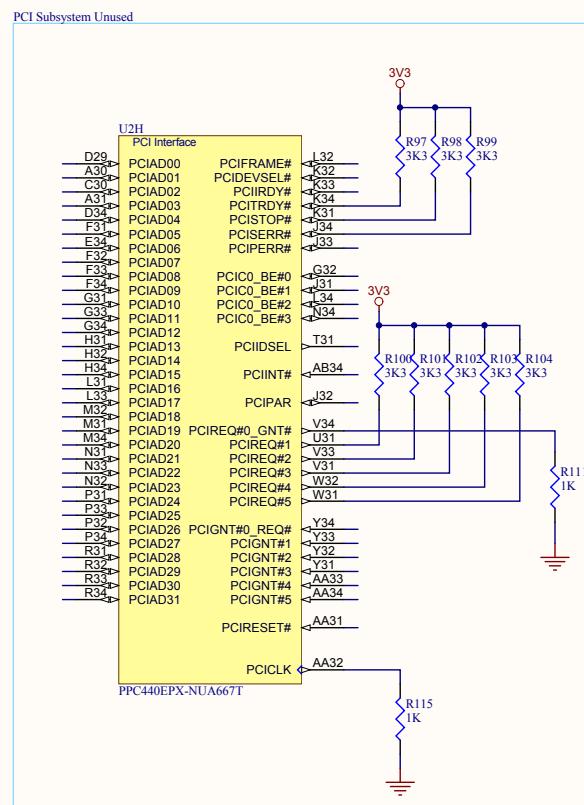
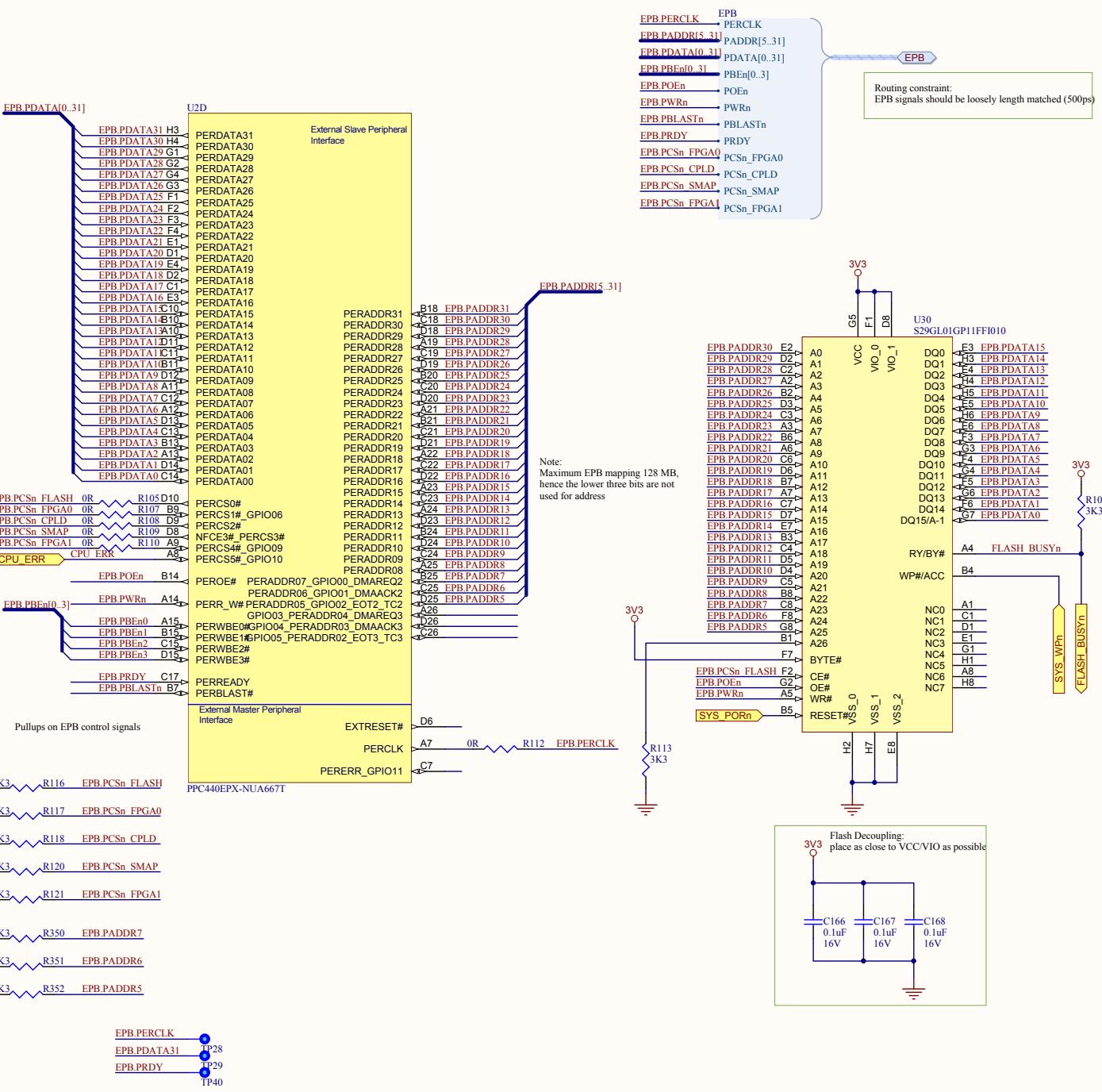
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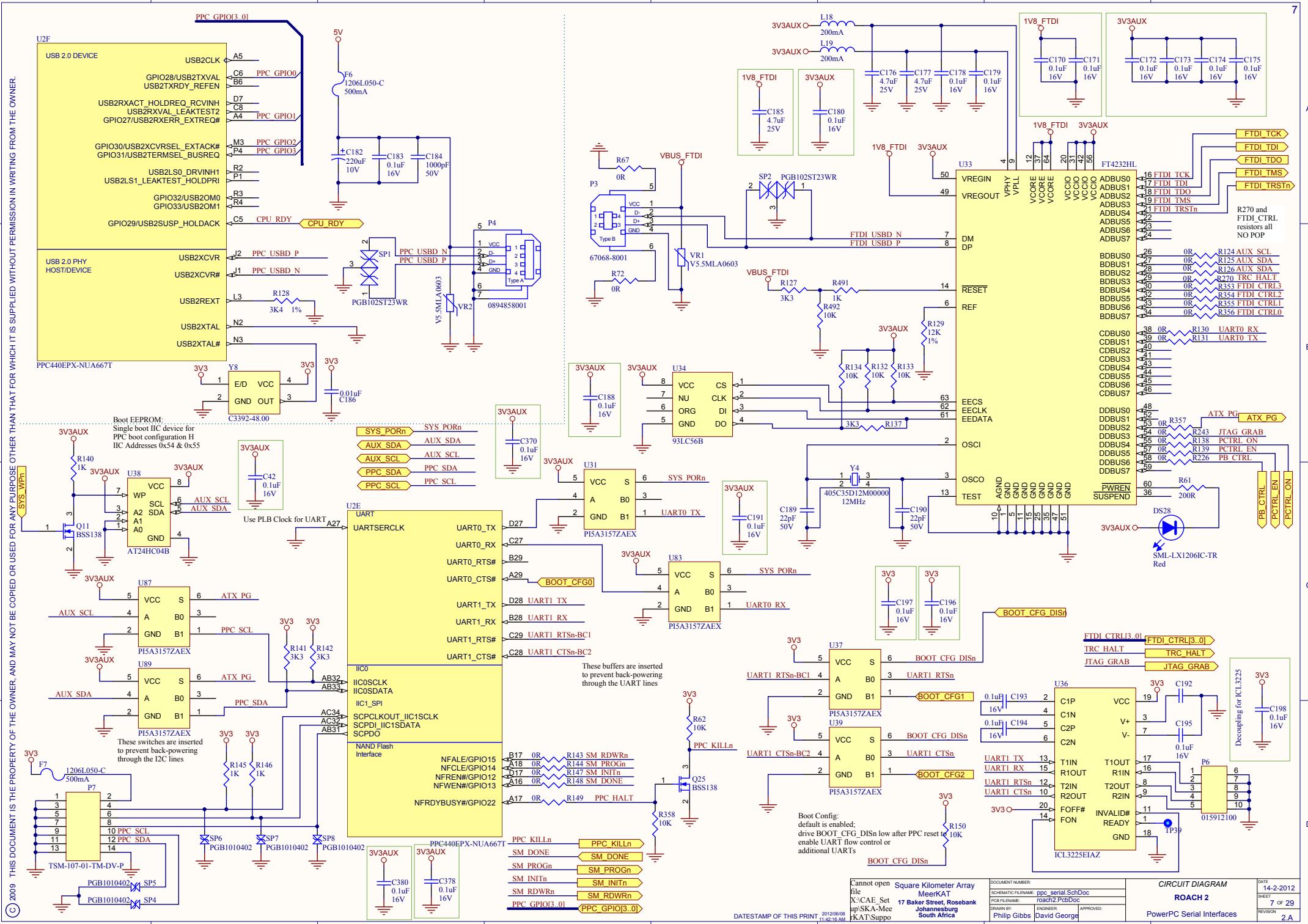


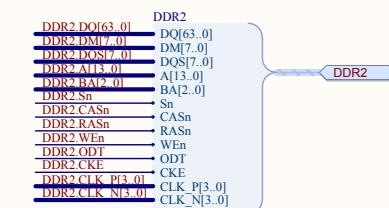
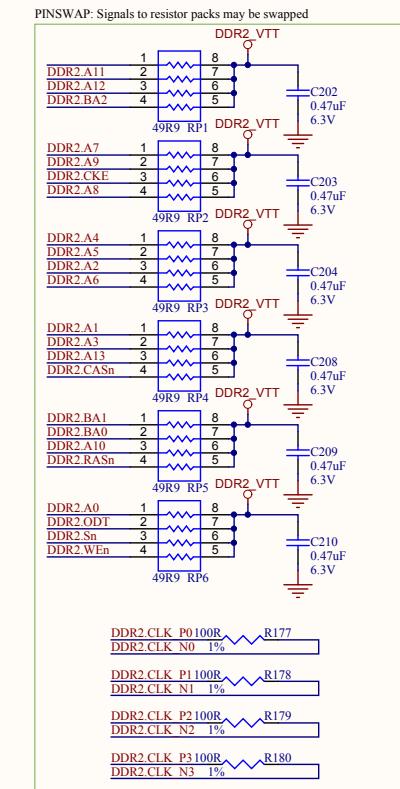
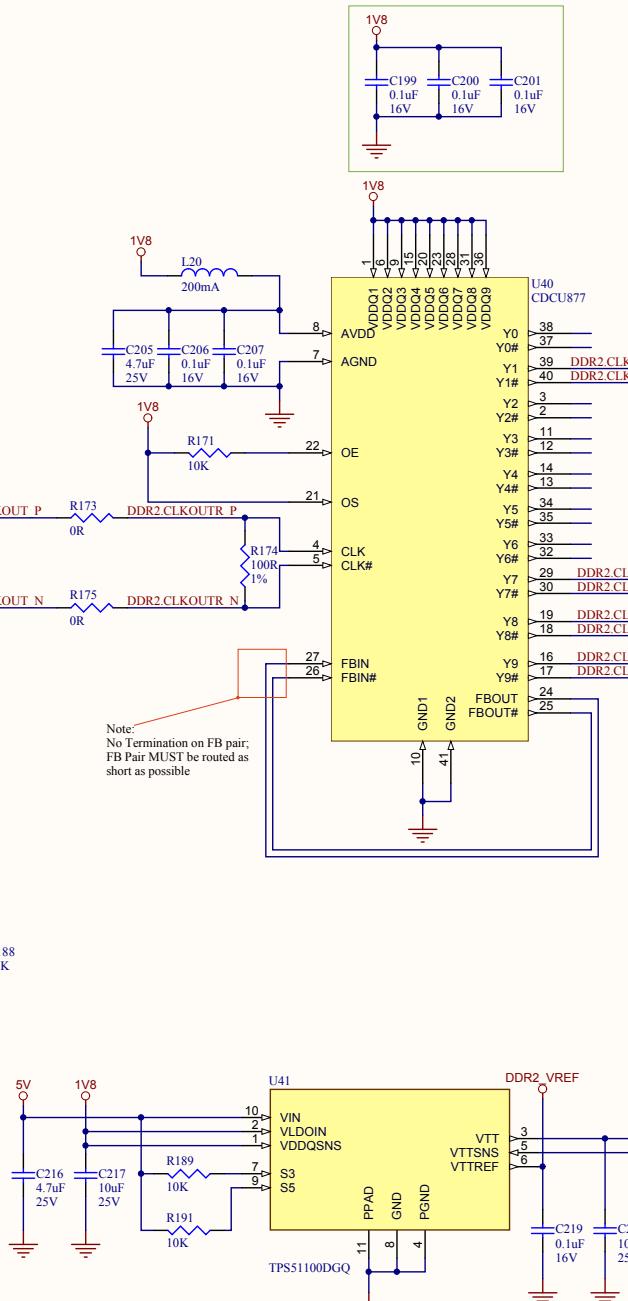
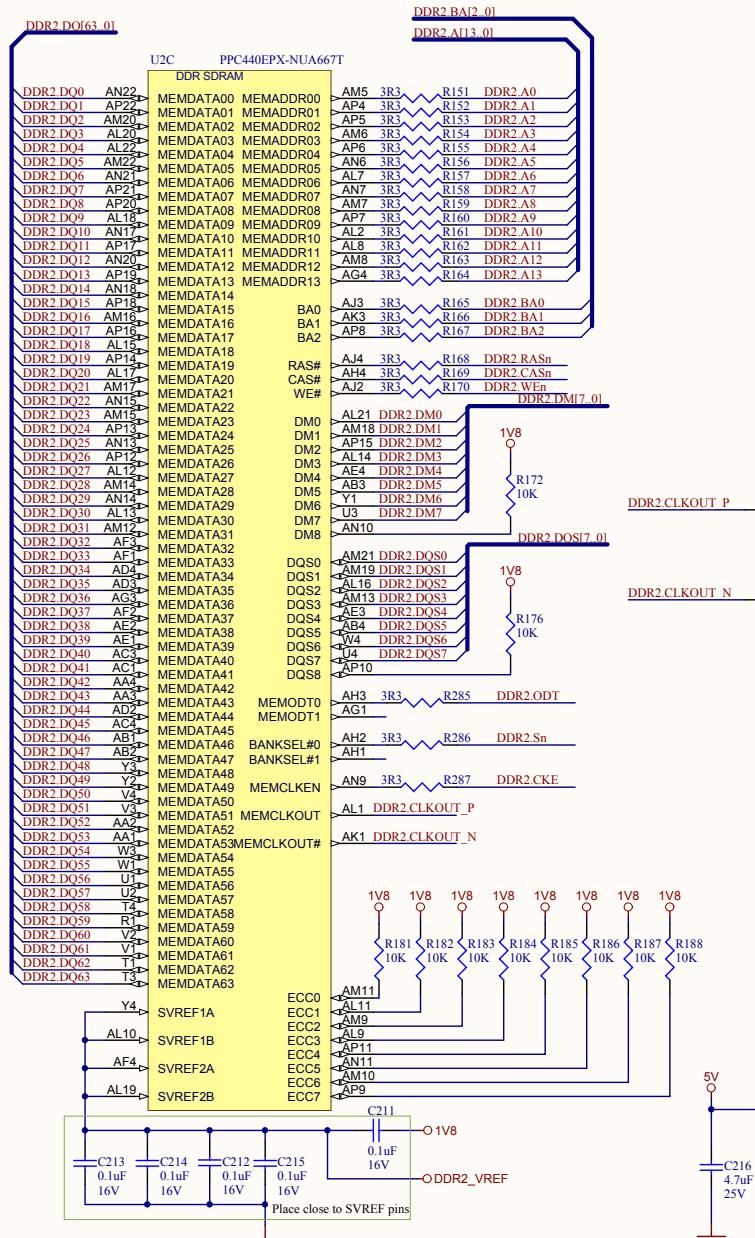


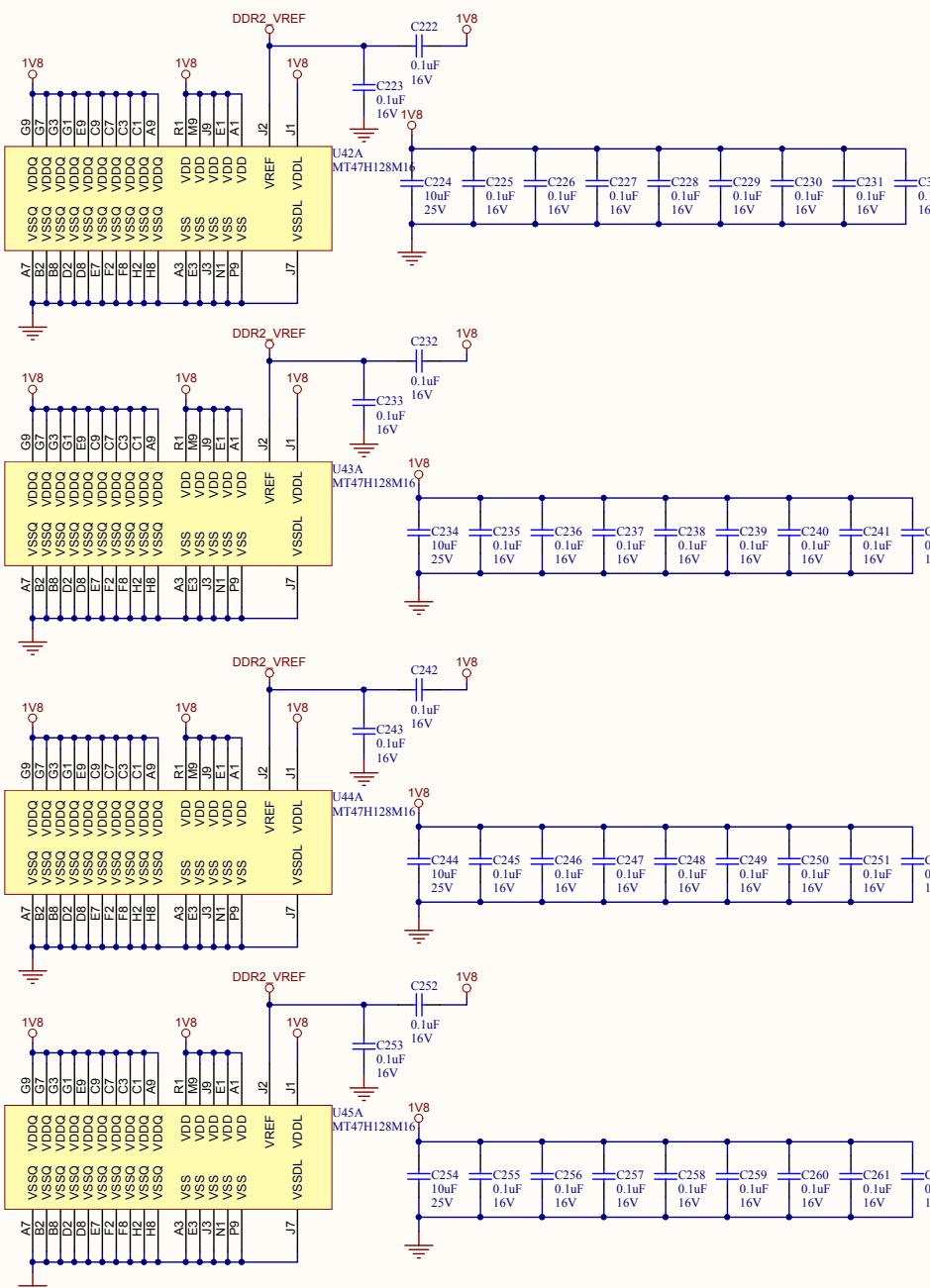
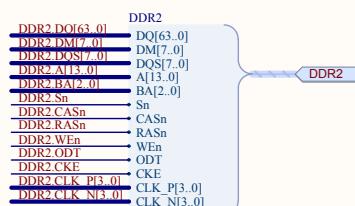
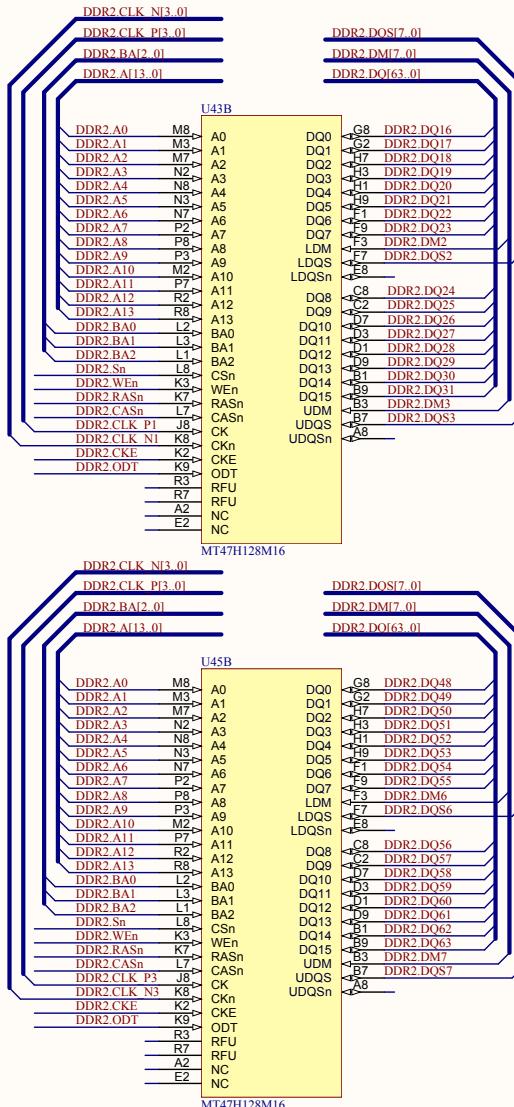
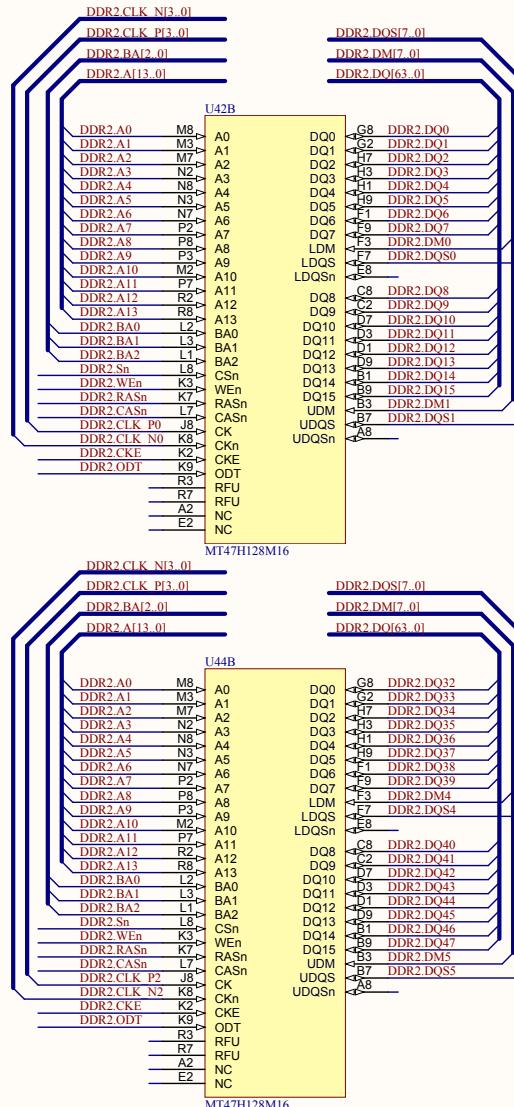
Note:
Analogue grounds EAGND, AGND and UAGND to be routed to GND pin of decoupling CAP











PINSWAP:
 CPLD_CLK and EPB.PERCLK MUST go on GCK pins
 SYS_PORn MUST go on GSR pin
 EPB.POEn MUST go on GTS pin
 Otherwise, swap away

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BANK 1	
I/O, GCK1	23 CPLD CLK
I/O, GCK0	42 EPB.PERCLK
I/O, CDRST	44
I/O, GCK2	47
I/O, DGE	48
I/O	49
I/O	50
I/O	51
I/O	52
I/O, FLASH BUSYn	57
I/O	58
I/O	59
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I/O	61
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I/O	65
I/O	66
I/O	67
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XC2C256-5VQG100C

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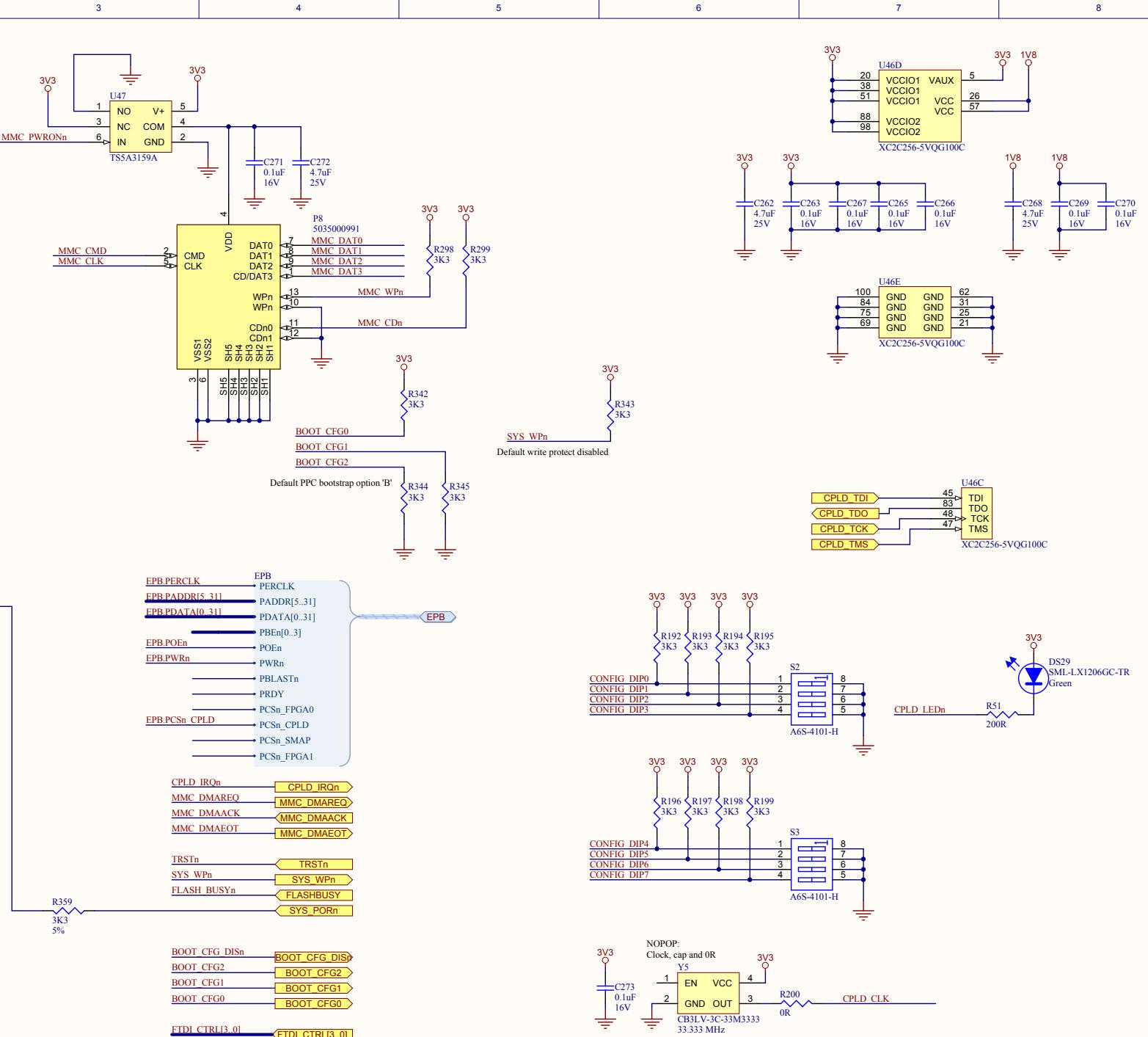
BANK 2	
I/O, GSR	99 EPB.PCSn CPLD
I/O	98 EPB.PWRn CPLD
I/O	97 EPB.POEn CPLD
I/O	96 EPB.PADDR5..31 CPLD
I/O	95 EPB.PDATA0..31 CPLD
I/O	94 EPB.POEn EPB
I/O	93 EPB.PWRn EPB
I/O	92 EPB.PBLASTn EPB
I/O	91 EPB.PRDY EPB
I/O	90 EPB.PCSn_FPGA0 EPB
I/O	89 EPB.PCSn_CPLD EPB
I/O	88 EPB.PCSn_SMAP EPB
I/O	87 EPB.PCSn_FPGA1 EPB
I/O	86 EPB.IRQn EPB
I/O	85 EPB.PADDR26 EPB
I/O	84 EPB.PDATA7 EPB
I/O	83 EPB.PDATA6 EPB
I/O	82 EPB.PDATA5 EPB
I/O	81 EPB.PDATA4 EPB
I/O	80 EPB.PDATA3 EPB
I/O	79 EPB.PDATA2 EPB
I/O	78 SM_DBUSY EPB
I/O	77
I/O	76
I/O	75
I/O	74 BOOT CFG0
I/O	73 BOOT CFG1
I/O	72 BOOT CFG2
I/O	71 BOOT CFG DISn
I/O	70 FTDI CTRL3
I/O	69
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I/O	67
I/O	66
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I/O	2
I/O	1

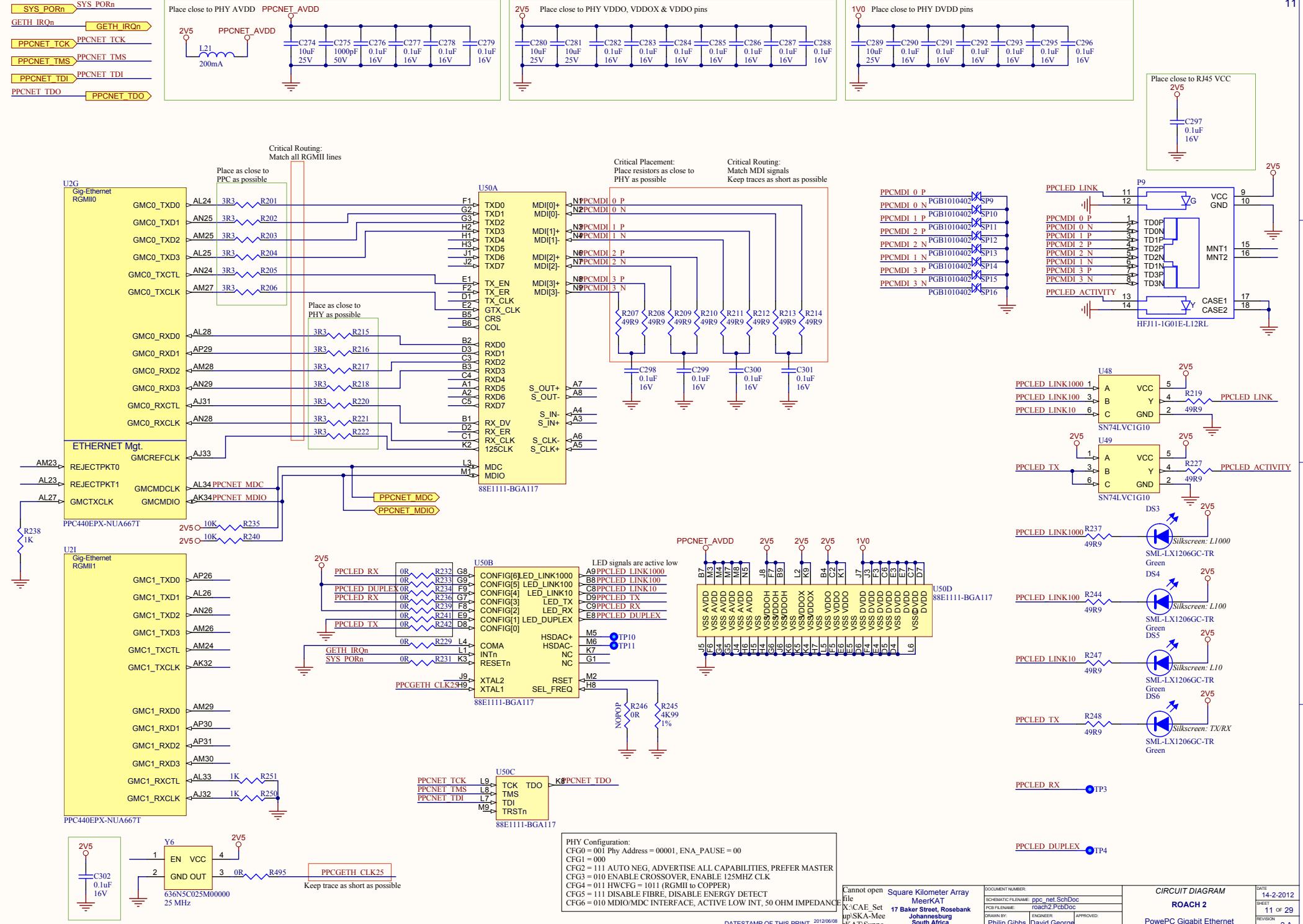
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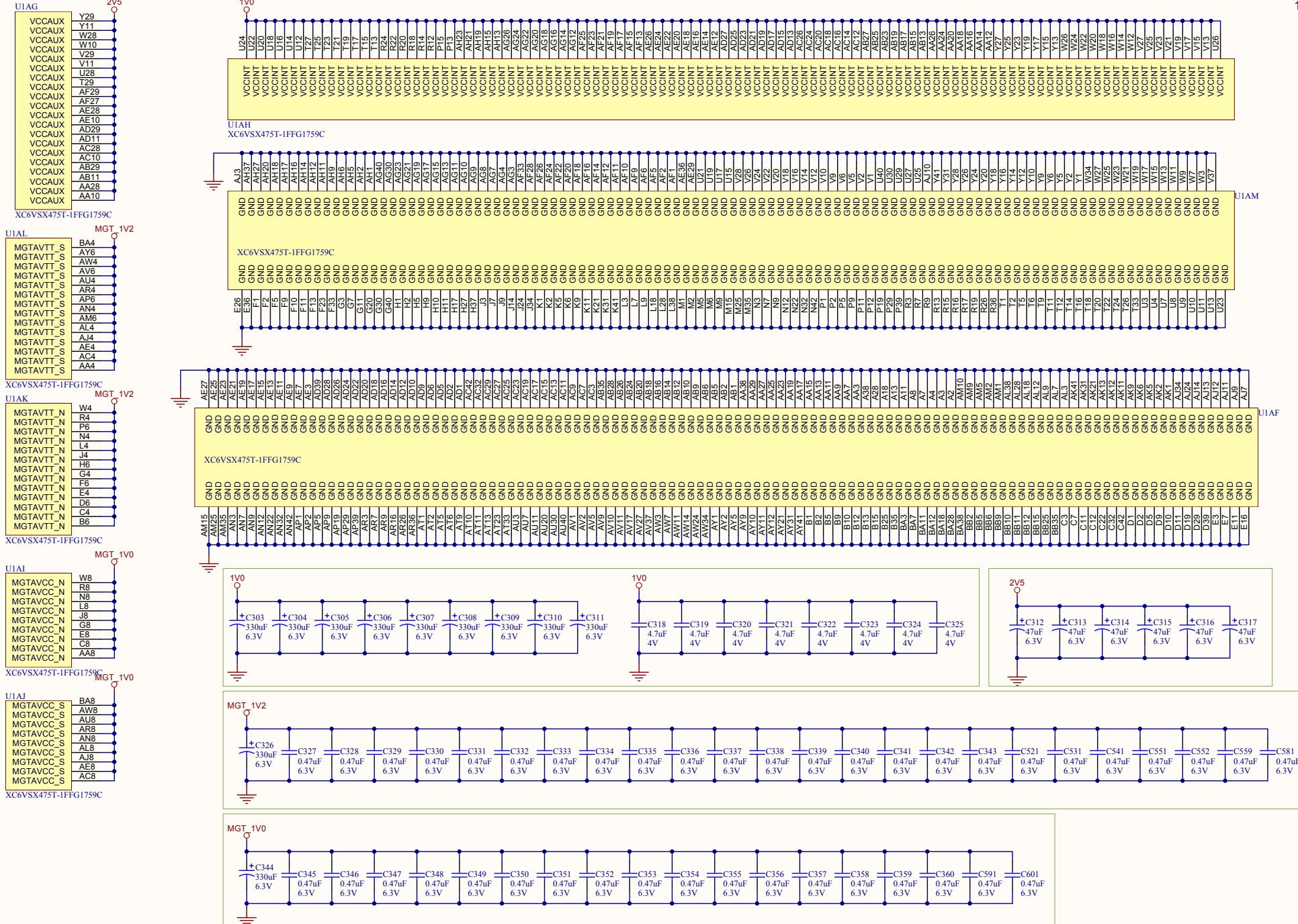
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I/O, CDRST	44
I/O, GCK2	47
I/O, DGE	48
I/O	49
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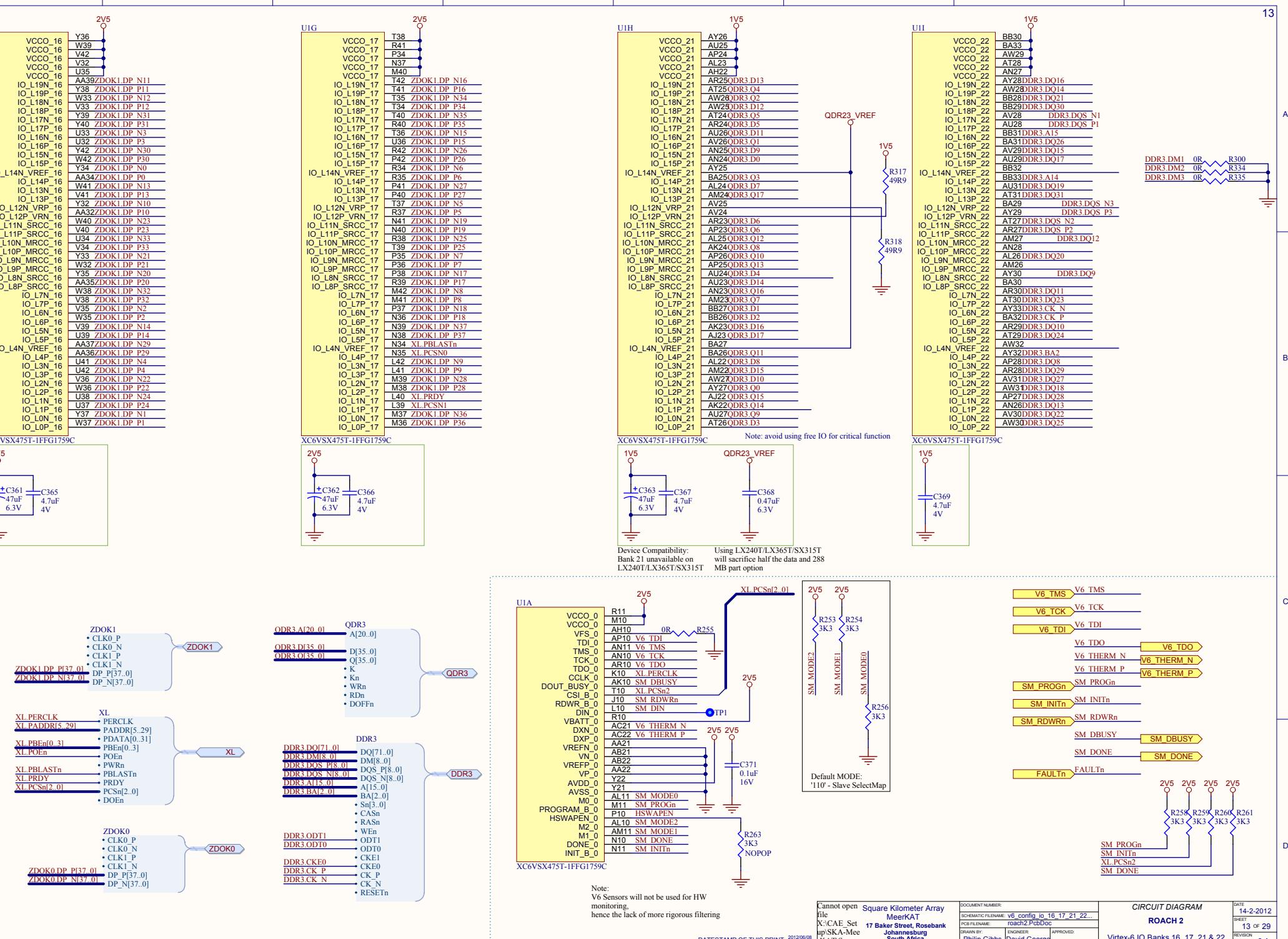
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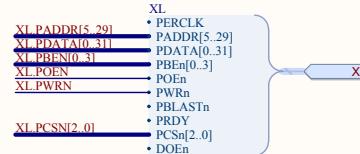
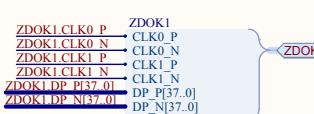
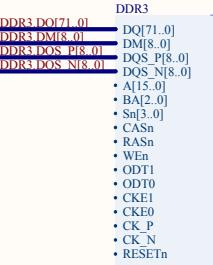
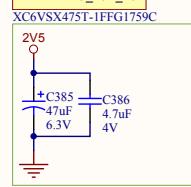
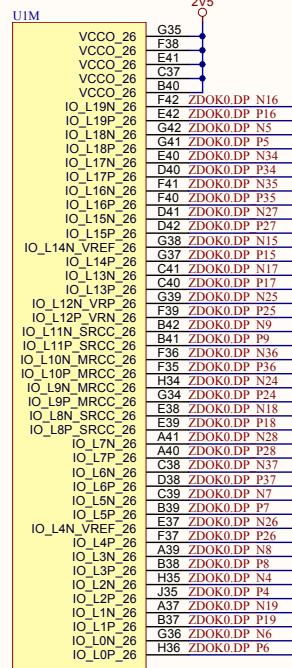
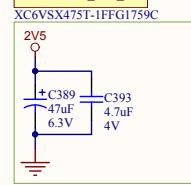
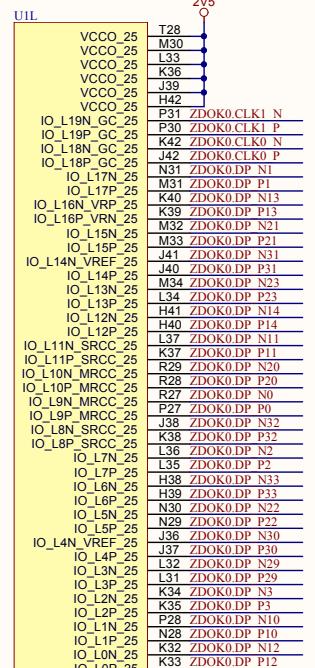
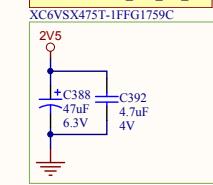
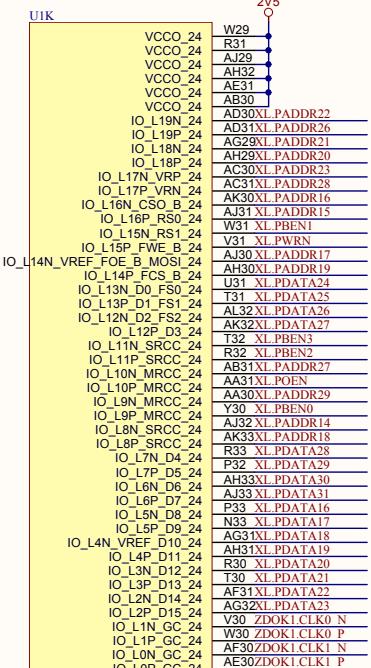
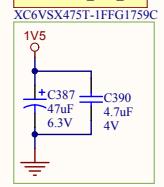
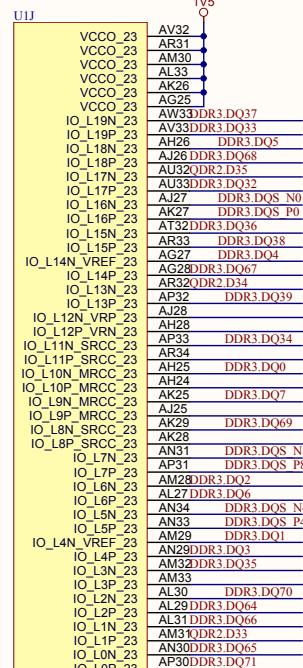


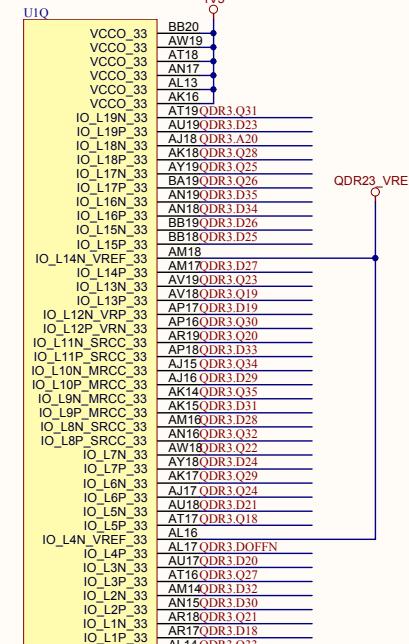
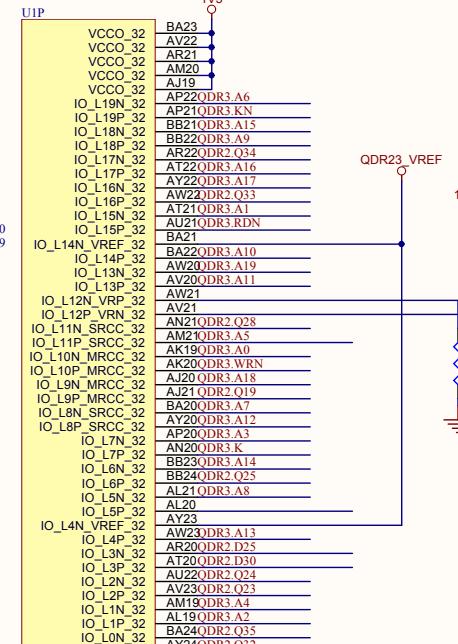
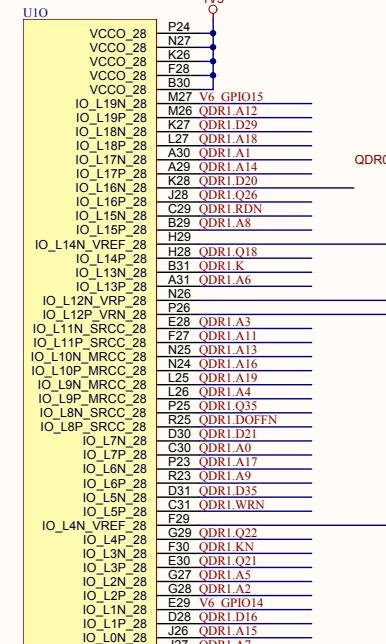
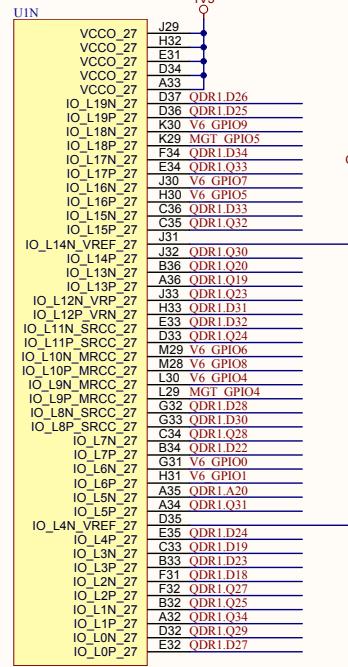
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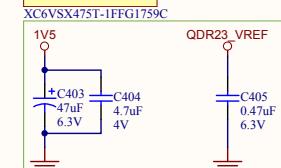
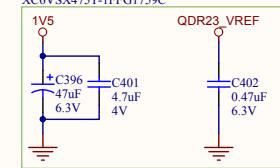
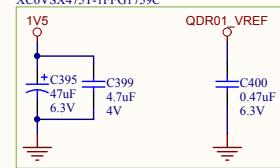
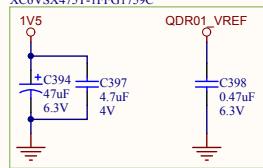


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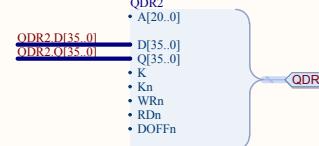
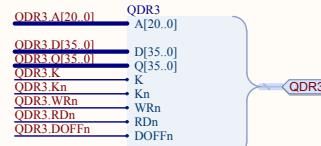
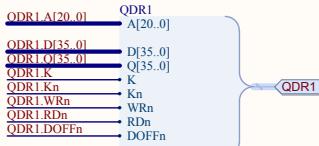


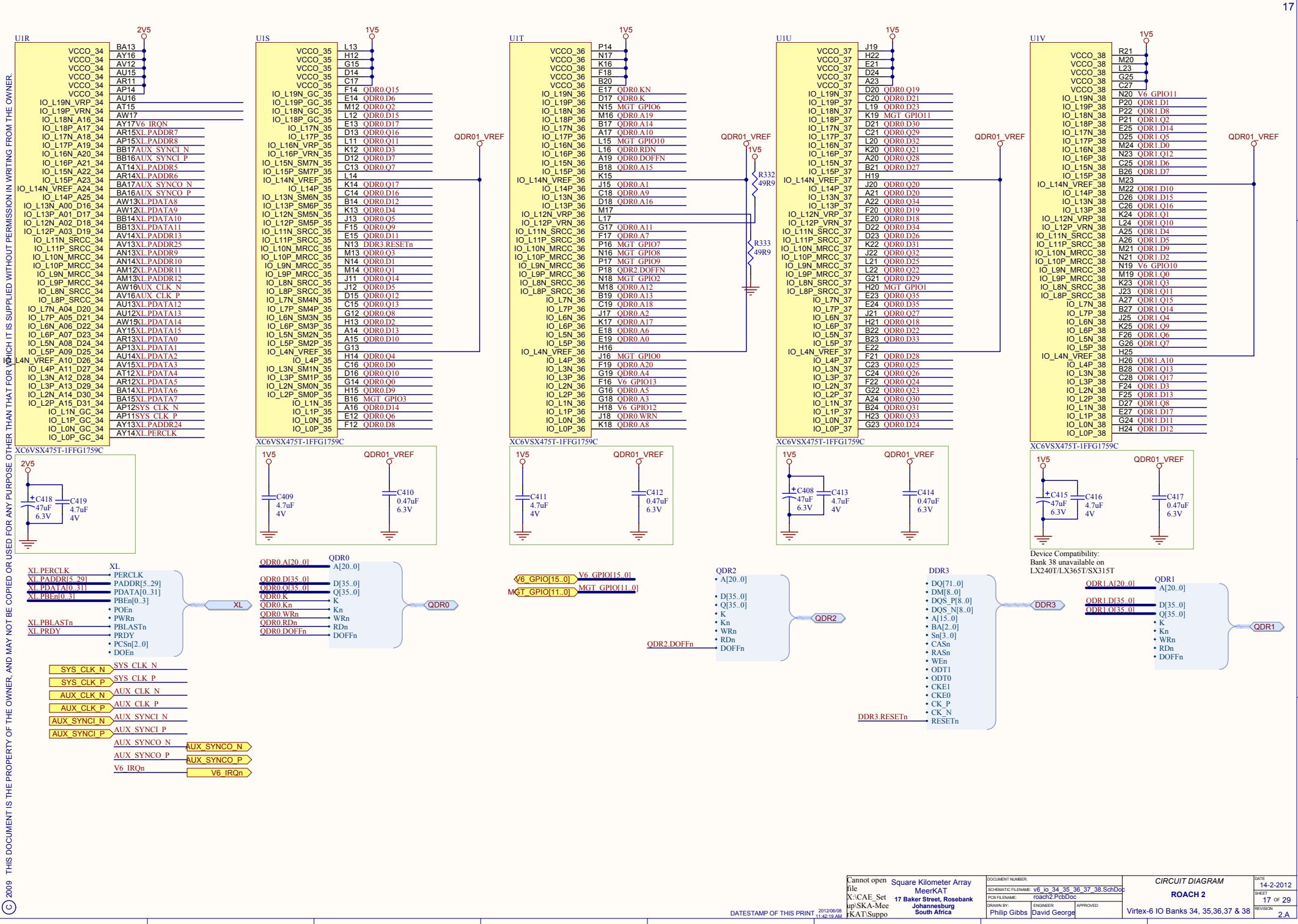


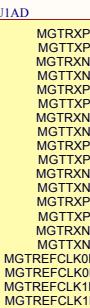
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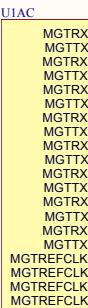
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LX240T/LX365T/SX315T



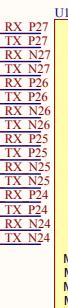




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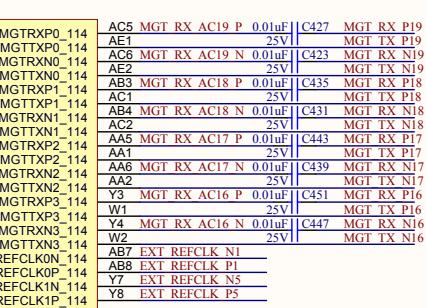


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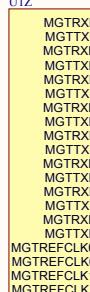
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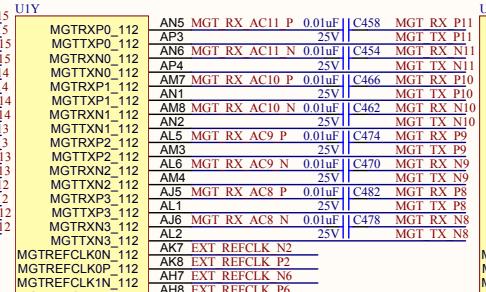


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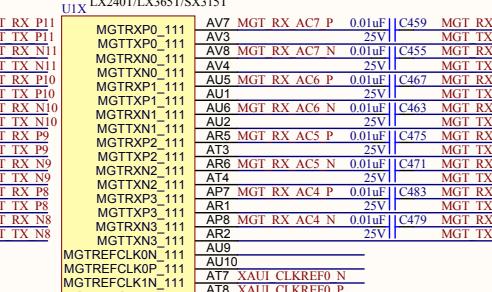
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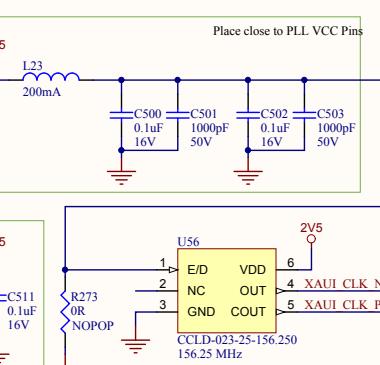
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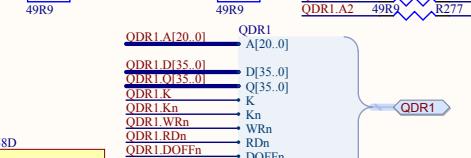
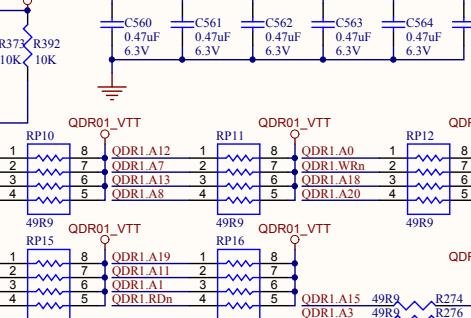
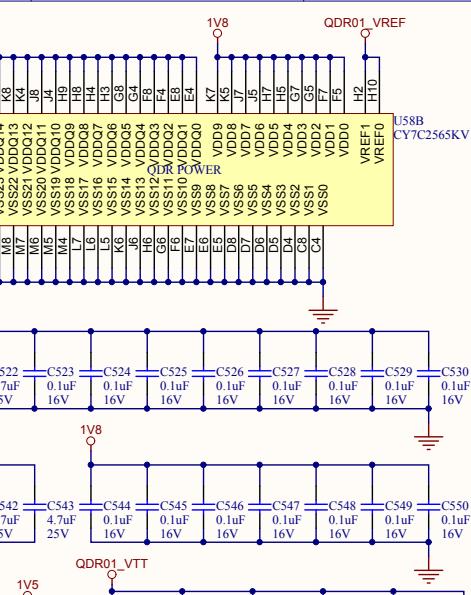
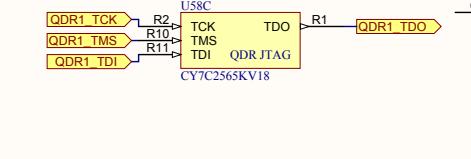
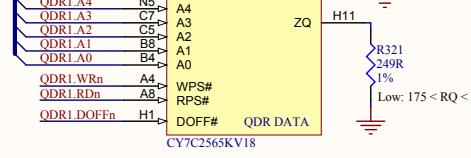
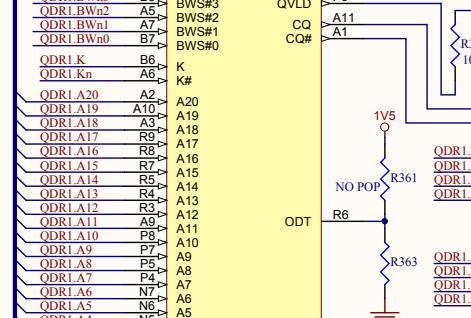
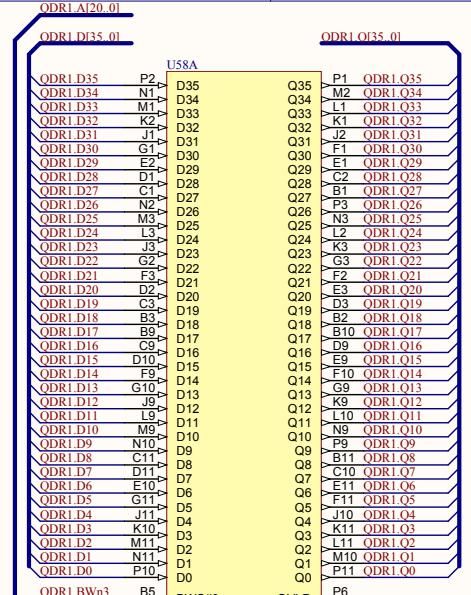
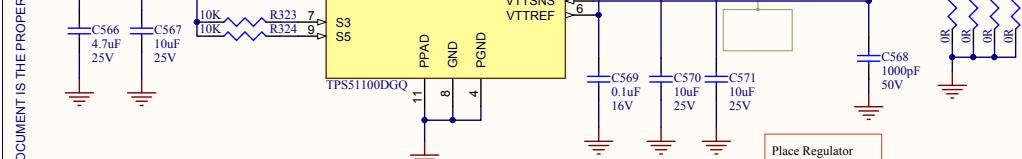
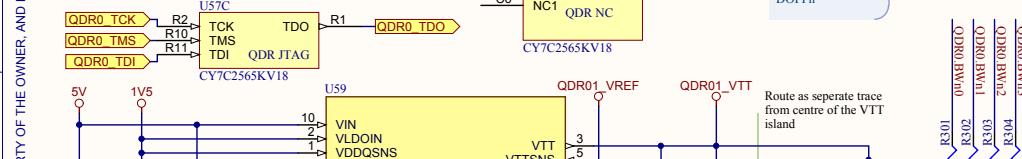
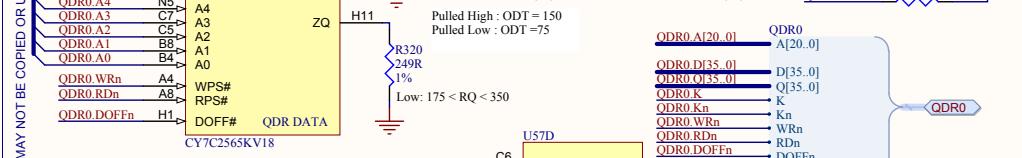
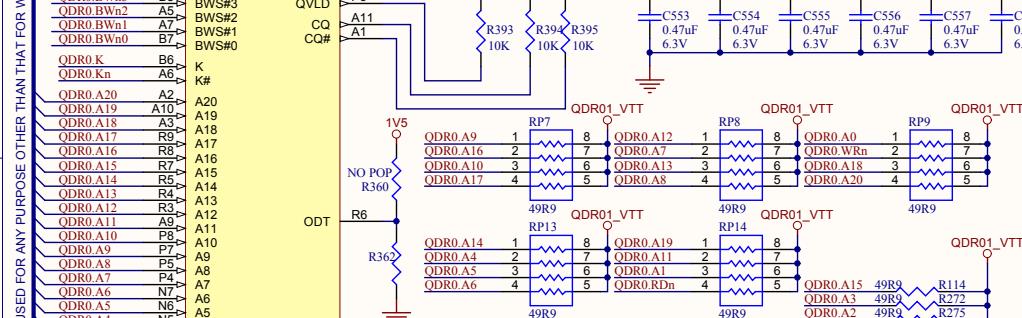
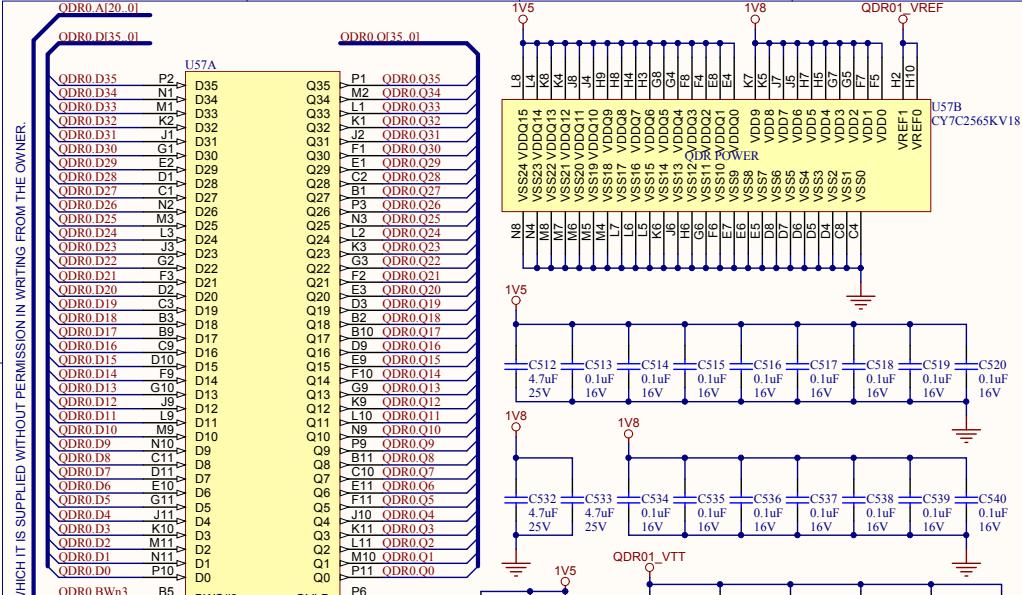
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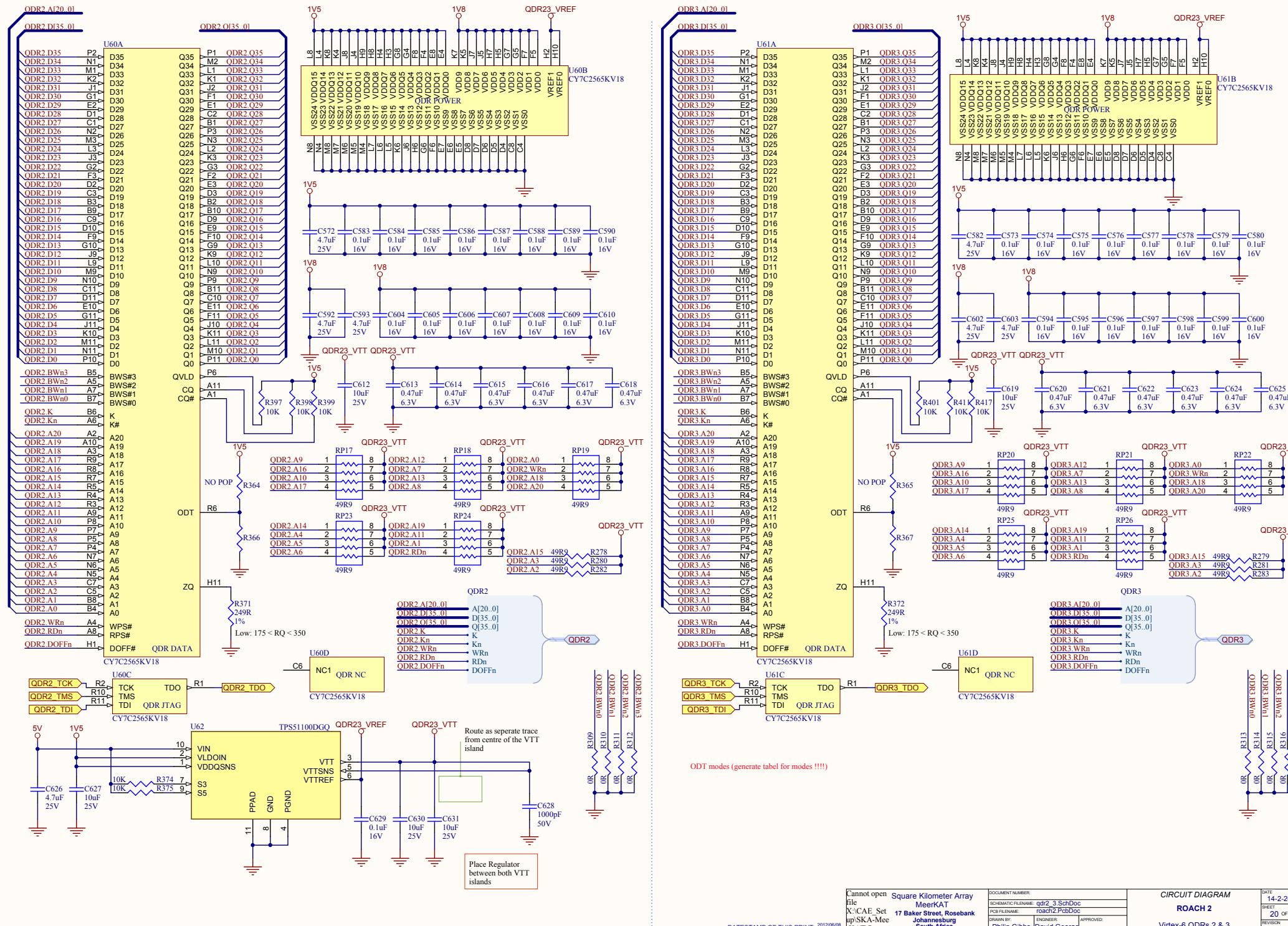
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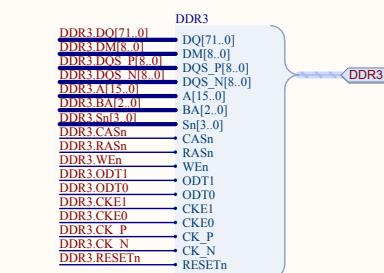
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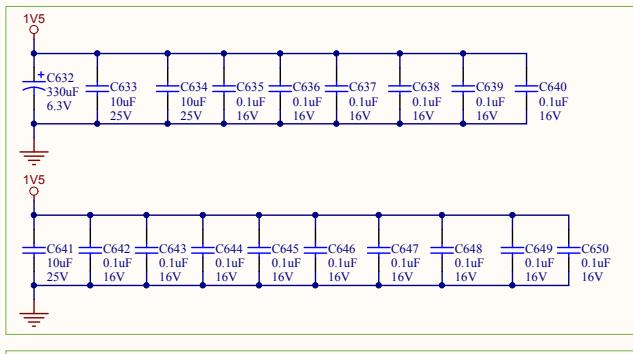
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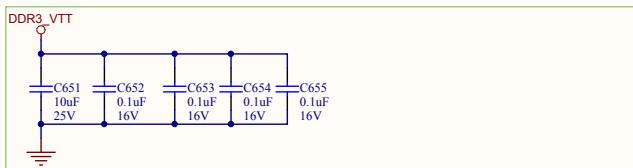
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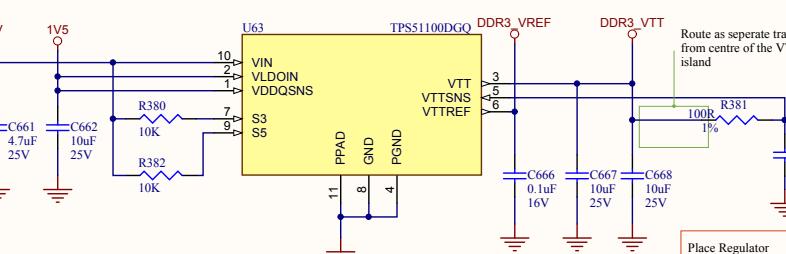
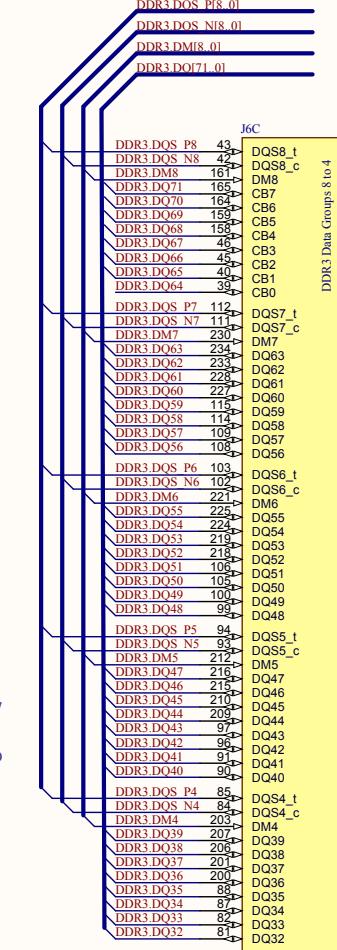
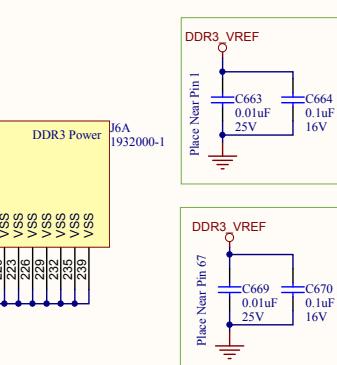
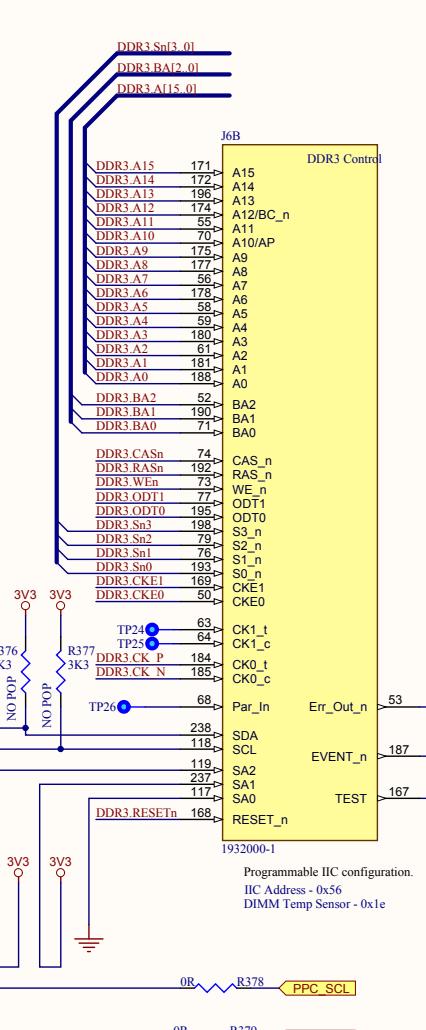
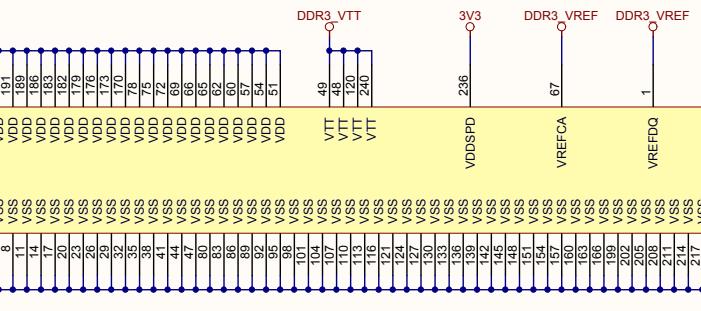
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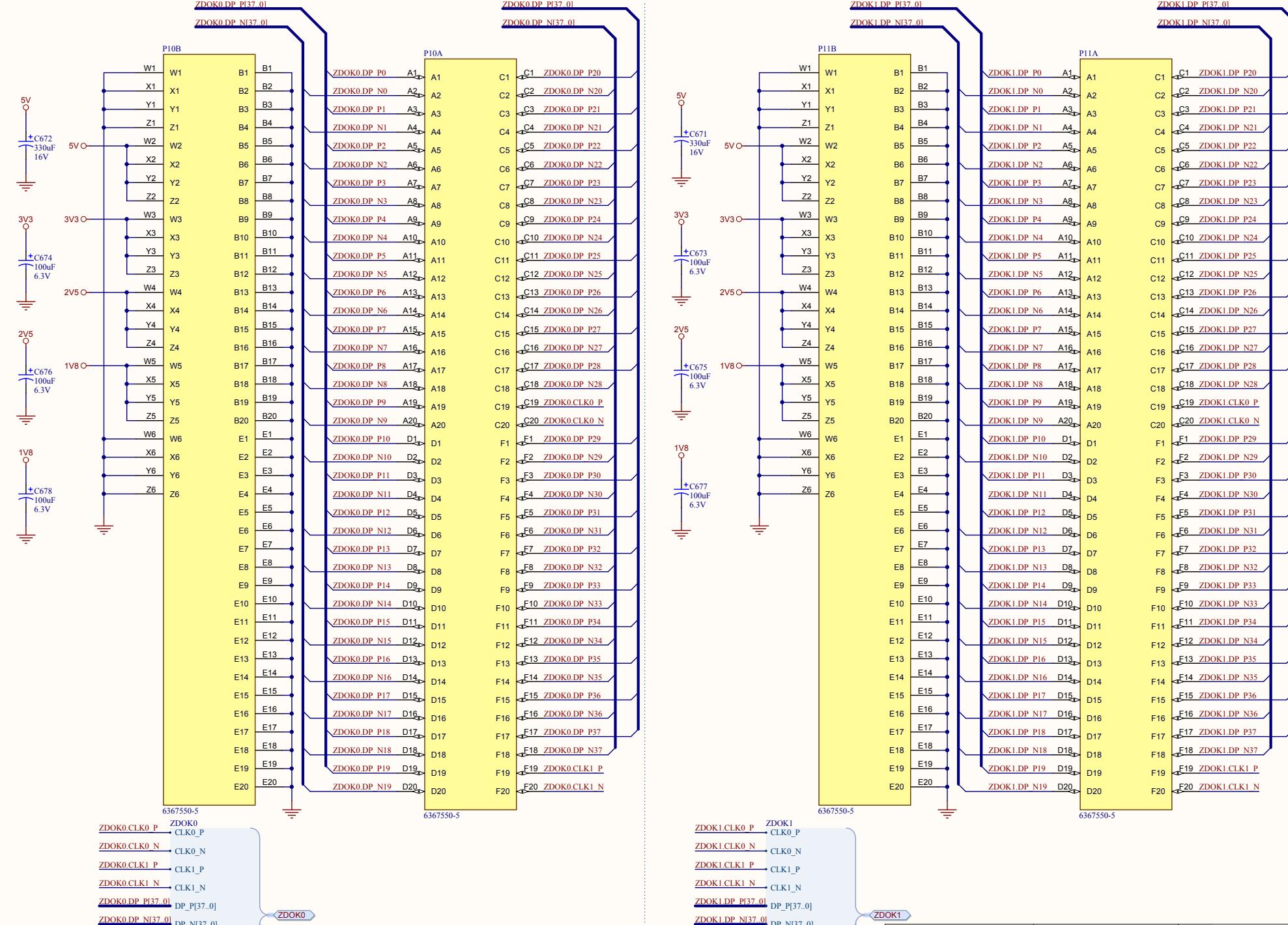
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Philip Gibbs
ENGINEER:
David George
APPROVED:

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Virtex-6 DDR3 DIMM
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SHEET: 21 OF 29
REVISION: 2.A

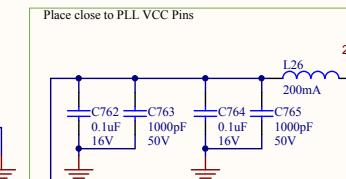
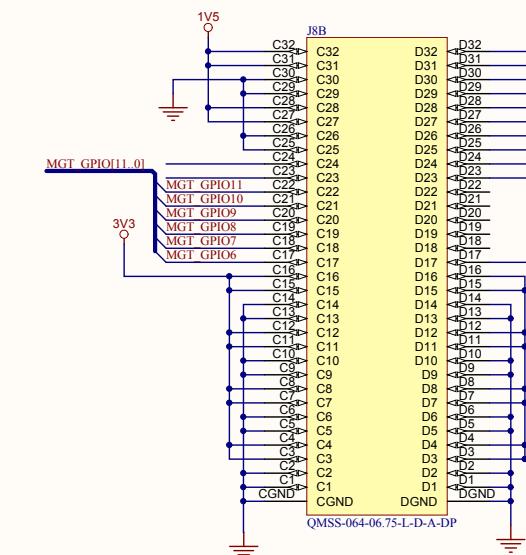
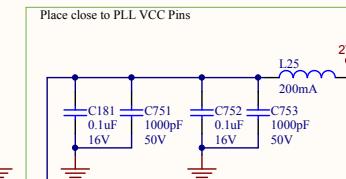
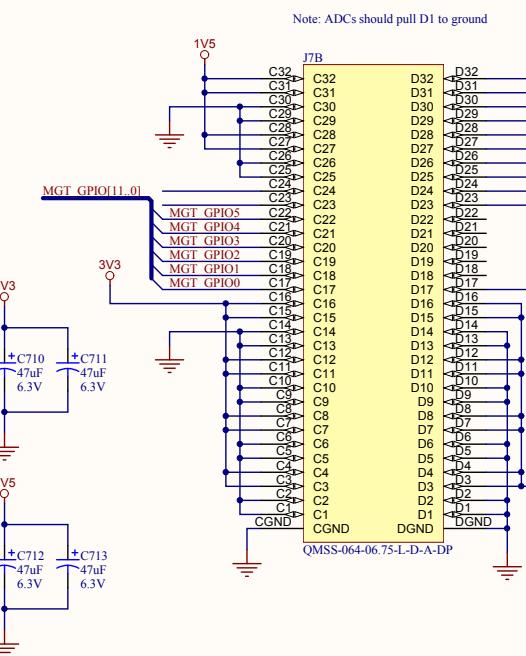
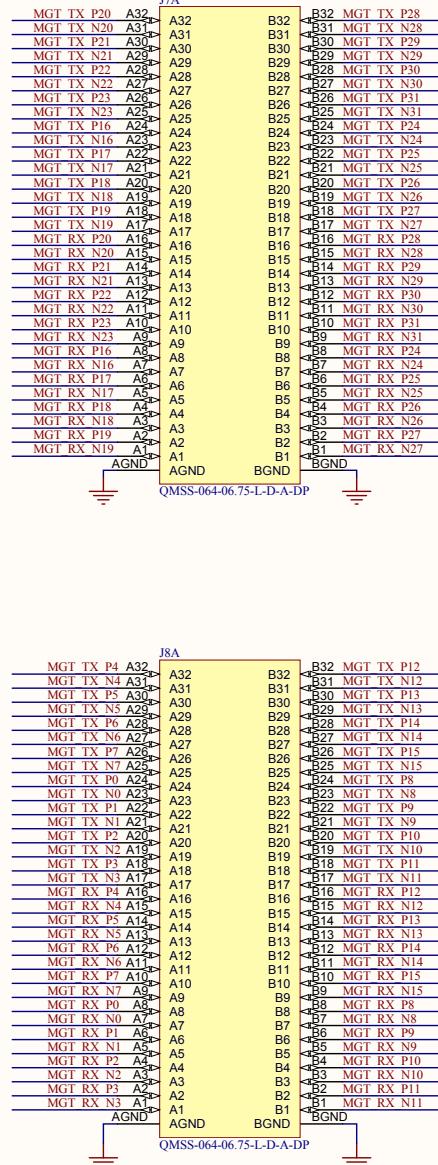
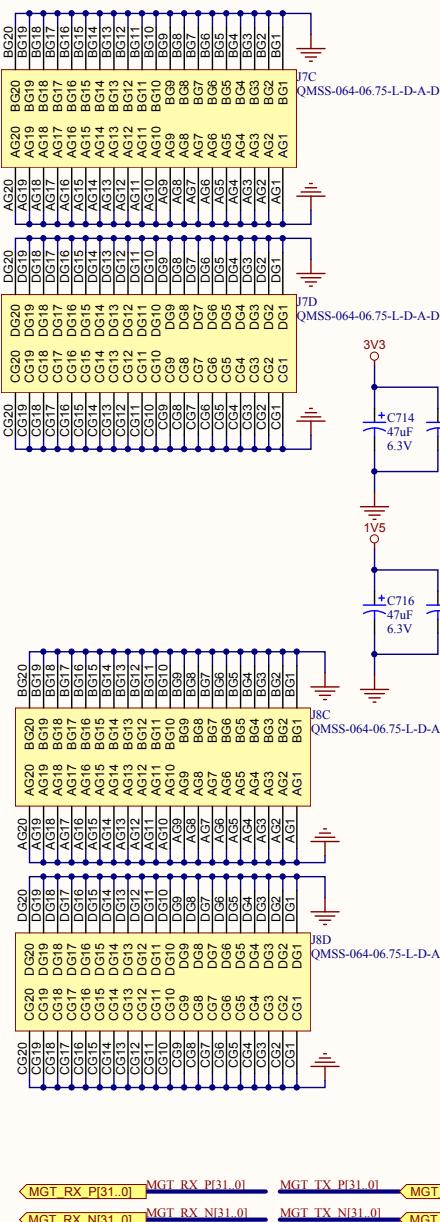
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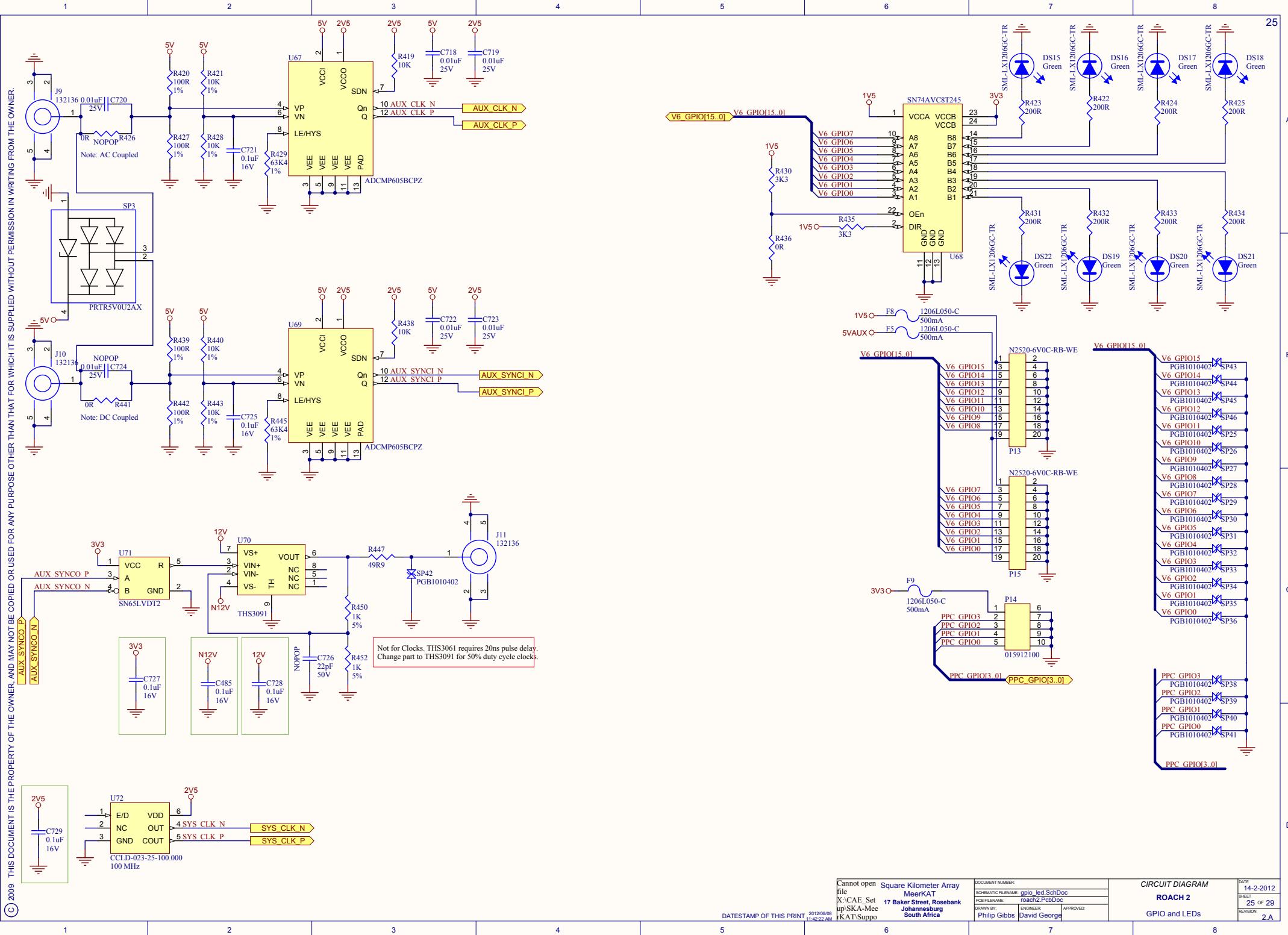
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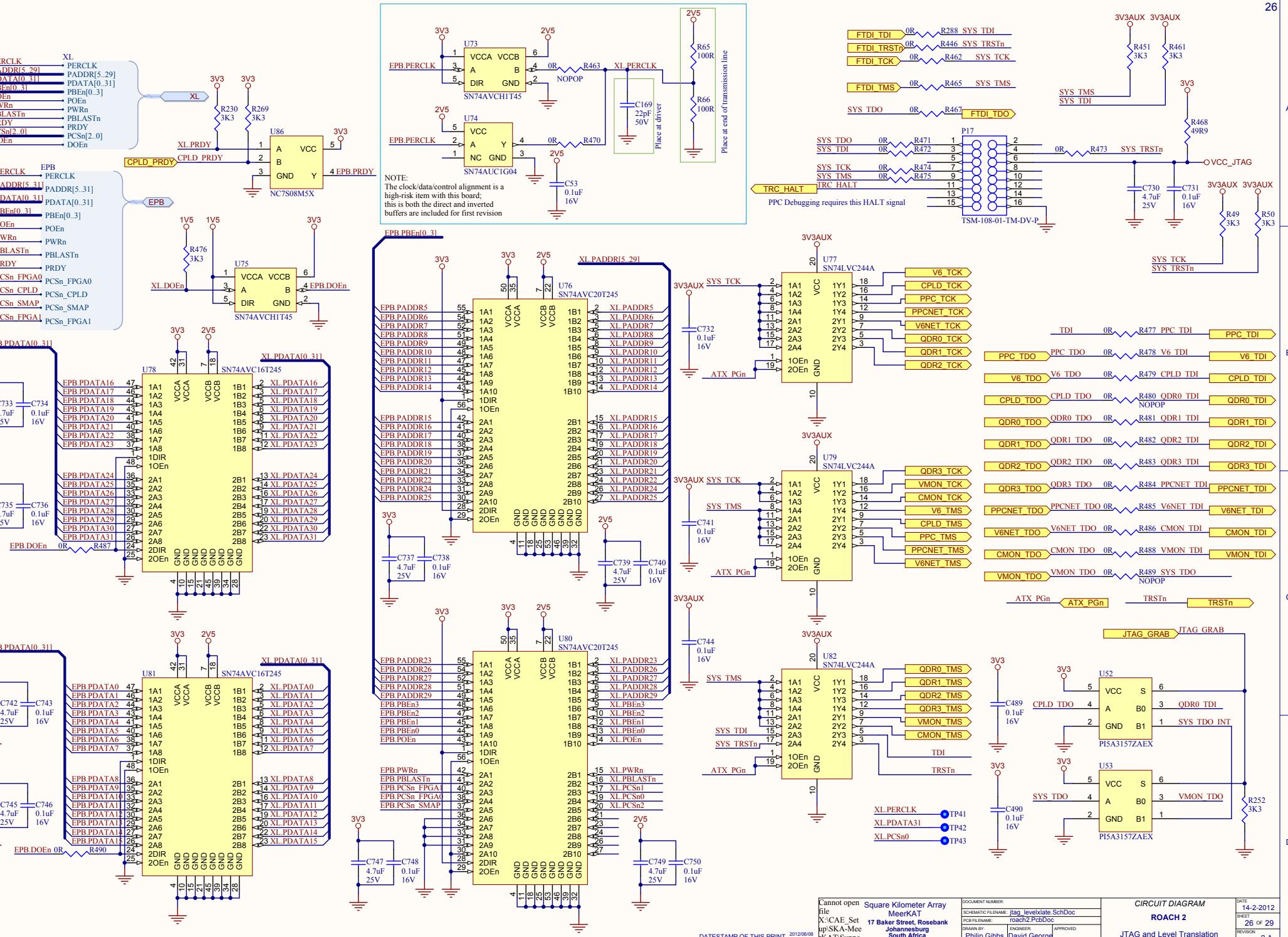
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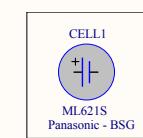
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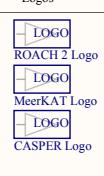
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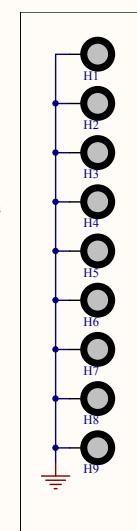
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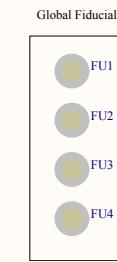
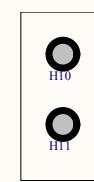
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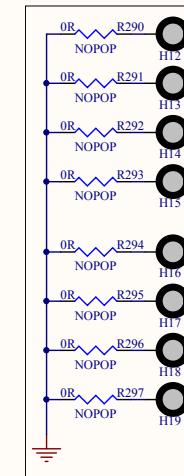
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ATX FAN Mounting Holes



Mezzanine Card Mounting Holes



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DRAWN BY: Philip Gibbs
ENGINEER: David George
APPROVED:

CIRCUIT DIAGRAM
ROACH 2
Miscellaneous Design Items
DATE 14-2-2012
SHEET 27 OF 29
REVISION 2.A

