Add A Programmable Sound Generator

Connecting The General Instruments AY-3-8910 Programmable Sound Generator To The 6502/6800 Bus

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The AY-3-8910 sound generator is a particularly versatile device capable of generating three simultaneous tones, each of which can be separately controlled in amplitude and/or mixed with noise to produce a wide range of sound effects. The particular merit of the GI chip, compared to other sound generators, is that its operation is entirely digitally controlled, making it suitable for use with a microprocessor.

In addition to its sound generator functions, the AY-3-8910 also features two 8-bit wide general purpose I/O ports (labelled IOA and IOB in the pin diagram of Fig. 1). All functions are controlled by sixteen internal registers accessed by a combined data and address 8 bit port (DA0-7 in Fig. 1). The AY-3-8910 is designed principally for use with GI's PIC1600 and 1650 series of microprocessor with bus control pins BC1, BC2 and BDIR determining whether the DA0-7 lines are to be interpreted as address or data lines.

The combined function of the DA0-7 lines do not allow for easy interfacing to other microprocessors such as the 6502 and 6800 series. One method of interfacing that has been proposed uses a 6820 programmable interface adaptor (PIA) with 8 lines of port A connected to the DA0-7 pins of the sound generator and three of the port B lines for the three bus control pins.

This means of interfacing makes programming the sound chip cumbersome. One needs to simulate the bus waveforms shown in Fig 2. Assuming that one is writing in BASIC, then two POKE commands are needed to set up the 6820 ports as outputs. Then one needs a POKE to send the address of the required internal register to the DA0-7 pins, another POKE to send LATCH ADDRESS to the bus control pins, a third POKE to send BUS INACTIVE, followed by a fourth POKE to send the data to the DA0-7 pins, a fifth POKE to send WRITE DATA to the bus control pins, and a sixth POKE to return the bus control pins to BUS INACTIVE. These last six POKES must be repeated for each of the sixteen internal registers needing input.

Why can one not make the sixteen registers in the sound generator part of the addressable memory of the microprocessor? Then a single POKE to the relevant address would be all that is needed.

The reason that this is not straightforward is that the AY-3-8910 is too slow to respond to the 1uS processor cycle of the 6502/6800 families. Following a falling edge of the 02 clock the minimum time intervals needed are:

delay until the processor address is valid	**300 nS**
AY-3-8910 address set up time	**400 nS**
AY-3-8910 address hold time	**100 nS**
AY-3-8910 data set up time	**50 nS**
AY-3-8910 data pulse width	**500 nS**
AY-3-8910 data hold time	**100 nS**
	1.45uS

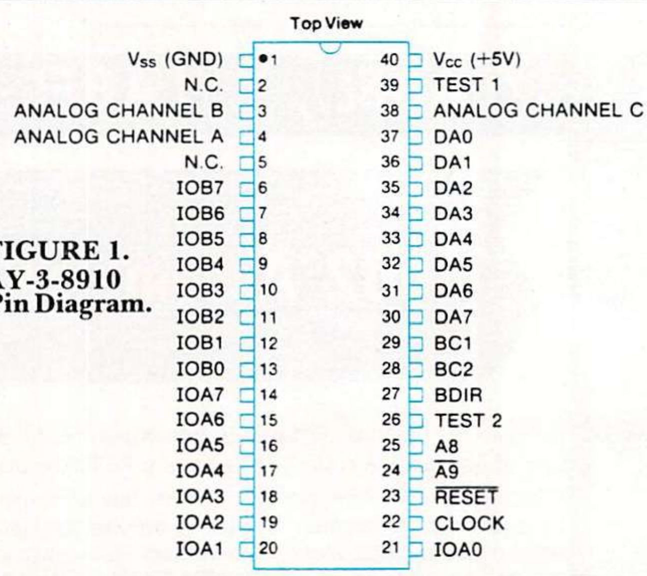

FIGURE 1. AY-3-8910 Pin Diagram.

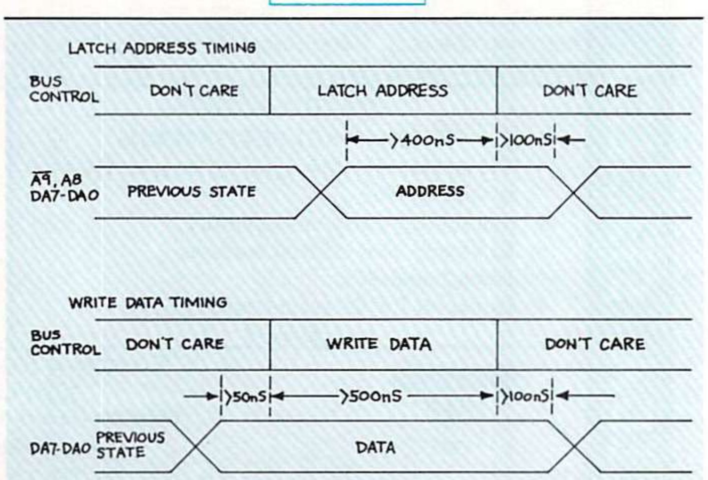

FIGURE 2. Sound Generator Timing (Write Mode).

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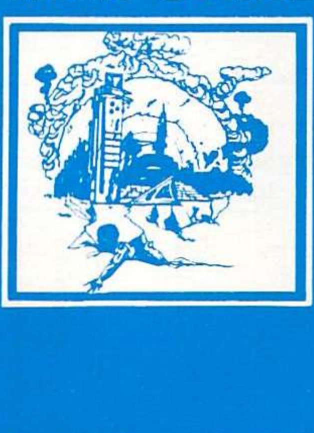

WORLD WAR III — This is a three scenario war game in Hires graphics with sound. It is not merely the conversion of a board game to computer, nor are your pieces represented by lifeless text charcters. It may be played by two persons and takes about 8 hours to complete. The rules are simple enough that you won't have to spend several days reading your manual before you can play. It contains 2 world maps and a fairly detailed map of the Iran-Iraq battle field. All scoring, animation, and positions are handled by the computer — no separate tablets to fool with. Moves are input by both players in series of 3 and when the space bar is pressed the battle becomes animated. A must see to believe $29.95

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The solution is to deliberately spread the writing to the sound chip over two processor cycles. The circuit in Fig. 3 does this. The relevant signal waveforms are shown in Fig. 4. Circuits IC1 and IC2 decode the top eight address lines A15-8 and their outputs feed the additional address select pins A8 and A9 on the sound generator IC8. The quiescent state of IC5 leaves a one on its terminal Q and a zero on Q, the latter enabling the tristate output of IC3 and thereby applying the lower address lines A7-A0 to the combined data/address pins of the sound generator. The first half of the dual monostable IC7 triggers off each falling edge of 02 and produces a 300 nS pulse. The back edge of this pulse triggers the second half generating a delayed 550nS pulse. This latter pulse is applied to pin BDIR of the sound generator, which together with the output Q of IC5 on BC1 (also high during this period) codes LATCH ADDRESS on the bus control pins. The LATCH ADDRESS condition terminates 150nS before the computer address lines A15-A0 change. Only the lowest four address lines A3-A0, of the eight A7-A0 lines, address a register in the sound generator, if the other four lines A7-A4 are not zero, or if A8 and A9 are not 10 respectively then the address is invalid and the sound generator takes no further action.

On the next falling edge of 02 (rising edge of 02), two things happen. The data on the data lines D7-D0 from the microprocessor are latched into IC4, and the low, now on pin D of IC5, is clocked through to the Q terminal. This latter signal enables the tristate output of IC4 at the same time

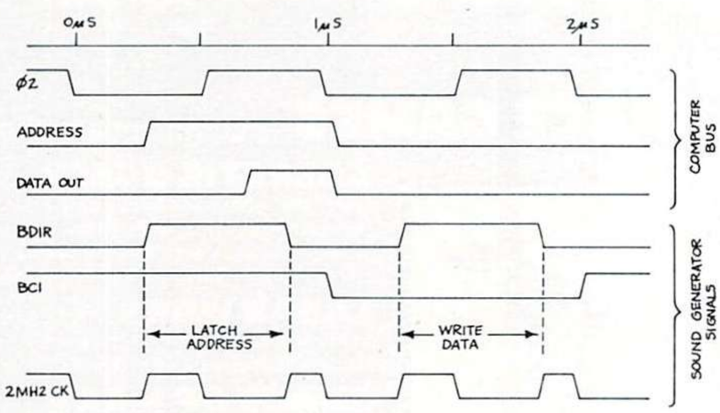
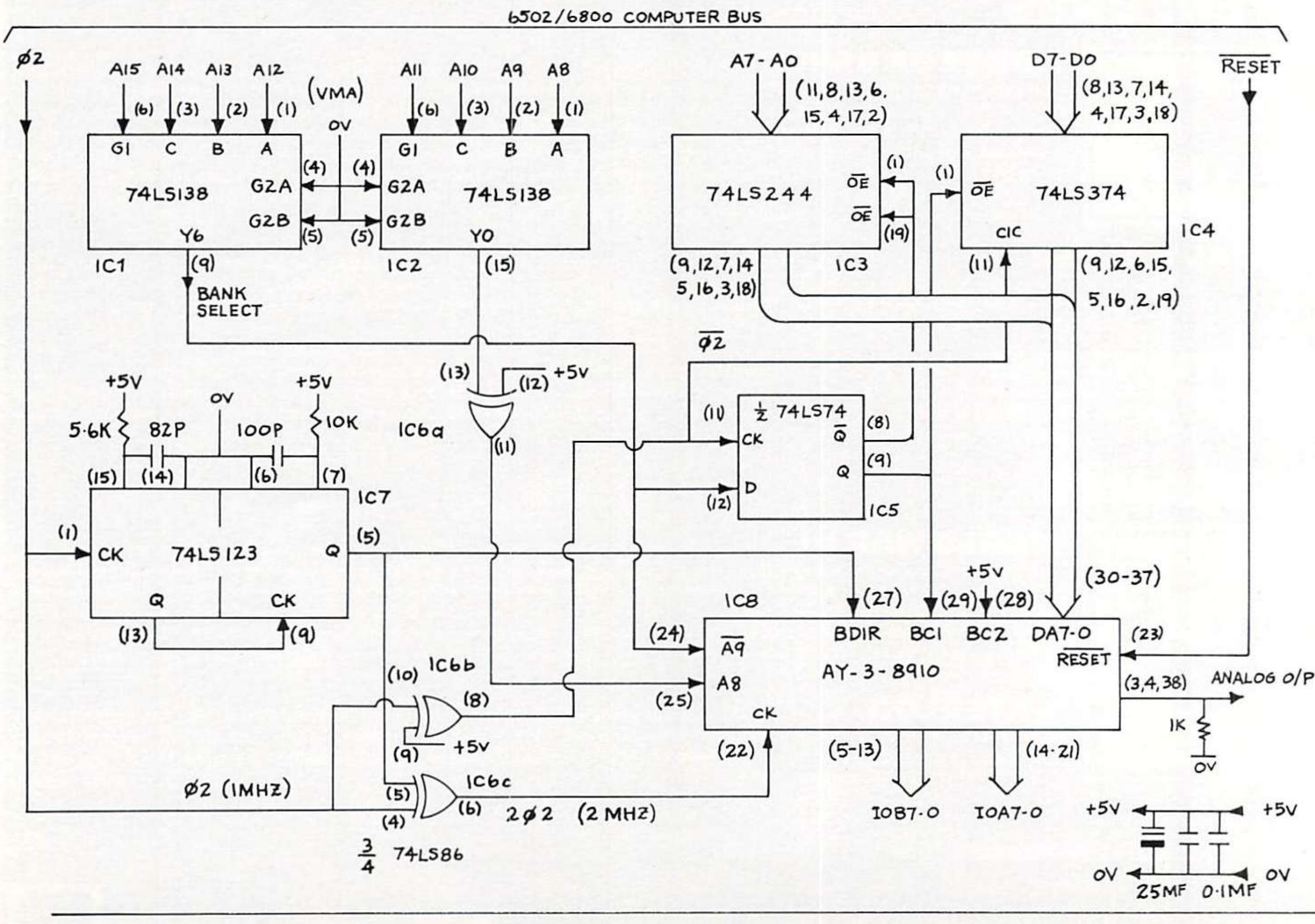


FIGURE 4. Signal Timing.

FIGURE 3. AY-3-8910. Memory Mapped On The 6502/6800 Bus.



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as the output of IC3 is disabled. Data, not address, is now applied to the combined data/address lines of the sound generator IC8. The monostables continue to produce delayed 550nS pulses and, when BDIR is high again, BC1 is now low giving a READ DATA command to the sound generator. Circuit IC6c is an exclusive OR which inverts 02 whenever the monostable output is high. The result is to convert the 1 MHz 02 into a 2MHz clock which is fed to the clock terminal of the sound generator. This 2MHz clock enables the generation of more precise tones at the higher frequencies than a 1MHz clock would allow. (See Table 1.) Circuits IC6a and IC6b are simple inverters and could be replaced by a 74LS04 if the frequency doubling function of IC6a is not required.

I have constructed the circuit for use with a Commodore PET. For this purpose I do not really need IC1, since it duplicates the Bank Select signals which are available on this expansion bus. I have chosen to place the sound generator at memory addresses E800 to E80F, which is in the I/0 area of the PET. Other addresses are possible by choosing different outputs of IC1 and IC2, and possibly the use of the G2 chip select pins. If the circuit is used with the 6800 processor, then VMA should be connected to one of the G2 select pins.

The circuit achieves the objective of permitting POKES directly to the sound generator registers and is only slightly more complex than the use of a 6820 PIA, if one includes the chip select decoding that is also necessary with the PIA. One function that my circuit does not allow is the reading of the register data. To add this feature is not difficult, although it will require a double PEEK: one to strobe in the address, and the second to read the data. There seems little purpose in having a read function. I have yet to use the two output data ports IOA and IOB, but plan them for two D to A converters to provide, additionally, two directly synthesized tone channels.

TABLE 1. Coarse (HI) And Fine (LO) Tuning Register Values Using A 2MHZ Clock.

NOTE		--- FREQUENCY (HZ) --- IDEAL	ACTUAL	ERROR	POKE HI	LO
C	1	32.70	32.71	.0%	14	238
C#	1	34.65	34.65	.0%	14	24
D	1	36.71	36.71	.0%	13	77
D#	1	38.89	38.89	.0%	12	142
E	1	41.20	41.20	.0%	11	218
F	1	43.65	43.66	.0%	11	47
F#	1	46.25	46.24	.0%	10	143
G	1	49.00	49.00	.0%	9	247
G#	1	51.91	51.91	.0%	9	104
A	1	55.00	54.99	.0%	8	225
A#	1	58.27	58.28	.0%	8	97
B	1	61.74	61.73	.0%	7	233
C	2	65.41	65.41	.0%	7	119
C#	2	69.30	69.29	.0%	7	12
D	2	73.42	73.40	.0%	6	167
D#	2	77.78	77.78	.0%	6	71
E	2	82.41	82.40	.0%	5	237
F	2	87.31	87.29	.0%	5	152
F#	2	92.50	92.52	.0%	5	71
G	2	98.00	97.96	.0%	4	252
G#	2	103.83	103.82	.0%	4	180
A	2	110.00	110.04	.0%	4	112
A#	2	116.54	116.50	.0%	4	49
B	2	123.47	123.52	.0%	3	244
C	3	130.81	130.75	.0%	3	188
C#	3	138.59	138.58	.0%	3	134
D	3	146.83	146.89	.0%	3	83
D#	3	155.56	155.47	-.1%	3	36
E	3	164.81	164.91	.1%	2	246
F	3	174.61	174.58	.0%	2	204
F#	3	185.00	184.91	.0%	2	164
G	3	196.00	195.92	.0%	2	126
G#	3	207.65	207.64	.0%	2	90
A	3	220.00	220.07	.0%	2	56
A#	3	233.08	233.21	.1%	2	24
B	3	246.94	247.04	.0%	1	250
C	4	261.63	261.51	.0%	1	222
C#	4	277.18	277.16	.0%	1	195
D	4	293.66	293.43	-.1%	1	170
D#	4	311.13	310.95	-.1%	1	146
E	4	329.63	329.82	.1%	1	123
F	4	349.23	349.16	.0%	1	102
F#	4	369.99	369.82	.0%	1	82
G	4	392.00	391.85	.0%	1	63
G#	4	415.30	415.28	.0%	1	45
A	4	440.00	440.14	.0%	1	28
A#	4	466.16	466.42	.1%	1	12
B	4	493.88	494.07	.0%	0	253
C	5	523.25	523.01	.0%	0	239
C#	5	554.37	555.56	.2%	0	225
D	5	587.33	586.85	-.1%	0	213
D#	5	622.25	621.89	-.1%	0	201
E	5	659.26	657.89	-.2%	0	190
F	5	698.46	698.32	.0%	0	179
F#	5	739.99	739.64	.0%	0	169
G	5	783.99	786.16	.3%	0	159
G#	5	830.61	833.33	.3%	0	150
A	5	880.00	880.28	.0%	0	142
A#	5	932.33	932.84	.1%	0	134
B	5	987.77	984.25	-.4%	0	127
C	6	1046.50	1050.42	.4%	0	119
C#	6	1108.73	1106.19	-.2%	0	113
D	6	1174.66	1179.25	.4%	0	106
D#	6	1244.51	1250.00	.4%	0	100
E	6	1318.51	1315.79	-.2%	0	95
F	6	1396.91	1404.49	.5%	0	89
F#	6	1479.98	1488.10	.5%	0	84
G	6	1567.98	1562.50	-.3%	0	80
G#	6	1661.22	1666.67	.3%	0	75
A	6	1760.00	1760.56	.0%	0	71
A#	6	1864.66	1865.67	.1%	0	67
B	6	1975.53	1984.13	.4%	0	63
C	7	2093.00	2083.33	-.5%	0	60
C#	7	2217.46	2232.14	.7%	0	56
D	7	2349.32	2358.49	.4%	0	53
D#	7	2489.02	2500.00	.4%	0	50
E	7	2637.02	2659.57	.9%	0	47

F	7	2793.83	2777.78	-.6%	0	45
F#	7	2959.96	2976.19	.5%	0	42
G	7	3135.96	3125.00	-.3%	0	40
G#	7	3322.44	3289.47	-1.0%	0	38
A	7	3520.00	3472.22	-1.4%	0	36
A#	7	3729.31	3676.47	-1.4%	0	34
B	7	3951.07	3906.25	-1.1%	0	32
C	8	4186.01	4166.67	-.5%	0	30
C#	8	4434.92	4464.29	.7%	0	28
D	8	4698.64	4629.63	-1.5%	0	27
D#	8	4978.03	5000.00	.4%	0	25
E	8	5274.04	5208.33	-1.2%	0	24
F	8	5587.65	5681.82	1.7%	0	22
F#	8	5919.91	5952.38	.5%	0	21
G	8	6271.93	6250.00	-.3%	0	20
G#	8	6644.88	6578.95	-1.0%	0	19
A	8	7040.00	6944.44	-1.4%	0	18
A#	8	7458.62	7352.94	-1.4%	0	17
B	8	7902.13	7812.50	-1.1%	0	16

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