Hexagons are the Bestagons: Design Automation for Silicon Dangling Bond Logic

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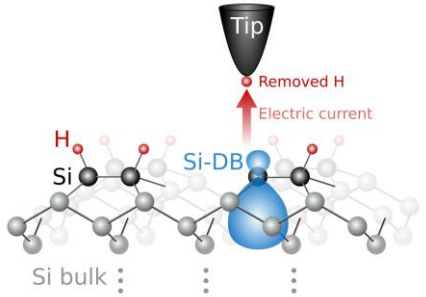
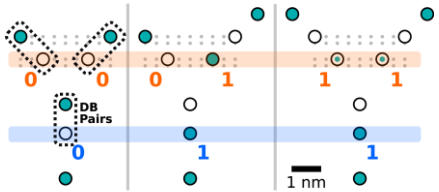
Abstract

Recent breakthroughs in the fabrication of ***Silicon Dangling Bonds*** (SiDBs) acting as **quantum dots** enabled the demonstration of logic gates **at the limit of scaling**. However, design automation for the SiDB technology platform does not yet exist. This work establishes a flexible layout topology based on a **hexagonal** tiling as well as a corresponding ML-generated ***Bestagon*** gate library, and additionally, provides **automatic methods** for physical design. All design, simulation, and code files are publicly available on ***GitHub***.

Nanoscale Fabrication

SiDBs on the H-Si(100)-2×1 surface can act as **atomically-sized quantum dots**. The surface has discretely defined sites where SiDBs can be fabricated with atomic precision using the probe of a **scanning tunneling microscope**.

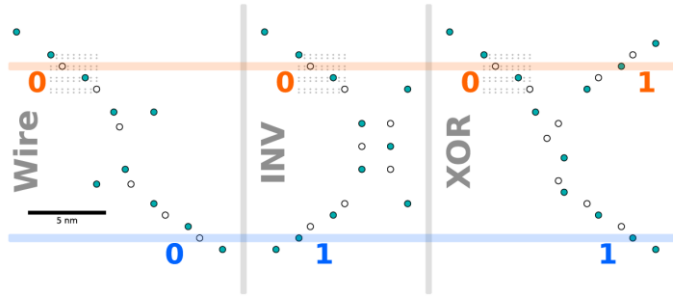


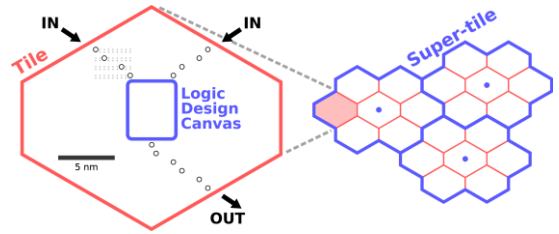


In 2018, *Huff et al.* have **experimentally demonstrated** that SiDBs can be used to construct **logic components**. These are, however, **Y-shaped** and to not fit in with established design flows in the domain. Furthermore, only a single gate has been shown, thus the approach is not yet **computationally universal**.

Logic Design at the Limit of Scaling – Our Contribution

We aim at establishing the first physically sound **design flow** for SiDBs. To this end, this work heavily considers the **experimentally proven implementations**, existing **physical models**, and **realistic fabrication capabilities** of s-o-t-a lithography. Our design flow starts with **netlist descriptions** (e.g., gate-level Verilog), performs logic optimization, technology mapping, placement & routing, equivalence checking, and physical simulation of the obtained **dot-accurate circuit layouts**.





- **Bestagon Gate Library**: ML-generated hexagonal standard component tiles, carefully attuned to the SiDB technology constraints.
- **Design Rule Framework**: Respects current fabrication technology for clocking electrodes, physical limitations of Coulombic bias, and similar constraints.
- **Physical Design Flow**: Automatically generates dot-accurate SiDB circuit layouts from netlist specifications.

Open Source & Open Data

All design and simulation files as well as our code to **reproduce the experiments** have been made **publicly available on *GitHub***. Thereby, we support ***Open Research*** and enable the community to build upon our findings.

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