Inferred Port Mapping for the AMD Zen+ Microarchitecture

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This port mapping was inferred with the technique described in the paper *Explainable Port Mapping Inference with Sparse Performance Counters for AMD's Zen Architectures* by Fabian Ritter and Sebastian Hack. Limitations and caveats are also discussed there. The columns contain the following information:

Instruction Scheme: An instruction scheme, i.e., an instruction representation that abstracts from concrete operands. Click on one to open the corresponding entry in the ISA reference.

tp^{-1}**:** The inverse throughput we measured for the instruction scheme, i.e., the number of cycles required on average to execute instances of the instruction scheme in a steady state. For instance, an inverse throughput of 0.25 cycles means that 4 instructions are executed simultaneously.

#μ**ops:** The number of micro-operations (μops) observed when executing instances of the instruction scheme. We obtain this number by correcting the readings of a hardware performance counter as described in the paper. If such a correction took place for a particular instruction scheme, the addition is made explicit in the table. An asterisk here marks that the number of μops does not match the number of characterized μops in the port usage.

Port Usage: The ports used by the μops of the instruction scheme. For instance, the port usage $1 \times [a] + 2 \times [b, c]$ means that the instruction scheme is decomposed into one μop that can only be executed on port a and two μops that can be executed on port b or port c. All μops need to be executed when executing an instance of the instruction scheme. An empty entry means that no valid and stable port usage could be inferred in the last stage of the algorithm.

The ports roughly correspond to the following hardware resources:

Port	Resource	Comment
0	FP0	Floating Point and Vector Units
1	FP1	
2	FP2	
3	FP3	
4	AGU	Address Generation Units
5	AGU/store	
6	ALU	Scalar Integer Arithmetic and Logical Units
7	ALU	
8	ALU	
9	ALU	

Instruction Scheme	tp^{-1}	#μops	Port Usage
`add RW:GPR:16, 0x0`	0.25	1	1×[6,7,8,9]
`add RW:GPR:16, IMM(16)`	0.25	1	1×[6,7,8,9]
`add RW:GPR:16, IMM(8)`	0.25	1	1×[6,7,8,9]
`add RW:GPR:16, R:GPR:16`	0.25	1	1×[6,7,8,9]
`add RW:GPR:16, word ptr R:MEM(16)`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`add RW:GPR:32, 0x0`	0.25	1	1×[6,7,8,9]
`add RW:GPR:32, IMM(32)`	0.25	1	1×[6,7,8,9]
`add RW:GPR:32, IMM(8)`	0.25	1	1×[6,7,8,9]
`add RW:GPR:32, R:GPR:32`	0.25	1	1×[6,7,8,9]
`add RW:GPR:32, dword ptr R:MEM(32)`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`add RW:GPR:64, 0x0`	0.25	1	1×[6,7,8,9]
`add RW:GPR:64, IMM(32)`	0.25	1	1×[6,7,8,9]
`add RW:GPR:64, IMM(8)`	0.25	1	1×[6,7,8,9]
`add RW:GPR:64, R:GPR:64`	0.25	1	1×[6,7,8,9]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
add RW:GPR:64, qword ptr R:MEM(64)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
add RW:GPR:8, R:GPR:8	0.25	1	1×[6,7,8,9]
add RW:GPR:8, byte ptr R:MEM(8)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
add byte ptr RW:MEM(8), 0x0	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
add byte ptr RW:MEM(8), IMM(8)	1.36	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
add byte ptr RW:MEM(8), R:GPR:8	1.38	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
add dword ptr RW:MEM(32), 0x0	1.00	1+1	1×[6,7,8,9] + 1×[5]
add dword ptr RW:MEM(32), IMM(32)	1.00	1+1	1×[6,7,8,9] + 1×[5]
add dword ptr RW:MEM(32), IMM(8)	1.00	1+1	1×[6,7,8,9] + 1×[5]
add dword ptr RW:MEM(32), R:GPR:32	1.00	1+1	1×[6,7,8,9] + 1×[5]
add qword ptr RW:MEM(64), 0x0	1.00	1+1	1×[6,7,8,9] + 1×[5]
add qword ptr RW:MEM(64), IMM(32)	1.00	1+1	1×[6,7,8,9] + 1×[5]
add qword ptr RW:MEM(64), IMM(8)	1.00	1+1	1×[6,7,8,9] + 1×[5]
add qword ptr RW:MEM(64), R:GPR:64	1.00	1+1	1×[6,7,8,9] + 1×[5]
add word ptr RW:MEM(16), 0x0	1.36	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
add word ptr RW:MEM(16), IMM(16)	1.36	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
add word ptr RW:MEM(16), IMM(8)	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
add word ptr RW:MEM(16), R:GPR:16	1.38	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
and RW:GPR:16, 0x0	0.25	1	1×[6,7,8,9]
and RW:GPR:16, IMM(16)	0.25	1	1×[6,7,8,9]
and RW:GPR:16, IMM(8)	0.25	1	1×[6,7,8,9]
and RW:GPR:16, R:GPR:16	0.25	1	1×[6,7,8,9]
and RW:GPR:16, word ptr R:MEM(16)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
and RW:GPR:32, 0x0	0.25	1	1×[6,7,8,9]
and RW:GPR:32, IMM(32)	0.25	1	1×[6,7,8,9]
and RW:GPR:32, IMM(8)	0.25	1	1×[6,7,8,9]
and RW:GPR:32, R:GPR:32	0.25	1	1×[6,7,8,9]
and RW:GPR:32, dword ptr R:MEM(32)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
and RW:GPR:64, 0x0	0.25	1	1×[6,7,8,9]
and RW:GPR:64, IMM(32)	0.25	1	1×[6,7,8,9]
and RW:GPR:64, IMM(8)	0.25	1	1×[6,7,8,9]
and RW:GPR:64, R:GPR:64	0.25	1	1×[6,7,8,9]
and RW:GPR:64, qword ptr R:MEM(64)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
and RW:GPR:8, R:GPR:8	0.25	1	1×[6,7,8,9]
and RW:GPR:8, byte ptr R:MEM(8)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
and byte ptr RW:MEM(8), 0x0	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
and byte ptr RW:MEM(8), IMM(8)	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
and byte ptr RW:MEM(8), R:GPR:8	1.38	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
and dword ptr RW:MEM(32), 0x0	1.00	1+1	1×[6,7,8,9] + 1×[5]
and dword ptr RW:MEM(32), IMM(32)	1.00	1+1	1×[6,7,8,9] + 1×[5]
and dword ptr RW:MEM(32), IMM(8)	1.00	1+1	1×[6,7,8,9] + 1×[5]
and dword ptr RW:MEM(32), R:GPR:32	1.00	1+1	1×[6,7,8,9] + 1×[5]
and qword ptr RW:MEM(64), 0x0	1.00	1+1	1×[6,7,8,9] + 1×[5]
and qword ptr RW:MEM(64), IMM(32)	1.00	1+1	1×[6,7,8,9] + 1×[5]
and qword ptr RW:MEM(64), IMM(8)	1.00	1+1	1×[6,7,8,9] + 1×[5]
and qword ptr RW:MEM(64), R:GPR:64	1.00	1+1	1×[6,7,8,9] + 1×[5]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
`and word ptr RW:MEM(16), 0x0`	1.36	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`and word ptr RW:MEM(16), IMM(16)`	1.36	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`and word ptr RW:MEM(16), IMM(8)`	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`and word ptr RW:MEM(16), R:GPR:16`	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`andn W:GPR:32, R:GPR:32, R:GPR:32`	0.25	1	1×[6,7,8,9]
`andn W:GPR:32, R:GPR:32, dword ptr R:MEM(32)`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`andn W:GPR:64, R:GPR:64, R:GPR:64`	0.25	1	1×[6,7,8,9]
`andn W:GPR:64, R:GPR:64, qword ptr R:MEM(64)`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`bextr W:GPR:32, R:GPR:32, R:GPR:32`	0.25	1	1×[6,7,8,9]
`bextr W:GPR:32, dword ptr R:MEM(32), R:GPR:32`	0.50	2+1*	1×[6,7,8,9] + 1×[4,5]
`bextr W:GPR:64, R:GPR:64, R:GPR:64`	0.25	1	1×[6,7,8,9]
`bextr W:GPR:64, qword ptr R:MEM(64), R:GPR:64`	0.50	2+1*	1×[6,7,8,9] + 1×[4,5]
`blsi W:GPR:32, R:GPR:32`	0.50	2	2×[6,7,8,9]
`blsi W:GPR:32, dword ptr R:MEM(32)`	2.00	3+1*	4×[6,7,8,9] + 1×[4,5] + 4×[0,1,2,3]
`blsi W:GPR:64, R:GPR:64`	0.50	2	2×[6,7,8,9]
`blsi W:GPR:64, qword ptr R:MEM(64)`	2.00	3+1*	4×[6,7,8,9] + 1×[4,5] + 4×[0,1,2,3]
`blsmsk W:GPR:32, R:GPR:32`	0.50	2	2×[6,7,8,9]
`blsmsk W:GPR:32, dword ptr R:MEM(32)`	2.00	3+1*	4×[6,7,8,9] + 1×[4,5] + 4×[0,1,2,3]
`blsmsk W:GPR:64, R:GPR:64`	0.50	2	2×[6,7,8,9]
`blsmsk W:GPR:64, qword ptr R:MEM(64)`	2.00	3+1*	4×[6,7,8,9] + 1×[4,5] + 4×[0,1,2,3]
`blsr W:GPR:32, R:GPR:32`	0.50	2	2×[6,7,8,9]
`blsr W:GPR:32, dword ptr R:MEM(32)`	2.01	3+1*	4×[6,7,8,9] + 1×[4,5] + 4×[0,1,2,3]
`blsr W:GPR:64, R:GPR:64`	0.50	2	2×[6,7,8,9]
`blsr W:GPR:64, qword ptr R:MEM(64)`	2.00	3+1*	4×[6,7,8,9] + 1×[4,5] + 4×[0,1,2,3]
`bsf RW:GPR:16, R:GPR:16`	3.00	6*	8×[6,7,8,9] + 3×[0,1,3] + 6×[0,1,2,3]
`bsf RW:GPR:16, word ptr R:MEM(16)`	4.00	8+1*	9×[6,7,8,9] + 1×[4,5] + 9×[0,1,2,3]
`bsf RW:GPR:32, R:GPR:32`	3.00	6	
`bsf RW:GPR:32, dword ptr R:MEM(32)`	4.00	8+1*	9×[6,7,8,9] + 1×[4,5] + 9×[0,1,2,3]
`bsf RW:GPR:64, R:GPR:64`	3.00	6*	9×[6,7,8,9] + 3×[0,1,3] + 6×[0,1,2,3]
`bsf RW:GPR:64, qword ptr R:MEM(64)`	4.00	8+1*	9×[6,7,8,9] + 1×[4,5] + 9×[0,1,2,3]
`bsr RW:GPR:16, R:GPR:16`	4.00	6*	12×[6,7,8,9] + 6×[0,1,3] + 6×[0,1,2,3]
`bsr RW:GPR:16, word ptr R:MEM(16)`	5.00	8+1*	13×[6,7,8,9] + 1×[4,5] + 3×[0,1,3] + 10×[0,1,2,3]
`bsr RW:GPR:32, R:GPR:32`	4.00	6	
`bsr RW:GPR:32, dword ptr R:MEM(32)`	5.00	8+1*	13×[6,7,8,9] + 1×[4,5] + 3×[0,1,3] + 10×[0,1,2,3]
`bsr RW:GPR:64, R:GPR:64`	4.00	6*	13×[6,7,8,9] + 6×[0,1,3] + 7×[0,1,2,3]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
`bsr RW:GPR:64, qword ptr R:MEM(64)`	4.98	8+1*	13×[6,7,8,9] + 1×[4,5] + 3×[0,1,3] + 10×[0,1,2,3]
`bswap RW:GPR:32`	0.25	1	1×[6,7,8,9]
`bswap RW:GPR:64`	0.25	1	1×[6,7,8,9]
`bt R:GPR:16, 0x0`	0.25	1	1×[6,7,8,9]
`bt R:GPR:16, IMM(8)`	0.25	1	1×[6,7,8,9]
`bt R:GPR:16, R:GPR:16`	0.25	1	1×[6,7,8,9]
`bt R:GPR:32, 0x0`	0.25	1	1×[6,7,8,9]
`bt R:GPR:32, IMM(8)`	0.25	1	1×[6,7,8,9]
`bt R:GPR:32, R:GPR:32`	0.25	1	1×[6,7,8,9]
`bt R:GPR:64, 0x0`	0.25	1	1×[6,7,8,9]
`bt R:GPR:64, IMM(8)`	0.25	1	1×[6,7,8,9]
`bt R:GPR:64, R:GPR:64`	0.25	1	1×[6,7,8,9]
`bt dword ptr R:MEM(32), 0x0`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`bt dword ptr R:MEM(32), IMM(8)`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`bt dword ptr R:MEM(32), R:GPR:32`	3.00	5+1	
`bt qword ptr R:MEM(64), 0x0`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`bt qword ptr R:MEM(64), IMM(8)`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`bt qword ptr R:MEM(64), R:GPR:64`	3.00	5+1	
`bt word ptr R:MEM(16), 0x0`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`bt word ptr R:MEM(16), IMM(8)`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`bt word ptr R:MEM(16), R:GPR:16`	3.00	5+1*	8×[6,7,8,9] + 2×[4,5] + 3×[0,1,3] + 6×[0,1,2,3]
`btc RW:GPR:16, 0x0`	0.50	2	2×[6,7,8,9]
`btc RW:GPR:16, IMM(8)`	0.50	2	2×[6,7,8,9]
`btc RW:GPR:16, R:GPR:16`	0.50	2	2×[6,7,8,9]
`btc RW:GPR:32, 0x0`	0.50	2	2×[6,7,8,9]
`btc RW:GPR:32, IMM(8)`	0.50	2	2×[6,7,8,9]
`btc RW:GPR:32, R:GPR:32`	0.50	2	2×[6,7,8,9]
`btc RW:GPR:64, 0x0`	0.50	2	2×[6,7,8,9]
`btc RW:GPR:64, IMM(8)`	0.50	2	2×[6,7,8,9]
`btc RW:GPR:64, R:GPR:64`	0.50	2	2×[6,7,8,9]
`btc dword ptr RW:MEM(32), 0x0`	2.00	4+1	
`btc dword ptr RW:MEM(32), IMM(8)`	2.00	4+1*	4×[6,7,8,9] + 1×[5] + 6×[0,1,2,3]
`btc dword ptr RW:MEM(32), R:GPR:32`	3.00	8+1*	9×[6,7,8,9] + 1×[5] + 1×[4,5] + 9×[0,1,2,3]
`btc qword ptr RW:MEM(64), 0x0`	2.00	4+1*	4×[6,7,8,9] + 1×[5] + 4×[0,1,2,3]
`btc qword ptr RW:MEM(64), IMM(8)`	2.00	4+1	
`btc qword ptr RW:MEM(64), R:GPR:64`	3.00	8+1*	9×[6,7,8,9] + 1×[5] + 1×[4,5] + 9×[0,1,2,3]
`btc word ptr RW:MEM(16), 0x0`	2.00	4+1*	4×[6,7,8,9] + 1×[5] + 1×[4,5] + 4×[0,1,2,3]
`btc word ptr RW:MEM(16), IMM(8)`	2.00	4+1*	4×[6,7,8,9] + 1×[5] + 1×[4,5] + 4×[0,1,2,3]
`btc word ptr RW:MEM(16), R:GPR:16`	3.00	8+1*	9×[6,7,8,9] + 1×[5] + 1×[4,5] + 9×[0,1,2,3]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
`btr RW:GPR:16, 0x0`	0.50	2	2×[6,7,8,9]
`btr RW:GPR:16, IMM(8)`	0.50	2	2×[6,7,8,9]
`btr RW:GPR:16, R:GPR:16`	0.50	2	2×[6,7,8,9]
`btr RW:GPR:32, 0x0`	0.50	2	2×[6,7,8,9]
`btr RW:GPR:32, IMM(8)`	0.51	2	2×[6,7,8,9]
`btr RW:GPR:32, R:GPR:32`	0.50	2	2×[6,7,8,9]
`btr RW:GPR:64, 0x0`	0.50	2	2×[6,7,8,9]
`btr RW:GPR:64, IMM(8)`	0.50	2	2×[6,7,8,9]
`btr RW:GPR:64, R:GPR:64`	0.50	2	2×[6,7,8,9]
`btr dword ptr RW:MEM(32), 0x0`	2.00	4+1*	4×[6,7,8,9] + 1×[5] + 4×[0,1,2,3]
`btr dword ptr RW:MEM(32), IMM(8)`	2.00	4+1*	4×[6,7,8,9] + 1×[5] + 5×[0,1,2,3]
`btr dword ptr RW:MEM(32), R:GPR:32`	3.00	8+1*	9×[6,7,8,9] + 1×[5] + 1×[4,5] + 9×[0,1,2,3]
`btr qword ptr RW:MEM(64), 0x0`	2.00	4+1*	4×[6,7,8,9] + 1×[5] + 6×[0,1,2,3]
`btr qword ptr RW:MEM(64), IMM(8)`	2.00	4+1*	4×[6,7,8,9] + 1×[5] + 6×[0,1,2,3]
`btr qword ptr RW:MEM(64), R:GPR:64`	3.00	8+1*	9×[6,7,8,9] + 1×[5] + 1×[4,5] + 9×[0,1,2,3]
`btr word ptr RW:MEM(16), 0x0`	2.00	4+1*	4×[6,7,8,9] + 1×[5] + 1×[4,5] + 4×[0,1,2,3]
`btr word ptr RW:MEM(16), IMM(8)`	2.00	4+1*	4×[6,7,8,9] + 1×[5] + 1×[4,5] + 4×[0,1,2,3]
`btr word ptr RW:MEM(16), R:GPR:16`	3.00	8+1*	9×[6,7,8,9] + 1×[5] + 1×[4,5] + 9×[0,1,2,3]
`bts RW:GPR:16, 0x0`	0.50	2	2×[6,7,8,9]
`bts RW:GPR:16, IMM(8)`	0.50	2	2×[6,7,8,9]
`bts RW:GPR:16, R:GPR:16`	0.50	2	2×[6,7,8,9]
`bts RW:GPR:32, 0x0`	0.50	2	2×[6,7,8,9]
`bts RW:GPR:32, IMM(8)`	0.50	2	2×[6,7,8,9]
`bts RW:GPR:32, R:GPR:32`	0.50	2	2×[6,7,8,9]
`bts RW:GPR:64, 0x0`	0.50	2	2×[6,7,8,9]
`bts RW:GPR:64, IMM(8)`	0.50	2	2×[6,7,8,9]
`bts RW:GPR:64, R:GPR:64`	0.50	2	2×[6,7,8,9]
`bts dword ptr RW:MEM(32), 0x0`	2.00	4+1*	4×[6,7,8,9] + 1×[5] + 6×[0,1,2,3]
`bts dword ptr RW:MEM(32), IMM(8)`	2.00	4+1*	4×[6,7,8,9] + 1×[5] + 6×[0,1,2,3]
`bts dword ptr RW:MEM(32), R:GPR:32`	3.00	8+1*	9×[6,7,8,9] + 1×[5] + 1×[4,5] + 9×[0,1,2,3]
`bts qword ptr RW:MEM(64), 0x0`	2.00	4+1*	4×[6,7,8,9] + 1×[5] + 4×[0,1,2,3]
`bts qword ptr RW:MEM(64), IMM(8)`	2.00	4+1*	4×[6,7,8,9] + 1×[5] + 6×[0,1,2,3]
`bts qword ptr RW:MEM(64), R:GPR:64`	3.01	8+1*	9×[6,7,8,9] + 1×[5] + 1×[4,5] + 9×[0,1,2,3]
`bts word ptr RW:MEM(16), 0x0`	2.00	4+1*	4×[6,7,8,9] + 1×[5] + 1×[4,5] + 4×[0,1,2,3]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
`bts word ptr RW:MEM(16), IMM(8)`	2.00	4+1*	4×[6,7,8,9] + 1×[5] + 1×[4,5] + 4×[0,1,2,3]
`bts word ptr RW:MEM(16), R:GPR:16`	3.00	8+1*	9×[6,7,8,9] + 1×[5] + 1×[4,5] + 9×[0,1,2,3]
`bzhi W:GPR:32, R:GPR:32, R:GPR:32`	0.25	1	1×[6,7,8,9]
`bzhi W:GPR:32, dword ptr R:MEM(32), R:GPR:32`	0.50	2+1*	1×[6,7,8,9] + 1×[4,5]
`bzhi W:GPR:64, R:GPR:64, R:GPR:64`	0.25	1	1×[6,7,8,9]
`bzhi W:GPR:64, qword ptr R:MEM(64), R:GPR:64`	0.50	2+1*	1×[6,7,8,9] + 1×[4,5]
`clc`	0.25	1	1×[6,7,8,9]
`cmp R:GPR:16, 0x0`	0.25	1	1×[6,7,8,9]
`cmp R:GPR:16, IMM(16)`	0.25	1	1×[6,7,8,9]
`cmp R:GPR:16, IMM(8)`	0.25	1	1×[6,7,8,9]
`cmp R:GPR:16, R:GPR:16`	0.25	1	1×[6,7,8,9]
`cmp R:GPR:16, word ptr R:MEM(16)`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`cmp R:GPR:32, 0x0`	0.25	1	1×[6,7,8,9]
`cmp R:GPR:32, IMM(32)`	0.25	1	1×[6,7,8,9]
`cmp R:GPR:32, IMM(8)`	0.25	1	1×[6,7,8,9]
`cmp R:GPR:32, R:GPR:32`	0.25	1	1×[6,7,8,9]
`cmp R:GPR:32, dword ptr R:MEM(32)`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`cmp R:GPR:64, 0x0`	0.25	1	1×[6,7,8,9]
`cmp R:GPR:64, IMM(32)`	0.25	1	1×[6,7,8,9]
`cmp R:GPR:64, IMM(8)`	0.25	1	1×[6,7,8,9]
`cmp R:GPR:64, R:GPR:64`	0.25	1	1×[6,7,8,9]
`cmp R:GPR:64, qword ptr R:MEM(64)`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`cmp R:al, 0x0`	0.25	1	1×[6,7,8,9]
`cmp R:al, IMM(8)`	0.25	1	1×[6,7,8,9]
`cmp R:GPR:8, R:GPR:8`	0.25	1	1×[6,7,8,9]
`cmp R:GPR:8, byte ptr R:MEM(8)`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`cmp R:al,bl,cl,dl,r10b,r11b,r8b,r9b, 0x0`	0.25	1	1×[6,7,8,9]
`cmp R:al,bl,cl,dl,r10b,r11b,r8b,r9b, IMM(8)`	0.25	1	1×[6,7,8,9]
`cmp R:ax, IMM(16)`	0.25	1	1×[6,7,8,9]
`cmp R:bpl,dil,r12b,r13b,r14b,r15b,sil,spl, 0x0`	0.25	1	1×[6,7,8,9]
`cmp R:bpl,dil,r12b,r13b,r14b,r15b,sil,spl, IMM(8)`	0.25	1	1×[6,7,8,9]
`cmp R:eax, IMM(32)`	0.25	1	1×[6,7,8,9]
`cmp R:rax, IMM(32)`	0.25	1	1×[6,7,8,9]
`cmp byte ptr R:MEM(8), 0x0`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`cmp byte ptr R:MEM(8), IMM(8)`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`cmp byte ptr R:MEM(8), R:GPR:8`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`cmp dword ptr R:MEM(32), 0x0`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`cmp dword ptr R:MEM(32), IMM(32)`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`cmp dword ptr R:MEM(32), IMM(8)`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`cmp dword ptr R:MEM(32), R:GPR:32`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`cmp qword ptr R:MEM(64), 0x0`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`cmp qword ptr R:MEM(64), IMM(32)`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`cmp qword ptr R:MEM(64), IMM(8)`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`cmp qword ptr R:MEM(64), R:GPR:64`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
`cmp word ptr R:MEM(16), 0x0`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`cmp word ptr R:MEM(16), IMM(16)`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`cmp word ptr R:MEM(16), IMM(8)`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`cmp word ptr R:MEM(16), R:GPR:16`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`dec RW:GPR:16`	0.25	1	1×[6,7,8,9]
`dec RW:GPR:32`	0.25	1	1×[6,7,8,9]
`dec RW:GPR:64`	0.25	1	1×[6,7,8,9]
`dec RW:GPR:8`	0.25	1	1×[6,7,8,9]
`dec byte ptr RW:MEM(8)`	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`dec dword ptr RW:MEM(32)`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`dec qword ptr RW:MEM(64)`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`dec word ptr RW:MEM(16)`	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`inc RW:GPR:16`	0.25	1	1×[6,7,8,9]
`inc RW:GPR:32`	0.25	1	1×[6,7,8,9]
`inc RW:GPR:64`	0.25	1	1×[6,7,8,9]
`inc RW:GPR:8`	0.25	1	1×[6,7,8,9]
`inc byte ptr RW:MEM(8)`	1.38	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`inc dword ptr RW:MEM(32)`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`inc qword ptr RW:MEM(64)`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`inc word ptr RW:MEM(16)`	1.38	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`lea RW:GPR:16, MEM(0)`	0.50	2	2×[6,7,8,9]
`lea W:GPR:32, MEM(0)`	0.25	1	1×[6,7,8,9]
`lea W:GPR:64, MEM(0)`	0.25	1	1×[6,7,8,9]
`lzcnt RW:GPR:16, R:GPR:16`	0.26	1	1×[6,7,8,9]
`lzcnt RW:GPR:16, word ptr R:MEM(16)`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`lzcnt W:GPR:32, R:GPR:32`	0.25	1	1×[6,7,8,9]
`lzcnt W:GPR:32, dword ptr R:MEM(32)`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`lzcnt W:GPR:64, R:GPR:64`	0.25	1	1×[6,7,8,9]
`lzcnt W:GPR:64, qword ptr R:MEM(64)`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`mov RW:GPR:16, IMM(16)`	0.25	1	1×[6,7,8,9]
`mov RW:GPR:16, R:GPR:16`	0.25	1	1×[6,7,8,9]
`mov RW:GPR:16, word ptr R:MEM(16)`	0.50	1	1×[4,5]
`mov RW:GPR:8, 0x0`	0.25	1	1×[6,7,8,9]
`mov RW:GPR:8, IMM(8)`	0.25	1	1×[6,7,8,9]
`mov RW:GPR:8, R:GPR:8`	0.25	1	1×[6,7,8,9]
`mov RW:GPR:8, byte ptr R:MEM(8)`	0.50	1	1×[4,5]
`mov W:GPR:32, IMM(32)`	0.25	1	1×[6,7,8,9]
`mov W:GPR:32, dword ptr R:MEM(32)`	0.50	1	1×[4,5]
`mov W:GPR:64, IMM(32)`	0.25	1	1×[6,7,8,9]
`mov W:GPR:64, qword ptr R:MEM(64)`	0.50	1	1×[4,5]
`mov W:eax, dword ptr R:MEM(32)`	0.50	1	1×[4,5]
`mov W:rax, qword ptr R:MEM(64)`	0.50	1	1×[4,5]
`mov byte ptr RW:MEM(8), 0x0`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`mov byte ptr RW:MEM(8), IMM(8)`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`mov byte ptr RW:MEM(8), R:al`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`mov byte ptr RW:MEM(8), R:GPR:8`	1.00	1+1	1×[6,7,8,9] + 1×[5]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
mov dword ptr W:MEM(32), IMM(32)	1.00	1+1	1×[6,7,8,9] + 1×[5]
mov dword ptr W:MEM(32), R:GPR:32	1.00	1+1	1×[6,7,8,9] + 1×[5]
mov dword ptr W:MEM(32), R:eax	1.00	1+1	1×[6,7,8,9] + 1×[5]
mov qword ptr W:MEM(64), IMM(32)	1.00	1+1	1×[6,7,8,9] + 1×[5]
mov qword ptr W:MEM(64), R:GPR:64	1.00	1+1	1×[6,7,8,9] + 1×[5]
mov qword ptr W:MEM(64), R:rax	1.00	1+1	1×[6,7,8,9] + 1×[5]
mov word ptr RW:MEM(16), IMM(16)	1.00	1+1	1×[6,7,8,9] + 1×[5]
mov word ptr RW:MEM(16), R:GPR:16	1.00	1+1	1×[6,7,8,9] + 1×[5]
mov word ptr RW:MEM(16), R:ax	1.00	1+1	1×[6,7,8,9] + 1×[5]
movbe RW:GPR:16, word ptr R:MEM(16)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
movbe W:GPR:32, dword ptr R:MEM(32)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
movbe W:GPR:64, qword ptr R:MEM(64)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
movbe dword ptr W:MEM(32), R:GPR:32	1.00	1+1	1×[6,7,8,9] + 1×[5]
movbe qword ptr W:MEM(64), R:GPR:64	1.00	1+1	1×[6,7,8,9] + 1×[5]
movbe word ptr RW:MEM(16), R:GPR:16	1.00	1+1	1×[6,7,8,9] + 1×[5]
movsx RW:GPR:16, R:GPR:8	0.25	1	1×[6,7,8,9]
movsx RW:GPR:16, byte ptr R:MEM(8)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
movsx W:GPR:32, R:GPR:16	0.25	1	1×[6,7,8,9]
movsx W:GPR:32, R:GPR:8	0.25	1	1×[6,7,8,9]
movsx W:GPR:32, byte ptr R:MEM(8)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
movsx W:GPR:32, word ptr R:MEM(16)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
movsx W:GPR:64, R:GPR:16	0.25	1	1×[6,7,8,9]
movsx W:GPR:64, R:GPR:8	0.25	1	1×[6,7,8,9]
movsx W:GPR:64, byte ptr R:MEM(8)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
movsx W:GPR:64, word ptr R:MEM(16)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
movsxd W:GPR:64, R:GPR:32	0.25	1	1×[6,7,8,9]
movsxd W:GPR:64, dword ptr R:MEM(32)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
movzx RW:GPR:16, R:GPR:8	0.25	1	1×[6,7,8,9]
movzx RW:GPR:16, byte ptr R:MEM(8)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
movzx W:GPR:32, R:GPR:16	0.25	1	1×[6,7,8,9]
movzx W:GPR:32, R:GPR:8	0.25	1	1×[6,7,8,9]
movzx W:GPR:32, byte ptr R:MEM(8)	0.50	1+1*	1×[4,5]
movzx W:GPR:32, word ptr R:MEM(16)	0.50	1+1*	1×[4,5]
movzx W:GPR:64, R:GPR:16	0.25	1	1×[6,7,8,9]
movzx W:GPR:64, R:GPR:8	0.25	1	1×[6,7,8,9]
movzx W:GPR:64, byte ptr R:MEM(8)	0.50	1+1*	1×[4,5]
movzx W:GPR:64, word ptr R:MEM(16)	0.50	1+1*	1×[4,5]
mulx W:GPR:32, W:GPR:32, R:GPR:32	2.00	2*	3×[6,7,8,9]
mulx W:GPR:32, W:GPR:32, dword ptr R:MEM(32)	2.00	2+1*	4×[6,7,8,9] + 1×[4,5]
mulx W:GPR:64, W:GPR:64, R:GPR:64	2.00	2*	3×[6,7,8,9]
mulx W:GPR:64, W:GPR:64, qword ptr R:MEM(64)	2.00	2+1*	3×[6,7,8,9] + 1×[4,5]
neg RW:GPR:16	0.25	1	1×[6,7,8,9]
neg RW:GPR:32	0.25	1	1×[6,7,8,9]
neg RW:GPR:64	0.25	1	1×[6,7,8,9]
neg RW:GPR:8	0.25	1	1×[6,7,8,9]
neg byte ptr RW:MEM(8)	1.38	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
neg dword ptr RW:MEM(32)	1.00	1+1	1×[6,7,8,9] + 1×[5]
neg qword ptr RW:MEM(64)	1.00	1+1	1×[6,7,8,9] + 1×[5]
neg word ptr RW:MEM(16)	1.38	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
not RW:GPR:16	0.25	1	1×[6,7,8,9]
not RW:GPR:32	0.25	1	1×[6,7,8,9]
not RW:GPR:64	0.25	1	1×[6,7,8,9]
not RW:GPR:8	0.25	1	1×[6,7,8,9]
not byte ptr RW:MEM(8)	1.38	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
not dword ptr RW:MEM(32)	1.00	1+1	1×[6,7,8,9] + 1×[5]
not qword ptr RW:MEM(64)	1.00	1+1	1×[6,7,8,9] + 1×[5]
not word ptr RW:MEM(16)	1.39	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
or RW:GPR:16, 0x0	0.25	1	1×[6,7,8,9]
or RW:GPR:16, IMM(16)	0.25	1	1×[6,7,8,9]
or RW:GPR:16, IMM(8)	0.25	1	1×[6,7,8,9]
or RW:GPR:16, R:GPR:16	0.25	1	1×[6,7,8,9]
or RW:GPR:16, word ptr R:MEM(16)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
or RW:GPR:32, 0x0	0.25	1	1×[6,7,8,9]
or RW:GPR:32, IMM(32)	0.25	1	1×[6,7,8,9]
or RW:GPR:32, IMM(8)	0.25	1	1×[6,7,8,9]
or RW:GPR:32, R:GPR:32	0.25	1	1×[6,7,8,9]
or RW:GPR:32, dword ptr R:MEM(32)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
or RW:GPR:64, 0x0	0.25	1	1×[6,7,8,9]
or RW:GPR:64, IMM(32)	0.25	1	1×[6,7,8,9]
or RW:GPR:64, IMM(8)	0.25	1	1×[6,7,8,9]
or RW:GPR:64, R:GPR:64	0.25	1	1×[6,7,8,9]
or RW:GPR:64, qword ptr R:MEM(64)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
or RW:GPR:8, R:GPR:8	0.25	1	1×[6,7,8,9]
or RW:GPR:8, byte ptr R:MEM(8)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
or byte ptr RW:MEM(8), 0x0	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
or byte ptr RW:MEM(8), IMM(8)	1.36	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
or byte ptr RW:MEM(8), R:GPR:8	1.39	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
or dword ptr RW:MEM(32), 0x0	1.00	1+1	1×[6,7,8,9] + 1×[5]
or dword ptr RW:MEM(32), IMM(32)	1.00	1+1	1×[6,7,8,9] + 1×[5]
or dword ptr RW:MEM(32), IMM(8)	1.00	1+1	1×[6,7,8,9] + 1×[5]
or dword ptr RW:MEM(32), R:GPR:32	1.00	1+1	1×[6,7,8,9] + 1×[5]
or qword ptr RW:MEM(64), 0x0	1.00	1+1	1×[6,7,8,9] + 1×[5]
or qword ptr RW:MEM(64), IMM(32)	1.00	1+1	1×[6,7,8,9] + 1×[5]
or qword ptr RW:MEM(64), IMM(8)	1.00	1+1	1×[6,7,8,9] + 1×[5]
or qword ptr RW:MEM(64), R:GPR:64	1.00	1+1	1×[6,7,8,9] + 1×[5]
or word ptr RW:MEM(16), 0x0	1.36	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
or word ptr RW:MEM(16), IMM(16)	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
or word ptr RW:MEM(16), IMM(8)	1.36	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
or word ptr RW:MEM(16), R:GPR:16	1.38	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
pclmulqdq RW:XMM, R:XMM, IMM(8)	2.00	4*	1×[0,1] + 4×[6,7,8,9] + 4×[1,2]
pclmulqdq RW:XMM, xmmword ptr R:MEM(128), IMM(8)	2.00	4+1	

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
`rcl RW:GPR:16, 0x0`	4.00	9*	13×[6,7,8,9] + 3×[0,1,3] + 10×[0,1,2,3]
`rcl RW:GPR:32, 0x0`	4.00	9*	13×[6,7,8,9] + 3×[0,1,3] + 10×[0,1,2,3]
`rcl RW:GPR:64, 0x0`	4.00	9*	13×[6,7,8,9] + 3×[0,1,3] + 10×[0,1,2,3]
`rcl byte ptr RW:MEM(8), 0x0`	4.00	11+1*	13×[6,7,8,9] + 1×[5] + 1×[4,5] + 1×[0,1,3] + 12×[0,1,2,3]
`rcl dword ptr RW:MEM(32), 0x0`	4.00	11+1	
`rcl qword ptr RW:MEM(64), 0x0`	4.00	11+1*	13×[6,7,8,9] + 1×[5] + 1×[0,1,3] + 12×[0,1,2,3]
`rcl word ptr RW:MEM(16), 0x0`	4.00	11+1*	13×[6,7,8,9] + 1×[5] + 1×[4,5] + 1×[0,1,3] + 12×[0,1,2,3]
`rcr RW:GPR:16, 0x0`	3.00	7*	9×[6,7,8,9] + 3×[0,1,3] + 6×[0,1,2,3]
`rcr RW:GPR:32, 0x0`	3.00	7*	9×[6,7,8,9] + 3×[0,1,3] + 6×[0,1,2,3]
`rcr RW:GPR:64, 0x0`	3.00	7*	9×[6,7,8,9] + 3×[0,1,3] + 6×[0,1,2,3]
`rcr byte ptr RW:MEM(8), 0x0`	4.00	10+1*	13×[6,7,8,9] + 1×[5] + 1×[4,5] + 3×[0,1,3] + 10×[0,1,2,3]
`rcr dword ptr RW:MEM(32), 0x0`	4.00	10+1*	13×[6,7,8,9] + 1×[5] + 3×[0,1,3] + 10×[0,1,2,3]
`rcr qword ptr RW:MEM(64), 0x0`	4.00	10+1*	13×[6,7,8,9] + 1×[5] + 3×[0,1,3] + 10×[0,1,2,3]
`rcr word ptr RW:MEM(16), 0x0`	4.00	10+1*	13×[6,7,8,9] + 1×[5] + 1×[4,5] + 3×[0,1,3] + 10×[0,1,2,3]
`rol RW:GPR:16`	0.25	1	1×[6,7,8,9]
`rol RW:GPR:16, 0x0`	0.25	1	1×[6,7,8,9]
`rol RW:GPR:16, IMM(8)`	0.25	1	1×[6,7,8,9]
`rol RW:GPR:16, R:cl`	0.25	1	1×[6,7,8,9]
`rol RW:GPR:32`	0.25	1	1×[6,7,8,9]
`rol RW:GPR:32, 0x0`	0.25	1	1×[6,7,8,9]
`rol RW:GPR:32, IMM(8)`	0.25	1	1×[6,7,8,9]
`rol RW:GPR:32, R:cl`	0.25	1	1×[6,7,8,9]
`rol RW:GPR:64`	0.25	1	1×[6,7,8,9]
`rol RW:GPR:64, 0x0`	0.25	1	1×[6,7,8,9]
`rol RW:GPR:64, IMM(8)`	0.25	1	1×[6,7,8,9]
`rol RW:GPR:64, R:cl`	0.25	1	1×[6,7,8,9]
`rol RW:GPR:8, R:cl`	0.25	1	1×[6,7,8,9]
`rol byte ptr RW:MEM(8)`	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`rol byte ptr RW:MEM(8), 0x0`	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`rol byte ptr RW:MEM(8), IMM(8)`	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`rol byte ptr RW:MEM(8), R:cl`	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`rol dword ptr RW:MEM(32)`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`rol dword ptr RW:MEM(32), 0x0`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`rol dword ptr RW:MEM(32), IMM(8)`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`rol dword ptr RW:MEM(32), R:cl`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`rol qword ptr RW:MEM(64)`	1.00	1+1	1×[6,7,8,9] + 1×[5]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
`rol qword ptr RW:MEM(64), 0x0`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`rol qword ptr RW:MEM(64), IMM(8)`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`rol qword ptr RW:MEM(64), R:cl`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`rol word ptr RW:MEM(16)`	1.38	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`rol word ptr RW:MEM(16), 0x0`	1.36	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`rol word ptr RW:MEM(16), IMM(8)`	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`rol word ptr RW:MEM(16), R:cl`	1.38	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`ror RW:GPR:16`	0.25	1	1×[6,7,8,9]
`ror RW:GPR:16, 0x0`	0.25	1	1×[6,7,8,9]
`ror RW:GPR:16, IMM(8)`	0.25	1	1×[6,7,8,9]
`ror RW:GPR:16, R:cl`	0.25	1	1×[6,7,8,9]
`ror RW:GPR:32`	0.25	1	1×[6,7,8,9]
`ror RW:GPR:32, 0x0`	0.25	1	1×[6,7,8,9]
`ror RW:GPR:32, IMM(8)`	0.25	1	1×[6,7,8,9]
`ror RW:GPR:32, R:cl`	0.25	1	1×[6,7,8,9]
`ror RW:GPR:64`	0.25	1	1×[6,7,8,9]
`ror RW:GPR:64, 0x0`	0.25	1	1×[6,7,8,9]
`ror RW:GPR:64, IMM(8)`	0.25	1	1×[6,7,8,9]
`ror RW:GPR:64, R:cl`	0.25	1	1×[6,7,8,9]
`ror RW:GPR:8, R:cl`	0.25	1	1×[6,7,8,9]
`ror byte ptr RW:MEM(8)`	1.38	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`ror byte ptr RW:MEM(8), 0x0`	1.36	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`ror byte ptr RW:MEM(8), IMM(8)`	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`ror byte ptr RW:MEM(8), R:cl`	1.39	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`ror dword ptr RW:MEM(32)`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`ror dword ptr RW:MEM(32), 0x0`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`ror dword ptr RW:MEM(32), IMM(8)`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`ror dword ptr RW:MEM(32), R:cl`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`ror qword ptr RW:MEM(64)`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`ror qword ptr RW:MEM(64), 0x0`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`ror qword ptr RW:MEM(64), IMM(8)`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`ror qword ptr RW:MEM(64), R:cl`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`ror word ptr RW:MEM(16)`	1.38	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`ror word ptr RW:MEM(16), 0x0`	1.36	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`ror word ptr RW:MEM(16), IMM(8)`	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`ror word ptr RW:MEM(16), R:cl`	1.38	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`rorx W:GPR:32, R:GPR:32, IMM(8)`	0.26	1	1×[6,7,8,9]
`rorx W:GPR:32, dword ptr R:MEM(32), IMM(8)`	0.50	2+1*	1×[6,7,8,9] + 1×[4,5]
`rorx W:GPR:64, R:GPR:64, IMM(8)`	0.26	1	1×[6,7,8,9]
`rorx W:GPR:64, qword ptr R:MEM(64), IMM(8)`	0.50	2+1*	1×[6,7,8,9] + 1×[4,5]
`sar RW:GPR:16`	0.25	1	1×[6,7,8,9]
`sar RW:GPR:16, 0x0`	0.25	1	1×[6,7,8,9]
`sar RW:GPR:16, IMM(8)`	0.25	1	1×[6,7,8,9]
`sar RW:GPR:16, R:cl`	0.25	1	1×[6,7,8,9]
`sar RW:GPR:32`	0.25	1	1×[6,7,8,9]
`sar RW:GPR:32, 0x0`	0.25	1	1×[6,7,8,9]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
sar RW:GPR:32, IMM(8)	0.25	1	1×[6,7,8,9]
sar RW:GPR:32, R:cl	0.25	1	1×[6,7,8,9]
sar RW:GPR:64	0.25	1	1×[6,7,8,9]
sar RW:GPR:64, 0x0	0.25	1	1×[6,7,8,9]
sar RW:GPR:64, IMM(8)	0.25	1	1×[6,7,8,9]
sar RW:GPR:64, R:cl	0.25	1	1×[6,7,8,9]
sar RW:GPR:8, R:cl	0.25	1	1×[6,7,8,9]
sar byte ptr RW:MEM(8)	1.38	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
sar byte ptr RW:MEM(8), 0x0	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
sar byte ptr RW:MEM(8), IMM(8)	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
sar byte ptr RW:MEM(8), R:cl	1.39	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
sar dword ptr RW:MEM(32)	1.00	1+1	1×[6,7,8,9] + 1×[5]
sar dword ptr RW:MEM(32), 0x0	1.00	1+1	1×[6,7,8,9] + 1×[5]
sar dword ptr RW:MEM(32), IMM(8)	1.00	1+1	1×[6,7,8,9] + 1×[5]
sar dword ptr RW:MEM(32), R:cl	1.00	1+1	1×[6,7,8,9] + 1×[5]
sar qword ptr RW:MEM(64)	1.00	1+1	1×[6,7,8,9] + 1×[5]
sar qword ptr RW:MEM(64), 0x0	1.00	1+1	1×[6,7,8,9] + 1×[5]
sar qword ptr RW:MEM(64), IMM(8)	1.00	1+1	1×[6,7,8,9] + 1×[5]
sar qword ptr RW:MEM(64), R:cl	1.00	1+1	1×[6,7,8,9] + 1×[5]
sar word ptr RW:MEM(16)	1.38	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
sar word ptr RW:MEM(16), 0x0	1.36	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
sar word ptr RW:MEM(16), IMM(8)	1.36	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
sar word ptr RW:MEM(16), R:cl	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
sarx W:GPR:32, R:GPR:32, R:GPR:32	0.25	1	1×[6,7,8,9]
sarx W:GPR:32, dword ptr R:MEM(32), R:GPR:32	0.50	2+1*	1×[6,7,8,9] + 1×[4,5]
sarx W:GPR:64, R:GPR:64, R:GPR:64	0.25	1	1×[6,7,8,9]
sarx W:GPR:64, qword ptr R:MEM(64), R:GPR:64	0.50	2+1*	1×[6,7,8,9] + 1×[4,5]
shl RW:GPR:16	0.25	1	1×[6,7,8,9]
shl RW:GPR:16, 0x0	0.25	1	1×[6,7,8,9]
shl RW:GPR:16, IMM(8)	0.25	1	1×[6,7,8,9]
shl RW:GPR:16, R:cl	0.25	1	1×[6,7,8,9]
shl RW:GPR:32	0.25	1	1×[6,7,8,9]
shl RW:GPR:32, 0x0	0.25	1	1×[6,7,8,9]
shl RW:GPR:32, IMM(8)	0.25	1	1×[6,7,8,9]
shl RW:GPR:32, R:cl	0.25	1	1×[6,7,8,9]
shl RW:GPR:64	0.25	1	1×[6,7,8,9]
shl RW:GPR:64, 0x0	0.25	1	1×[6,7,8,9]
shl RW:GPR:64, IMM(8)	0.25	1	1×[6,7,8,9]
shl RW:GPR:64, R:cl	0.25	1	1×[6,7,8,9]
shl RW:GPR:8, R:cl	0.25	1	1×[6,7,8,9]
shl byte ptr RW:MEM(8)	1.39	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
shl byte ptr RW:MEM(8), 0x0	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
shl byte ptr RW:MEM(8), IMM(8)	1.36	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
shl byte ptr RW:MEM(8), R:cl	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
shl dword ptr RW:MEM(32)	1.00	1+1	1×[6,7,8,9] + 1×[5]
shl dword ptr RW:MEM(32), 0x0	1.00	1+1	1×[6,7,8,9] + 1×[5]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
`shl dword ptr RW:MEM(32), IMM(8)`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`shl dword ptr RW:MEM(32), R:cl`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`shl qword ptr RW:MEM(64)`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`shl qword ptr RW:MEM(64), 0x0`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`shl qword ptr RW:MEM(64), IMM(8)`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`shl qword ptr RW:MEM(64), R:cl`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`shl word ptr RW:MEM(16)`	1.38	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`shl word ptr RW:MEM(16), 0x0`	1.36	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`shl word ptr RW:MEM(16), IMM(8)`	1.35	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`shl word ptr RW:MEM(16), R:cl`	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`shld RW:GPR:16, R:GPR:16, 0x0`	3.00	6*	9×[6,7,8,9] + 3×[0,1,3] + 5×[0,1,2,3]
`shld RW:GPR:16, R:GPR:16, IMM(8)`	3.00	6	
`shld RW:GPR:32, R:GPR:32, 0x0`	3.00	6*	8×[6,7,8,9] + 3×[0,1,3] + 5×[0,1,2,3]
`shld RW:GPR:32, R:GPR:32, IMM(8)`	3.00	6*	9×[6,7,8,9] + 3×[0,1,3] + 5×[0,1,2,3]
`shld RW:GPR:64, R:GPR:64, 0x0`	3.01	6*	9×[6,7,8,9] + 3×[0,1,3] + 5×[0,1,2,3]
`shld RW:GPR:64, R:GPR:64, IMM(8)`	3.00	6	
`shld dword ptr RW:MEM(32), R:GPR:32, 0x0`	3.00	8+1*	9×[6,7,8,9] + 1×[5] + 9×[0,1,2,3]
`shld dword ptr RW:MEM(32), R:GPR:32, IMM(8)`	3.00	8+1*	9×[6,7,8,9] + 1×[5] + 9×[0,1,2,3]
`shld qword ptr RW:MEM(64), R:GPR:64, 0x0`	3.00	8+1*	9×[6,7,8,9] + 1×[5] + 9×[0,1,2,3]
`shld qword ptr RW:MEM(64), R:GPR:64, IMM(8)`	3.00	8+1*	9×[6,7,8,9] + 1×[5] + 9×[0,1,2,3]
`shld word ptr RW:MEM(16), R:GPR:16, 0x0`	3.00	8+1*	9×[6,7,8,9] + 1×[5] + 1×[4,5] + 9×[0,1,2,3]
`shld word ptr RW:MEM(16), R:GPR:16, IMM(8)`	3.00	8+1*	9×[6,7,8,9] + 1×[5] + 1×[4,5] + 9×[0,1,2,3]
`shlx W:GPR:32, R:GPR:32, R:GPR:32`	0.25	1	1×[6,7,8,9]
`shlx W:GPR:32, dword ptr R:MEM(32), R:GPR:32`	0.50	2+1*	1×[6,7,8,9] + 1×[4,5]
`shlx W:GPR:64, R:GPR:64, R:GPR:64`	0.25	1	1×[6,7,8,9]
`shlx W:GPR:64, qword ptr R:MEM(64), R:GPR:64`	0.50	2+1*	1×[6,7,8,9] + 1×[4,5]
`shr RW:GPR:16`	0.25	1	1×[6,7,8,9]
`shr RW:GPR:16, 0x0`	0.25	1	1×[6,7,8,9]
`shr RW:GPR:16, IMM(8)`	0.25	1	1×[6,7,8,9]
`shr RW:GPR:16, R:cl`	0.25	1	1×[6,7,8,9]
`shr RW:GPR:32`	0.25	1	1×[6,7,8,9]
`shr RW:GPR:32, 0x0`	0.25	1	1×[6,7,8,9]
`shr RW:GPR:32, IMM(8)`	0.25	1	1×[6,7,8,9]
`shr RW:GPR:32, R:cl`	0.25	1	1×[6,7,8,9]
`shr RW:GPR:64`	0.25	1	1×[6,7,8,9]
`shr RW:GPR:64, 0x0`	0.25	1	1×[6,7,8,9]
`shr RW:GPR:64, IMM(8)`	0.25	1	1×[6,7,8,9]
`shr RW:GPR:64, R:cl`	0.25	1	1×[6,7,8,9]
`shr RW:GPR:8, R:cl`	0.25	1	1×[6,7,8,9]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
shr byte ptr RW:MEM(8)	1.38	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
shr byte ptr RW:MEM(8), 0x0	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
shr byte ptr RW:MEM(8), IMM(8)	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
shr byte ptr RW:MEM(8), R:cl	1.38	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
shr dword ptr RW:MEM(32)	1.00	1+1	1×[6,7,8,9] + 1×[5]
shr dword ptr RW:MEM(32), 0x0	1.00	1+1	1×[6,7,8,9] + 1×[5]
shr dword ptr RW:MEM(32), IMM(8)	1.00	1+1	1×[6,7,8,9] + 1×[5]
shr dword ptr RW:MEM(32), R:cl	1.00	1+1	1×[6,7,8,9] + 1×[5]
shr qword ptr RW:MEM(64)	1.00	1+1	1×[6,7,8,9] + 1×[5]
shr qword ptr RW:MEM(64), 0x0	1.00	1+1	1×[6,7,8,9] + 1×[5]
shr qword ptr RW:MEM(64), IMM(8)	1.00	1+1	1×[6,7,8,9] + 1×[5]
shr qword ptr RW:MEM(64), R:cl	1.00	1+1	1×[6,7,8,9] + 1×[5]
shr word ptr RW:MEM(16)	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
shr word ptr RW:MEM(16), 0x0	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
shr word ptr RW:MEM(16), IMM(8)	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
shr word ptr RW:MEM(16), R:cl	1.39	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
shrd RW:GPR:16, R:GPR:16, 0x0	3.00	6*	9×[6,7,8,9] + 3×[0,1,3] + 6×[0,1,2,3]
shrd RW:GPR:16, R:GPR:16, IMM(8)	3.00	6*	9×[6,7,8,9] + 3×[0,1,3] + 6×[0,1,2,3]
shrd RW:GPR:32, R:GPR:32, 0x0	3.00	6	
shrd RW:GPR:32, R:GPR:32, IMM(8)	3.00	6*	8×[6,7,8,9] + 3×[0,1,3] + 5×[0,1,2,3]
shrd RW:GPR:64, R:GPR:64, 0x0	3.00	6*	9×[6,7,8,9] + 3×[0,1,3] + 6×[0,1,2,3]
shrd RW:GPR:64, R:GPR:64, IMM(8)	3.00	6*	9×[6,7,8,9] + 3×[0,1,3] + 6×[0,1,2,3]
shrd dword ptr RW:MEM(32), R:GPR:32, 0x0	3.00	8+1*	9×[6,7,8,9] + 1×[5] + 9×[0,1,2,3]
shrd dword ptr RW:MEM(32), R:GPR:32, IMM(8)	3.00	8+1*	9×[6,7,8,9] + 1×[5] + 9×[0,1,2,3]
shrd qword ptr RW:MEM(64), R:GPR:64, 0x0	3.01	8+1*	9×[6,7,8,9] + 1×[5] + 9×[0,1,2,3]
shrd qword ptr RW:MEM(64), R:GPR:64, IMM(8)	3.00	8+1*	9×[6,7,8,9] + 1×[5] + 9×[0,1,2,3]
shrd word ptr RW:MEM(16), R:GPR:16, 0x0	3.00	8+1*	9×[6,7,8,9] + 1×[5] + 1×[4,5] + 9×[0,1,2,3]
shrd word ptr RW:MEM(16), R:GPR:16, IMM(8)	3.00	8+1*	9×[6,7,8,9] + 1×[5] + 1×[4,5] + 9×[0,1,2,3]
shrx W:GPR:32, R:GPR:32, R:GPR:32	0.25	1	1×[6,7,8,9]
shrx W:GPR:32, dword ptr R:MEM(32), R:GPR:32	0.50	2+1*	1×[6,7,8,9] + 1×[4,5]
shrx W:GPR:64, R:GPR:64, R:GPR:64	0.25	1	1×[6,7,8,9]
shrx W:GPR:64, qword ptr R:MEM(64), R:GPR:64	0.50	2+1*	1×[6,7,8,9] + 1×[4,5]
stc	0.25	1	1×[6,7,8,9]
sub RW:GPR:16, 0x0	0.25	1	1×[6,7,8,9]
sub RW:GPR:16, IMM(16)	0.25	1	1×[6,7,8,9]
sub RW:GPR:16, IMM(8)	0.25	1	1×[6,7,8,9]
sub RW:GPR:16, R:GPR:16	0.25	1	1×[6,7,8,9]
sub RW:GPR:16, word ptr R:MEM(16)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
sub RW:GPR:32, 0x0	0.25	1	1×[6,7,8,9]
sub RW:GPR:32, IMM(32)	0.25	1	1×[6,7,8,9]
sub RW:GPR:32, IMM(8)	0.25	1	1×[6,7,8,9]
sub RW:GPR:32, R:GPR:32	0.25	1	1×[6,7,8,9]
sub RW:GPR:32, dword ptr R:MEM(32)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
sub RW:GPR:64, 0x0	0.25	1	1×[6,7,8,9]
sub RW:GPR:64, IMM(32)	0.25	1	1×[6,7,8,9]
sub RW:GPR:64, IMM(8)	0.25	1	1×[6,7,8,9]
sub RW:GPR:64, R:GPR:64	0.25	1	1×[6,7,8,9]
sub RW:GPR:64, qword ptr R:MEM(64)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
sub RW:GPR:8, R:GPR:8	0.25	1	1×[6,7,8,9]
sub RW:GPR:8, byte ptr R:MEM(8)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
sub byte ptr RW:MEM(8), 0x0	1.36	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
sub byte ptr RW:MEM(8), IMM(8)	1.36	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
sub byte ptr RW:MEM(8), R:GPR:8	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
sub dword ptr RW:MEM(32), 0x0	1.00	1+1	1×[6,7,8,9] + 1×[5]
sub dword ptr RW:MEM(32), IMM(32)	1.00	1+1	1×[6,7,8,9] + 1×[5]
sub dword ptr RW:MEM(32), IMM(8)	1.00	1+1	1×[6,7,8,9] + 1×[5]
sub dword ptr RW:MEM(32), R:GPR:32	1.00	1+1	1×[6,7,8,9] + 1×[5]
sub qword ptr RW:MEM(64), 0x0	1.00	1+1	1×[6,7,8,9] + 1×[5]
sub qword ptr RW:MEM(64), IMM(32)	1.00	1+1	1×[6,7,8,9] + 1×[5]
sub qword ptr RW:MEM(64), IMM(8)	1.00	1+1	1×[6,7,8,9] + 1×[5]
sub qword ptr RW:MEM(64), R:GPR:64	1.00	1+1	1×[6,7,8,9] + 1×[5]
sub word ptr RW:MEM(16), 0x0	1.35	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
sub word ptr RW:MEM(16), IMM(16)	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
sub word ptr RW:MEM(16), IMM(8)	1.36	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
sub word ptr RW:MEM(16), R:GPR:16	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
test R:GPR:16, IMM(16)	0.25	1	1×[6,7,8,9]
test R:GPR:16, R:GPR:16	0.25	1	1×[6,7,8,9]
test R:GPR:32, IMM(32)	0.25	1	1×[6,7,8,9]
test R:GPR:32, R:GPR:32	0.25	1	1×[6,7,8,9]
test R:GPR:64, IMM(32)	0.25	1	1×[6,7,8,9]
test R:GPR:64, R:GPR:64	0.25	1	1×[6,7,8,9]
test R:al, 0x0	0.25	1	1×[6,7,8,9]
test R:al, IMM(8)	0.25	1	1×[6,7,8,9]
test R:GPR:8, R:GPR:8	0.25	1	1×[6,7,8,9]
test R:al,bl,cl,dl,r10b,r11b,r8b,r9b, 0x0	0.25	1	1×[6,7,8,9]
test R:al,bl,cl,dl,r10b,r11b,r8b,r9b, IMM(8)	0.25	1	1×[6,7,8,9]
test R:ax, IMM(16)	0.25	1	1×[6,7,8,9]
test R:bpl,dil,r12b,r13b,r14b,r15b,sil,spl, 0x0	0.25	1	1×[6,7,8,9]
test R:bpl,dil,r12b,r13b,r14b,r15b,sil,spl, IMM(8)	0.25	1	1×[6,7,8,9]
test R:eax, IMM(32)	0.25	1	1×[6,7,8,9]
test R:rax, IMM(32)	0.25	1	1×[6,7,8,9]
test byte ptr R:MEM(8), 0x0	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
test byte ptr R:MEM(8), IMM(8)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
test byte ptr R:MEM(8), R:GPR:8	0.50	1+1	1×[6,7,8,9] + 1×[4,5]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
test dword ptr R:MEM(32), IMM(32)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
test dword ptr R:MEM(32), R:GPR:32	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
test qword ptr R:MEM(64), IMM(32)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
test qword ptr R:MEM(64), R:GPR:64	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
test word ptr R:MEM(16), IMM(16)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
test word ptr R:MEM(16), R:GPR:16	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
tzcnt RW:GPR:16, R:GPR:16	0.51	2	2×[6,7,8,9]
tzcnt RW:GPR:16, word ptr R:MEM(16)	0.54	2+1	2×[6,7,8,9] + 1×[4,5]
tzcnt W:GPR:32, R:GPR:32	0.50	2	2×[6,7,8,9]
tzcnt W:GPR:32, dword ptr R:MEM(32)	0.55	2+1	2×[6,7,8,9] + 1×[4,5]
tzcnt W:GPR:64, R:GPR:64	0.50	2	2×[6,7,8,9]
tzcnt W:GPR:64, qword ptr R:MEM(64)	0.55	2+1	2×[6,7,8,9] + 1×[4,5]
vaddpd W:XMM, R:XMM, R:XMM	0.50	1	1×[2,3]
vaddpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[2,3] + 1×[4,5]
vaddpd W:YMM, R:YMM, R:YMM	1.00	2	2×[2,3]
vaddpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[2,3] + 2×[4,5]
vaddps W:XMM, R:XMM, R:XMM	0.50	1	1×[2,3]
vaddps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[2,3] + 1×[4,5]
vaddps W:YMM, R:YMM, R:YMM	1.00	2	2×[2,3]
vaddps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[2,3] + 2×[4,5]
vaddsd W:XMM, R:XMM, R:XMM	0.50	1	1×[2,3]
vaddsd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[2,3] + 1×[4,5]
vaddss W:XMM, R:XMM, R:XMM	0.50	1	1×[2,3]
vaddss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[2,3] + 1×[4,5]
vaddsubpd W:XMM, R:XMM, R:XMM	0.50	1	1×[2,3]
vaddsubpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[2,3] + 1×[4,5]
vaddsubpd W:YMM, R:YMM, R:YMM	1.00	2	2×[2,3]
vaddsubpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[2,3] + 2×[4,5]
vaddsubps W:XMM, R:XMM, R:XMM	0.50	1	1×[2,3]
vaddsubps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[2,3] + 1×[4,5]
vaddsubps W:YMM, R:YMM, R:YMM	1.00	2	2×[2,3]
vaddsubps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[2,3] + 2×[4,5]
vandnpd W:XMM, R:XMM, R:XMM	0.25	1	1×[0,1,2,3]
vandnpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vandnpd W:YMM, R:YMM, R:YMM	0.50	2	2×[0,1,2,3]
vandnpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,2,3]
vandnps W:XMM, R:XMM, R:XMM	0.25	1	1×[0,1,2,3]
vandnps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vandnps W:YMM, R:YMM, R:YMM	0.50	2	2×[0,1,2,3]
vandnps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,2,3]
vandpd W:XMM, R:XMM, R:XMM	0.25	1	1×[0,1,2,3]
vandpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vandpd W:YMM, R:YMM, R:YMM	0.50	2	2×[0,1,2,3]
vandpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,2,3]
vandps W:XMM, R:XMM, R:XMM	0.25	1	1×[0,1,2,3]
vandps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
vandps W:YMM, R:YMM, R:YMM	0.50	2	2×[0,1,2,3]
vandps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,2,3]
vblendpd W:XMM, R:XMM, R:XMM, IMM(8)	0.50	1	1×[0,1]
vblendpd W:XMM, R:XMM, xmmword ptr R:MEM(128), IMM(8)	0.50	1+1	1×[0,1] + 1×[4,5]
vblendpd W:YMM, R:YMM, R:YMM, IMM(8)	1.00	2	2×[0,1]
vblendpd W:YMM, R:YMM, ymmword ptr R:MEM(256), IMM(8)	1.00	2+2	2×[0,1] + 2×[4,5]
vblendps W:XMM, R:XMM, R:XMM, IMM(8)	0.50	1	1×[0,1]
vblendps W:XMM, R:XMM, xmmword ptr R:MEM(128), IMM(8)	0.50	1+1	1×[0,1] + 1×[4,5]
vblendps W:YMM, R:YMM, R:YMM, IMM(8)	1.00	2	2×[0,1]
vblendps W:YMM, R:YMM, ymmword ptr R:MEM(256), IMM(8)	1.00	2+2	2×[0,1] + 2×[4,5]
vbroadcastf128 W:YMM, xmmword ptr R:MEM(128)	0.50	2+1	1×[4,5] + 2×[0,1,2,3]
vbroadcasti128 W:YMM, xmmword ptr R:MEM(128)	0.50	2+1	1×[4,5] + 2×[0,1,2,3]
vbroadcastsd W:YMM, R:XMM	1.00	2	2×[1,2]
vbroadcastsd W:YMM, qword ptr R:MEM(64)	0.50	2+1	1×[4,5] + 2×[0,1,2,3]
vbroadcastss W:XMM, R:XMM	0.50	1	1×[1,2]
vbroadcastss W:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vbroadcastss W:YMM, R:XMM	1.00	2	2×[1,2]
vbroadcastss W:YMM, dword ptr R:MEM(32)	0.50	2+1	1×[4,5] + 2×[0,1,2,3]
vcmpeq_ospd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpeq_ospd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpeq_ospd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpeq_ospd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpeq_osps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpeq_osps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpeq_osps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpeq_osps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpeq_ossd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpeq_ossd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpeq_osss W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpeq_osss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpeq_uqpd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpeq_uqpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpeq_uqpd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpeq_uqpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpeq_uqps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpeq_uqps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpeq_uqps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpeq_uqps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpeq_uqsd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpeq_uqsd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpeq_uqss W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpeq_uqss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpeq_uspd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpeq_uspd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpeq_uspd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpeq_uspd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
vcmpeq_usps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpeq_usps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpeq_usps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpeq_usps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpeq_ussd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpeq_ussd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpeq_usss W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpeq_usss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpeqpd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpeqpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpeqpd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpeqpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpeqps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpeqps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpeqps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpeqps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpeqsd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpeqsd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpeqss W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpeqss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpfalse_ospd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpfalse_ospd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpfalse_ospd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpfalse_ospd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpfalse_osps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpfalse_osps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpfalse_osps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpfalse_osps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpfalse_ossd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpfalse_ossd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpfalse_osss W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpfalse_osss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpfalsepd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpfalsepd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpfalsepd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpfalsepd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpfalseps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpfalseps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpfalseps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpfalseps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpfalsesd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpfalsesd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpfalsess W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpfalsess W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpge_oqpd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpge_oqpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
vcmpge_oqpd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpge_oqpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpge_oqps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpge_oqps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpge_oqps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpge_oqps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpge_oqsd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpge_oqsd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpge_oqss W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpge_oqss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpgepd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpgepd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpgepd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpgepd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpgeps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpgeps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpgeps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpgeps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpgesd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpgesd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpgess W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpgess W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpgt_oqpd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpgt_oqpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpgt_oqpd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpgt_oqpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpgt_oqps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpgt_oqps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpgt_oqps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpgt_oqps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpgt_oqsd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpgt_oqsd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpgt_oqss W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpgt_oqss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpgtpd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpgtpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpgtpd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpgtpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpgtps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpgtps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpgtps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpgtps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpgtsd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpgtsd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpgtss W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpgtss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
vcmple_oqpd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmple_oqpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmple_oqpd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmple_oqpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmple_oqps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmple_oqps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmple_oqps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmple_oqps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmple_oqsd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmple_oqsd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmple_oqss W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmple_oqss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmplepd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmplepd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmplepd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmplepd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpleps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpleps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpleps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpleps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmplesd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmplesd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpless W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpless W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmplt_oqpd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmplt_oqpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmplt_oqpd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmplt_oqpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmplt_oqps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmplt_oqps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmplt_oqps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmplt_oqps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmplt_oqsd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmplt_oqsd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmplt_oqss W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmplt_oqss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpltpd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpltpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpltpd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpltpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpltps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpltps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpltps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpltps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpltsd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpltsd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
vcmpltss W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpltss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpneq_oqpd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpneq_oqpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpneq_oqpd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpneq_oqpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpneq_oqps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpneq_oqps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpneq_oqps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpneq_oqps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpneq_oqsd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpneq_oqsd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpneq_oqss W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpneq_oqss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpneq_ospd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpneq_ospd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpneq_ospd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpneq_ospd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpneq_osps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpneq_osps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpneq_osps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpneq_osps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpneq_ossd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpneq_ossd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpneq_osss W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpneq_osss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpneq_uspd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpneq_uspd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpneq_uspd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpneq_uspd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpneq_usps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpneq_usps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpneq_usps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpneq_usps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpneq_ussd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpneq_ussd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpneq_usss W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpneq_usss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpneqpd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpneqpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpneqpd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpneqpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpneqps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpneqps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpneqps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpneqps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
vcmpneqsd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpneqsd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpneqss W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpneqss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpnge_uqpd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpnge_uqpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpnge_uqpd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpnge_uqpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpnge_uqps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpnge_uqps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpnge_uqps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpnge_uqps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpnge_uqsd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpnge_uqsd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpnge_uqss W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpnge_uqss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpngepd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpngepd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpngepd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpngepd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpngeps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpngeps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpngeps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpngeps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpngesd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpngesd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpngess W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpngess W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpngt_uqpd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpngt_uqpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpngt_uqpd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpngt_uqpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpngt_uqps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpngt_uqps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpngt_uqps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpngt_uqps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpngt_uqsd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpngt_uqsd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpngt_uqss W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpngt_uqss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpngtpd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpngtpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpngtpd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpngtpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpngtps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpngtps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
vcmpngtps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpngtps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpngtsd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpngtsd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpngtss W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpngtss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpnle_uqpd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpnle_uqpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpnle_uqpd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpnle_uqpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpnle_uqps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpnle_uqps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpnle_uqps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpnle_uqps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpnle_uqsd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpnle_uqsd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpnle_uqss W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpnle_uqss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpnlepd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpnlepd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpnlepd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpnlepd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpnleps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpnleps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpnleps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpnleps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpnlesd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpnlesd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpnless W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpnless W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpnlt_uqpd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpnlt_uqpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpnlt_uqpd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpnlt_uqpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpnlt_uqps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpnlt_uqps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpnlt_uqps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpnlt_uqps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpnlt_uqsd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpnlt_uqsd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpnlt_uqss W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpnlt_uqss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpnltpd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpnltpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpnltpd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpnltpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
vcmpnltps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpnltps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpnltps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpnltps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpnltsd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpnltsd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpnltss W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpnltss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpord_spd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpord_spd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpord_spd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpord_spd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpord_sps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpord_sps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpord_sps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpord_ssd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpord_ssd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpord_sss W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpord_sss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpordpd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpordpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpordpd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpordpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpordps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpordps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpordps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpordps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpordsd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpordsd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpordss W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpordss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmppd W:XMM, R:XMM, R:XMM, IMM(8)	0.50	1	1×[0,1]
vcmppd W:XMM, R:XMM, xmmword ptr R:MEM(128), IMM(8)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmppd W:YMM, R:YMM, R:YMM, IMM(8)	1.00	2	2×[0,1]
vcmppd W:YMM, R:YMM, ymmword ptr R:MEM(256), IMM(8)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpps W:XMM, R:XMM, R:XMM, IMM(8)	0.50	1	1×[0,1]
vcmpps W:XMM, R:XMM, xmmword ptr R:MEM(128), IMM(8)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpps W:YMM, R:YMM, R:YMM, IMM(8)	1.00	2	2×[0,1]
vcmpps W:YMM, R:YMM, ymmword ptr R:MEM(256), IMM(8)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpsd W:XMM, R:XMM, R:XMM, IMM(8)	0.50	1	1×[0,1]
vcmpsd W:XMM, R:XMM, qword ptr R:MEM(64), IMM(8)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpss W:XMM, R:XMM, R:XMM, IMM(8)	0.50	1	1×[0,1]
vcmpss W:XMM, R:XMM, dword ptr R:MEM(32), IMM(8)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmptrue_uspd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmptrue_uspd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmptrue_uspd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
vcmptrue_uspd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmptrue_usps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmptrue_usps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmptrue_usps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmptrue_usps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmptrue_ussd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmptrue_ussd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmptrue_usss W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmptrue_usss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmptruepd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmptruepd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmptruepd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmptruepd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmptrueps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmptrueps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmptrueps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmptrueps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmptruesd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmptruesd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmptruess W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmptruess W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpunord_spd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpunord_spd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpunord_spd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpunord_spd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpunord_sps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpunord_sps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpunord_sps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpunord_sps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpunord_ssd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpunord_ssd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpunord_sss W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpunord_sss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpunordpd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpunordpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpunordpd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpunordpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpunordps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpunordps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpunordps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vcmpunordps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vcmpunordsd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpunordsd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vcmpunordss W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vcmpunordss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vcomisd R:XMM, R:XMM	1.00	2*	1×[2] + 1×[0,1] + 2×[6,7,8,9]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
`vcomisd R:XMM, qword ptr R:MEM(64)`	1.00	2+1*	1×[2] + 1×[0,1] + 2×[6,7,8,9] + 1×[4,5]
`vcomiss R:XMM, R:XMM`	1.00	2*	1×[2] + 1×[0,1] + 2×[6,7,8,9]
`vcomiss R:XMM, dword ptr R:MEM(32)`	1.00	2+1*	1×[2] + 1×[0,1] + 2×[6,7,8,9] + 1×[4,5]
`vdppd W:XMM, R:XMM, R:XMM, IMM(8)`	3.00	3	
`vdppd W:XMM, R:XMM, xmmword ptr R:MEM(128), IMM(8)`	4.00	5+1	
`vdpps W:XMM, R:XMM, R:XMM, IMM(8)`	4.00	8	
`vdpps W:XMM, R:XMM, xmmword ptr R:MEM(128), IMM(8)`	5.00	10+1	
`vdpps W:YMM, R:YMM, R:YMM, IMM(8)`	5.00	13	
`vdpps W:YMM, R:YMM, ymmword ptr R:MEM(256), IMM(8)`	5.00	14+2	
`vextractf128 W:XMM, R:YMM, IMM(8)`	0.33	1	1×[0,1,3]
`vextractf128 xmmword ptr W:MEM(128), R:YMM, IMM(8)`	1.00	2+1	1×[2] + 1×[5] + 1×[0,1,3]
`vextracti128 W:XMM, R:YMM, IMM(8)`	0.33	1	1×[0,1,3]
`vextracti128 xmmword ptr W:MEM(128), R:YMM, IMM(8)`	1.00	2+1	1×[2] + 1×[5] + 1×[0,1,3]
`vextractps W:GPR:32, R:XMM, IMM(8)`	1.00	2*	1×[2] + 2×[6,7,8,9] + 1×[1,2]
`vextractps dword ptr W:MEM(32), R:XMM, IMM(8)`	1.00	2+1	1×[2] + 1×[1,2] + 1×[5]
`vhaddpd W:XMM, R:XMM, R:XMM`	2.00	4*	4×[6,7,8,9] + 2×[1,2] + 1×[2,3] + 1×[0,1,2,3]
`vhaddpd W:XMM, R:XMM, xmmword ptr R:MEM(128)`	2.00	4+1*	4×[6,7,8,9] + 2×[1,2] + 1×[2,3] + 1×[4,5] + 1×[0,1,2,3]
`vhaddpd W:YMM, R:YMM, R:YMM`	3.00	8*	9×[6,7,8,9] + 4×[1,2] + 2×[2,3] + 3×[0,1,2,3]
`vhaddpd W:YMM, R:YMM, ymmword ptr R:MEM(256)`	4.00	10+2	
`vhaddps W:XMM, R:XMM, R:XMM`	2.00	4*	4×[6,7,8,9] + 2×[1,2] + 1×[2,3] + 1×[0,1,2,3]
`vhaddps W:XMM, R:XMM, xmmword ptr R:MEM(128)`	2.00	4+1*	4×[6,7,8,9] + 2×[1,2] + 1×[2,3] + 1×[4,5] + 1×[0,1,2,3]
`vhaddps W:YMM, R:YMM, R:YMM`	3.00	8*	9×[6,7,8,9] + 4×[1,2] + 2×[2,3] + 3×[0,1,2,3]
`vhaddps W:YMM, R:YMM, ymmword ptr R:MEM(256)`	4.01	11+2*	13×[6,7,8,9] + 4×[1,2] + 2×[2,3] + 2×[4,5] + 7×[0,1,2,3]
`vhsubpd W:XMM, R:XMM, R:XMM`	2.00	4*	4×[6,7,8,9] + 2×[1,2] + 1×[2,3] + 1×[0,1,2,3]
`vhsubpd W:XMM, R:XMM, xmmword ptr R:MEM(128)`	2.00	4+1*	4×[6,7,8,9] + 2×[1,2] + 1×[2,3] + 1×[4,5] + 1×[0,1,2,3]
`vhsubpd W:YMM, R:YMM, R:YMM`	3.00	8*	9×[6,7,8,9] + 4×[1,2] + 2×[2,3] + 3×[0,1,2,3]
`vhsubpd W:YMM, R:YMM, ymmword ptr R:MEM(256)`	4.01	10+2	
`vhsubps W:XMM, R:XMM, R:XMM`	2.00	4*	4×[6,7,8,9] + 2×[1,2] + 1×[2,3] + 1×[0,1,2,3]
`vhsubps W:XMM, R:XMM, xmmword ptr R:MEM(128)`	2.00	4+1*	4×[6,7,8,9] + 2×[1,2] + 1×[2,3] + 1×[4,5] + 1×[0,1,2,3]
`vhsubps W:YMM, R:YMM, R:YMM`	3.00	8*	9×[6,7,8,9] + 4×[1,2] + 2×[2,3] + 3×[0,1,2,3]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
vhsubps W:YMM, R:YMM, ymmword ptr R:MEM(256)	4.00	10+2*	13×[6,7,8,9] + 4×[1,2] + 2×[2,3] + 2×[4,5] + 1×[0,1,3] + 6×[0,1,2,3]
vinsertf128 W:YMM, R:YMM, R:XMM, IMM(8)	0.67	2	2×[0,1,3]
vinsertf128 W:YMM, R:YMM, xmmword ptr R:MEM(128), IMM(8)	1.00	2+1*	2×[4,5] + 2×[0,1,3]
vinserti128 W:YMM, R:YMM, R:XMM, IMM(8)	0.67	2	2×[0,1,3]
vinserti128 W:YMM, R:YMM, xmmword ptr R:MEM(128), IMM(8)	1.00	2+1*	2×[4,5] + 2×[0,1,3]
vinsertps W:XMM, R:XMM, R:XMM, IMM(8)	0.50	1	1×[1,2]
vinsertps W:XMM, R:XMM, dword ptr R:MEM(32), IMM(8)	0.50	1+1	1×[1,2] + 1×[4,5]
vlddqu W:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vlddqu W:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,2,3]
vmaskmovpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	4.00	12+1*	1×[3] + 1×[2] + 2×[0,1] + 13×[6,7,8,9] + 1×[0,3] + 1×[2,3] + 3×[4,5] + 7×[0,1,2,3]
vmaskmovpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	7.00	24+2*	2×[3] + 1×[2] + 4×[0,1] + 26×[6,7,8,9] + 2×[0,3] + 2×[2,3] + 5×[4,5] + 15×[0,1,2,3]
vmaskmovpd xmmword ptr W:MEM(128), R:XMM, R:XMM	4.00	10+1*	3×[2] + 13×[6,7,8,9] + 1×[1,2] + 2×[5] + 3×[4,5] + 3×[0,1,3] + 6×[0,1,2,3]
vmaskmovpd ymmword ptr W:MEM(256), R:YMM, R:YMM	6.00	18+2	
vmaskmovps W:XMM, R:XMM, xmmword ptr R:MEM(128)	6.00	20+1	
vmaskmovps W:YMM, R:YMM, ymmword ptr R:MEM(256)	10.00	36+2	
vmaskmovps xmmword ptr W:MEM(128), R:XMM, R:XMM	6.00	19+1	
vmaskmovps ymmword ptr W:MEM(256), R:YMM, R:YMM	12.00	42+2	
vmaxpd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vmaxpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vmaxpd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vmaxpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vmaxps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vmaxps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vmaxps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vmaxps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vmaxsd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vmaxsd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]
vmaxss W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vmaxss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vminpd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vminpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vminpd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vminpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vminps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vminps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,1] + 1×[4,5]
vminps W:YMM, R:YMM, R:YMM	1.00	2	2×[0,1]
vminps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,1] + 2×[4,5]
vminsd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vminsd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[0,1] + 1×[4,5]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
vminss W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vminss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[0,1] + 1×[4,5]
vmovapd W:XMM, R:XMM	0.25	1	1×[0,1,2,3]
vmovapd W:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vmovapd W:YMM, R:YMM	0.50	2	2×[0,1,2,3]
vmovapd W:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,2,3]
vmovapd xmmword ptr W:MEM(128), R:XMM	1.00	1+1	1×[2] + 1×[5]
vmovapd ymmword ptr W:MEM(256), R:YMM	2.00	2+2	2×[2] + 2×[5]
vmovaps W:XMM, R:XMM	0.25	1	1×[0,1,2,3]
vmovaps W:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vmovaps W:YMM, R:YMM	0.50	2	2×[0,1,2,3]
vmovaps W:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,2,3]
vmovaps xmmword ptr W:MEM(128), R:XMM	1.00	1+1	1×[2] + 1×[5]
vmovaps ymmword ptr W:MEM(256), R:YMM	2.00	2+2	2×[2] + 2×[5]
vmovd W:GPR:32, R:XMM	1.00	1	1×[2]
vmovd dword ptr W:MEM(32), R:XMM	1.00	1+1	1×[2] + 1×[5]
vmovddup W:XMM, R:XMM	0.50	1	1×[1,2]
vmovddup W:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vmovddup W:YMM, R:YMM	1.00	2	2×[1,2]
vmovddup W:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,2,3]
vmovdqa W:XMM, R:XMM	0.25	1	1×[0,1,2,3]
vmovdqa W:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vmovdqa W:YMM, R:YMM	0.50	2	2×[0,1,2,3]
vmovdqa W:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,2,3]
vmovdqa xmmword ptr W:MEM(128), R:XMM	1.00	1+1	1×[2] + 1×[5]
vmovdqa ymmword ptr W:MEM(256), R:YMM	2.00	2+2	2×[2] + 2×[5]
vmovdqu W:XMM, R:XMM	0.25	1	1×[0,1,2,3]
vmovdqu W:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vmovdqu W:YMM, R:YMM	0.50	2	2×[0,1,2,3]
vmovdqu W:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,2,3]
vmovdqu xmmword ptr W:MEM(128), R:XMM	1.00	1+1	1×[2] + 1×[5]
vmovdqu ymmword ptr W:MEM(256), R:YMM	2.00	2+2	2×[2] + 2×[5]
vmovhlps W:XMM, R:XMM, R:XMM	0.50	1	1×[1,2]
vmovhpd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[1,2] + 1×[4,5]
vmovhpd qword ptr W:MEM(64), R:XMM	1.00	2+1	1×[2] + 1×[1,2] + 1×[5]
vmovhps W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[1,2] + 1×[4,5]
vmovhps qword ptr W:MEM(64), R:XMM	1.00	2+1	1×[2] + 1×[1,2] + 1×[5]
vmovlhps W:XMM, R:XMM, R:XMM	0.50	1	1×[1,2]
vmovlpd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vmovlpd qword ptr W:MEM(64), R:XMM	1.00	1+1	1×[2] + 1×[5]
vmovlps W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vmovlps qword ptr W:MEM(64), R:XMM	1.00	1+1	1×[2] + 1×[5]
vmovmskpd W:GPR:32, R:XMM	1.00	1	1×[2]
vmovmskpd W:GPR:32, R:YMM	1.00	1	1×[2]
vmovmskps W:GPR:32, R:XMM	1.00	1	1×[2]
vmovmskps W:GPR:32, R:YMM	1.00	1	1×[2]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
vmovntdq xmmword ptr W:MEM(128), R:XMM	1.00	1+1	
vmovntdq ymmword ptr W:MEM(256), R:YMM	2.00	2+2	
vmovntdqa W:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vmovntdqa W:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,2,3]
vmovntpd xmmword ptr W:MEM(128), R:XMM	1.00	1+1	
vmovntpd ymmword ptr W:MEM(256), R:YMM	2.00	2+2	
vmovntps xmmword ptr W:MEM(128), R:XMM	1.00	1+1	
vmovntps ymmword ptr W:MEM(256), R:YMM	2.00	2+2	
vmovq W:GPR:64, R:XMM	1.00	1	1×[2]
vmovq W:XMM, R:XMM	0.25	1	1×[0,1,2,3]
vmovq qword ptr W:MEM(64), R:XMM	1.00	1+1	1×[2] + 1×[5]
vmovsd W:XMM, R:XMM, R:XMM	0.25	1	1×[0,1,2,3]
vmovsd W:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vmovsd qword ptr W:MEM(64), R:XMM	1.00	1+1	1×[2] + 1×[5]
vmovshdup W:XMM, R:XMM	0.50	1	1×[1,2]
vmovshdup W:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vmovshdup W:YMM, R:YMM	1.00	2	2×[1,2]
vmovshdup W:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,2,3]
vmovsldup W:XMM, R:XMM	0.50	1	1×[1,2]
vmovsldup W:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vmovsldup W:YMM, R:YMM	1.00	2	2×[1,2]
vmovsldup W:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,2,3]
vmovss W:XMM, R:XMM, R:XMM	0.25	1	1×[0,1,2,3]
vmovss W:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vmovss dword ptr W:MEM(32), R:XMM	1.00	1+1	1×[2] + 1×[5]
vmovupd W:XMM, R:XMM	0.25	1	1×[0,1,2,3]
vmovupd W:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vmovupd W:YMM, R:YMM	0.50	2	2×[0,1,2,3]
vmovupd W:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,2,3]
vmovupd xmmword ptr W:MEM(128), R:XMM	1.00	1+1	1×[2] + 1×[5]
vmovupd ymmword ptr W:MEM(256), R:YMM	2.00	2+2	2×[2] + 2×[5]
vmovups W:XMM, R:XMM	0.25	1	1×[0,1,2,3]
vmovups W:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vmovups W:YMM, R:YMM	0.50	2	2×[0,1,2,3]
vmovups W:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,2,3]
vmovups xmmword ptr W:MEM(128), R:XMM	1.00	1+1	1×[2] + 1×[5]
vmovups ymmword ptr W:MEM(256), R:YMM	2.00	2+2	2×[2] + 2×[5]
vmpsadbw W:XMM, R:XMM, R:XMM, IMM(8)	2.01	4	
vmpsadbw W:XMM, R:XMM, xmmword ptr R:MEM(128), IMM(8)	3.00	6+1	
vmpsadbw W:YMM, R:YMM, R:YMM, IMM(8)	3.00	8	
vmpsadbw W:YMM, R:YMM, ymmword ptr R:MEM(256), IMM(8)	4.00	12+2	
vmulps W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]
vmulps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	
vmulps W:YMM, R:YMM, R:YMM	1.00	2	
vmulps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	
vmulss W:XMM, R:XMM, R:XMM	0.50	1	1×[0,1]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
vmulss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	
vorpd W:XMM, R:XMM, R:XMM	0.25	1	1×[0,1,2,3]
vorpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vorpd W:YMM, R:YMM, R:YMM	0.50	2	2×[0,1,2,3]
vorpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,2,3]
vorps W:XMM, R:XMM, R:XMM	0.25	1	1×[0,1,2,3]
vorps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vorps W:YMM, R:YMM, R:YMM	0.50	2	2×[0,1,2,3]
vorps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,2,3]
vpabsb W:XMM, R:XMM	0.50	1	1×[0,3]
vpabsb W:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,3] + 1×[4,5]
vpabsb W:YMM, R:YMM	1.00	2	2×[0,3]
vpabsb W:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,3] + 2×[4,5]
vpabsd W:XMM, R:XMM	0.50	1	1×[0,3]
vpabsd W:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,3] + 1×[4,5]
vpabsd W:YMM, R:YMM	1.00	2	2×[0,3]
vpabsd W:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,3] + 2×[4,5]
vpabsw W:XMM, R:XMM	0.50	1	1×[0,3]
vpabsw W:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,3] + 1×[4,5]
vpabsw W:YMM, R:YMM	1.00	2	2×[0,3]
vpabsw W:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,3] + 2×[4,5]
vpackssdw W:XMM, R:XMM, R:XMM	0.50	1	1×[1,2]
vpackssdw W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[1,2] + 1×[4,5]
vpackssdw W:YMM, R:YMM, R:YMM	1.00	2	2×[1,2]
vpackssdw W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[1,2] + 2×[4,5]
vpacksswb W:XMM, R:XMM, R:XMM	0.50	1	1×[1,2]
vpacksswb W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[1,2] + 1×[4,5]
vpacksswb W:YMM, R:YMM, R:YMM	1.00	2	2×[1,2]
vpacksswb W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[1,2] + 2×[4,5]
vpackusdw W:XMM, R:XMM, R:XMM	0.50	1	1×[1,2]
vpackusdw W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[1,2] + 1×[4,5]
vpackusdw W:YMM, R:YMM, R:YMM	1.00	2	2×[1,2]
vpackusdw W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[1,2] + 2×[4,5]
vpackuswb W:XMM, R:XMM, R:XMM	0.50	1	1×[1,2]
vpackuswb W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[1,2] + 1×[4,5]
vpackuswb W:YMM, R:YMM, R:YMM	1.00	2	2×[1,2]
vpackuswb W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[1,2] + 2×[4,5]
vpaddb W:XMM, R:XMM, R:XMM	0.33	1	1×[0,1,3]
vpaddb W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,3]
vpaddb W:YMM, R:YMM, R:YMM	0.67	2	2×[0,1,3]
vpaddb W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,3]
vpaddd W:XMM, R:XMM, R:XMM	0.33	1	1×[0,1,3]
vpaddd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,3]
vpaddd W:YMM, R:YMM, R:YMM	0.67	2	2×[0,1,3]
vpaddd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,3]
vpaddq W:XMM, R:XMM, R:XMM	0.33	1	1×[0,1,3]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
vpaddq W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,3]
vpaddq W:YMM, R:YMM, R:YMM	0.67	2	2×[0,1,3]
vpaddq W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,3]
vpaddsb W:XMM, R:XMM, R:XMM	0.50	1	1×[0,3]
vpaddsb W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,3] + 1×[4,5]
vpaddsb W:YMM, R:YMM, R:YMM	1.00	2	2×[0,3]
vpaddsb W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,3] + 2×[4,5]
vpaddsw W:XMM, R:XMM, R:XMM	0.50	1	1×[0,3]
vpaddsw W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,3] + 1×[4,5]
vpaddsw W:YMM, R:YMM, R:YMM	1.00	2	2×[0,3]
vpaddsw W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,3] + 2×[4,5]
vpaddusb W:XMM, R:XMM, R:XMM	0.50	1	1×[0,3]
vpaddusb W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,3] + 1×[4,5]
vpaddusb W:YMM, R:YMM, R:YMM	1.00	2	2×[0,3]
vpaddusb W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,3] + 2×[4,5]
vpaddusw W:XMM, R:XMM, R:XMM	0.50	1	1×[0,3]
vpaddusw W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,3] + 1×[4,5]
vpaddusw W:YMM, R:YMM, R:YMM	1.00	2	2×[0,3]
vpaddusw W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,3] + 2×[4,5]
vpaddw W:XMM, R:XMM, R:XMM	0.33	1	1×[0,1,3]
vpaddw W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,3]
vpaddw W:YMM, R:YMM, R:YMM	0.67	2	2×[0,1,3]
vpaddw W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,3]
vpalignr W:XMM, R:XMM, R:XMM, IMM(8)	0.50	1	1×[1,2]
vpalignr W:XMM, R:XMM, xmmword ptr R:MEM(128), IMM(8)	0.50	1+1	1×[1,2] + 1×[4,5]
vpalignr W:YMM, R:YMM, R:YMM, IMM(8)	1.00	2	2×[1,2]
vpalignr W:YMM, R:YMM, ymmword ptr R:MEM(256), IMM(8)	1.00	2+2	2×[1,2] + 2×[4,5]
vpand W:XMM, R:XMM, R:XMM	0.25	1	1×[0,1,2,3]
vpand W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vpand W:YMM, R:YMM, R:YMM	0.50	2	2×[0,1,2,3]
vpand W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,2,3]
vpandn W:XMM, R:XMM, R:XMM	0.25	1	1×[0,1,2,3]
vpandn W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vpandn W:YMM, R:YMM, R:YMM	0.50	2	2×[0,1,2,3]
vpandn W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,2,3]
vpavgb W:XMM, R:XMM, R:XMM	0.50	1	1×[0,3]
vpavgb W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,3] + 1×[4,5]
vpavgb W:YMM, R:YMM, R:YMM	1.00	2	2×[0,3]
vpavgb W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,3] + 2×[4,5]
vpavgw W:XMM, R:XMM, R:XMM	0.50	1	1×[0,3]
vpavgw W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,3] + 1×[4,5]
vpavgw W:YMM, R:YMM, R:YMM	1.00	2	2×[0,3]
vpavgw W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,3] + 2×[4,5]
vpblendd W:XMM, R:XMM, R:XMM, IMM(8)	0.33	1	1×[0,1,3]
vpblendd W:XMM, R:XMM, xmmword ptr R:MEM(128), IMM(8)	0.50	1+1	1×[4,5] + 1×[0,1,3]
vpblendd W:YMM, R:YMM, R:YMM, IMM(8)	0.67	2	2×[0,1,3]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
vpblendd W:YMM, R:YMM, ymmword ptr R:MEM(256), IMM(8)	1.00	2+2	2×[4,5] + 2×[0,1,3]
vpblendw W:XMM, R:XMM, R:XMM, IMM(8)	0.33	1	1×[0,1,3]
vpblendw W:XMM, R:XMM, xmmword ptr R:MEM(128), IMM(8)	0.50	1+1	1×[4,5] + 1×[0,1,3]
vpblendw W:YMM, R:YMM, R:YMM, IMM(8)	0.67	2	2×[0,1,3]
vpblendw W:YMM, R:YMM, ymmword ptr R:MEM(256), IMM(8)	1.00	2+2	2×[4,5] + 2×[0,1,3]
vpbroadcastb W:XMM, R:XMM	0.50	1	1×[1,2]
vpbroadcastb W:XMM, byte ptr R:MEM(8)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vpbroadcastb W:YMM, R:XMM	1.00	2	2×[1,2]
vpbroadcastb W:YMM, byte ptr R:MEM(8)	0.50	2+1	1×[4,5] + 2×[0,1,2,3]
vpbroadcastd W:XMM, R:XMM	0.50	1	1×[1,2]
vpbroadcastd W:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vpbroadcastd W:YMM, R:XMM	1.00	2	2×[1,2]
vpbroadcastd W:YMM, dword ptr R:MEM(32)	0.50	2+1	1×[4,5] + 2×[0,1,2,3]
vpbroadcastq W:XMM, R:XMM	0.50	1	1×[1,2]
vpbroadcastq W:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vpbroadcastq W:YMM, R:XMM	1.00	2	2×[1,2]
vpbroadcastq W:YMM, qword ptr R:MEM(64)	0.50	2+1	1×[4,5] + 2×[0,1,2,3]
vpbroadcastw W:XMM, R:XMM	0.50	1	1×[1,2]
vpbroadcastw W:XMM, word ptr R:MEM(16)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vpbroadcastw W:YMM, R:XMM	1.00	2	2×[1,2]
vpbroadcastw W:YMM, word ptr R:MEM(16)	0.50	2+1	1×[4,5] + 2×[0,1,2,3]
vpclmulqdq W:XMM, R:XMM, R:XMM, IMM(8)	2.00	4	
vpclmulqdq W:XMM, R:XMM, xmmword ptr R:MEM(128), IMM(8)	2.00	4+1	
vpcmpeqb W:XMM, R:XMM, R:XMM	0.33	1	1×[0,1,3]
vpcmpeqb W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,3]
vpcmpeqb W:YMM, R:YMM, R:YMM	0.67	2	2×[0,1,3]
vpcmpeqb W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,3]
vpcmpeqd W:XMM, R:XMM, R:XMM	0.33	1	1×[0,1,3]
vpcmpeqd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,3]
vpcmpeqd W:YMM, R:YMM, R:YMM	0.67	2	2×[0,1,3]
vpcmpeqd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,3]
vpcmpeqq W:XMM, R:XMM, R:XMM	0.50	1	1×[0,3]
vpcmpeqq W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,3] + 1×[4,5]
vpcmpeqq W:YMM, R:YMM, R:YMM	1.00	2	2×[0,3]
vpcmpeqq W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,3] + 2×[4,5]
vpcmpeqw W:XMM, R:XMM, R:XMM	0.33	1	1×[0,1,3]
vpcmpeqw W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,3]
vpcmpeqw W:YMM, R:YMM, R:YMM	0.67	2	2×[0,1,3]
vpcmpeqw W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,3]
vpcmpestrm R:XMM, R:XMM, IMM(8)	3.00	7	
vpcmpestrm R:XMM, xmmword ptr R:MEM(128), IMM(8)	4.01	12+1	
vpcmpgtb W:XMM, R:XMM, R:XMM	0.33	1	1×[0,1,3]
vpcmpgtb W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,3]
vpcmpgtb W:YMM, R:YMM, R:YMM	0.67	2	2×[0,1,3]
vpcmpgtb W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,3]
vpcmpgtd W:XMM, R:XMM, R:XMM	0.33	1	1×[0,1,3]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
vpcmpgtd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,3]
vpcmpgtd W:YMM, R:YMM, R:YMM	0.67	2	2×[0,1,3]
vpcmpgtd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,3]
vpcmpgtw W:XMM, R:XMM, R:XMM	0.33	1	1×[0,1,3]
vpcmpgtw W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,3]
vpcmpgtw W:YMM, R:YMM, R:YMM	0.67	2	2×[0,1,3]
vpcmpgtw W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,3]
vpcmpistrm R:XMM, R:XMM, IMM(8)	2.00	3	
vpcmpistrm R:XMM, xmmword ptr R:MEM(128), IMM(8)	2.00	4+1	
vperm2f128 W:YMM, R:YMM, R:YMM, IMM(8)	3.01	8*	9×[6,7,8,9] + 6×[0,1,3] + 3×[0,1,2,3]
vperm2f128 W:YMM, R:YMM, ymmword ptr R:MEM(256), IMM(8)	4.00	12+2*	13×[6,7,8,9] + 2×[4,5] + 6×[0,1,3] + 7×[0,1,2,3]
vperm2i128 W:YMM, R:YMM, R:YMM, IMM(8)	3.00	8*	9×[6,7,8,9] + 6×[0,1,3] + 3×[0,1,2,3]
vperm2i128 W:YMM, R:YMM, ymmword ptr R:MEM(256), IMM(8)	4.00	12+2*	13×[6,7,8,9] + 2×[4,5] + 6×[0,1,3] + 7×[0,1,2,3]
vpermd W:YMM, R:YMM, ymmword ptr R:MEM(256)	4.00	4+2	
vpermilpd W:XMM, R:XMM, IMM(8)	0.50	1	1×[1,2]
vpermilpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	2.00	1+1	
vpermilpd W:XMM, xmmword ptr R:MEM(128), IMM(8)	0.50	1+1	1×[1,2] + 1×[4,5]
vpermilpd W:YMM, R:YMM, IMM(8)	1.00	2	2×[1,2]
vpermilpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	4.00	2+2	
vpermilpd W:YMM, ymmword ptr R:MEM(256), IMM(8)	1.00	2+2	2×[1,2] + 2×[4,5]
vpermilps W:XMM, R:XMM, IMM(8)	0.50	1	1×[1,2]
vpermilps W:XMM, R:XMM, xmmword ptr R:MEM(128)	2.00	1+1	
vpermilps W:XMM, xmmword ptr R:MEM(128), IMM(8)	0.50	1+1	1×[1,2] + 1×[4,5]
vpermilps W:YMM, R:YMM, IMM(8)	1.00	2	2×[1,2]
vpermilps W:YMM, R:YMM, ymmword ptr R:MEM(256)	4.00	2+2	
vpermilps W:YMM, ymmword ptr R:MEM(256), IMM(8)	1.00	2+2	2×[1,2] + 2×[4,5]
vpermpd W:YMM, R:YMM, IMM(8)	2.01	3*	4×[6,7,8,9] + 2×[1,2] + 2×[0,1,2,3]
vpermpd W:YMM, ymmword ptr R:MEM(256), IMM(8)	2.00	4+2	
vpermps W:YMM, R:YMM, ymmword ptr R:MEM(256)	4.00	4+2	
vpermq W:YMM, R:YMM, IMM(8)	2.00	3*	4×[6,7,8,9] + 2×[1,2] + 2×[0,1,3]
vpermq W:YMM, ymmword ptr R:MEM(256), IMM(8)	2.00	4+2*	5×[6,7,8,9] + 2×[1,2] + 2×[4,5] + 3×[0,1,2,3]
vpextrb W:GPR:32, R:XMM, IMM(8)	1.00	2*	1×[2] + 2×[6,7,8,9] + 1×[1,2]
vpextrb byte ptr RW:MEM(8), R:XMM, IMM(8)	1.00	2+1	1×[2] + 1×[1,2] + 1×[5]
vpextrd W:GPR:32, R:XMM, IMM(8)	1.00	2*	1×[2] + 2×[6,7,8,9] + 1×[1,2]
vpextrd dword ptr W:MEM(32), R:XMM, IMM(8)	1.00	2+1	1×[2] + 1×[1,2] + 1×[5]
vpextrq W:GPR:64, R:XMM, IMM(8)	1.00	2*	1×[2] + 2×[6,7,8,9] + 1×[1,2]
vpextrq qword ptr W:MEM(64), R:XMM, IMM(8)	1.00	2+1	1×[2] + 1×[1,2] + 1×[5]
vpextrw W:GPR:32, R:XMM, IMM(8)	1.00	2*	1×[2] + 2×[6,7,8,9] + 1×[1,2]
vpextrw word ptr RW:MEM(16), R:XMM, IMM(8)	1.00	2+1	1×[2] + 1×[1,2] + 1×[5]
vphaddd W:XMM, R:XMM, R:XMM	2.00	4*	4×[6,7,8,9] + 2×[1,2] + 1×[0,1,3] + 1×[0,1,2,3]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
`vphaddd W:XMM, R:XMM, xmmword ptr R:MEM(128)`	2.00	4+1*	4×[6,7,8,9] + 2×[1,2] + 1×[4,5] + 1×[0,1,3] + 1×[0,1,2,3]
`vphaddd W:YMM, R:YMM, R:YMM`	3.00	8*	9×[6,7,8,9] + 4×[1,2] + 2×[0,1,3] + 3×[0,1,2,3]
`vphaddd W:YMM, R:YMM, ymmword ptr R:MEM(256)`	4.00	10+2*	13×[6,7,8,9] + 4×[1,2] + 2×[4,5] + 2×[0,1,3] + 7×[0,1,2,3]
`vphaddsw W:XMM, R:XMM, R:XMM`	2.00	4*	4×[6,7,8,9] + 2×[1,2] + 1×[0,3] + 1×[0,1,2,3]
`vphaddsw W:XMM, R:XMM, xmmword ptr R:MEM(128)`	2.00	4+1*	4×[6,7,8,9] + 2×[1,2] + 1×[0,3] + 1×[4,5] + 1×[0,1,2,3]
`vphaddsw W:YMM, R:YMM, R:YMM`	3.00	8*	9×[6,7,8,9] + 4×[1,2] + 2×[0,3] + 3×[0,1,2,3]
`vphaddsw W:YMM, R:YMM, ymmword ptr R:MEM(256)`	4.00	10+2*	13×[6,7,8,9] + 4×[1,2] + 2×[0,3] + 2×[4,5] + 7×[0,1,2,3]
`vphaddw W:XMM, R:XMM, R:XMM`	2.00	4*	4×[6,7,8,9] + 2×[1,2] + 1×[0,1,3] + 1×[0,1,2,3]
`vphaddw W:XMM, R:XMM, xmmword ptr R:MEM(128)`	2.01	4+1*	4×[6,7,8,9] + 2×[1,2] + 1×[4,5] + 1×[0,1,3] + 1×[0,1,2,3]
`vphaddw W:YMM, R:YMM, R:YMM`	3.00	8*	9×[6,7,8,9] + 4×[1,2] + 2×[0,1,3] + 3×[0,1,2,3]
`vphaddw W:YMM, R:YMM, ymmword ptr R:MEM(256)`	4.00	10+2*	13×[6,7,8,9] + 4×[1,2] + 2×[4,5] + 2×[0,1,3] + 7×[0,1,2,3]
`vphminposuw W:XMM, xmmword ptr R:MEM(128)`	2.00	1+1	
`vphsubd W:XMM, R:XMM, R:XMM`	2.01	4*	4×[6,7,8,9] + 2×[1,2] + 1×[0,1,3] + 1×[0,1,2,3]
`vphsubd W:XMM, R:XMM, xmmword ptr R:MEM(128)`	2.01	4+1*	4×[6,7,8,9] + 2×[1,2] + 1×[4,5] + 1×[0,1,3] + 1×[0,1,2,3]
`vphsubd W:YMM, R:YMM, R:YMM`	3.00	8*	9×[6,7,8,9] + 4×[1,2] + 2×[0,1,3] + 3×[0,1,2,3]
`vphsubd W:YMM, R:YMM, ymmword ptr R:MEM(256)`	4.00	10+2*	13×[6,7,8,9] + 4×[1,2] + 2×[4,5] + 2×[0,1,3] + 7×[0,1,2,3]
`vphsubsw W:XMM, R:XMM, R:XMM`	2.01	4*	4×[6,7,8,9] + 2×[1,2] + 1×[0,3] + 1×[0,1,2,3]
`vphsubsw W:XMM, R:XMM, xmmword ptr R:MEM(128)`	2.00	4+1*	4×[6,7,8,9] + 2×[1,2] + 1×[0,3] + 1×[4,5] + 1×[0,1,2,3]
`vphsubsw W:YMM, R:YMM, R:YMM`	3.00	8*	9×[6,7,8,9] + 4×[1,2] + 2×[0,3] + 3×[0,1,2,3]
`vphsubsw W:YMM, R:YMM, ymmword ptr R:MEM(256)`	4.00	10+2*	13×[6,7,8,9] + 4×[1,2] + 2×[0,3] + 2×[4,5] + 7×[0,1,2,3]
`vphsubw W:XMM, R:XMM, R:XMM`	2.00	4*	4×[6,7,8,9] + 2×[1,2] + 1×[0,1,3] + 1×[0,1,2,3]
`vphsubw W:XMM, R:XMM, xmmword ptr R:MEM(128)`	2.00	4+1*	4×[6,7,8,9] + 2×[1,2] + 1×[4,5] + 1×[0,1,3] + 1×[0,1,2,3]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
vphsubw W:YMM, R:YMM, R:YMM	3.01	8*	9×[6,7,8,9] + 4×[1,2] + 2×[0,1,3] + 3×[0,1,2,3]
vphsubw W:YMM, R:YMM, ymmword ptr R:MEM(256)	4.00	10+2*	13×[6,7,8,9] + 4×[1,2] + 2×[4,5] + 2×[0,1,3] + 7×[0,1,2,3]
vpinsrb W:XMM, R:XMM, R:GPR:32, IMM(8)	1.25	2*	1×[2] + 1×[6,7,8,9] + 1×[1,2]
vpinsrb W:XMM, R:XMM, byte ptr R:MEM(8), IMM(8)	0.50	1+1	1×[1,2] + 1×[4,5]
vpinsrd W:XMM, R:XMM, R:GPR:32, IMM(8)	1.25	2*	1×[2] + 1×[6,7,8,9] + 1×[1,2]
vpinsrd W:XMM, R:XMM, dword ptr R:MEM(32), IMM(8)	0.50	1+1	1×[1,2] + 1×[4,5]
vpinsrq W:XMM, R:XMM, R:GPR:64, IMM(8)	1.25	2*	1×[2] + 1×[6,7,8,9] + 1×[1,2]
vpinsrq W:XMM, R:XMM, qword ptr R:MEM(64), IMM(8)	0.50	1+1	1×[1,2] + 1×[4,5]
vpinsrw W:XMM, R:XMM, R:GPR:32, IMM(8)	1.24	2*	1×[2] + 1×[6,7,8,9] + 1×[1,2]
vpinsrw W:XMM, R:XMM, word ptr R:MEM(16), IMM(8)	0.50	1+1	1×[1,2] + 1×[4,5]
vpmaskmovd W:XMM, R:XMM, xmmword ptr R:MEM(128)	6.02	20+1*	4×[0,1] + 1×[2] + 21×[6,7,8,9] + 2×[3] + 2×[0,3] + 2×[2,3] + 5×[4,5] + 11×[0,1,2,3]
vpmaskmovd W:YMM, R:YMM, ymmword ptr R:MEM(256)	10.04	36+2	
vpmaskmovd xmmword ptr W:MEM(128), R:XMM, R:XMM	6.00	19+1	
vpmaskmovd ymmword ptr W:MEM(256), R:YMM, R:YMM	12.04	42+2	
vpmaskmovq W:XMM, R:XMM, xmmword ptr R:MEM(128)	4.00	12+1*	1×[3] + 1×[2] + 2×[0,1] + 13×[6,7,8,9] + 1×[0,3] + 1×[2,3] + 3×[4,5] + 7×[0,1,2,3]
vpmaskmovq W:YMM, R:YMM, ymmword ptr R:MEM(256)	7.00	24+2*	2×[3] + 1×[2] + 4×[0,1] + 26×[6,7,8,9] + 2×[0,3] + 2×[2,3] + 5×[4,5] + 15×[0,1,2,3]
vpmaskmovq xmmword ptr W:MEM(128), R:XMM, R:XMM	4.02	10+1*	3×[2] + 13×[6,7,8,9] + 1×[1,2] + 2×[5] + 3×[4,5] + 3×[0,1,3] + 6×[0,1,2,3]
vpmaskmovq ymmword ptr W:MEM(256), R:YMM, R:YMM	6.03	18+2	
vpmaxsb W:XMM, R:XMM, R:XMM	0.33	1	1×[0,1,3]
vpmaxsb W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,3]
vpmaxsb W:YMM, R:YMM, R:YMM	0.67	2	2×[0,1,3]
vpmaxsb W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,3]
vpmaxsd W:XMM, R:XMM, R:XMM	0.33	1	1×[0,1,3]
vpmaxsd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,3]
vpmaxsd W:YMM, R:YMM, R:YMM	0.67	2	2×[0,1,3]
vpmaxsd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,3]
vpmaxsw W:XMM, R:XMM, R:XMM	0.33	1	1×[0,1,3]
vpmaxsw W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,3]
vpmaxsw W:YMM, R:YMM, R:YMM	0.67	2	2×[0,1,3]
vpmaxsw W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,3]
vpmaxub W:XMM, R:XMM, R:XMM	0.33	1	1×[0,1,3]
vpmaxub W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,3]
vpmaxub W:YMM, R:YMM, R:YMM	0.67	2	2×[0,1,3]
vpmaxub W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,3]
vpmaxud W:XMM, R:XMM, R:XMM	0.33	1	1×[0,1,3]
vpmaxud W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,3]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
vpmaxud W:YMM, R:YMM, R:YMM	0.67	2	2×[0,1,3]
vpmaxud W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,3]
vpmaxuw W:XMM, R:XMM, R:XMM	0.33	1	1×[0,1,3]
vpmaxuw W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,3]
vpmaxuw W:YMM, R:YMM, R:YMM	0.67	2	2×[0,1,3]
vpmaxuw W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,3]
vpminsb W:XMM, R:XMM, R:XMM	0.33	1	1×[0,1,3]
vpminsb W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,3]
vpminsb W:YMM, R:YMM, R:YMM	0.67	2	2×[0,1,3]
vpminsb W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,3]
vpminsd W:XMM, R:XMM, R:XMM	0.33	1	1×[0,1,3]
vpminsd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,3]
vpminsd W:YMM, R:YMM, R:YMM	0.67	2	2×[0,1,3]
vpminsd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,3]
vpminsw W:XMM, R:XMM, R:XMM	0.33	1	1×[0,1,3]
vpminsw W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,3]
vpminsw W:YMM, R:YMM, R:YMM	0.67	2	2×[0,1,3]
vpminsw W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,3]
vpminub W:XMM, R:XMM, R:XMM	0.33	1	1×[0,1,3]
vpminub W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,3]
vpminub W:YMM, R:YMM, R:YMM	0.67	2	2×[0,1,3]
vpminub W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,3]
vpminud W:XMM, R:XMM, R:XMM	0.33	1	1×[0,1,3]
vpminud W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,3]
vpminud W:YMM, R:YMM, R:YMM	0.67	2	2×[0,1,3]
vpminud W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,3]
vpminuw W:XMM, R:XMM, R:XMM	0.33	1	1×[0,1,3]
vpminuw W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,3]
vpminuw W:YMM, R:YMM, R:YMM	0.67	2	2×[0,1,3]
vpminuw W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,3]
vpmovmskb W:GPR:32, R:XMM	1.00	1	1×[2]
vpmovmskb W:GPR:32, R:YMM	1.00	1	1×[2]
vpmovsxbd W:XMM, R:XMM	0.50	1	1×[1,2]
vpmovsxbd W:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[1,2] + 1×[4,5]
vpmovsxbd W:YMM, R:XMM	2.00	3	
vpmovsxbd W:YMM, qword ptr R:MEM(64)	2.00	4+1*	4×[6,7,8,9] + 3×[1,2] + 1×[4,5] + 1×[0,1,2,3]
vpmovsxbq W:XMM, R:XMM	0.50	1	1×[1,2]
vpmovsxbq W:XMM, word ptr R:MEM(16)	0.50	1+1	1×[1,2] + 1×[4,5]
vpmovsxbq W:YMM, R:XMM	2.00	3	
vpmovsxbq W:YMM, dword ptr R:MEM(32)	2.00	4+1*	4×[6,7,8,9] + 3×[1,2] + 1×[4,5] + 1×[0,1,2,3]
vpmovsxbw W:XMM, R:XMM	0.50	1	1×[1,2]
vpmovsxbw W:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[1,2] + 1×[4,5]
vpmovsxbw W:YMM, R:XMM	2.00	3	

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
vpmovsxbw W:YMM, xmmword ptr R:MEM(128)	2.01	4+1*	4×[6,7,8,9] + 3×[1,2] + 1×[4,5] + 1×[0,1,2,3]
vpmovsxdq W:XMM, R:XMM	0.50	1	1×[1,2]
vpmovsxdq W:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[1,2] + 1×[4,5]
vpmovsxdq W:YMM, R:XMM	2.00	3	
vpmovsxdq W:YMM, xmmword ptr R:MEM(128)	2.00	4+1*	4×[6,7,8,9] + 3×[1,2] + 1×[4,5] + 1×[0,1,2,3]
vpmovsxwd W:XMM, R:XMM	0.50	1	1×[1,2]
vpmovsxwd W:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[1,2] + 1×[4,5]
vpmovsxwd W:YMM, R:XMM	2.00	3	
vpmovsxwd W:YMM, xmmword ptr R:MEM(128)	2.00	4+1*	4×[6,7,8,9] + 3×[1,2] + 1×[4,5] + 1×[0,1,2,3]
vpmovsxwq W:XMM, R:XMM	0.50	1	1×[1,2]
vpmovsxwq W:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[1,2] + 1×[4,5]
vpmovsxwq W:YMM, R:XMM	2.00	3	
vpmovsxwq W:YMM, qword ptr R:MEM(64)	2.00	4+1*	4×[6,7,8,9] + 3×[1,2] + 1×[4,5] + 1×[0,1,2,3]
vpmovzxbd W:XMM, R:XMM	0.50	1	1×[1,2]
vpmovzxbd W:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[1,2] + 1×[4,5]
vpmovzxbd W:YMM, R:XMM	2.00	3	
vpmovzxbd W:YMM, qword ptr R:MEM(64)	2.00	4+1*	4×[6,7,8,9] + 3×[1,2] + 1×[4,5] + 1×[0,1,2,3]
vpmovzxbq W:XMM, R:XMM	0.50	1	1×[1,2]
vpmovzxbq W:XMM, word ptr R:MEM(16)	0.50	1+1	1×[1,2] + 1×[4,5]
vpmovzxbq W:YMM, R:XMM	2.00	3	
vpmovzxbq W:YMM, dword ptr R:MEM(32)	2.00	4+1*	4×[6,7,8,9] + 3×[1,2] + 1×[4,5] + 1×[0,1,2,3]
vpmovzxbw W:XMM, R:XMM	0.50	1	1×[1,2]
vpmovzxbw W:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[1,2] + 1×[4,5]
vpmovzxbw W:YMM, R:XMM	2.00	3	
vpmovzxbw W:YMM, xmmword ptr R:MEM(128)	2.00	4+1*	4×[6,7,8,9] + 3×[1,2] + 1×[4,5] + 1×[0,1,2,3]
vpmovzxdq W:XMM, R:XMM	0.50	1	1×[1,2]
vpmovzxdq W:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[1,2] + 1×[4,5]
vpmovzxdq W:YMM, R:XMM	2.00	3	
vpmovzxdq W:YMM, xmmword ptr R:MEM(128)	2.00	4+1*	4×[6,7,8,9] + 3×[1,2] + 1×[4,5] + 1×[0,1,2,3]
vpmovzxwd W:XMM, R:XMM	0.50	1	1×[1,2]
vpmovzxwd W:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[1,2] + 1×[4,5]
vpmovzxwd W:YMM, R:XMM	2.00	3	
vpmovzxwd W:YMM, xmmword ptr R:MEM(128)	2.00	4+1*	4×[6,7,8,9] + 3×[1,2] + 1×[4,5] + 1×[0,1,2,3]
vpmovzxwq W:XMM, R:XMM	0.50	1	1×[1,2]
vpmovzxwq W:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[1,2] + 1×[4,5]
vpmovzxwq W:YMM, R:XMM	2.00	3	
vpmovzxwq W:YMM, qword ptr R:MEM(64)	2.00	4+1*	4×[6,7,8,9] + 3×[1,2] + 1×[4,5] + 1×[0,1,2,3]
vpmulld W:XMM, R:XMM, xmmword ptr R:MEM(128)	2.00	1+1	
vpmulld W:YMM, R:YMM, ymmword ptr R:MEM(256)	4.00	2+2	

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
vpor W:XMM, R:XMM, R:XMM	0.25	1	1×[0,1,2,3]
vpor W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vpor W:YMM, R:YMM, R:YMM	0.50	2	2×[0,1,2,3]
vpor W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,2,3]
vpshufb W:XMM, R:XMM, R:XMM	0.50	1	1×[1,2]
vpshufb W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[1,2] + 1×[4,5]
vpshufb W:YMM, R:YMM, R:YMM	1.00	2	2×[1,2]
vpshufb W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[1,2] + 2×[4,5]
vpshufd W:XMM, R:XMM, IMM(8)	0.50	1	1×[1,2]
vpshufd W:XMM, xmmword ptr R:MEM(128), IMM(8)	0.50	1+1	1×[1,2] + 1×[4,5]
vpshufd W:YMM, R:YMM, IMM(8)	1.00	2	2×[1,2]
vpshufd W:YMM, ymmword ptr R:MEM(256), IMM(8)	1.00	2+2	2×[1,2] + 2×[4,5]
vpshufhw W:XMM, R:XMM, IMM(8)	0.50	1	1×[1,2]
vpshufhw W:XMM, xmmword ptr R:MEM(128), IMM(8)	0.50	1+1	1×[1,2] + 1×[4,5]
vpshufhw W:YMM, R:YMM, IMM(8)	1.00	2	2×[1,2]
vpshufhw W:YMM, ymmword ptr R:MEM(256), IMM(8)	1.00	2+2	2×[1,2] + 2×[4,5]
vpshuflw W:XMM, R:XMM, IMM(8)	0.50	1	1×[1,2]
vpshuflw W:XMM, xmmword ptr R:MEM(128), IMM(8)	0.50	1+1	1×[1,2] + 1×[4,5]
vpshuflw W:YMM, R:YMM, IMM(8)	1.00	2	2×[1,2]
vpshuflw W:YMM, ymmword ptr R:MEM(256), IMM(8)	1.00	2+2	2×[1,2] + 2×[4,5]
vpsignb W:XMM, R:XMM, R:XMM	0.50	1	1×[0,3]
vpsignb W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,3] + 1×[4,5]
vpsignb W:YMM, R:YMM, R:YMM	1.00	2	2×[0,3]
vpsignb W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,3] + 2×[4,5]
vpsignd W:XMM, R:XMM, R:XMM	0.50	1	1×[0,3]
vpsignd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,3] + 1×[4,5]
vpsignd W:YMM, R:YMM, R:YMM	1.00	2	2×[0,3]
vpsignd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,3] + 2×[4,5]
vpsignw W:XMM, R:XMM, R:XMM	0.50	1	1×[0,3]
vpsignw W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,3] + 1×[4,5]
vpsignw W:YMM, R:YMM, R:YMM	1.00	2	2×[0,3]
vpsignw W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,3] + 2×[4,5]
vpslld W:XMM, R:XMM, IMM(8)	1.00	1	1×[2]
vpslld W:XMM, R:XMM, R:XMM	1.00	1	1×[2]
vpslld W:XMM, R:XMM, xmmword ptr R:MEM(128)	1.00	1+1	
vpslld W:YMM, R:YMM, IMM(8)	2.00	2	
vpslld W:YMM, R:YMM, R:XMM	2.00	2	
vpslld W:YMM, R:YMM, xmmword ptr R:MEM(128)	2.00	3+1	
vpslldq W:XMM, R:XMM, IMM(8)	0.50	1	1×[1,2]
vpslldq W:YMM, R:YMM, IMM(8)	1.00	2	2×[1,2]
vpsllq W:XMM, R:XMM, IMM(8)	1.00	1	1×[2]
vpsllq W:XMM, R:XMM, R:XMM	1.00	1	1×[2]
vpsllq W:XMM, R:XMM, xmmword ptr R:MEM(128)	1.00	1+1	
vpsllq W:YMM, R:YMM, IMM(8)	2.00	2	
vpsllq W:YMM, R:YMM, R:XMM	2.00	2	
vpsllq W:YMM, R:YMM, xmmword ptr R:MEM(128)	2.00	3+1	

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
vpsllvd W:XMM, R:XMM, xmmword ptr R:MEM(128)	2.00	1+1	
vpsllvd W:YMM, R:YMM, ymmword ptr R:MEM(256)	4.00	2+2	
vpsllvq W:XMM, R:XMM, xmmword ptr R:MEM(128)	2.00	1+1	
vpsllvq W:YMM, R:YMM, ymmword ptr R:MEM(256)	4.00	2+2	
vpsllw W:XMM, R:XMM, IMM(8)	1.00	1	1×[2]
vpsllw W:XMM, R:XMM, R:XMM	1.00	1	1×[2]
vpsllw W:XMM, R:XMM, xmmword ptr R:MEM(128)	1.00	1+1	
vpsllw W:YMM, R:YMM, IMM(8)	2.00	2	
vpsllw W:YMM, R:YMM, R:XMM	2.00	2	
vpsllw W:YMM, R:YMM, xmmword ptr R:MEM(128)	2.00	3+1	
vpsrad W:XMM, R:XMM, IMM(8)	1.00	1	1×[2]
vpsrad W:XMM, R:XMM, R:XMM	1.00	1	1×[2]
vpsrad W:XMM, R:XMM, xmmword ptr R:MEM(128)	1.00	1+1	
vpsrad W:YMM, R:YMM, IMM(8)	2.00	2	
vpsrad W:YMM, R:YMM, R:XMM	2.00	2	
vpsrad W:YMM, R:YMM, xmmword ptr R:MEM(128)	2.00	3+1	
vpsravd W:XMM, R:XMM, xmmword ptr R:MEM(128)	2.00	1+1	
vpsravd W:YMM, R:YMM, ymmword ptr R:MEM(256)	4.00	2+2	
vpsraw W:XMM, R:XMM, IMM(8)	1.00	1	1×[2]
vpsraw W:XMM, R:XMM, R:XMM	1.00	1	1×[2]
vpsraw W:XMM, R:XMM, xmmword ptr R:MEM(128)	1.00	1+1	
vpsraw W:YMM, R:YMM, IMM(8)	2.00	2	
vpsraw W:YMM, R:YMM, R:XMM	2.00	2	
vpsraw W:YMM, R:YMM, xmmword ptr R:MEM(128)	2.00	3+1	
vpsrld W:XMM, R:XMM, IMM(8)	1.00	1	1×[2]
vpsrld W:XMM, R:XMM, R:XMM	1.00	1	1×[2]
vpsrld W:XMM, R:XMM, xmmword ptr R:MEM(128)	1.00	1+1	
vpsrld W:YMM, R:YMM, IMM(8)	2.00	2	
vpsrld W:YMM, R:YMM, R:XMM	2.00	2	
vpsrld W:YMM, R:YMM, xmmword ptr R:MEM(128)	2.00	3+1	
vpsrldq W:XMM, R:XMM, IMM(8)	0.50	1	1×[1,2]
vpsrldq W:YMM, R:YMM, IMM(8)	1.00	2	2×[1,2]
vpsrlq W:XMM, R:XMM, IMM(8)	1.00	1	1×[2]
vpsrlq W:XMM, R:XMM, R:XMM	1.00	1	1×[2]
vpsrlq W:XMM, R:XMM, xmmword ptr R:MEM(128)	1.00	1+1	
vpsrlq W:YMM, R:YMM, IMM(8)	2.00	2	
vpsrlq W:YMM, R:YMM, R:XMM	2.00	2	
vpsrlq W:YMM, R:YMM, xmmword ptr R:MEM(128)	2.00	3+1	
vpsrlvd W:XMM, R:XMM, xmmword ptr R:MEM(128)	2.00	1+1	
vpsrlvd W:YMM, R:YMM, ymmword ptr R:MEM(256)	4.00	2+2	
vpsrlvq W:XMM, R:XMM, xmmword ptr R:MEM(128)	2.00	1+1	
vpsrlvq W:YMM, R:YMM, ymmword ptr R:MEM(256)	4.00	2+2	
vpsrlw W:XMM, R:XMM, IMM(8)	1.00	1	1×[2]
vpsrlw W:XMM, R:XMM, R:XMM	1.00	1	1×[2]
vpsrlw W:XMM, R:XMM, xmmword ptr R:MEM(128)	1.00	1+1	
vpsrlw W:YMM, R:YMM, IMM(8)	2.00	2	

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
vpsrlw W:YMM, R:YMM, R:XMM	2.00	2	
vpsrlw W:YMM, R:YMM, xmmword ptr R:MEM(128)	2.00	3+1	
vpsubb W:XMM, R:XMM, R:XMM	0.33	1	1×[0,1,3]
vpsubb W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,3]
vpsubb W:YMM, R:YMM, R:YMM	0.67	2	2×[0,1,3]
vpsubb W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,3]
vpsubd W:XMM, R:XMM, R:XMM	0.33	1	1×[0,1,3]
vpsubd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,3]
vpsubd W:YMM, R:YMM, R:YMM	0.67	2	2×[0,1,3]
vpsubd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,3]
vpsubq W:XMM, R:XMM, R:XMM	0.33	1	1×[0,1,3]
vpsubq W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,3]
vpsubq W:YMM, R:YMM, R:YMM	0.67	2	2×[0,1,3]
vpsubq W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,3]
vpsubsb W:XMM, R:XMM, R:XMM	0.50	1	1×[0,3]
vpsubsb W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,3] + 1×[4,5]
vpsubsb W:YMM, R:YMM, R:YMM	1.00	2	2×[0,3]
vpsubsb W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,3] + 2×[4,5]
vpsubsw W:XMM, R:XMM, R:XMM	0.50	1	1×[0,3]
vpsubsw W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,3] + 1×[4,5]
vpsubsw W:YMM, R:YMM, R:YMM	1.00	2	2×[0,3]
vpsubsw W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,3] + 2×[4,5]
vpsubusb W:XMM, R:XMM, R:XMM	0.50	1	1×[0,3]
vpsubusb W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,3] + 1×[4,5]
vpsubusb W:YMM, R:YMM, R:YMM	1.00	2	2×[0,3]
vpsubusb W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,3] + 2×[4,5]
vpsubusw W:XMM, R:XMM, R:XMM	0.50	1	1×[0,3]
vpsubusw W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[0,3] + 1×[4,5]
vpsubusw W:YMM, R:YMM, R:YMM	1.00	2	2×[0,3]
vpsubusw W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[0,3] + 2×[4,5]
vpsubw W:XMM, R:XMM, R:XMM	0.33	1	1×[0,1,3]
vpsubw W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,3]
vpsubw W:YMM, R:YMM, R:YMM	0.67	2	2×[0,1,3]
vpsubw W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,3]
vptest R:XMM, R:XMM	1.00	1	1×[2]
vptest R:XMM, xmmword ptr R:MEM(128)	1.00	2+1*	1×[2] + 2×[6,7,8,9] + 1×[1,2] + 1×[4,5]
vptest R:YMM, R:YMM	2.00	3	
vptest R:YMM, ymmword ptr R:MEM(256)	3.01	5+2*	1×[2] + 9×[6,7,8,9] + 2×[1,2] + 3×[0,1,3] + 2×[4,5] + 4×[0,1,2,3]
vpunpckhbw W:XMM, R:XMM, R:XMM	0.50	1	1×[1,2]
vpunpckhbw W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[1,2] + 1×[4,5]
vpunpckhbw W:YMM, R:YMM, R:YMM	1.00	2	2×[1,2]
vpunpckhbw W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[1,2] + 2×[4,5]
vpunpckhdq W:XMM, R:XMM, R:XMM	0.50	1	1×[1,2]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
vpunpckhdq W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[1,2] + 1×[4,5]
vpunpckhdq W:YMM, R:YMM, R:YMM	1.00	2	2×[1,2]
vpunpckhdq W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[1,2] + 2×[4,5]
vpunpckhqdq W:XMM, R:XMM, R:XMM	0.50	1	1×[1,2]
vpunpckhqdq W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[1,2] + 1×[4,5]
vpunpckhqdq W:YMM, R:YMM, R:YMM	1.00	2	2×[1,2]
vpunpckhqdq W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[1,2] + 2×[4,5]
vpunpckhwd W:XMM, R:XMM, R:XMM	0.50	1	1×[1,2]
vpunpckhwd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[1,2] + 1×[4,5]
vpunpckhwd W:YMM, R:YMM, R:YMM	1.00	2	2×[1,2]
vpunpckhwd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[1,2] + 2×[4,5]
vpunpcklbw W:XMM, R:XMM, R:XMM	0.50	1	1×[1,2]
vpunpcklbw W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[1,2] + 1×[4,5]
vpunpcklbw W:YMM, R:YMM, R:YMM	1.00	2	2×[1,2]
vpunpcklbw W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[1,2] + 2×[4,5]
vpunpckldq W:XMM, R:XMM, R:XMM	0.50	1	1×[1,2]
vpunpckldq W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[1,2] + 1×[4,5]
vpunpckldq W:YMM, R:YMM, R:YMM	1.00	2	2×[1,2]
vpunpckldq W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[1,2] + 2×[4,5]
vpunpcklqdq W:XMM, R:XMM, R:XMM	0.50	1	1×[1,2]
vpunpcklqdq W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[1,2] + 1×[4,5]
vpunpcklqdq W:YMM, R:YMM, R:YMM	1.00	2	2×[1,2]
vpunpcklqdq W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[1,2] + 2×[4,5]
vpunpcklwd W:XMM, R:XMM, R:XMM	0.50	1	1×[1,2]
vpunpcklwd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[1,2] + 1×[4,5]
vpunpcklwd W:YMM, R:YMM, R:YMM	1.00	2	2×[1,2]
vpunpcklwd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[1,2] + 2×[4,5]
vpxor W:XMM, R:XMM, R:XMM	0.25	1	1×[0,1,2,3]
vpxor W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vpxor W:YMM, R:YMM, R:YMM	0.50	2	2×[0,1,2,3]
vpxor W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,2,3]
vroundpd W:XMM, R:XMM, IMM(8)	1.00	1	1×[3]
vroundpd W:XMM, xmmword ptr R:MEM(128), IMM(8)	1.00	1+1	1×[3] + 1×[4,5]
vroundpd W:YMM, R:YMM, IMM(8)	2.00	2	2×[3]
vroundpd W:YMM, ymmword ptr R:MEM(256), IMM(8)	2.00	2+2	2×[3] + 2×[4,5]
vroundps W:XMM, R:XMM, IMM(8)	1.00	1	1×[3]
vroundps W:XMM, xmmword ptr R:MEM(128), IMM(8)	1.00	1+1	1×[3] + 1×[4,5]
vroundps W:YMM, R:YMM, IMM(8)	2.00	2	2×[3]
vroundps W:YMM, ymmword ptr R:MEM(256), IMM(8)	2.00	2+2	2×[3] + 2×[4,5]
vroundsd W:XMM, R:XMM, R:XMM, IMM(8)	1.00	1	1×[3]
vroundsd W:XMM, R:XMM, qword ptr R:MEM(64), IMM(8)	1.00	1+1	1×[3] + 1×[4,5]
vroundss W:XMM, R:XMM, R:XMM, IMM(8)	1.00	1	1×[3]
vroundss W:XMM, R:XMM, dword ptr R:MEM(32), IMM(8)	1.00	1+1	1×[3] + 1×[4,5]
vshufpd W:XMM, R:XMM, R:XMM, IMM(8)	0.50	1	1×[1,2]
vshufpd W:XMM, R:XMM, xmmword ptr R:MEM(128), IMM(8)	0.50	1+1	1×[1,2] + 1×[4,5]
vshufpd W:YMM, R:YMM, R:YMM, IMM(8)	1.00	2	2×[1,2]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
vshufpd W:YMM, R:YMM, ymmword ptr R:MEM(256), IMM(8)	1.00	2+2	2×[1,2] + 2×[4,5]
vshufps W:XMM, R:XMM, R:XMM, IMM(8)	0.50	1	1×[1,2]
vshufps W:XMM, R:XMM, xmmword ptr R:MEM(128), IMM(8)	0.50	1+1	1×[1,2] + 1×[4,5]
vshufps W:YMM, R:YMM, R:YMM, IMM(8)	1.00	2	2×[1,2]
vshufps W:YMM, R:YMM, ymmword ptr R:MEM(256), IMM(8)	1.00	2+2	2×[1,2] + 2×[4,5]
vsubpd W:XMM, R:XMM, R:XMM	0.50	1	1×[2,3]
vsubpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[2,3] + 1×[4,5]
vsubpd W:YMM, R:YMM, R:YMM	1.00	2	2×[2,3]
vsubpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[2,3] + 2×[4,5]
vsubps W:XMM, R:XMM, R:XMM	0.50	1	1×[2,3]
vsubps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[2,3] + 1×[4,5]
vsubps W:YMM, R:YMM, R:YMM	1.00	2	2×[2,3]
vsubps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2*	2×[2,3] + 2×[4,5] + 1×[0,1,2,3]
vsubsd W:XMM, R:XMM, R:XMM	0.50	1	1×[2,3]
vsubsd W:XMM, R:XMM, qword ptr R:MEM(64)	0.50	1+1	1×[2,3] + 1×[4,5]
vsubss W:XMM, R:XMM, R:XMM	0.50	1	1×[2,3]
vsubss W:XMM, R:XMM, dword ptr R:MEM(32)	0.50	1+1	1×[2,3] + 1×[4,5]
vtestpd R:XMM, R:XMM	1.00	1	1×[2]
vtestpd R:XMM, xmmword ptr R:MEM(128)	1.00	2+1*	1×[2] + 2×[6,7,8,9] + 1×[1,2] + 1×[4,5]
vtestpd R:YMM, R:YMM	2.00	3	
vtestpd R:YMM, ymmword ptr R:MEM(256)	3.01	5+2*	1×[2] + 9×[6,7,8,9] + 2×[1,2] + 3×[0,1,3] + 2×[4,5] + 3×[0,1,2,3]
vtestps R:XMM, R:XMM	1.00	1	1×[2]
vtestps R:XMM, xmmword ptr R:MEM(128)	1.00	2+1*	1×[2] + 2×[6,7,8,9] + 1×[1,2] + 1×[4,5]
vtestps R:YMM, R:YMM	2.00	3	
vtestps R:YMM, ymmword ptr R:MEM(256)	3.00	5+2*	1×[2] + 9×[6,7,8,9] + 2×[1,2] + 2×[4,5] + 3×[0,1,3] + 4×[0,1,2,3]
vucomisd R:XMM, R:XMM	1.00	2*	1×[2] + 1×[0,1] + 2×[6,7,8,9]
vucomisd R:XMM, qword ptr R:MEM(64)	1.00	2+1*	1×[2] + 1×[0,1] + 2×[6,7,8,9] + 1×[4,5]
vucomiss R:XMM, R:XMM	1.00	2*	1×[2] + 1×[0,1] + 2×[6,7,8,9]
vucomiss R:XMM, dword ptr R:MEM(32)	1.00	2+1*	1×[2] + 1×[0,1] + 2×[6,7,8,9] + 1×[4,5]
vunpckhpd W:XMM, R:XMM, R:XMM	0.50	1	1×[1,2]
vunpckhpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[1,2] + 1×[4,5]
vunpckhpd W:YMM, R:YMM, R:YMM	1.00	2	2×[1,2]
vunpckhpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[1,2] + 2×[4,5]
vunpckhps W:XMM, R:XMM, R:XMM	0.50	1	1×[1,2]
vunpckhps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[1,2] + 1×[4,5]
vunpckhps W:YMM, R:YMM, R:YMM	1.00	2	2×[1,2]
vunpckhps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[1,2] + 2×[4,5]
vunpcklpd W:XMM, R:XMM, R:XMM	0.50	1	1×[1,2]
vunpcklpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[1,2] + 1×[4,5]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
vunpcklpd W:YMM, R:YMM, R:YMM	1.00	2	2×[1,2]
vunpcklpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[1,2] + 2×[4,5]
vunpcklps W:XMM, R:XMM, R:XMM	0.50	1	1×[1,2]
vunpcklps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[1,2] + 1×[4,5]
vunpcklps W:YMM, R:YMM, R:YMM	1.00	2	2×[1,2]
vunpcklps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[1,2] + 2×[4,5]
vxorpd W:XMM, R:XMM, R:XMM	0.25	1	1×[0,1,2,3]
vxorpd W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vxorpd W:YMM, R:YMM, R:YMM	0.50	2	2×[0,1,2,3]
vxorpd W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,2,3]
vxorps W:XMM, R:XMM, R:XMM	0.25	1	1×[0,1,2,3]
vxorps W:XMM, R:XMM, xmmword ptr R:MEM(128)	0.50	1+1	1×[4,5] + 1×[0,1,2,3]
vxorps W:YMM, R:YMM, R:YMM	0.50	2	2×[0,1,2,3]
vxorps W:YMM, R:YMM, ymmword ptr R:MEM(256)	1.00	2+2	2×[4,5] + 2×[0,1,2,3]
vzeroall	11.00	33*	38×[6,7,8,9] + 2×[4,5] + 3×[0,1,3] + 35×[0,1,2,3]
vzeroupper	6.00	17	
xadd RW:GPR:16, RW:GPR:16	0.50	2	2×[6,7,8,9]
xadd RW:GPR:32, RW:GPR:32	0.34	2*	1×[6,7,8,9]
xadd RW:GPR:64, RW:GPR:64	0.34	2*	1×[6,7,8,9]
xadd RW:GPR:8, RW:GPR:8	0.50	2	2×[6,7,8,9]
xadd byte ptr RW:MEM(8), RW:GPR:8	2.00	4+1*	4×[6,7,8,9] + 1×[5] + 1×[4,5] + 4×[0,1,2,3]
xadd dword ptr RW:MEM(32), RW:GPR:32	2.00	4+1*	4×[6,7,8,9] + 1×[5] + 4×[0,1,2,3]
xadd qword ptr RW:MEM(64), RW:GPR:64	2.00	4+1*	4×[6,7,8,9] + 1×[5] + 4×[0,1,2,3]
xadd word ptr RW:MEM(16), RW:GPR:16	2.00	4+1	
xchg RW:GPR:16, RW:GPR:16	0.50	2	2×[6,7,8,9]
xchg RW:GPR:32, RW:GPR:32	0.34	2	
xchg RW:GPR:64, RW:GPR:64	0.33	2	
xchg RW:GPR:8, RW:GPR:8	0.50	2	2×[6,7,8,9]
xor RW:GPR:16, 0x0	0.25	1	1×[6,7,8,9]
xor RW:GPR:16, IMM(16)	0.25	1	1×[6,7,8,9]
xor RW:GPR:16, IMM(8)	0.25	1	1×[6,7,8,9]
xor RW:GPR:16, R:GPR:16	0.25	1	1×[6,7,8,9]
xor RW:GPR:16, word ptr R:MEM(16)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
xor RW:GPR:32, 0x0	0.25	1	1×[6,7,8,9]
xor RW:GPR:32, IMM(32)	0.25	1	1×[6,7,8,9]
xor RW:GPR:32, IMM(8)	0.25	1	1×[6,7,8,9]
xor RW:GPR:32, R:GPR:32	0.25	1	1×[6,7,8,9]
xor RW:GPR:32, dword ptr R:MEM(32)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
xor RW:GPR:64, 0x0	0.25	1	1×[6,7,8,9]
xor RW:GPR:64, IMM(32)	0.25	1	1×[6,7,8,9]
xor RW:GPR:64, IMM(8)	0.25	1	1×[6,7,8,9]
xor RW:GPR:64, R:GPR:64	0.25	1	1×[6,7,8,9]
xor RW:GPR:64, qword ptr R:MEM(64)	0.50	1+1	1×[6,7,8,9] + 1×[4,5]

Instruction Scheme	tp^{-1}	$\#\mu$ops	Port Usage
`xor RW:GPR:8, R:GPR:8`	0.25	1	1×[6,7,8,9]
`xor RW:GPR:8, byte ptr R:MEM(8)`	0.50	1+1	1×[6,7,8,9] + 1×[4,5]
`xor byte ptr RW:MEM(8), 0x0`	1.36	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`xor byte ptr RW:MEM(8), IMM(8)`	1.36	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`xor byte ptr RW:MEM(8), R:GPR:8`	1.38	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`xor dword ptr RW:MEM(32), 0x0`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`xor dword ptr RW:MEM(32), IMM(32)`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`xor dword ptr RW:MEM(32), IMM(8)`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`xor dword ptr RW:MEM(32), R:GPR:32`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`xor qword ptr RW:MEM(64), 0x0`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`xor qword ptr RW:MEM(64), IMM(32)`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`xor qword ptr RW:MEM(64), IMM(8)`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`xor qword ptr RW:MEM(64), R:GPR:64`	1.00	1+1	1×[6,7,8,9] + 1×[5]
`xor word ptr RW:MEM(16), 0x0`	1.36	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`xor word ptr RW:MEM(16), IMM(16)`	1.36	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`xor word ptr RW:MEM(16), IMM(8)`	1.37	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]
`xor word ptr RW:MEM(16), R:GPR:16`	1.38	1+1*	1×[6,7,8,9] + 1×[5] + 1×[4,5]