	CaLinx2+	ML505/XUPv5	DE2-70 (with TRDB-LTM, TRDB-D5M)	DE3 (with MTDB, THDB-ADA)
FPGA	Xilinx™ VirtexE XCV2000E	Xilinx™ Virtex5 XC5VLX50T (110)	Altera™ Cyclone II EP2C70	Altera™ Stratix III EP3SL150 (340)
LUTs/LEs	43K (4LUTs)	29K (70K) 6LUTs	68K LEs (4LUTs)	57K (135K) (ALM / 8LUTs)
RAM	655Kb (Block) 614Kb (Distributed)	2Mb	1Mb	5Mb (16Mb)
Working Freq.	27Mhz	500Mhz (Tested and Proven)	250Mhz	500Mhz
On Board Clocks	1 × 27MHz 1 × 25MHz	1 × 100Mhz, 1 × 33MHz, 1 × 27Mhz 1 × 200Mhz (differential) Other Frequencies by DLL	3 × 50MHz 1 × 28.63Mhz Other Frequencies by PLL	2 × 50MHz 1 × 24Mhz Other Frequencies by PLL
Memory				
DRAM	2 × 256MB SDRAM	DDR2 SO-DIMM (256MB Included)	2 × 32MB SDRAM	DDR2 SO-DIMM (2GB Included)
SRAM	None	1MB	2MB	None
Flash	None	32MB	8MB	None
Removable (Flash)	CompactFlash (SystemACE)	CompactFlash (SystemACE)	SD Card	2 × SD Card
User Level I/O				
Slide Switches	None	None	18	4
DIP Switches	16	8	None	8 (Tiny)
Push Buttons	8	5 + Dedicated Reset	4	4 + Dedicated Reset
Rotary Encoder	None	1	None	None
7-Segment Display	8	None	8	2
LEDs	8 × Red	15 × Green	18 × Red 9 × Green	8 × RGB
LCD	16 × 2 Character Matrix	16 × 2 Character Matrix	16 × 2 Character Matrix	None - possible connection to DE2
LCD Screen	None	None	4.3” LCD Touch Panel (800×480 Res)	4.3” LCD Touch Panel (800×480 Res)
Camera	None	None	5 Megapixel (Up to 15 fps)	5 Megapixel (Up to 15 fps) Daughter Card
Ethernet	4 × 10/100 (PHY Interface)	1 × 10/100/1000 (PHY Interface)	1 × 10/100 (MAC Interface)	1 × 10/100 (MAC Interface)
High-Speed Network	None	SMA, SATA, SFP	None	1 x HDMI In and Out
USB	1 (PHY)	1 × Host 1 × Device	1 × Host 1 × Device	2/3 × Host 1/0 × Device (Chosen by jumper)
RS232	2	1	1	1
PS/2	1	2	1	1
ADC / DAC	1 × ADC	None	2 × High-Speed ADC 2 × High-Speed DAC	2 × High-Speed ADC 2 × High-Speed DAC
Video In	1 × TV In (NTSC)	1 × VGA In (8-bit)	2 × TV In (NTSC)	1 × TV In (NTSC)
Video Out	1 × TV Out (NTSC) 1 × S-Video Out (NTSC)	1 × DVI Out	1 × VGA Out (10 bit)	1 × VGA Out (10 bit) 1 x CameraLink/HDMI In and Out Daughter Card
Audio In	1 × Mic 1 × Stereo	1 × Mic 1 × Line In (Stereo)	1 × Mic 1 × Line In (Stereo)	1 × Mic 1 × Line In (Stereo)
Audio Out	1 × Headphones 1 × Stereo	1 × Headphones 1 × Line Out (Stereo)	1 x Line Out (Stereo)	1 x Line Out (Stereo)
GPIO	120-pin	1 × 32 single-ended 1 × 16 high-speed differential pair	2 × 40-pin GPIO-0: TRDB-D5M GPIO-1: TRDB-LTM	4 × 120-pin high-speed A: 2 × 40-pin OR 1 × 120-pin high-speed B: DDR2 SO-DIMM C: MTDB (Touch Screen) D: THDB-ADA (A2D & D2A Board)
Other I/O	ZigBee, 2 × N64 Controller	PCIe 1×, Buzzer, Xilinx XC95144XL CPLD	IrDA	PCI-X, PCIe, Temp. Sensor
Synopsis	-Dated I/O, Slower FPGA -Breaking down, No more being built	-Want more rugged/durable design (Plexiglas enclosure) -Want Heat sink/Fan for FPGA -Want more GPIO (i.e. Test Headers, RGB LEDs, DIP switches, 7-seg. Display, and radio (Bluetooth or ZigBee)) reference designs provided by Xilinx	+Tested, proven durable design +Commitment from Altera for future upgrades of FPGA/IC +Designed for Education +DE1 purchased/Donated for home study -Want GPIO radio (Bluetooth or ZigBee) Other schools released solutions	Graphic interface for generating top-level code +Significant amount of GPIO for future expansion +GPIO can be high-speed differential pairs -Want GPIO radio (Bluetooth or ZigBee)