SYA1232

Datasheet LCOS Controller

Features

- Controls up to FHD (1920x1080) resolution panels
- Integrated frame buffer
- 24-bit RGB or YCbCr (444)
- Compatible with SYL2281, 1080p, .37” and SYL2282, 1080p, .55” display panels
- Supports color field rates up to 9 per frame
- I2C Interface
- Optional direct SPI Flash interface
- Keystone correction

Overview

Syndiant’s **SYA1232** LCOS controller is a high performance, low power, highly integrated display driver that converts video signals into an efficient format used by Syndiant’s LCOS display panels.

Features include video formatting, gamma control, color field sequential panel control, integrated video frame buffer, illumination synchronization and modulation, keystone correction and others. The controller’s high level of programmability and interface flexibility allows integration into a wide array of projection systems.

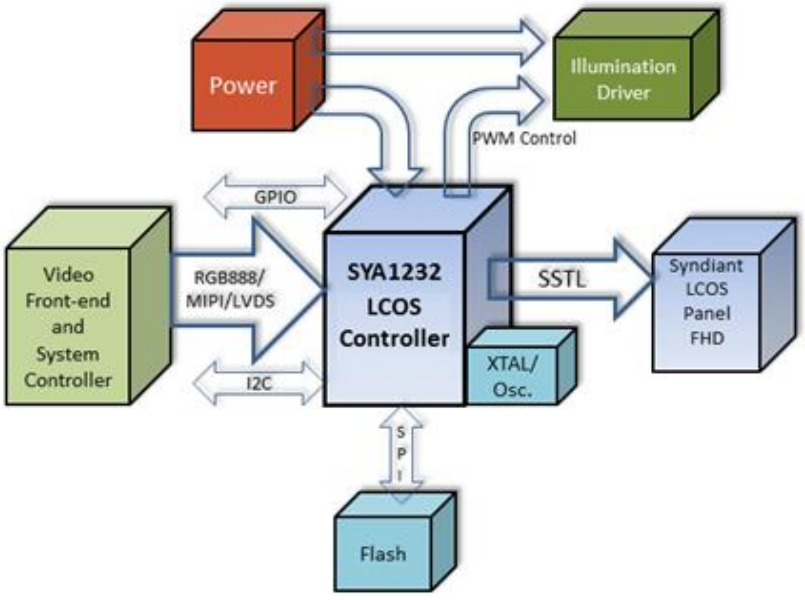


Figure 1: System Block Diagram

Revision History:

Syndiant Document #9D-2019-10

Date	Revision	Description
July 2018	V1.0	Initial Release

Table of Contents:

1 System Level Functionality

The SYA1232 LCOS controller is a high performance, low power, highly integrated system-on-chip that converts video signals into a proprietary format used by Syndiant LCOS display panels. It is designed to interface directly with peripheral devices needed in a typical projection system and supports either an RGB or YCbCr digital video input. Video input via MIPI and LVDS interface is also supported. The SYA1232 includes a display controller, power management and video input processing circuitries, SPI and I2C, and illumination control circuitry. It also integrates a frame buffer and configuration memory to reduce pin count and board space.

The SYA1232 is supported by software tools, application specific firmware, utilities and libraries, etc. that enhance the projected display, facilitate hardware and software development, minimize engineering development efforts and shorten the product's time to market.

This document gives details of the SYA1232 controller architecture, outlines supported features, gives a brief description of the functionality of each major module, details the operating modes, defines the control registers, and describes the overall usage to provide technical information suitable for design, software, and test engineers.

1.1 System Architecture

Figure 1 (page 1) illustrates a typical system using the SYA1232 LCOS Controller.

Figure **2** below shows the major SYA1232 LCOS Controller internal blocks. The following sections describe the features available in the SYA1232.

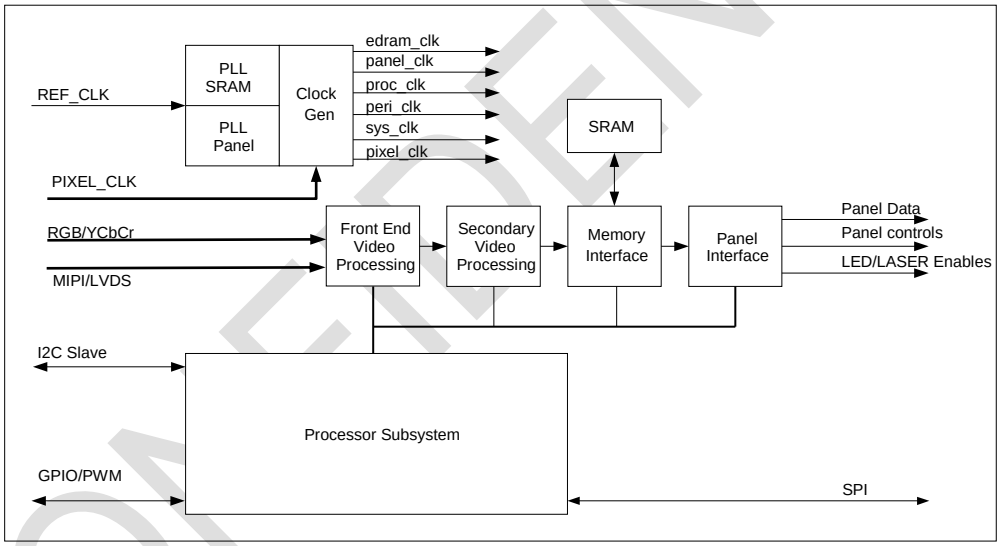


Figure 2: SYA1232 Controller block Diagram

Notes:

1. The processor subsystem includes a processor, memory and peripherals suitable for controlling the hardware within the LCOS Controller and is not intended to be user programmable.

1.2 Video Input

The SYA1232 controller supports 720p and 1080p input resolutions and auto-detects for both activity and frequency. The built-in scaler is flexible enough to either adjust the input to fill the display or create a sub-image based on user settings. Basic keystone correction can also be applied.

- 720p (1280 x 720)
- FHD (1920 x 1080)

The input timing is flexible and supports frame rates from 10 Hz to 75 Hz with a maximum pixel clock rate of 148.5 MHz. In addition to standard 24-bit RGB (RGB888) data, the video input can also support parallel YCbCr444. Color space conversion and basic deinterlacing are available to support these modes. Other video processing features including brightness, contrast and saturation controls are available as well as gamma correction. This allows the system designer the option of using the red, green and blue illuminators together to create a white color field in addition to the primary colors resulting in enhanced brightness and efficiency.

1.3 Panel Interface

The video output interface to the LCOS panel is flexible enough to enable power/performance trade-offs when using different display modes. The limits on the color field rates and ratios for each color are defined by the algorithm used. The typical duty cycle adjustment range is from 10% to 60% per color with field rates from 3 to 9 color fields per frame. For customization of these parameters including reduced power LC drive algorithms please contact Syndiant directly for support.

1.4 SPI flash Interface

The SPI flash interface is designed to allow initial configuration to be loaded quickly from an external SPI flash device. This feature also allows multiple configurations to be loaded quickly from flash on mode change requests from a system host processor. A recommended 8MBit flash chip is the Winbond W25Q80DVSNIG.

The specific location of the data within the flash is flexible and can be defined by user command (see page 19) using a configuration block. The Config Block is a series of address pointers used by the SYA1232 to identify the starting point in flash for various blocks of data. The diagram below illustrates one possible configuration identifying application code necessary to support user commands, storage space for splash screen data and several other blocks used to form a display **"**Mode**".** When the user selects a "Bank" to load, one selection from each of these are loaded together to create the display "Mode" desired. In particular, a selection from the Schedule, ReGamma, Gamma and Register Banks makes up a display "Mode".

0x0F FFFF	(for W25Q80 or W25X80)
0x07 C000	Application Code (SYA1232 or SYA1311)
0x01 9000	Index 0-7 Schedule
0x01 1000	Index 0-7 ReGamma (4 x 256 x 32 bits each -> 1 sector for each index)
0x00 9000	Index 0-7 Gamma (3 x 256 x 16 bits each -> 1 sector for each index)
0x00 1000	Index 0-7 (Index 8 and above are in ROM and cannot be addressed in flash) Configuration/register Settings (1 sector for each index)
0x14	ROM version, 0x0001
0	Config Block; pointers for start address Gam, RGM, SCH, Ssize, Reserved, APP 0xB0 = 00009000, 00011000, 0019000, 0600, 00049000, 07C0

Note: The Black outline indicates blocks that can be moved by changing the Config Block (command 0xB0)

1.4.1 Bypassed SPI flash Interface mode (ROM only)

The SPI flash interface is optional. The boot from flash option can be bypassed by using a pull-down instead of a pull-up connected to Flash CS. This results in a slightly reduced set of valid I2C commands and features as follows.

- Projector powers down with no video source, (boots to 0x16 = 0x03)
- No Splash screen support, Affects registers 0x10,0x16
- No GPIO[1:0] PWM support, No support for register 0x3B
- No Flash control 0xB0 – 0xB6

1.5 GPIO

Up to eight general purpose input/output pins may be used to access and control peripheral devices.

1.6 Illuminator Enables

Three (RGB) illuminator enables provide synchronization for LED or Laser illuminators. Optional user-configurable PWM may also be added on top of the enable signals to independently control power to each illuminator.

The frequency of each of the LED enable signals is the number of color fields times the frame sync input. For example for a 6 color field schedule GRGBGR with 60Hz Frame sync. The Green enable is 3 * 60 = 180 Hz, the red is 2 * 60 = 120 Hz, and the blue is 1 * 60 = 60Hz.

The minimum value for the PWM on the enable signals is panel clock divided by 16, the typical set value is 10KHz.

1.7 External Crystal Resonator Connections

Typical connection of an external crystal resonator to the oscillator cell is shown in figure below. External circuit parameters (Rfb, Rd, CIN, COUT) depend on manufacturer specifications for the specific crystal used. Refer to the *SYA1232 Refererence Design Schematic* for an example of this circuit and device selection.

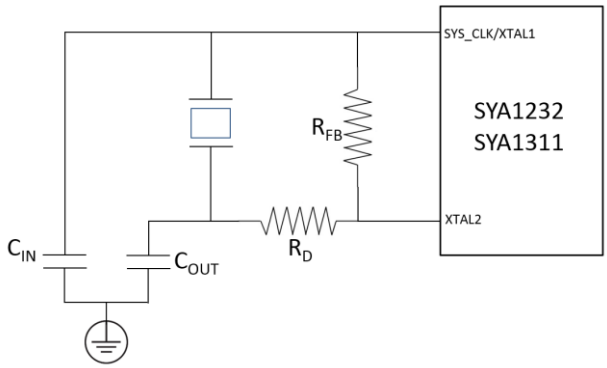


Figure 3 Typical Crystal Resonator Connections

1.8 Suggested PCB Layout Guidelines

Since the panel interface is a critical system interface it is recommended that the following layout guidelines be followed to optimize the interface timing between the SYA1232 and the LCOS panel.

- Trace Widths: Outer layers 0.125mm (.005”), inner layers 0.100mm (.004”)
- Trace/trace spacing: Top side routing to ASIC escape (no vias): trace spacing 0.1-0.125mm(1x).
- Length matching and 50 Ohms impedance matching for panel interface signals (P_DATA[31:0], P_CMD, P_DVLD and P_CLK)
- Add a 10 ohm, ¼ watt, 1% series termination resistors on all panel interface signals placed close to the SYA1232 outputs.
- The absolute length (ASIC PCB + ASIC Connector + Flex Cable + Panel Connector + Panel PCB) shall be less than or equal to 5.5”
- Strip line design for the Flex cable is recommended.

2 I2C Command Definition

An I2C slave interface allows a system host controller to communicate with the SYA1232 controller. This I2C bus can be used to configure or monitor operation of the SYA1232.

Key features of the SYA1232 I2C interface are listed below:

- Conforms to version 2.1 of the I2C specification.
- 400kb/s maximum speed
- Slave address 0x67 or 0x77 selectable by (FIELD/) I2C_SEL pin

2.1 Command format for I2C writes

Figure 4 shows an example of writing a command to the SYA1232 via I2C. The first byte of the transaction is the slave address for the controller and direction flag (LSB, write=0). This value can be set in hardware by tying the I2C_SEL signal High - 0xEE (1110 111x b) or Low - 0xCE (1100 111x b). In the example, the 7-bit address is 0x77 (0xEE with direction flag appended). The second byte is the command ID within the controller that will be written. In the example, data 0x07 is the data associated with the command 0x10 (projection mode). The commands of the SYA1232 use a variable number of data bytes.

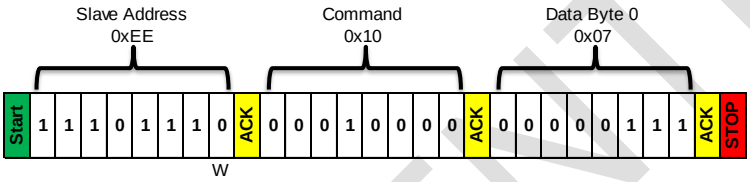


Figure 4: I2C Format for Writing Registers

Where:

- START = I2C Start protocol
- ACK = I2C Acknowledge protocol
- STOP = I2C Stop protocol

2.2 Command format for I2C reads

A read operation consists of two I2C transactions; a write (direction flag = 0) of the address of the command ID of interest within the controller followed by a read (direction flag = 1) of the expected number of bytes. In the example shown in Figure 5, data 0x07 is read from command address 0x10. The first byte of the write operation is the slave address for the controller and direction flag for the write (0xEE with direction flag appended). The second byte is the address for the command ID that will be read. After this, either a restart or stop then start condition is issued before the slave address is sent by the master again but with the direction flag = 0 (address = 0xEF with direction flag). The next byte(s) are the data read from the SYA1232 – in this case 0x07 which is the value of command 0x10. The number of bytes varies by command.

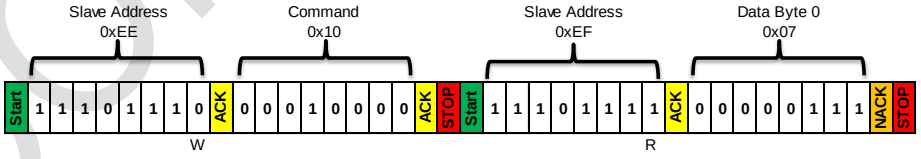


Figure 5: I2C Format for Reading Registers

Where:

- START = I2C Start protocol
- ACK = I2C Acknowledge protocol
- NACK = I2C Not-Acknowledged protocol
- STOP = I2C Stop protocol

2.3 Command Operation Descriptions:

The following sections describe each of the I2C commands in detail. Default values are provided for reference only and are user configurable with an external flash. The values are denoted in binary unless described with '0x' prefix (hex notation). Grayed out default values are dependent on system configuration or inputs.

2.3.1 Status and Informational commands:

<table>
<tr><th>CMD</th><th>Dir.</th><th>Description</th><th>Bytes</th></tr>
<tr><td>0x00</td><td>R</td><td>Status:
<table>
<tr><th>Byte</th><th>Bits</th><th>Typical</th><th>Description</th></tr>
<tr><td rowspan="2">[3]</td><td>[7:4]</td><td>0</td><td>Current video source:
0 = External video
1 = MIPI
2 = Splash Screen (future implementation)
3 = Internal Test Pattern
4-6 = Reserved
7 = No Video input</td></tr>
<tr><td>[3:0]</td><td>9</td><td>Video Input auto-set state machine state:
0 = initialization (no video)
1-8 = transitioning
9 = Displaying video (idle)</td></tr>
<tr><td>[2]</td><td>[7:0]</td><td>00</td><td>Reserved</td></tr>
<tr><td rowspan="8">[1]</td><td>[7]</td><td>0</td><td>Reserved</td></tr>
<tr><td>[6]</td><td>0</td><td>Reserved</td></tr>
<tr><td>[5]</td><td>0</td><td>Vsync timer expired</td></tr>
<tr><td>[4]</td><td>0</td><td>Panel interface error</td></tr>
<tr><td>[3]</td><td>0</td><td>Missing DE</td></tr>
<tr><td>[2]</td><td>0</td><td>Syncs missing</td></tr>
<tr><td>[1]</td><td>0</td><td>Status change</td></tr>
<tr><td>[0]</td><td>0</td><td>Video lost</td></tr>
<tr><td rowspan="8">[0]</td><td>[7]</td><td>0</td><td>Missed schedule write</td></tr>
<tr><td>[6]</td><td>0</td><td>Invalid I2C read command</td></tr>
<tr><td>[5]</td><td>0</td><td>Invalid I2C write command
(stop occurred that did not go with cmd)</td></tr>
<tr><td>[4]</td><td>0</td><td>Invalid app code pointer found in flash</td></tr>
<tr><td>[3]</td><td>0</td><td>I2C write data wrong size</td></tr>
<tr><td>[2]</td><td>0</td><td>Panel register read timeout</td></tr>
<tr><td>[1]</td><td>0</td><td>Incorrect app code flag in flash</td></tr>
<tr><td>[0]</td><td>0</td><td>App code load from flash failed</td></tr>
</table></td><td>4</td></tr>
<tr><td></td><td>0x09</td><td>Read Firmware Version (hex – readable):
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>[9:8]</td><td>[15:0]</td><td>0x2013</td><td>App code Year</td></tr>
<tr><td>[7]</td><td>[7:0]</td><td>0x05</td><td>App code Month</td></tr>
<tr><td>[6]</td><td>[7:0]</td><td>0x01</td><td>App code Day</td></tr>
<tr><td>[5]</td><td>[7:0]</td><td>0x02</td><td>App code Version</td></tr>
<tr><td>[4:3]</td><td>[15:0]</td><td>0x2011</td><td>ROM code Year</td></tr>
<tr><td>[2]</td><td>[7:0]</td><td>0x10</td><td>ROM code Month</td></tr>
<tr><td>[1]</td><td>[7:0]</td><td>0x11</td><td>ROM code Day</td></tr>
<tr><td>[0]</td><td>[[7:4]</td><td>0x00</td><td>Reserved</td></tr>
<tr><td>[0]</td><td>[3:0]</td><td>0x02</td><td>Package type:
00,01 = Reserved
02 = SYA1232
03 =S YA1311
04-07 = Reserved</td></tr>
</table></td><td>10</td></tr>
</table>

<table>
<tr><th>CMD</th><th>Dir.</th><th>Description</th><th>Bytes</th></tr>
<tr><td>0x0B</td><td>W</td><td>Reload Schedule Summary:
This command must be sent after loading a new schedule to synchronize ARC (processor) data with a newly loaded schedule. This is not required when loading the mode file from flash since it is automatically performed by firmware at that time. Must include 0 as data byte (0B00).
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>[0]</td><td>[7:0]</td><td>00</td><td>Reserved</td></tr>
</table></td><td>1</td></tr>
<tr><td>0x0C</td><td>R</td><td>Read Video Input Status Summary:
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td rowspan="4">[42]</td><td>[7:3]</td><td>00</td><td>Reserved</td></tr>
<tr><td>[2]</td><td></td><td>Vertical sync polarity</td></tr>
<tr><td>[1]</td><td></td><td>Field value</td></tr>
<tr><td>[0]</td><td></td><td>Horizontal sync polarity</td></tr>
<tr><td>[41:39]</td><td>[7:0]</td><td></td><td>Vertical sync width</td></tr>
<tr><td>[38:36]</td><td>[7:0]</td><td></td><td>Vertical sync period</td></tr>
<tr><td>[35:33]</td><td>[7:0]</td><td></td><td>Vertical sync period [in System Clocks]</td></tr>
<tr><td>[32:31]</td><td>[7:0]</td><td></td><td>Vertical sync to Horizontal sync [in pixel clocks]</td></tr>
<tr><td>[30:28]</td><td>[7:0]</td><td></td><td>Vertical sync to field [pixels]</td></tr>
<tr><td>[27:26]</td><td>[7:0]</td><td></td><td>Horizontal sync width</td></tr>
<tr><td>[25:24]</td><td>[7:0]</td><td></td><td>Horizontal sync period [in pixel clocks]</td></tr>
<tr><td>[23:22]</td><td>[7:0]</td><td></td><td>Horizontal sync period [in System Clocks]</td></tr>
<tr><td>[21:20]</td><td>[7:0]</td><td></td><td>Total lines per frame</td></tr>
<tr><td>[19:18]</td><td>[7:0]</td><td></td><td>Horizontal front porch</td></tr>
<tr><td>[17:16]</td><td>[7:0]</td><td></td><td>Horizontal back porch</td></tr>
<tr><td>[15:14]</td><td>[7:0]</td><td></td><td>Vertical front porch</td></tr>
<tr><td>[13:12]</td><td>[7:0]</td><td></td><td>Vertical back porch</td></tr>
<tr><td>[11:10]</td><td>[7:0]</td><td></td><td>Actual pixels per line</td></tr>
<tr><td>[9:8]</td><td>[7:0]</td><td></td><td>Actual lines per frame (based on Horizontal sync)</td></tr>
<tr><td>[7:6]</td><td>[7:0]</td><td></td><td>Actual pixels per line (based on Data Enable)</td></tr>
<tr><td>[5]</td><td>[7:0]</td><td></td><td>Minimum Red level</td></tr>
<tr><td>[4]</td><td>[7:0]</td><td></td><td>Maximum Red level</td></tr>
<tr><td>[3]</td><td>[7:0]</td><td></td><td>Minimum Green level</td></tr>
<tr><td>[2]</td><td>[7:0]</td><td></td><td>Maximum Green level</td></tr>
<tr><td>[1]</td><td>[7:0]</td><td></td><td>Minimum Blue level</td></tr>
<tr><td>[0]</td><td>[7:0]</td><td></td><td>Maximum Blue level</td></tr>
</table></td><td>43</td></tr>
</table>

2.3.2 Mode selection and control commands:

<table>
<tr><th>CMD</th><th>Dir.</th><th>Description</th><th>Bytes</th></tr>
<tr><td>0x0D</td><td>W</td><td>Capture Input video timing parameters for quickboot.
<table>
<tr><th>Byte</th><th>Bits</th><th>Description</th></tr>
<tr><td rowspan="3">[0]</td><td>[7:2]</td><td>Reserved</td></tr>
<tr><td>[1]</td><td>Quickboot Enable</td></tr>
<tr><td>[0]</td><td>Quickboot Settings capture from current incoming video</td></tr>
</table></td><td>1</td></tr>
<tr><td>0x10</td><td>R/W</td><td>Projection Mode:
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td rowspan="5">[0]</td><td>[7]</td><td>0</td><td>Panel Off</td></tr>
<tr><td>[6]</td><td>0</td><td>Freeze Image (presentation mode)</td></tr>
<tr><td>[5:4]</td><td>00</td><td><u>Video Protocol</u>:
00 – RGB888
01 – YCbCr444
10 – Reserved
11 – Reserved</td></tr>
<tr><td>[3]</td><td>0</td><td>Reserved</td></tr>
<tr><td>[2:0]</td><td>000</td><td><u>Video Input bus select</u>:
000 – External RGB
001 – MIPI/LVDS
010 – Splash Screen (future implementation)
011 – Internal Test Pattern
111 – Power Down Mode – Panel off and all but I2C power down (min power)
others – Reserved</td></tr>
</table></td><td>1</td></tr>
<tr><td>0x11</td><td>R/W</td><td>Horizontal Image position/flip:
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>[0]</td><td>[7]</td><td>1</td><td>Horizontal Flip</td></tr>
<tr><td>[0]</td><td>[6:0]</td><td>000 0000</td><td>Horizontal offset (signed, 2’s complement format)</td></tr>
</table>
NOTE: The valid range for offset depends on the schedule being used and resolution of the input. Invalid settings will cause the image to become unstable.</td><td>1</td></tr>
<tr><td>0x12</td><td>R/W</td><td>Vertical Image position/flip:
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>[0]</td><td>[7]</td><td>0</td><td>Vertical Flip</td></tr>
<tr><td>[0]</td><td>[6:0]</td><td>000 0000</td><td>Vertical offset (signed, 2’s complement format)</td></tr>
</table>
NOTE: The valid range for offset depends on the schedule being used and resolution of the input. Invalid settings will cause the image to become unstable.</td><td>1</td></tr>
<tr><td>0x13</td><td>R/W</td><td>Input Scaling Configuration to scale input to output video data:
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td rowspan="2">[0]</td><td>[7:2]</td><td>0000 00</td><td>Reserved</td></tr>
<tr><td>[1:0]</td><td>01</td><td>Scale Mode:
00 = Original (no scale)
01 = Panel size (720p or 1080p)
10 = Scaled to max while maintaining aspect ratio of input
11 = Reserved</td></tr>
</table></td><td>1</td></tr>
</table>

<table>
<tr><td>0x14</td><td>R/W</td><td>Sync source selection:
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>[0]</td><td>[7:1]</td><td>0000 000</td><td>Reserved</td></tr>
<tr><td>[0]</td><td>[0]</td><td>0</td><td>0 = Use external syncs
1 = Generate DE based on Command 0x15</td></tr>
</table>
Note: The settings for internal Data Enable must be configured using command 0x15.</td><td>1</td></tr>
</table>

<table>
<tr><th>CMD</th><th>Dir.</th><th>Description</th><th>Bytes</th></tr>
<tr><td>0x15</td><td>R/W</td><td>Internal DE Config:
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td rowspan="2">[7]</td><td>[7:3]</td><td>0000 0</td><td>Reserved</td></tr>
<tr><td>[2:0]</td><td rowspan="2">0x000</td><td rowspan="2">X Resolution (11-bits)</td></tr>
<tr><td>[6]</td><td>[7:0]</td></tr>
<tr><td rowspan="2">[5]</td><td>[7:2]</td><td>0000 00</td><td>Reserved</td></tr>
<tr><td>[1:0]</td><td rowspan="2">0x000</td><td rowspan="2">Horizontal delay [clks]</td></tr>
<tr><td>[4]</td><td>[7:0]</td></tr>
<tr><td rowspan="2">[3]</td><td>[7:2]</td><td>0000 00</td><td>Reserved</td></tr>
<tr><td>[1:0]</td><td rowspan="2">0x000</td><td rowspan="2">Y resolution</td></tr>
<tr><td>[2]</td><td>[7:0]</td></tr>
<tr><td rowspan="2">[1]</td><td>[7:2]</td><td>0000 00</td><td>Reserved</td></tr>
<tr><td>[1:0]</td><td rowspan="2">0x000</td><td rowspan="2">Vertical delay [lines]</td></tr>
<tr><td>[0]</td><td>[7:0]</td></tr>
</table>
Note: Internal DE must be selected using command 0x14 before these settings will be applied to the incoming video.</td><td>8</td></tr>
<tr><td>0x16</td><td>R/W</td><td>Input Loss Configuration:
Upon detection of loss of video input signal (Vsync), internal syncs will automatically be selected. This command allows the user to select which internal projection mode will be used (similar to using the manual command 0x10 mode setting).
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td rowspan="2">[0]</td><td>[7:2]</td><td>0</td><td>Reserved</td></tr>
<tr><td>[1:0]</td><td>1</td><td>Mode selection (see below)</td></tr>
</table>
<table>
<tr><th>[1:0]</th><th>Mode Selection</th></tr>
<tr><td>00b (0d)</td><td>Splash Screen (future implementation)</td></tr>
<tr><td>01b (1d)</td><td>Internal Test Pattern (Default)</td></tr>
<tr><td>10b (2d)</td><td>Reserved</td></tr>
<tr><td>11b (3d)</td><td>Power Down Mode</td></tr>
</table></td><td>1</td></tr>
<tr><td>0x18</td><td>R/W</td><td>MIPI/LVDS Video Input Configuration:
Configures the high speed interface to properly interpret input data.
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td rowspan="3">[3]</td><td>[7]</td><td></td><td>1=LVDS mode enable
0=MIPI mode enable</td></tr>
<tr><td>[6:3]</td><td></td><td>Reserved</td></tr>
<tr><td>[2:0]</td><td>0</td><td>Number of MIPI Clock Lanes used:
000=4 lanes (Default)
001 = 1 Lane
…
100 = 4 lanes</td></tr>
</table></td><td></td></tr>
</table>

<table>
<tr><th>CMD</th><th>Dir.</th><th>Description</th><th>Bytes</th></tr>
<tr><td></td><td></td><td>
<table>
<tr><td>[2:0]</td><td>[23:0]</td><td></td><td>24-bits; MIPI Clock Lane Frequency = frequency [kHz] x 1024</td></tr>
</table>
Default = 0x04075AD0; 4 lanes and clock lane frequency of 482Mhz which will support 1080p.
</td><td></td></tr>
<tr><td>0x1A</td><td>R/W</td><td>
Test Pattern Generator [TPG] Selection:
When no video input is available the currently configured TPG will be selected automatically.
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td rowspan="2">[0]</td><td>[7:4]</td><td>0x0</td><td>Reserved</td></tr>
<tr><td>[3:0]</td><td>0x0</td><td>TPG selection (see below)</td></tr>
</table>
<table>
<tr><th>[3:0]</th><th>TPG Selection</th></tr>
<tr><td>0x0</td><td>Solid Field</td></tr>
<tr><td>0x1</td><td>Color Bar</td></tr>
<tr><td>0x2</td><td>Vertical Lines</td></tr>
<tr><td>0x3</td><td>Horizontal Lines</td></tr>
<tr><td>0x4</td><td>Grid</td></tr>
<tr><td>0x5</td><td>Diagonal Lines</td></tr>
<tr><td>0x6</td><td>Checkerboard</td></tr>
<tr><td>0x7</td><td>Vertical Ramp</td></tr>
<tr><td>0x8</td><td>Horizontal Ramp</td></tr>
<tr><td>others</td><td>Reserved</td></tr>
</table>
Note: Appropriate configurations for commands 0x1B, 0x1C, 0x1D and 0x1E need to be made for each TPG selection.
</td><td>1</td></tr>
<tr><td>0x1B</td><td>R/W</td><td>
TPG Border Config:
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td rowspan="2">[0]</td><td>[7:6]</td><td>00</td><td>Border Color (see table)</td></tr>
<tr><td>[5:0]</td><td>00 0000</td><td>Border Width</td></tr>
</table>
<table>
<tr><th>[1:0]</th><th>Border Color</th></tr>
<tr><td>00</td><td>Border Color = Black</td></tr>
<tr><td>01</td><td>Border Color = White</td></tr>
<tr><td>10</td><td>Border Color = C1 (0x1C)</td></tr>
<tr><td>11</td><td>Border Color = C2 (0x1D)</td></tr>
</table>
</td><td>1</td></tr>
<tr><td>0x1C</td><td>R/W</td><td>
TPG Color 1 Config:
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>[2]</td><td>[7:0]</td><td>0x00</td><td>Red value (0-255)</td></tr>
<tr><td>[1]</td><td>[7:0]</td><td>0x00</td><td>Green value (0-255)</td></tr>
<tr><td>[0]</td><td>[7:0]</td><td>0xFF</td><td>Blue value (0-255)</td></tr>
</table>
.
</td><td>3</td></tr>
<tr><td></td><td></td><td></td><td></td></tr>
</table>

<table>
<tr><th>CMD</th><th>Dir.</th><th>Description</th><th>Bytes</th></tr>
<tr><td>0x1D</td><td>R/W</td><td>TPG Color 2 Config:
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>[2]</td><td>[7:0]</td><td>0x00</td><td>Red value (0-255)</td></tr>
<tr><td>[1]</td><td>[7:0]</td><td>0x00</td><td>Green value (0-255)</td></tr>
<tr><td>[0]</td><td>[7:0]</td><td>0x00</td><td>Blue value (0-255)</td></tr>
</table></td><td>3</td></tr>
<tr><td>0x1E</td><td>R/W</td><td>TPG Size Config:
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>[1]</td><td>[7:0]</td><td>0x00</td><td>Size Component (0-255)</td></tr>
<tr><td>[0]</td><td>[7:0]</td><td>0x00</td><td>Size Component (0-255)</td></tr>
</table></td><td>2</td></tr>
<tr><td>0x1F</td><td>R/W</td><td>TPG Resolution:
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>[3:2]</td><td>[7:0]</td><td>0500</td><td>11-bit Horizontal Resolution [pixels]</td></tr>
<tr><td>[1:0]</td><td>[7:0]</td><td>02D0</td><td>11-bit Vertical Resolution [pixels]</td></tr>
</table></td><td>4</td></tr>
</table>

2.3.3 Peripheral Configuration and Control Commands:

<table>
<tr><th>CMD</th><th>Dir.</th><th>Description</th><th>Bytes</th></tr>
<tr><td>0x30</td><td>R/W</td><td>Red Illuminator Configuration:
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td rowspan="2">[3]</td><td>[7]</td><td>1</td><td>Enable</td></tr>
<tr><td>[6:4]</td><td>000</td><td>Reserved</td></tr>
<tr><td rowspan="2">[2]</td><td>[3:0]</td><td rowspan="2">0x064</td><td rowspan="2">Turn-On Delay [12-bit, in µs]</td></tr>
<tr><td>[7:0]</td></tr>
<tr><td rowspan="2">[1]</td><td>[7:4]</td><td>0000</td><td>Reserved</td></tr>
<tr><td>[3:0]</td><td rowspan="2">0x064</td><td rowspan="2">Turn-Off Delay [12-bit, in µs]</td></tr>
<tr><td>[0]</td><td>[7:0]</td></tr>
</table>
Note: ‘Turn-Off’ must be > ‘Turn-On’ or it will be set to ‘Turn-On’ + 1</td><td>4</td></tr>
<tr><td>0x31</td><td>R/W</td><td>Green Illuminator Configuration:
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td rowspan="2">[3]</td><td>[7]</td><td>1</td><td>Enable</td></tr>
<tr><td>[6:4]</td><td>000</td><td>Reserved</td></tr>
<tr><td rowspan="2">[2]</td><td>[3:0]</td><td rowspan="2">0x064</td><td rowspan="2">Turn-On Delay [12-bit, in µs]</td></tr>
<tr><td>[7:0]</td></tr>
<tr><td rowspan="2">[1]</td><td>[7:4]</td><td>0000</td><td>Reserved</td></tr>
<tr><td>[3:0]</td><td rowspan="2">0x064</td><td rowspan="2">Turn-Off Delay [12-bit, in µs]</td></tr>
<tr><td>[0]</td><td>[7:0]</td></tr>
</table>
Note: ‘Turn-Off’ must be > ‘Turn-On’ or it will be set to ‘Turn-On’ + 1</td><td>4</td></tr>
<tr><td>0x32</td><td>R/W</td><td>Blue Illuminator Configuration:
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td rowspan="2">[3]</td><td>[7]</td><td>1</td><td>Enable</td></tr>
<tr><td>[6:4]</td><td>000</td><td>Reserved</td></tr>
<tr><td rowspan="2">[2]</td><td>[3:0]</td><td rowspan="2">0x064</td><td rowspan="2">Turn-On Delay [12-bit, in µs]</td></tr>
<tr><td>[7:0]</td></tr>
<tr><td rowspan="2">[1]</td><td>[7:4]</td><td>0000</td><td>Reserved</td></tr>
<tr><td>[3:0]</td><td rowspan="2">0x064</td><td rowspan="2">Turn-Off Delay [12-bit, in µs]</td></tr>
<tr><td>[0]</td><td>[7:0]</td></tr>
</table>
Note: ‘Turn-Off’ must be > ‘Turn-On’ or it will be set to ‘Turn-On’ + 1</td><td>4</td></tr>
</table>

.

<table>
<tr><th>CMD</th><th>Dir.</th><th>Description</th><th>Bytes</th></tr>
<tr><td>0x36</td><td>R/W</td><td>Red Channel PWM Configuration:
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td rowspan="2">[1]</td><td>[7:2]</td><td>0000 00</td><td>Reserved</td></tr>
<tr><td>[1:0]</td><td rowspan="2">0x000</td><td rowspan="2">Red Illuminator PWM percentage (1023=100%).</td></tr>
<tr><td>[0]</td><td>[7:0]</td></tr>
</table>
If no desaturation is required the PWM for colors other than Red should be set to 0.</td><td>2</td></tr>
<tr><td>0x37</td><td>R/W</td><td>Green Channel PWM Configuration:
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td rowspan="2">[1]</td><td>[7:2]</td><td>0000 00</td><td>Reserved</td></tr>
<tr><td>[1:0]</td><td rowspan="2">0x000</td><td rowspan="2">Green Illuminator PWM percentage (1023=100%).</td></tr>
<tr><td>[0]</td><td>[7:0]</td></tr>
</table>
If no desaturation is required the PWM for colors other than Green should be set to 0.</td><td>2</td></tr>
<tr><td>0x38</td><td>R/W</td><td>Blue Channel PWM Configuration:
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td rowspan="2">[1]</td><td>[7:2]</td><td>0000 00</td><td>Reserved</td></tr>
<tr><td>[1:0]</td><td rowspan="2">0x000</td><td rowspan="2">Blue Illuminator PWM percentage (1023=100%).</td></tr>
<tr><td>[0]</td><td>[7:0]</td></tr>
</table>
If no desaturation is required the PWM for colors other than Blue should be set to 0.</td><td>2</td></tr>
<tr><td>0x3A</td><td>R/W</td><td>Illuminator PWM Frequency Configuration:
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>[5:4]</td><td>[15:0]</td><td>0x000a</td><td>Red Illuminator PWM Frequency target [kHz]</td></tr>
<tr><td>[3:2]</td><td>[15:0]</td><td>0x000a</td><td>Green Illuminator PWM Frequency target [kHz]</td></tr>
<tr><td>[1:0]</td><td>[15:0]</td><td>0x000a</td><td>Blue Illuminator PWM Frequency target [kHz]</td></tr>
</table>
Note: Minimum frequency is 5kHz.</td><td>6</td></tr>
<tr><td>0x3C</td><td>R/W</td><td>GPIO Configuration (mode for each I/O):
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>[2]</td><td>[7:0]</td><td>0</td><td>Reserved</td></tr>
<tr><td rowspan="5">[1]</td><td>[7:6]</td><td>0</td><td>GPIO 7</td></tr>
<tr><td>[5:4]</td><td>0</td><td>GPIO 6</td></tr>
<tr><td>[3:2]</td><td>0</td><td>GPIO 5</td></tr>
<tr><td>[1:0]</td><td>0</td><td>GPIO 4</td></tr>
<tr><td rowspan="4">[0]</td><td>[7:6]</td><td>0</td><td>GPIO 3</td></tr>
<tr><td>[5:4]</td><td>0</td><td>GPIO 2</td></tr>
<tr><td>[3:2]</td><td>0</td><td>GPIO 1</td></tr>
<tr><td>[1:0]</td><td>0</td><td>GPIO 0</td></tr>
</table>
<table>
<tr><th>Bit</th><th>Meaning</th></tr>
<tr><td>00 or 0</td><td>Static Input</td></tr>
<tr><td>01 or 1</td><td>Static Output</td></tr>
<tr><td>10</td><td>Reserved (PWM)</td></tr>
<tr><td>11</td><td>Reserved (Alternate Function)</td></tr>
</table></td><td>3</td></tr>
</table>

<table>
<tr><th>CMD</th><th>Dir.</th><th>Description</th><th>Bytes</th></tr>
<tr><td>0x40</td><td>R/W</td><td>GPIO Read/Write Value (for static I/O):
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>[1]</td><td>[7:0]</td><td>0</td><td>Reserved</td></tr>
<tr><td rowspan="8">[0]</td><td>[7]</td><td>0</td><td>GPIO 7</td></tr>
<tr><td>[6]</td><td>0</td><td>GPIO 6</td></tr>
<tr><td>[5]</td><td>0</td><td>GPIO 5</td></tr>
<tr><td>[4]</td><td>0</td><td>GPIO 4</td></tr>
<tr><td>[3]</td><td>0</td><td>GPIO 3</td></tr>
<tr><td>[2]</td><td>0</td><td>GPIO 2</td></tr>
</table></td><td>2</td></tr>
</table>

			[1]	0	GPIO 1	
			[0]	0	GPIO 0	

2.3.4 Image Processing and enhancement commands:

<table>
<tr><th>CMD</th><th>Dir.</th><th>Description</th><th>Bytes</th></tr>
<tr><td>0x50</td><td>R/W</td><td>Contrast:
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>[2]</td><td>[7:0]</td><td>0x0A</td><td>Red Contrast = Value * 10 (0x0A => 1.0)</td></tr>
<tr><td>[1]</td><td>[7:0]</td><td>0x0A</td><td>Green Contrast = Value * 10 (0x0A => 1.0)</td></tr>
<tr><td>[0]</td><td>[7:0]</td><td>0x0A</td><td>Blue Contrast = Value * 10 (0x0A => 1.0)</td></tr>
</table></td><td>3</td></tr>
<tr><td>0x53</td><td>R/W</td><td>Brightness:
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>[2]</td><td>[7:0]</td><td>0x00</td><td>Red (signed, 2’s complement formatted value)</td></tr>
<tr><td>[1]</td><td>[7:0]</td><td>0x00</td><td>Green (signed, 2’s complement formatted value)</td></tr>
<tr><td>[0]</td><td>[7:0]</td><td>0x00</td><td>Blue (signed, 2’s complement formatted value)</td></tr>
</table></td><td>3</td></tr>
<tr><td>0x56</td><td>R/W</td><td>Saturation: (uses CSC table)
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>[0]</td><td>[7:0]</td><td>0x0A</td><td>= Value * 10 (0x0A => 1.0)</td></tr>
</table></td><td>1</td></tr>
<tr><th>CMD</th><th>Dir.</th><th>Description</th><th>Bytes</th></tr>
<tr><td>0x57</td><td>R/W</td><td>Gamma Config:
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td rowspan="2">[1]</td><td>[7:2]</td><td>0010 00b</td><td>Reserved</td></tr>
<tr><td>[1:0]</td><td>10</td><td>Gamma Type Selection:
00 = Downloaded Table
01 = ITU-R BT.709
10 = Power Law (using Byte 0)
11 = Reserved</td></tr>
<tr><td>[0]</td><td>[7:0]</td><td>0x16</td><td>Power Law Gamma Curve
= Value * 10 (0x16 = power 2.2)</td></tr>
</table>
Note: Selecting Gamma type of ‘Downloaded Table’ requires that a custom table is downloaded using commands 0x80, 0x81 and 0x82.</td><td>2</td></tr>
</table>

<table>
<tr><th>CMD</th><th>Dir.</th><th>Description</th><th>Bytes</th></tr>
<tr><td>0x59</td><td>R/W</td><td>
Color Space Adjustment Config:
<table>
<tr><th>Byte</th><th>Bits</th><th>RGB*</th><th>YCbCr*</th><th>Description</th></tr>
<tr><td rowspan="8">[1]</td><td>[7]</td><td colspan="2">1</td><td>4:2:2 to 4:4:4 conversion enable</td></tr>
<tr><td>[6]</td><td colspan="2">1</td><td>Edge Compensation Enable</td></tr>
<tr><td>[5]</td><td colspan="2">1</td><td>Input Chroma order for 4:2:2 input:
0 = Cb first
1 = Cr first</td></tr>
<tr><td>[4]</td><td colspan="2">1</td><td>Flip MSB of Blue for 4:2:2 signed offset correction (0=no change)</td></tr>
<tr><td>[3]</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>[2]</td><td>0</td><td>1</td><td>Red input sign mode:
0 = unsigned
1 = signed</td></tr>
<tr><td>[1]</td><td>0</td><td>1</td><td>Red offset:
0 = Subtract 16 from Red input
1 = Flip MSB of Red</td></tr>
<tr><td>[0]</td><td>0</td><td>1</td><td>Red offset enable (0=disable bit 1)</td></tr>
<tr><td rowspan="8">[0]</td><td>[7]</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>[6]</td><td>0</td><td>0</td><td>Green input sign mode:
0 = unsigned
1 = signed</td></tr>
<tr><td>[5]</td><td>0</td><td>0</td><td>Green offset:
0 = Subtract 16 from Red input
1 = Flip MSB of Red</td></tr>
<tr><td>[4]</td><td>0</td><td>1</td><td>Green offset enable (0=disable bit 5)</td></tr>
<tr><td>[3]</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>[2]</td><td>0</td><td>1</td><td>Blue input sign mode:
0 = unsigned
1 = signed</td></tr>
<tr><td>[1]</td><td>0</td><td>1</td><td>Blue offset:
0 = Subtract 16 from Blue input
1 = Flip MSB of Blue</td></tr>
<tr><td>[0]</td><td>0</td><td>1</td><td>Blue offset enable (0=disable bit 1)</td></tr>
</table>
* The default values are 0xd000 for RGB and 0xd717 for YCbCr projection mode. These are set independantly based on the mode command selection (0x10)
</td><td>2</td></tr>
<tr><td>0x5A</td><td>R/W</td><td>
Load Color Space Table: (Coefficients = S2.8, Offsets = S9.6)
<table>
<tr><th>Byte</th><th>Bits</th><th>RGB*</th><th>YCbCr*</th><th>Description</th></tr>
<tr><td>[23:22]</td><td>[7:0]</td><td>0x0100</td><td>0x0199</td><td>Coefficient RC_1 (see below)</td></tr>
<tr><td>[21:20]</td><td>[7:0]</td><td>0x0000</td><td>0x012a</td><td>Coefficient GC_1 (see below)</td></tr>
<tr><td>[19:18]</td><td>[7:0]</td><td>0x0000</td><td>0x0000</td><td>Coefficient BC_1 (see below)</td></tr>
<tr><td>[17:16]</td><td>[7:0]</td><td>0x0000</td><td>0x0730</td><td>Coefficient RC_2 (see below)</td></tr>
<tr><td>[15:14]</td><td>[7:0]</td><td>0x0100</td><td>0x012a</td><td>Coefficient GC_2 (see below)</td></tr>
<tr><td>[13:12]</td><td>[7:0]</td><td>0x0000</td><td>0x079c</td><td>Coefficient BC_2 (see below)</td></tr>
<tr><td>[11:10]</td><td>[7:0]</td><td>0x0000</td><td>0x0700</td><td>Coefficient RC_3 (see below)</td></tr>
<tr><td>[9:8]</td><td>[7:0]</td><td>0x0000</td><td>0x012a</td><td>Coefficient GC_3 (see below)</td></tr>
<tr><td>[7:6]</td><td>[7:0]</td><td>0x0100</td><td>0x0205</td><td>Coefficient BC_3 (see below)</td></tr>
<tr><td>[5:4]</td><td>[7:0]</td><td>0x0000</td><td>0x0000</td><td>Red Offset C_r (see below)</td></tr>
<tr><td>[3:2]</td><td>[7:0]</td><td>0x0000</td><td>0x0000</td><td>Green Offset C_g (see below)</td></tr>
<tr><td>[1:0]</td><td>[7:0]</td><td>0x0000</td><td>0x0000</td><td>Blue Offset C_b (see below)</td></tr>
</table>
$$\begin{bmatrix} RC_1 & GC_1 & BC_1 \\ RC_2 & GC_2 & BC_2 \\ RC_3 & GC_3 & BC_3 \end{bmatrix} X \begin{bmatrix} R \\ G \\ B \end{bmatrix} + \begin{bmatrix} C_r \\ C_g \\ C_b \end{bmatrix} = \begin{bmatrix} Output_r \\ Output_g \\ Output_b \end{bmatrix}$$
*Note: Two CSC tables are stored within the device. One for RGB input mode and another for YCbCr projection mode. They are automatically addressed based on the Projection Mode (command 0x10).
</td><td>24</td></tr>
</table>

<table>
<tr><th>CMD</th><th>Dir.</th><th>Description</th><th>Bytes</th></tr>
<tr><td>0x5C</td><td>R/W</td><td>Interlace Configuration:
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td rowspan="4">[0]</td><td>[7:5]</td><td>000</td><td>Reserved</td></tr>
<tr><td>[4]</td><td>0</td><td>Field Polarity</td></tr>
<tr><td>[3:2]</td><td>00</td><td>Reserved</td></tr>
<tr><td>[1]</td><td>0</td><td>Mode (internal Field generation):
0 = Field signal toggles with Vsync
1 = Field signal generated by Vsync occurring within a window of time from Hsync</td></tr>
<tr><td>[0]</td><td>0</td><td>Internally Generated Field signal:
0 = Use External Field signal
1 = Use Internally Generated Field signal</td></tr>
</table></td><td>1</td></tr>
<tr><td>0x5F</td><td>R/W</td><td>Algorithm Control:
Regamma enable and jiggle table control for enhancing image based on frame rate/schedule
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td rowspan="8">[0]</td><td>[7]</td><td>0</td><td>Reserved</td></tr>
<tr><td>[6]</td><td>0</td><td>Watchdog disable</td></tr>
<tr><td>[5]</td><td></td><td>Reserved</td></tr>
<tr><td>[4]</td><td>0</td><td>0=Regamma computation OFF
1=Regamma computation ON</td></tr>
<tr><td>[3]</td><td>0</td><td>Reserved</td></tr>
<tr><td>[2]</td><td>0</td><td>SYL2271 mode enable</td></tr>
<tr><td>[1]</td><td>0</td><td>External frame buffer enable</td></tr>
<tr><td>[0]</td><td>0</td><td>Reserved</td></tr>
</table></td><td>1</td></tr>
</table>

<table>
<tr><th>CMD</th><th>Dir.</th><th>Description</th><th>Bytes</th></tr>
<tr><td>0x61</td><td>R/W</td><td>White Point Adjustment / Field Duration Selection:

User requested percentage of each color within the video frame time. Duration of an individual color field equals the percentage of that color divided by the number of scheduled fields displayed. The last color field receives any remaining time if the total percentage is <100%.
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>[5:4]</td><td>[15:0]</td><td></td><td>Red field(s) percentage of frame [%/100 * 1024]</td></tr>
<tr><td>[3:2]</td><td>[15:0]</td><td></td><td>Green field(s) percentage of frame [%/100 * 1024]</td></tr>
<tr><td>[1:0]</td><td>[15:0]</td><td></td><td>Blue field(s) percentage of frame [%/100 * 1024]</td></tr>
</table></td><td>6</td></tr>
<tr><td>0x62</td><td>R</td><td>Minimum Field Duration:
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>[5:4]</td><td>[15:0]</td><td></td><td>Red field(s) percentage of frame [%/100 * 1024]</td></tr>
<tr><td>[3:2]</td><td>[15:0]</td><td></td><td>Green field(s) percentage of frame [%/100 * 1024]</td></tr>
<tr><td>[1:0]</td><td>[15:0]</td><td></td><td>Blue field(s) percentage of frame [%/100 * 1024]</td></tr>
</table>
If the total ≥ 100%, no adjustment is possible with the current schedule.</td><td>6</td></tr>
<tr><td>0x63</td><td>R</td><td>Actual Field Duration:
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
</table></td><td>6</td></tr>
</table>

CMD	Dir.	Description	Bytes
		[5:4] [15:0] — Red field(s) percentage of frame [%/100 * 1024] [3:2] [15:0] — Green field(s) percentage of frame [%/100 * 1024] [1:0] [15:0] — Blue field(s) percentage of frame [%/100 * 1024] May be slightly < 100% but can be used to verify change requests to the DC.	

CMD	Dir.	Description	Bytes
0x68	R/W	Panel interface power selection: Determines how aggressive to set the panel clock vs dark time. [2] [1:0] Default 00 — Panel Clock Optimization: 0 = Maximize brightness, 1 = balanced, 2 = Minimize power [1:0] [15:0] Default 0x0c95 — Maximum Frequency selection: 0x0C95 = Max Freq x 32, (100MHz), 0x10C0 = 134MHz This setting will affect the minimum duty cycle (command 0x62).	3
0x6A	R/W	Keystone Correction: [1:0] [15:0] Default 0x0000 — Angle * 10 (signed value, range -30.0 to 30.0 degrees)	2
0x6B	R/W	Keystone Correction Config: [1] [7] Default 0 — Reserved [1] [6:0] Default 0x33 — Keystone Throw Ratio * 10, 0x33 = 5.1, (Range = 1.0 to 10.0) [0] [7:3] Default 0000 — Reserved [0] [2:0] Default 0000 — Alignment mode (see below) Bits 000: Far Edge Bits 001: Near Edge Bits 010: Center [default] Bits 011: Top Bits 100: Bottom Bits 101: Stretch (keeps max panel lines) Bits 110-111: Reserved	2

2.3.5 Table Upload commands:

<table>
<tr><th>CMD</th><th>Dir.</th><th>Description</th><th>Bytes</th></tr>
<tr><td></td><td></td><td></td><td></td></tr>
<tr><td>0x80</td><td>R/W</td><td>Red Gamma table:

Accesses the red gamma table in the controller memory.

<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>[511:510]</td><td>[15:0]</td><td></td><td>Gamma entry 0</td></tr>
<tr><td>…</td><td>[15:0]</td><td></td><td>…</td></tr>
<tr><td>[1:0]</td><td>[15:0]</td><td></td><td>Gamma entry 255</td></tr>
</table>
13 bits each entry</td><td>512</td></tr>
<tr><td>0x81</td><td>R/W</td><td>Green Gamma table:

Accesses the green gamma table in the controller memory.
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>[511:510]</td><td>[15:0]</td><td></td><td>Gamma entry 0</td></tr>
<tr><td>…</td><td>[15:0]</td><td></td><td>…</td></tr>
<tr><td>[1:0]</td><td>[15:0]</td><td></td><td>Gamma entry 255</td></tr>
</table>
13 bits each entry</td><td>512</td></tr>
<tr><td>0x82</td><td>R/W</td><td>Blue Gamma table:

Accesses the blue gamma table in the controller memory.
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>[511:510]</td><td>15:0]</td><td></td><td>Gamma entry 0</td></tr>
<tr><td>…</td><td>[15:0]</td><td></td><td>…</td></tr>
<tr><td>[1:0]</td><td>[15:0]</td><td></td><td>Gamma entry 255</td></tr>
</table>
13 bits each entry</td><td>512</td></tr>
<tr><td>0x83</td><td>R/W</td><td>Upload Red ReGamma table to memory:

<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>767:765</td><td>-</td><td></td><td>ReGamma entry 0</td></tr>
<tr><td>…</td><td>-</td><td></td><td>…</td></tr>
<tr><td>2:0</td><td>-</td><td></td><td>ReGamma entry 255</td></tr>
</table>
21 bits each entry</td><td>256 x 3
= 768</td></tr>
<tr><td>0x84</td><td>R/W</td><td>Upload Green ReGamma table to memory:

<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>767:765</td><td>-</td><td></td><td>ReGamma entry 0</td></tr>
<tr><td>…</td><td>-</td><td></td><td>…</td></tr>
<tr><td>2:0</td><td>-</td><td></td><td>ReGamma entry 255</td></tr>
</table>
21 bits each entry</td><td>256 x 3
= 768</td></tr>
<tr><td>0x85</td><td>R/W</td><td>Upload Blue ReGamma table to memory:

<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>767:765</td><td>-</td><td></td><td>ReGamma entry 0</td></tr>
<tr><td>…</td><td>-</td><td></td><td>…</td></tr>
<tr><td>2:0</td><td>-</td><td></td><td>ReGamma entry 255</td></tr>
</table>
21 bits each entry</td><td>256 x 3
= 768</td></tr>
</table>

2.3.6 Miscellaneous commands:

<table>
<tr><th>CMD</th><th>Dir.</th><th>Description</th><th>Bytes</th></tr>
<tr><td>0x91</td><td>R/W</td><td>Watchdog disable - Not saved to flash.
<table>
<tr><th>Byte</th><th>Bits</th><th>Description</th></tr>
<tr><td rowspan="2">[0]</td><td>[7:1]</td><td>Reserved</td></tr>
<tr><td>[0]</td><td>Disable Watchdog</td></tr>
</table></td><td>1</td></tr>
<tr><td>0x92</td><td>R/W</td><td>Watchdog reset count. The boot sequence will increment this count by 1. Count can be set to 0 by writing to this command. Otherwise it will start with undetermined value.
<table>
<tr><th>Byte</th><th>Bits</th><th>Description</th></tr>
<tr><td>[1:0]</td><td>[15:0]</td><td>Reset Count</td></tr>
</table></td><td>2</td></tr>
<tr><td>0xB0</td><td>R/W</td><td>Read/Write Config Block from/to Flash:
Sets the Bank address pointers used to position the start of each bank type in flash. A read will update controller memory from flash and then read back these loaded values over I2C. A write will store this table to flash starting at location 0.
<table>
<tr><th>Byte</th><th>Bits</th><th>Description</th></tr>
<tr><td>[19:16]</td><td>[31:0]</td><td>Start address in flash for gamma tables</td></tr>
<tr><td>[15:12]</td><td>[31:0]</td><td>Start address in flash for regamma tables</td></tr>
<tr><td>[11:08]</td><td>[31:0]</td><td>Start address in flash for schedules</td></tr>
<tr><td>[07:06]</td><td>[15:0]</td><td>Max size of schedules in instructions (rounded up to next 256 byte page boundary)</td></tr>
<tr><td>[05:02]</td><td>[31:0]</td><td>Start address in flash of splash screen (future implementation)</td></tr>
<tr><td>[01:00]</td><td>[15:0]</td><td>Starting page in flash (1 page = 256 bytes) for the location of the Application code. Default = 0x0400; can only be changed after ROM spin</td></tr>
</table></td><td>20</td></tr>
<tr><td>0xB5</td><td>W</td><td>Save current configuration Mode to Flash:
<table>
<tr><th>Byte</th><th>Bits</th><th>Description</th></tr>
<tr><td rowspan="2">[0]</td><td>[7:4]</td><td>Reserved</td></tr>
<tr><td>[3:0]</td><td>Register Bank Index</td></tr>
</table>WARNING: Saving to a Bank index beyond the capacity of the flash will result in corruption of the flash data.</td><td>1</td></tr>
<tr><td>0xB6</td><td>W</td><td>Load configuration Mode from Flash:
<table>
<tr><th>Byte</th><th>Bits</th><th>Description</th></tr>
<tr><td rowspan="3">[0]</td><td>[7:4]</td><td>Reserved</td></tr>
<tr><td>[3]</td><td>Memory Type: 1 = ROM
2 = Flash</td></tr>
<tr><td>[2:0]</td><td>Register Bank Index</td></tr>
</table>WARNING: Loading from a Bank index beyond the capacity of the flash will result in corruption of the configuration and require a reset to recover.</td><td>1</td></tr>
</table>

<table>
<tr><th>CMD</th><th>Dir.</th><th>Description</th><th>Bytes</th></tr>
<tr><td>0xBF</td><td>W</td><td>Set bank indices used for this mode:

Assigns the related schedule, Gamma, and Regamma bank index that will be used when a Load Mode (0xB6) or Save Mode (0xB5) command is issued. This command only sets the intended pointers and does not actually access the flash immediately. It is intended as a way to create more complex modes that resue existing banks, if desired, to optimize flash memory usage. Typically the index for each bank will be the same as the register bank to which it is associated.
<table>
<tr><th>Byte</th><th>Bits</th><th>Description</th></tr>
<tr><td rowspan="4">[1]</td><td>[7]</td><td>Memory Type: 1=ROM, 0=Flash</td></tr>
<tr><td>[6:4]</td><td>Gamma index</td></tr>
<tr><td>[3]</td><td>Memory Type: 1=ROM, 0=Flash</td></tr>
<tr><td>[2:0]</td><td>ReGamma index</td></tr>
<tr><td rowspan="4">[0]</td><td>[7]</td><td>Memory Type: 1=ROM, 0=Flash</td></tr>
<tr><td>[6:4]</td><td>Schedule index</td></tr>
<tr><td>[3:0]</td><td>Reserved</td></tr>
<tr><td></td><td></td></tr>
</table></td><td>2</td></tr>
</table>

<table>
<tr><td>0xDC</td><td>W</td><td>Jump to ARC application code:
• Must include 0 as data byte (DC00)
• After loading ARC application code by I2C into internal memory, this command sets the program counter to start execution of the code. (If the application code exists in flash memory, this command is not needed because the code will execute automatically.)</td><td>1</td></tr>
</table>

<table>
<tr><th>CMD</th><th>Dir.</th><th>Description</th><th>Bytes</th></tr>
<tr><td>0xE0</td><td>R/W</td><td>Configure Panel Temp Sensor I/F:
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td rowspan="3">[0]</td><td>[7]</td><td>0b</td><td>Enable Temp Sensor</td></tr>
<tr><td>[6:4]</td><td>000b</td><td>Reserved</td></tr>
<tr><td>[3:0]</td><td>0000b</td><td>Temp sensor range:
0 = min: 10 max: 70
1 = min: 5 max: 67
2 = min: 1 max: 62
3 = min: -5 max: 58
4 = min: 21 max: 80
5 = min: 16 max: 75
6 = min: 10 max: 71
7 = min: 5 max: 66
8 = min: 32 max: 89
9 = min: 27 max: 84
10 = min: 21 max: 79
11 = min: 15 max: 74
12 = min: 55 max: 108
13 = min: 49 max: 103
14 = min: 42 max: 97
15 = min: 32 max: 92</td></tr>
</table></td><td>1</td></tr>
<tr><td>0xE1</td><td>R/W</td><td>Configure Panel Temperature Sensor Interface:
<table>
<tr><th>Byte</th><th>Bits</th><th>Description</th></tr>
<tr><td>[1]</td><td>[7:0]</td><td>Maximum temperature [ºC]</td></tr>
<tr><td>[0]</td><td>[7:5]</td><td>Reserved</td></tr>
</table></td><td>2</td></tr>
</table>

<table>
<tr><th>CMD</th><th>Dir.</th><th>Description</th><th>Bytes</th></tr>
<tr><td></td><td></td><td>
<table>
<tr><td></td><td>[4]</td><td>Warm on boot enable</td></tr>
<tr><td></td><td>[3]</td><td>Reserved</td></tr>
<tr><td></td><td>[2]</td><td>Red field warm enable</td></tr>
<tr><td></td><td>[1]</td><td>Green field warm enable</td></tr>
<tr><td></td><td>[0]</td><td>Blue field warm enable</td></tr>
</table>
</td><td></td></tr>
<tr><td>0xE2</td><td>R</td><td>Read Panel Temp Sensor: [ºC]
A value of 0x80 indicates the temperature sensor is disabled.</td><td>1</td></tr>
<tr><td>0xE7</td><td>R/W</td><td>Panel Voltage PWM Control:
Used to optimize the contrast and brightness of the system due to LC biasing.
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td rowspan="2">[2]</td><td>[7:4]</td><td>0xA</td><td>Red Voltage PWM setting</td></tr>
<tr><td>[3:0]</td><td>0xA</td><td>Green Voltage PWM setting</td></tr>
<tr><td rowspan="2">[1]</td><td>[7:4]</td><td>0xA</td><td>Blue Voltage PWM setting</td></tr>
<tr><td>[3:0]</td><td>0xA</td><td>Reserved er</td></tr>
<tr><td>[0]</td><td>[7:0]</td><td>0x3C</td><td>PWM Frequency (in kHz – min 5kHz)</td></tr>
</table>
Note: The voltage PWM settings should be used as a fine adjustment after adjusting the overall ITO voltage using command 0xE9. The PWM frequency should not be changed from the default.</td><td>3</td></tr>
<tr><td>0xE9</td><td>R/W</td><td>Panel Charge Pump Control:
Used to optimize the contrast and brightness of the system due to LC biasing.
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td rowspan="2">[1]</td><td>[7]</td><td>1</td><td>Charge Pump Enable</td></tr>
<tr><td>[6:0]</td><td>000 0000</td><td>Vbb voltage setting</td></tr>
<tr><td rowspan="2">[0]</td><td>[7]</td><td>0</td><td>Reserved</td></tr>
<tr><td>[6:0]</td><td>000 0000</td><td>Vpp voltage setting</td></tr>
</table>
WARNING: Adjusting Vpp and Vbb to values different from each other will cause a DC imbalance on the panel and may result in image retention.</td><td>2</td></tr>
<tr><td>0xEA</td><td>R/W</td><td>Video Input Channel Mux:
Allows remapping of the video input data busses to simplify PCB layout. By default the hardware sets CH1= Red [R], CH2=Green [G], CH3=Blue [B].
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td rowspan="2">[0]</td><td>[7:3]</td><td>0000 0 b</td><td>Reserved</td></tr>
<tr><td>[2:0]</td><td>000 b</td><td>Bus Mapping (see below)</td></tr>
</table>
<table>
<tr><th></th><th>CH1:CH2:CH3 Bus Mapping</th></tr>
<tr><td>000</td><td>R:G:B</td></tr>
<tr><td>001</td><td>G:B:R</td></tr>
<tr><td>010</td><td>G:R:B</td></tr>
<tr><td>011</td><td>R:B:G</td></tr>
<tr><td>100</td><td>B:G:R</td></tr>
<tr><td>101</td><td>B:R:G</td></tr>
<tr><td>110</td><td>Reserved</td></tr>
<tr><td>111</td><td>Reserved</td></tr>
</table></td><td>1</td></tr>
</table>

0xEB | **R/W** | **12**

Video Input Bit Mux:
Allows remapping of the video input data bits within each color channel.

Byte	Bits	Default	Description
[11]	[7]	0	Reserved
	[6:4]	0x7	Red Bit 7 mapping (see table below)
	[3]	0	Reserved
	[2:0]	0x6	Red Bit 6 mapping (see table below)
[10]	[7]	0	Reserved
	[6:4]	0x5	Red Bit 5 mapping (see table below)
	[3]	0	Reserved
	[2:0]	0x4	Red Bit 4 mapping (see table below)
[9]	[7]	0	Reserved
	[6:4]	0x3	Red Bit 3 mapping (see table below)
	[3]	0	Reserved
	[2:0]	0x2	Red Bit 2 mapping (see table below)
[8]	[7]	0	Reserved
	[6:4]	0x1	Red Bit 1 mapping (see table below)
	[3]	0	Reserved
	[2:0]	0x0	Red Bit 0 mapping (see table below)
[7]	[7]	0	Reserved
	[6:4]	0x7	Green Bit 7 mapping (see table below)
	[3]	0	Reserved
	[2:0]	0x6	Green Bit 6 mapping (see table below)
[6]	[7]	0	Reserved
	[6:4]	0x5	Green Bit 5 mapping (see table below)
	[3]	0	Reserved
	[2:0]	0x4	Green Bit 4 mapping (see table below)
[5]	[7]	0	Reserved
	[6:4]	0x3	Green Bit 3 mapping (see table below)
	[3]	0	Reserved
	[2:0]	0x2	Green Bit 2 mapping (see table below)
[4]	[7]	0	Reserved
	[6:4]	0x1	Green Bit 1 mapping (see table below)
	[3]	0	Reserved
	[2:0]	0x0	Green Bit 0 mapping (see table below)
[3]	[7]	0	Reserved
	[6:4]	0x7	Blue Bit 7 mapping (see table below)
	[3]	0	Reserved
	[2:0]	0x6	Blue Bit 6 mapping (see table below)
[2]	[7]	0	Reserved
	[6:4]	0x5	Blue Bit 5 mapping (see table below)
	[3]	0	Reserved
	[2:0]	0x4	Blue Bit 4 mapping (see table below)
[1]	[7]	0	Reserved
	[6:4]	0x3	Blue Bit 3 mapping (see table below)
	[3]	0	Reserved
	[2:0]	0x2	Blue Bit 2 mapping (see table below)
[0]	[7]	0	Reserved
	[6:4]	0x1	Blue Bit 1 mapping (see table below)
	[3]	0	Reserved
	[2:0]	0x0	Blue Bit 0 mapping (see table below)

	bit mapping
000	maps to input bit 0
001	maps to input bit 1
…	…
111	maps to input bit 7

<table>
<tr>
<td>0xEE</td>
<td>R/W</td>
<td>Panel Clock Delay Conrol:
<table>
<tr><th>Byte</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td rowspan="2">[3]</td><td>[7:1]</td><td></td><td>Reserved</td></tr>
<tr><td>[0]</td><td>0</td><td>1: Invert panel clock
0: Normal panel clock</td></tr>
<tr><td>[2,1]</td><td colspan="2">all</td><td>Reserved</td></tr>
</table>
</td>
<td>2</td>
</tr>
</table>

3 Electrical Specifications

3.1 Absolute maximum ratings

Supply voltage range: V_{DD} (all V_{DD}'s) to GND ..... 0 to V_{DD}(typ) + 5% V
$V_{CCA\_11/18/33}$ to V_{SSA} ..... 0 to V_{DDA}(typ) + 5% V
Operating free-air temperature ..... -10 to 85 °C
Non-operational storage temperature ..... -40 to 110 °C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under DC and AC Electrical Specifications is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device stability.

Power cannot be applied to the device while it is subjected to nonoperational temperature. After the device has been subjected to nonoperational temperature, it must be returned (and stabilized) to a temperature within the proper range to avoid damage. **Failure to stabilize the device properly before applying power may cause permanent damage that will not be covered by device warranty**.

3.2 DC Electrical Specifications

Reference	Description	Min	Typ	Max	Unit	Note
V_{DD}	1.1V (nominal) Power supply	1.04	1.10	1.16	V	
V_{DD_SSTL}	1.2/3.3/1.8V (nominal) Power supply	1.71	1.80	1.89	V	
V_{DD_PIF}	1.2/3.3/1.8V (nominal) Power supply	1.71	1.80	1.89	V	
V_{DD_VID}	I/O Supply Voltage, Video input interface	V_{DD_VID}-5%	V_{DD_VID}	V_{DD_VID}+5%	V	1
V_{DD_LED}	I/O Supply Voltage, Illumination interface	V_{DD_LED}-5%	V_{DD_LED}	V_{DD_LED}+5%	V	1
V_{DD_XTAL}	1.8/2.5/3.3V Power supply, Crystal, OSC.				V	3
V_{DD_GPIO}	1.8/2.5/3.3V (nominal) GPIO Power supply	3.14	3.30	3.47	V	
V_{DD_SPI}	1.8/3.3V (nominal) Power supply, SPI I/F	3.14	3.30	3.47	V	
V_{DD_I2C}	1.8/3.3V (nominal) Power supply, SPI I/F	3.14	3.30	3.47	V	
GND	Digital Ground		0		V	
V_{CCA_11}	I/O Analog Supply Voltage	1.04	1.1	1.16	V	
V_{CCA_18}	I/O Analog Supply Voltage	1.71	1.80	1.89	V	
V_{CCA_33}	I/O Analog Supply Voltage	3.14	3.30	3.47	V	
V_{SSA}	I/O Analog Ground		0		V	2
V_{DD_FUSE}	Fuse programming option. GND		0		V	
V_{REF_SSTL}	SSTL buffer reference input		0		V	
I_{DD}	1.1V (nominal) Power supply		145		mA	
I_{DD_SSTL}	1.8V (nominal) Power supply		40		mA	
I_{DD_PIF}	1.8V (nominal) Power supply		<1		mA	
I_{DD_VID}	3.3V (nominal) Power supply		<1		mA	
I_{DD_LED}	3.3V (nominal) Power supply		<1		mA	
I_{DD_XTAL}	1.8V (nominal) Power supply		<1		mA	
I_{DD_GPIO}	3.3V (nominal) Power supply		1.75		mA	
I_{DD_SPI}	3.3V (nominal) Power supply		<1		mA	
I_{DD_I2C}	3.3V (nominal) Power supply		<1		mA	
MIPI_1.1	1.1V (nominal) Power supply		3.1		mA	
MIPI_1.8	1.8V (nominal) Power supply		1.5		mA	
MIPI_3.3	3.3V (nominal) Power supply		<1		mA	
F_{CLK}	System Clock frequency	24.75	25.0	25.25	Mhz	
T_A	Ambient Operating temperature	-10	40	85	°C	

Notes:
1. V_{DD_VID} and V_{DD_LED} supplies are determined by applications: 1.8V or 3.3V
2. V_{SSA} is isolated within the SYA1232 and must be tied together at one point on the system PCB.
3. Supports 1.8, 2.5, 3.3V crystals/oscillators.

3.3 ESD Rating

Human Body (HBM) +/- 3,000V (JEDEC-JESD22 A114E)
Charge Device Model (CDM)) +/-500V (JEDEC JS-002-2014)

3.4 Power Up/Down

The following power up/down sequence is recommended to prevent latch-up and damage to the SYA1232. I/O voltage must not be applied when core voltage is not present. Both I/O voltages may be turned on and off simultaneously. Depending on settings it can take up to 1.5 seconds after reset is released before the SYA1232 is ready to receive I2C commands. The time is greatly reduced if the gamma type selection of register 0x57 is set to downloaded table.

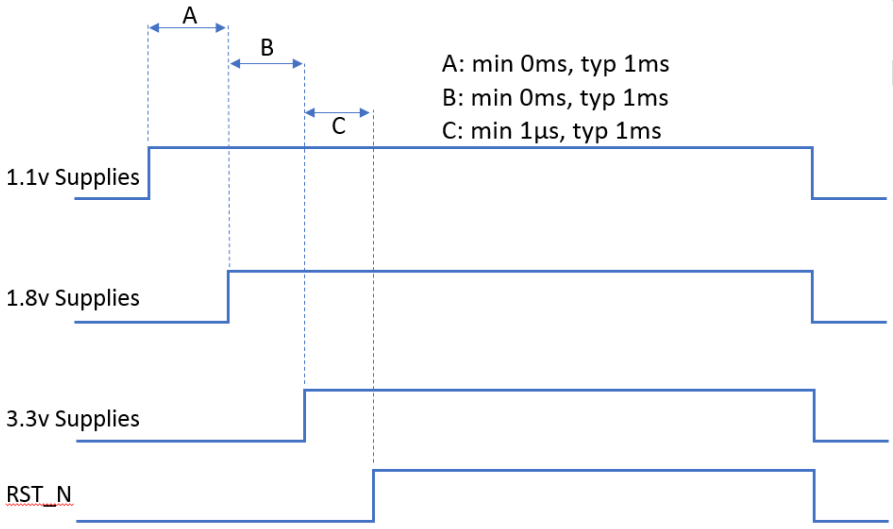


Figure 6. I/O and core voltages power-up sequence

3.5 Video Input Interface Specifications

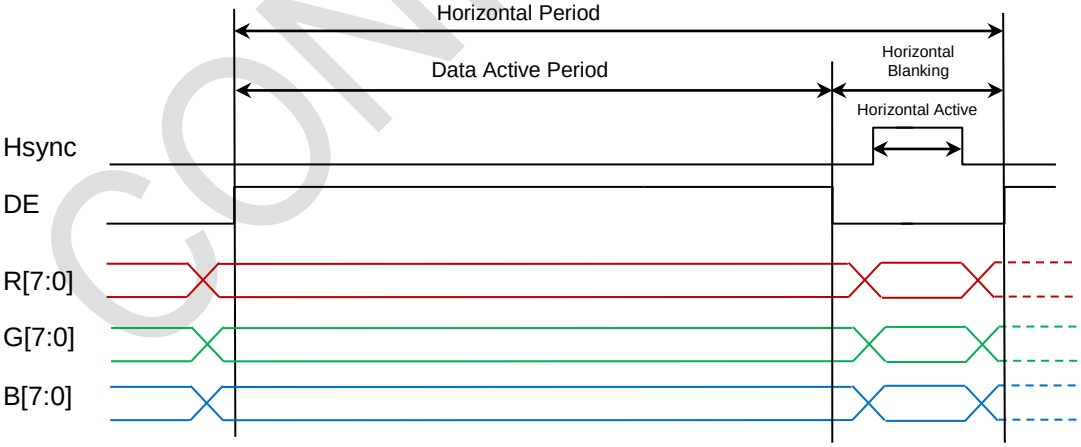


Figure 7. Horizontal Blanking and DE Active Relationship

Symbol	Description	Min	Max	Units
DE	Data Enable Active	320	1920	Cycles
H_B	Horizontal Blanking	30		Cycles

HS_{ACTIVE}	Horizontal Sync Active time	60		ns

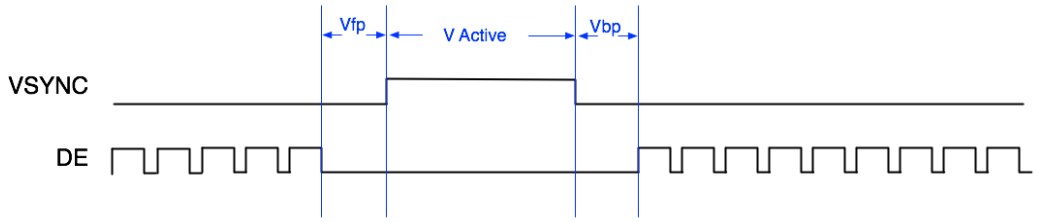


Figure 8. VSYNC and DE Relationship

Symbol	Description	Min	Max	Units
VS_{Active}	Vertical Sync Active	2		Lines
V_{FP}	Vertical Front-Porch	1		Lines
V_{BP}	Vertical Back-Porch	1		Lines
V_{BP} + V_{Active} + V_{FP}	Vertical Blanking	500		µs
VSYNC	Vertical Sync Rate	10*	75*	Hz
PIX_CLK	Pixel Clock	5	148.5	MHz
Data T_S	Data to clock Setup	See below		ps
Data T_H	Clock to data Hold	See below		ps

* Depends on the drive algorithm being used. 9-field capability shown.

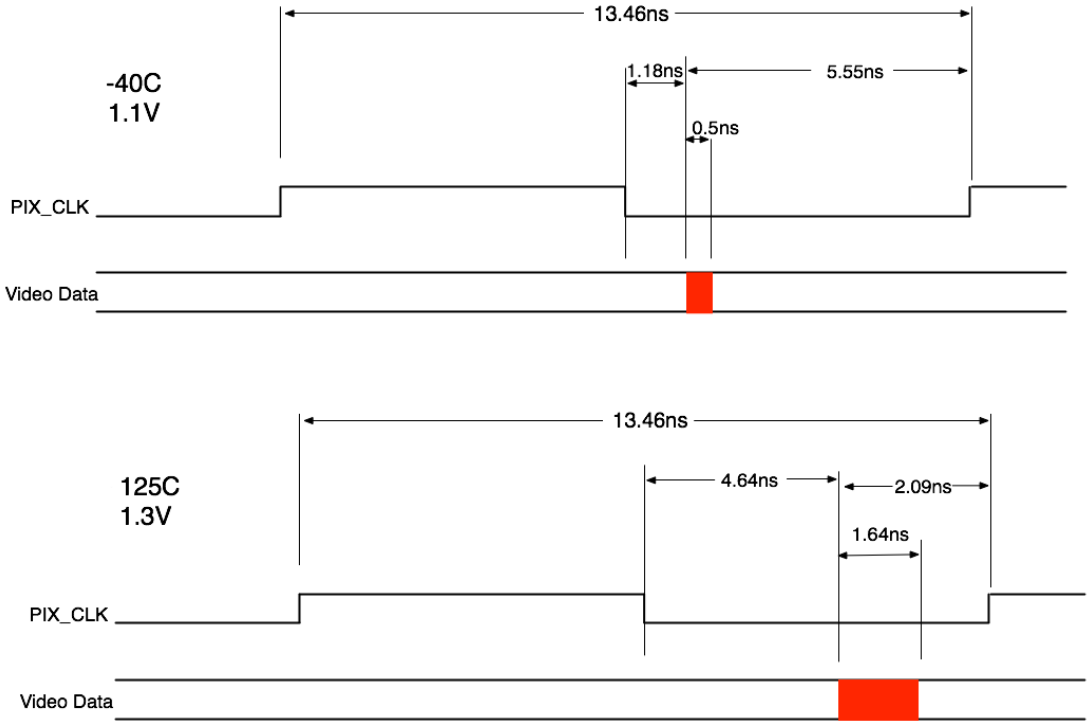


Figure 9. RGB video input timing (For setting 0xEF=0x10)

3.6 Panel Interface Output Timing

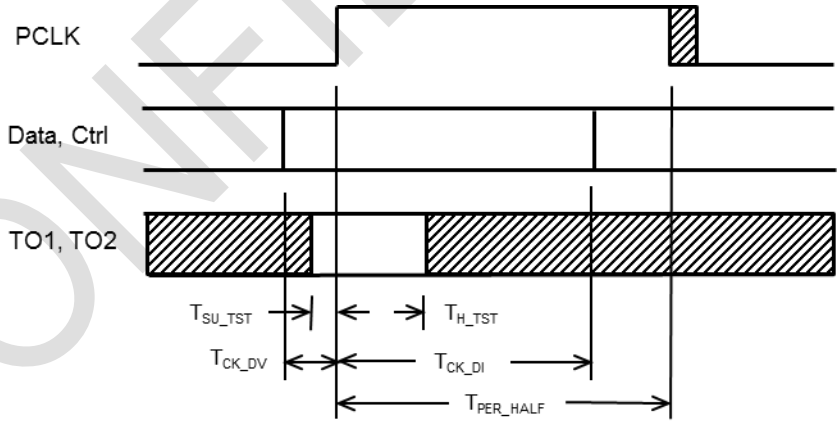


Figure 10. SYA1232 Panel Interface Timings

Symbol	Description	Min	Max	Units
t_{PER_HALF}	Panel clock half-period	3.7		ns
t_{CK_DV}	Clock to data valid	-0.25	-0.92	ns
t_{CK_DI}	Clock to data invalid	2.7		ns
t_{SU_TST}	Test input setup time	0.1		ns
t_{H_TST}	Test input hold time	2.7		ns

4 Package and Signal Definition

4.1 Signal Description

The following tables describe the basic functionality of the pins on the device. For a more complete implementation of these signals, refer to the SYA1232 reference design schematics.

Panel Interface (V_{DD_SSTL} and V_{DD_PIF} reference)

Pin Name	Description	BGA Pos	Type
P_CLK	Output clock sent to display panel.	N5	O
P_CMD	Serial command output to the panel, use for loading the chip control commands into the panel control memory.	K6	O
P_DVLD	Indicate the panel data is valid, this pin will assert for all but the last valid data cycle.	M5	O
P_DATA[31:0]	Formatted video data output to panel	G13,F12,F1, G11,G12,H11, H13,J13,K13, L13,K12,M13, N12,M12,L12, N11,M11,L10, M10,N10,M9, N9,K8,L8,M8, N8,L7,N7,M7, N6,M6,L6	O
TESTOUT1	This signal is tied to TO1 from the LCOS panel for receiving controller feedback from the panel after reset.	A5	I
TESTOUT2	This signal is tied to TO2 from the LCOS panel for receiving controller feedback from the panel after reset.	B5	I
VREF_SSTL	Reference input voltage to the controller's SSTL18 output driver. (not used) Connect to GND	L11	I

Video Input (V_{DD_VIN} reference, weak internal pull-ups)

Pin Name	Description	BGA Pos	Type
PIXEL_CLK	Pixel clock input.	F1	I
VSYNC	Vertical SYNC delineates the start of the video input frame.	G1	I
HSYNC	Horizontal SYNC delineates the start of each video input line within the frame.	H1	I
DE	Data enable. When asserted, indicates RGB inputs contains valid data.	J1	I
FIELD/I2C_SEL	Field control This pin provides the I2C slave address information to the ASIC at reset. The information is captured only when the system reset signal is asserted during power on reset. 1 = I2C slave address is 0xEE (1110 111x b) 0 = I2C slave address is 0xCE (1100 111x b) This pin must be pulled up or pulled down with respect to V_{DD_I2C} using an external 20K Ω resistor to indicate the appropriate state.	H2	I

Pin Name	Description	BGA Pos	Type
G[7:0]/ Y[7:0]	Video Input Channel 1. Default mapping sets the following: RGB input mode: Green data Component input mode: Luminance component	A4, C5, B4, C4, A3, B3 ,C3, B2	I
R[7:0]/ Cr[7:0]	Video Input Channel 2. Default mapping sets the following: RGB input mode: Red data Component input mode: Red component (Cr)	C2, A2, B1, C1, E1, E2, G2, F2	I
B[7:0]/ Cb[7:0]	Video Input Channel 3. Default mapping sets the following: RGB input mode: Blue data Component input mode: Blue component (Cb)	L1, K1, K3, K2, L3, M2, L2, K4	I
D[3:0]_DN D[3:0]_DP	MIPI/LVDS video differential inputs, lanes 3 to 0.	A8,A9,A11,A12 B8,B9,B11,B12	I
CL_DN CL_DP	MIPI differential input clock	A10 B10	I
RBIAS	External reference compensation resistor – 2Kohms 1% to ground	B13	

Illumination Interface (V_{DD_LED} reference, weak internal pull-downs)

Pin Name	Description	BGA Pos	Type
R_EN	Red illumination control. When High, illumination source is on. Tie to GND using an external pull-down resistor of ~100 kΩ.	M1	O
G_EN	Green illumination control. When High, illumination source is on. Tie to GND using an external pull-down resistor of ~100 kΩ.	N2	O
B_EN	Blue illumination control. When High, illumination source is on. Tie to GND using an external pull-down resistor of ~100 kΩ.	N3	O

General Purpose I/O Interface (V_{DD_GPIO} reference, weak internal pull-downs)

Pin Name	Description	BGA Pos	Type
SCL	I2C slave clock input	L5	I/O
SDA	I2C slave data input and output	L4	I/O
SCK	SPI clock output as master	B6	O
SCS_N/SPI_EN	SPI chip select output , active low This pin provides the system SPI Flash memory information to the ASIC. The information is captured only when the system reset signal is asserted during power on reset. 1 = SPI Flash present in the system 0 = no SPI Flash present in the system This pin must be pulled up or pulled down with respect to V_{DD_SPI} using an external 20K Ω resistor to indicate the appropriate state.	D6	O
SDO	SPI serial output data	A6	O
SDI	SPI serial input	D7	I
GPIO[7:0]	General purpose input and output, user configurable. Power up default as static input.	E11, E12, F13, E13, D12, D13, C12, C13	I/O
JTAG_EN	JTAG debug mode enable pin. (Not used) Connect to GND	N4	I
TEST_EN	Test debug mode enable pin. (Not used) Connect to GND	C6	I
TX	RS232 transmit pin. (Not used) N/C	M4	O
RX	RS232 receive pin. (Not used) Connect to GND	M3	I

System/Clock Interface (V_{DD_XTAL} reference)

Pin Name	Description	BGA Pos	Type

Pin Name	Description	BGA Pos	Type
RESET_N	System reset input. Active low. When asserted low , will reset the entire SYA1232. RST_N has to be asserted for at least 5 msec after power is stable. (Has a weak internal pull-up)	C11	I
SYS_CLK/ XIN	Input reference clock from 25 MHz external oscillator or the crystal from the system PCB. This is the reference clock for the internal PLL	D2	I
XOUT	Crystal oscillator output reflecting the input frequency. Leave as NC when using an external oscillator.	D1	O

Power and Ground

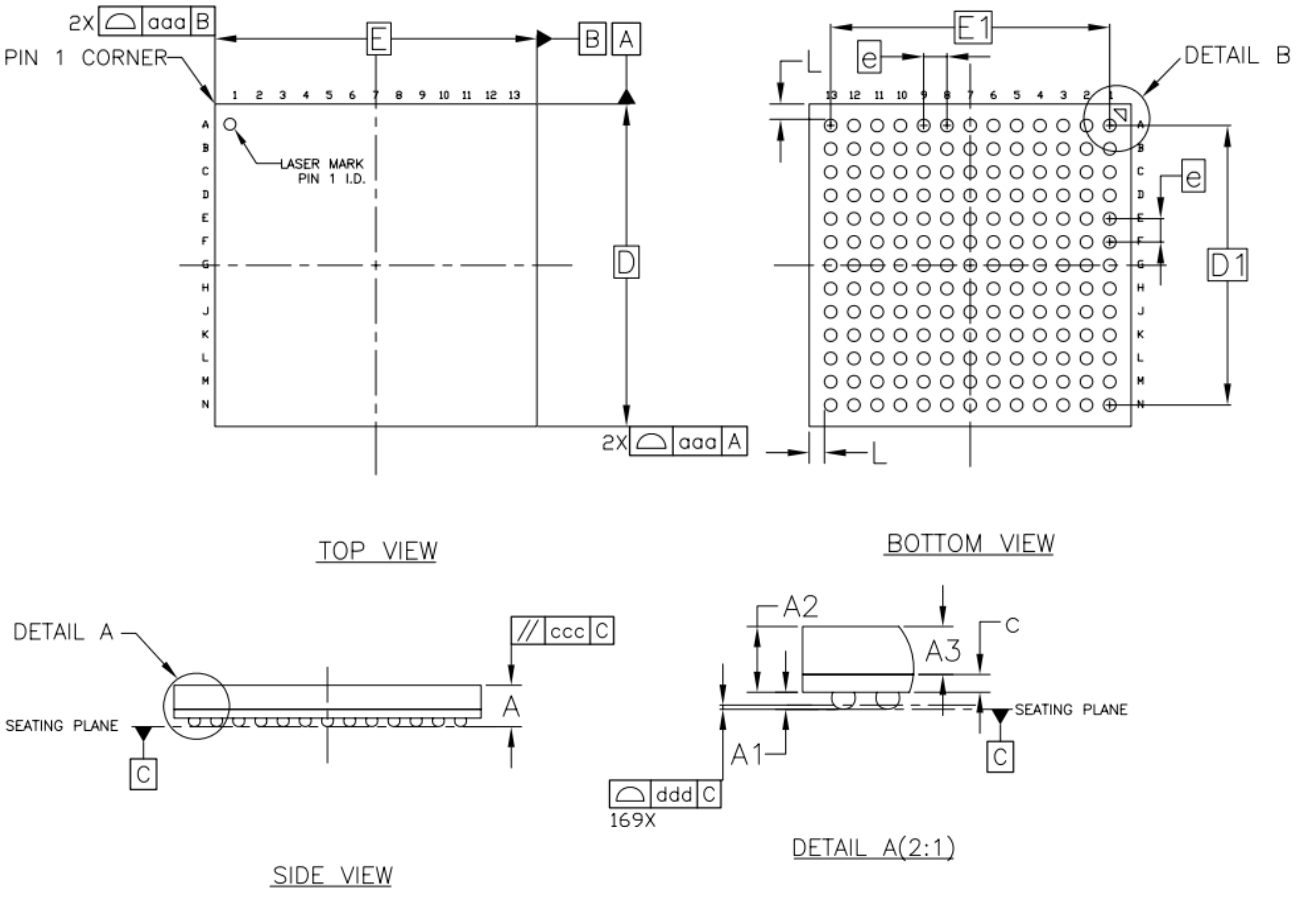
Pin Name	Description	BGA Pos	Type
VDD	1.1V (Nominal) core Power supply	F5,G5,H5,J5, F6,F7,F8,J6,J7, J8,E10,F10, G10,H10	DPWR
VDD_PIF	1.2/3.3/1.8V (Nominal) SSTL output driver Power supply	D4	DPWR
VDD_SSTL	1.2/3.3/1.8V (Nominal) SSTL output driver Power supply	J9,J10,J11,K9, K10,K11,	DPWR
VDD_FUSE	Connect to GND	H3	DGND
VDD_XTAL	1.8/2.5/3.3V (nominal) Crystal/Osicllator Power supply	E3	DPWR
VSS_XTAL	GND for Crystal	D3	
VDD_GPIO	1.8/2.5/3.3V (Nominal) GPIO Power supply	E6	DPWR
VDD_SPI	1.8/3.3V (Nominal) SPI Power supply	D5	DPWR
VDD_I2C	1.8/3.3V (Nominal) I2C Power supply	G3	DPWR
VDD_VID	1.8/3.3V (Nominal) Video IN Power supply (user option)	E4,F4	DPWR
VDD_LED	1.8/3.3V (Nominal) LED Enable Power supply (user option)	J3	DPWR
VCCA_11	Power supply for analog circuits (1.1V).	C7,C8	APWR
VCCA_18	Power supply for analog circuits (1.8V).	C10	APWR
VCCA_33	Power supply for analog circuits (3.3V).	D10	APWR
VSS	Digital ground	A1,N1,J2,F3,G 4,H4,J4,E5,K5, G6,H6,A7,B7,E 7,G7,H7,K7,E8, G8,H8,E9,F9,G 9,H9,L9,D11,H 12,J12, A13,N13	DGND
VSSA	Analog ground. Tie to GND at one point via a zero ohm resistor or ferrite bead on PCB.	D8,C9,D9	AGND
VREF_SSTL	SSTL Buffer reference input. Connect to ground	L11	DGND

4.2 Package Mechanical Dimensions

Table 1: SYA1232 Package Mechanical Dimension

Dimension		Value	Unit
P-TFBGA169 Package		9.0 X 9.0	mm
Pin Count (13 rows x 13 columns)		169	balls
Ball Pitch		0.65	mm
Ball Diameter		0.30 to 0.40	mm
Ball Attachment Pad Size on package		0.40 +/- 0.05	mm
Package Height, without balls		0.96	mm
Package Height, post-solder (estimate)		1.29	mm
PCB Recommended Routing Guidelines: (individual designs may vary)			
BGA pad size (diameter)		0.325 – 0.40	mm
Mechanical thru-hole drilled vias:			
Via pad diameter for Signal fan-out (max)		0.350 [1]	mm
Plated Via hole diameter (thru hole)		0.150 [2]	mm
Blind vias: (typically laser drilled)			
Via pad diameter (max)	Outer layer	0.30 – 0.32	mm
	Inner layer	0.25 – 0.30	mm
Laser drill (diameter)		0.10 – 0.15	mm

Notes: 1) 0.40 is possible by offsetting toward the BGA pad
2) 0.20 diameter is possible with a 0.40 pad size



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.29
A1	0.20	0.25	0.30
A2	0.91	0.96	1.01
A3	0.70 BASIC		
c	0.22	0.26	0.30
D	8.90	9.00	9.10
D1	7.80 BASIC		
E	8.90	9.00	9.10
E1	7.80 BASIC		
e	0.65 BASIC		
L	0.425 TYP		
b	0.30	0.35	0.40
aaa	0.10		
ccc	0.15		
ddd	0.10		
eee	0.15		
fff	0.08		

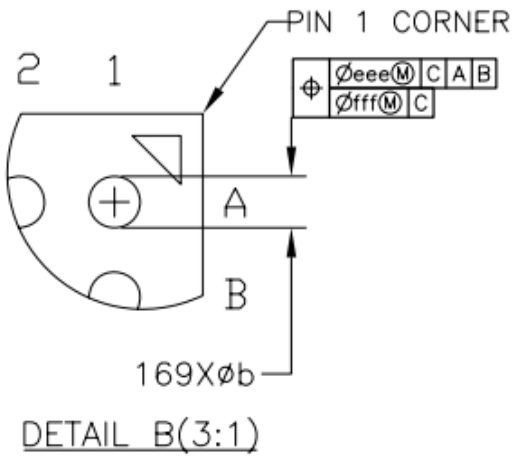
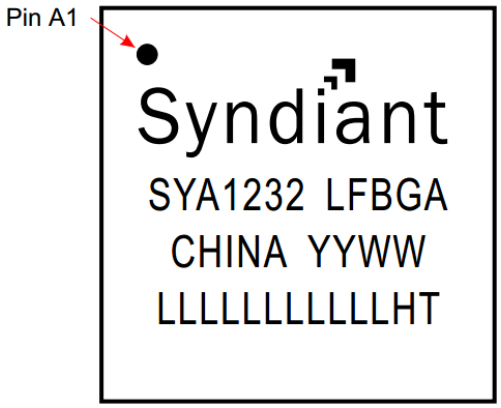


Figure 11. LFBGA169-0909-0.65A5 Package Dimensions

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	VSS	R[6]	G[3]	G[7]	TESTOUT1	SDO	VSS	D3_DN	D2_DN	CL_DN	D1_DN	D0_DN	VSS	A
B	R[5]	G[0]	G[2]	G[5]	TESTOUT2	SCK	VSS	D3_DP	D2_DP	CL_DP	D1_DP	D0_DP	RBIAS	B
C	R[4]	R[7]	G[1]	G[4]	G[6]	TEST_EN	VCCA_11	VCCA_11	VSSA	VCCA_18	RESET_N	GPIO[1]	GPIO[0]	C
D	XOUT	SYS_CLK/ XIN	VSS_XTAL	VDD_PIF	VDD_SPI	SCS_N/ SPI_EN	SDI	VSSA	VSSA	VCCA_33	VSS	GPIO[3]	GPIO[2]	D
E	R[3]	R[2]	VDD_XTAL	VDD_VID	VSS	VDD_GPIO	VSS	VSS	VSS	VDD	GPIO[7]	GPIO[6]	GPIO[4]	E
F	PIXEL_CLK	R[0]	VSS	VDD_VID	VDD	VDD	VDD	VDD	VSS	VDD	P_DATA[29]	P_DATA[30]	GPIO[5]	F
G	VSYNC	R[1]	VDD_I2C	VSS	VDD	VSS	VSS	VSS	VSS	VDD	P_DATA[28]	P_DATA[27]	P_DATA[31]	G
H	HSYNC	FIELD/ I2C_SEL	VDD_EFUSE	VSS	VDD	VSS	VSS	VSS	VSS	VDD	P_DATA[26]	VSS	P_DATA[25]	H
J	DE	VSS	VDD_LED	VSS	VDD	VDD	VDD	VDD	VDD_SSTL	VDD_SSTL	VDD_SSTL	VSS	P_DATA[24]	J
K	B[6]	B[4]	B[5]	B[0]	VSS	P_CMD	VSS	P_DATA[9]	VDD_SSTL	VDD_SSTL	VDD_SSTL	P_DATA[21]	P_DATA[23]	K
L	B[7]	B[1]	B[3]	SDA	SCL	P_DATA[0]	P_DATA[5]	P_DATA[8]	VSS	P_DATA[14]	VREF_SSTL	P_DATA[17]	P_DATA[22]	L
M	R_EN	B[2]	RX	TX	P_DVLD	P_DATA[1]	P_DATA[3]	P_DATA[7]	P_DATA[11]	P_DATA[13]	P_DATA[15]	P_DATA[18]	P_DATA[20]	M
N	VSS	G_EN	B_EN	JTAG_EN	P_CLK	P_DATA[2]	P_DATA[4]	P_DATA[6]	P_DATA[10]	P_DATA[12]	P_DATA[16]	P_DATA[19]	VSS	N
	1	2	3	4	5	6	7	8	9	10	11	12	13	

Panel Signals
Video IN
Analog PWR/GND
MIPI/LVDS

Figure 12: TFBGA-169 Pin Assignment; SYA1232 (top view)



4.3 Assembly Recommendations

The Pb-free reflow profile recommendations are listed in Table 2 and illustrated in

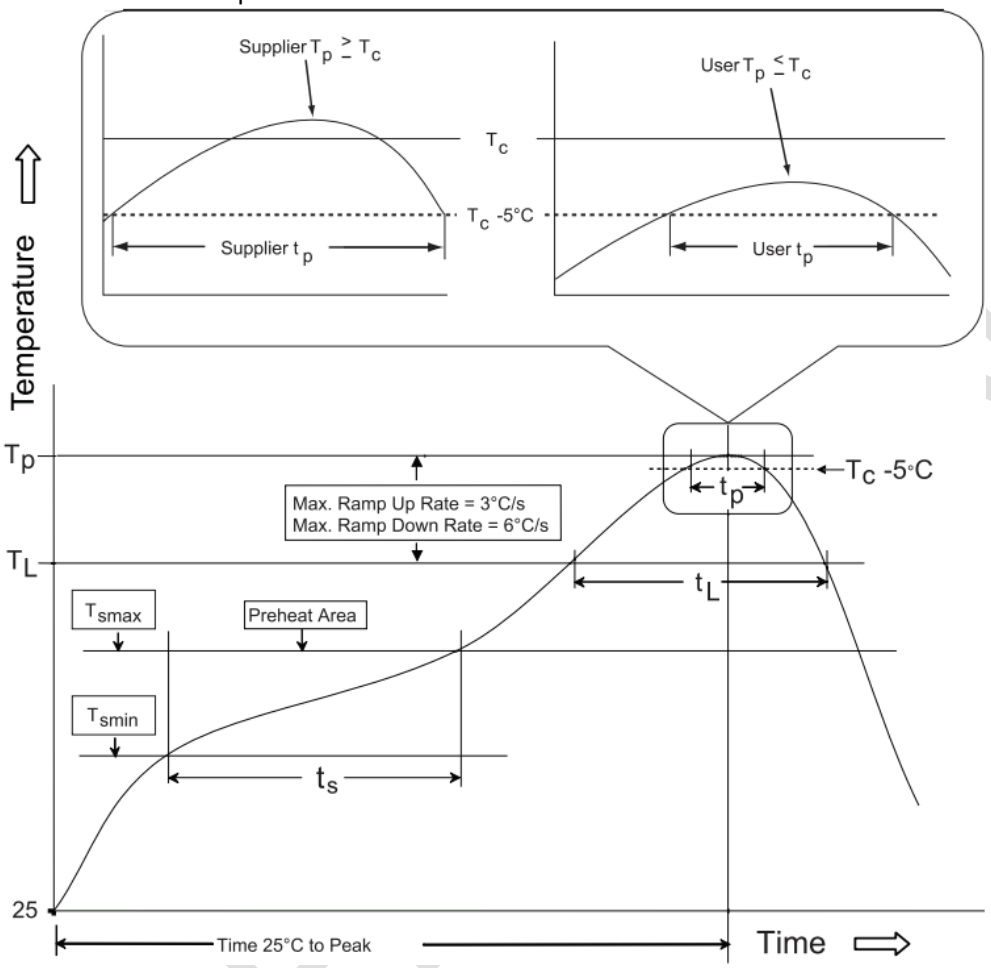


Figure 13 and Figure 14. All temperatures refer to the topside of the package, measured on the package body surface.

Table 2: Pb-Free Reflow Profile Recommendation (IPC/JEDEC J-STD-020 D.1)

Reflow Parameter	Pb-Free Assembly
Minimum preheat temperature (Ts_{MIN})	150°C
Maximum preheat temperature (Ts_{MAX})	200°C
Preheat time	60–180 seconds
Ts_{MAX} to T_L ramp-up rate	3°C/second maximum
Time above temperature T_L (t_L)	217°C, 60–150 seconds
Peak Temperature (T_P)	260°C
Time 25°C to T_P	6-minute maximum
Time within 5° of Peak T_P	30 seconds
Ramp-down rate	6°C/second maximum

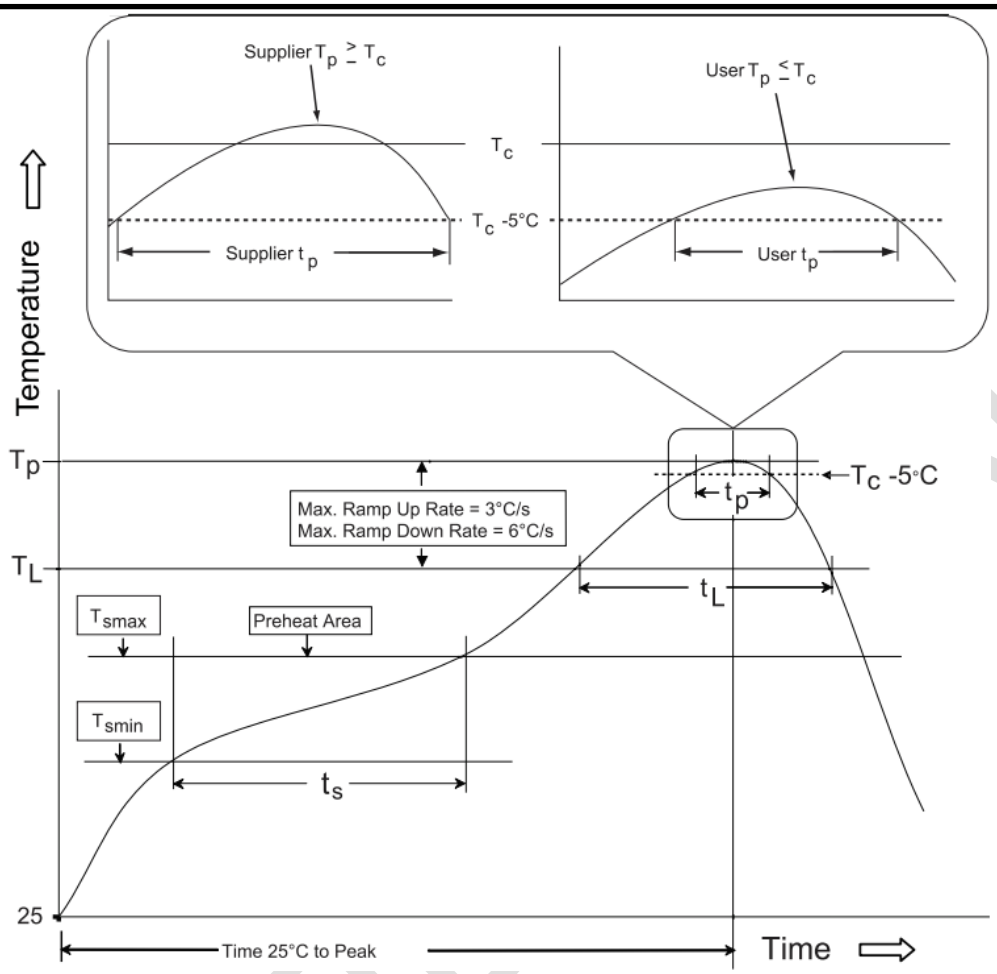


Figure 13. IR/Convection Reflow Profile (IPC/JEDEC J-STD-020 D.1)

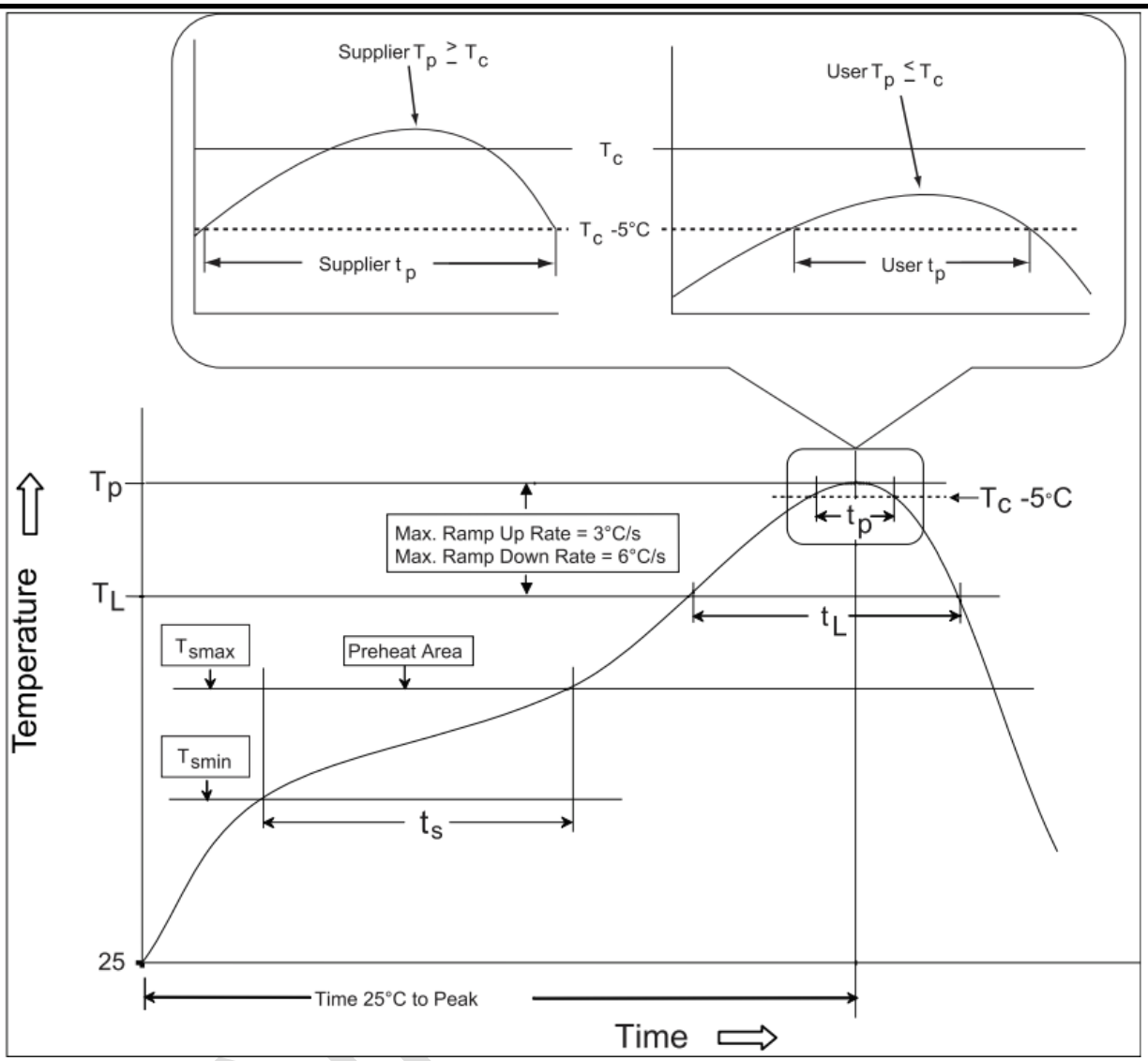


Figure 14. IR/Convection Reflow Profile (IPC/JEDEC J-STD-020 D.1) – Cont.

5 Part Ordering Information

The following table describes components that can be ordered from Syndiant related to this product:

	Ordering Part #	Description
SYA1232 Device Part Number:		
	22-1232-00	SYA1232 LCOS Controller
Compatible Development Kits:		
	71-2209-01	SYL2281 Basic Development Kit
	71-2209-02	SYL2281 Development Kit with LED Projector Optical Engine
	71-2210-01	SYL2282 Basic Development Kit
	71-2210-02	SYL2282 Development Kit with LED Projector Optical Engine

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