ISAAC iTools Documentation

Jason Zheng, Yutao He

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The following tools are discussed in this document:

- Mathworks Matlab (Matlab Design Entry/Verification)
- Xilinx AccelDSP (HDL Design Entry)
- Mentor Graphics Modelsim (HDL Verification)
- Xilinx ISE (Logic Synthesis/Place-n-Route)

3 Setting up Tools

3.1 Matlab

Matlab is a powerful modeling tools used by many engineers at JPL. JPL currently has 200 shared licenses for the main tool, and numerous licenses for different tool-boxes. Matlab can be installed on Windows PC, Mac OS/X, GNU/Linux, and Solaris platforms. Matlab is also a prerequisite for AccelDSP. Since AccelDSP currently supports Windows PC platform only, a Windows installation of the Matlab is required for AccelDSP. Detailed installation instructions can be found at `http://matlab.jpl.nasa.gov`

3.2 AccelDSP

AccelDSP is a tool developed to help DSP designers to implement DSP designs on FPGA platforms. The AccelDSP helps achieving this goal in the following ways:

- Helps a DSP designer convert a Matlab floating-point design to a fixed-point design with specified quantization parameters.
- Provides a verification platform to compare before- and after-quantization performance. Quantization errors can be discovered early in the design stage and fixed before HDL code is generated.
- Converts a fixed-point Matlab filter design to state-machine-based HDL code. The designer can specify how the loops are rolled and how much resource (multipliers, adders) is shared.
- Creates an HDL test-bench to verify that the HDL design matches that of the Matlab fixed-point design.

AccelDSP provides a useful bridge between the Matlab users and the HDL designers. However, in order to use AccelDSP to its full potential, the designer should be knowledgeable of both Matlab and HDL (either Verilog or VHDL). AccelDSP also has a strict requirement on what type of Matlab designs are acceptable. The requirements are discussed in detail in Section 4.

ISAAC project has acquired 1 full license for AccelDSP. The tools is currently installed on a Windows host (isaacdev3) in the ISAAC lab. Due to the nature of the license, AccelDSP can only be invoked on the hosting machine. There are two ways to do this:

- Use the tool locally in the lab. The AccelDSP tool can be launched by double-clicking on the AccelDSP icon on the Desktop.
- Used the tool remotely via VNC. The machine isaacdev3 has vnc service running in the background, and can be reached on port 5900 of the isaac sub-net. Use of bgr compression is recommended to speed up the VNC session. For example, from an X11 session, type

  ```
  $ vncviewer -bgr isaacdev:5900
  ```

  The vnc daemon will ask for a password. This password can be obtained from the system administrator of ISAAC.

3.3 Modelsim

Modelsim is an HDL simulation tool. In the ISAAC tool flow, Modelsim is used to verify the HDL implementation against the fixed-point Matlab design. JPL has a shared license for Modelsim. This tool can be downloaded from eCAE service and installed on Windows and GNU/Linux environments. To use the JPL floating license, environment variable MGLS_LICENSE_FILE must be set to:

```
2020@dhub-lmgr1,2020@dhub-lmgr2,2020@dhub-lmgr3
```

3.4 ISE

4 AccelDSP Detailed Discussions