

### Progress Report #1

So far, my research work has primarily involved the development and implementation of digital signal processing (DSP) algorithms on ISAAC-based platforms. The ISAAC—Instrument ShAred Artifact for Computing—project aims to provide a “highly capable, highly reusable, modular, and integrated FPGA-based common instrument control and computing platform that can be shared by multiple Earth-Science and planetary-exploration instruments [1].” Essentially, ISAAC allows instrument electronics designers to configure a complete instrument control and computing system by using its integrated framework. The motivation for ISAAC technology is to provide a platform that can be *shared* by a wide range of instruments, introducing a common spacecraft bus interface with on-board processing for systemic missions. ISAAC’s reusable framework offers a combination of “adaptability, computation power, I/O bandwidth, digital interface standards, and data processing capability in a single common low mass/power and small form factor platform with significantly reduced non-recurring cost and risk to Earth Science instruments [2]”. As future instruments require more demanding on-board processing capabilities, ISAAC will allow new instrumentation developments to meet performance requirements in a cost-efficient manner.

By focusing on sharable components for instruments, ISAAC technology allows JPL to compete in a host of instrument missions in which it was previously unable to compete competitively. Its use has been recommended for a wide range of future NASA/JPL missions, where it will be integral in data acquisition from digital electronics instruments such as GPS, radars, radiometers, interferometers, lasers, spectrometers, altimeters, and more. Although a few ISAAC prototypes have already been explored and developed by Dr. Yutao He and his team, there is still much more comprehensive work to be completed for ISAAC-planned capabilities. My efforts at JPL are working to improve the ISAAC framework and increase functionality for the strategic advancement of instrument development.

My research project involves using the ISAAC framework to perform system architecture exploration and design, algorithm development and simulation, FPGA implementation and testing, and benchmarking and integration. More specifically, I have been working on porting over the QM-FIR digital filter core from the older Virtex4-based system to the newer, more computationally advanced Virtex5-based iBoard. The Virtex5 device is a System-On-Chip FPGA that has flight-qualified parts, meaning it is cosmic radiation-hardened and is capable of operating in the extreme environments of outer space. The QM-FIR IP core is part of the iCore library, which consists of “standard and parameterized IP cores that implement common computationally-intensive instrument control and computing functions [1]”.

This past month, I have become more familiar with the necessary software development tools by first completing a small “tutorial” pulse-width-modulation (PWM) project. The PWM project allowed me to acquire hands-on experience in all aspects of a project, from algorithm-conception to real-time on-board processing. Working on an IP core requires the use of several software tools. First, Verilog HDL code is developed using the *Xilinx ISE* tool and then simulated with *ModelSim*. After the hardware is programmed, the FPGA hardware and software must be configured with the *Xilinx EDK* tool, which also builds C-code software applications. The project can then be downloaded onto the iBoard using *iMPact*, *XMD*, and then tested with the *ChipScope Inserter & Analyzer*. I have also been using *Matlab* and *WireShark* to deal with testing UDP communication over Ethernet.

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After completing the PWM project, I worked with my mentor and a few of the QM-FIR's developers to begin my integrating the old project with the newer hardware/software configuration. I am currently debugging issues with a UDP demo, which involves a Matlab GUI facilitating simulated data-communication between a host-machine and the iBoard. My goals for the next month are to completely port over the QM-FIR project and be able to demonstrate its functionality to my mentor and fellow interns. I will write extensive documentation for future users to comprehend and replicate my project design. I will also team up with another intern to develop a python-based GUI for analyzing the filter's outputs and simulate radar application. Before the month is over, I hope to get started on implementing the digital filter through hardware only—without a processor—and use python scripts to send data over UART. Then I can use a DAC board to implement and verify real-time data on-board processing.

I have encountered a few problems, which have hindered my research progress. My research requires me to work with a personal computer to develop and test the iBoard with oscilloscopes, function generators, power supplies, and various connection interface adapters. During the first week, I spent more time reading documentation because my computer account had not been set up yet. If it had been, I would have been able to get a head start on familiarizing myself with the various software development applications (as there is a steep learning curve). The internal computer network in the lab was sometimes buggy, which lead to restricted computer access and downtime. The lab computers are also slow for synthesizing and implementing a project design, which causes errors and is wasteful in the long run.

The interaction between my mentor and me has been exceptional. We have scheduled weekly “quiet hour” meetings to discuss my progress and approaches to problems, but I see Yutao almost every day in the lab. He is quite busy, but somehow he manages to work closely with his team of six student interns. Every week, the interns meet in a conference room to discuss weekly progress and present our work to each other. This gives us valuable project feedback, and allows us to prepare a presentation for practice. We also eat lunch together every other week, which is enjoyable.

#### References:

- [1] Y. He, C. Le, J. Zheng, K. Nguyen, and D. Bekker, “ISAAC a case of highly-reusable, highly-capable computing and control platform for radar applications,” in *IEEE 2009 Radar Conference*, May 2009.
- [2] K. Nguyen, J. Zheng, Y. He, and B. Shah, “A High-Throughput, Adaptive FFT Architecture for FPGA-Based Space-Borne Data Processors,” 2009.