Register Offset	Register Name	Description	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	ESCR	Error, Status and Control Register	Set/Clr	Spare												OVFL_MSK	WMI_MSK	Spare														OVFL	WMI	SYNC
0x1	WPTR	BRAM Write Pointer	Spare						SPTR[9:0]										Spare						CPTR[9:0]									
0x2	ICNT	Input Counter	ICNT[31:0]																															
0x3	OCNT	Output Counter and Watermark	OCNT_WM[15:0]																OCNT[15:0]															

Register Field	RW	Reset Value	Description
SYNC	RW	0	Write 1 to this bit (with Set bit of 1) re-synchronizes the internal QM and FIR filters, also writes SPTR to CPTR
WMI	RW	0	This bit is automatically asserted whenever OCNT increments to OCNT_WM
OVFL	RW	0	This bit is automatically asserted whenever CPTR overflows
WMI_MSK	RW	0	Asserting this bit disables the WMI interrupt, but WMI status bit would still automatically assert
OVFL_MSK	RW	0	Asserting this bit disables the OVFL interrupt, but OVFL status bit would still automatically assert
CPTR	R	0	This register field indicates the current BRAM write point location
SPTR	RW	0	This register field is used to automatically load CPTR when SYNC is issued
ICNT	RW	0	This register field automatically increments whenever a new input data arrives
OCNT	RW	0	This register field automatically increments whenever a new output data is written to BRAM
OCNT_WM	RW	0	This register field is used as a water-mark for the output counter