National Semiconductor
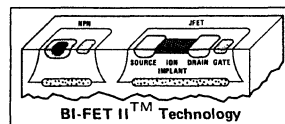
Operational Amplifiers/Buffers

BI-FET II™ Technology

LF412A/LF412 Low Offset, Low Drift Dual JFET Input Operational Amplifier

General Description

These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF412 dual is pin compatible with the LM1558, allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

- Internally trimmed offset voltage — 1 mV (max)
- Input offset voltage drift — 10 μV/°C (max)
- Low input bias current — 50 pA
- Low input noise current — 0.01 pA/$\sqrt{Hz}$
- Wide gain bandwidth — 3 MHz (min)
- High slew rate — 10V/μs (min)
- Low supply current — 1.8 mA/Amplifier
- High input impedance — $10^{12}\Omega$
- Low total harmonic distortion $A_V = 10$, — <0.02%
  $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz–20 kHz
- Low 1/f noise corner — 50 Hz
- Fast settling time to 0.01% — 2 μs

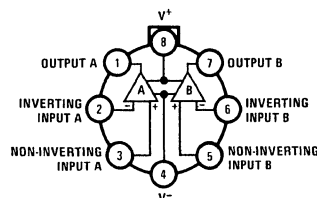## Typical Connection

Simplified Schematic

1/2 Dual
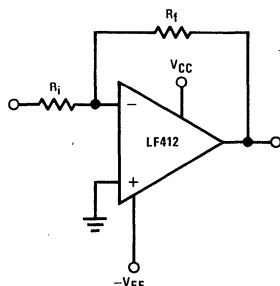
Ordering Information

LF412XYZ

X indicates electrical grade
Y indicates temperature range
  "M" for military
  "C" for commercial
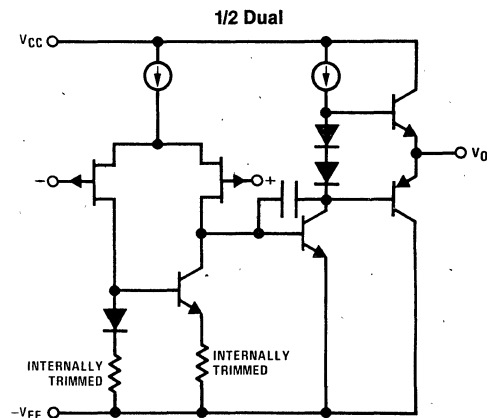Z indicates package type
  "H" or "N"

Connection Diagrams

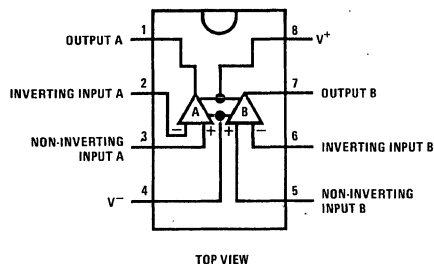**LF412AMH/LF412MH, LF412ACH/LF412CH
Metal Can Package**

Note. Pin 4 connected to case.
TOP VIEW

Order Number LF412AMH, LF412MH,
LF412ACH or LF412CH
See NS Package H08B

**LF412ACN, LF412CN
Dual-In-Line Package**

TOP VIEW

Order Number LF412ACN or LF412CN
See NS Package N08A

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Absolute Maximum Ratings

	LF412A	LF412		H Package	N Package
Supply Voltage	± 22V	± 18V	Power Dissipation (Note 3)	670 mW	500 mW
Differential Input Voltage	± 38V	± 30V	T_j max	150°C	115°C
Input Voltage Range (Note 1)	± 19V	± 15V	θ_{jA}	150°C/W	160°C/W
Output Short Circuit Duration (Note 2)	Continuous	Continuous	Operating Temperature Range	(Note 4)	(Note 4)
			Storage Temperature Range	$-65°C \leq T_A \leq 150°C$	$-65°C \leq T_A \leq 150°C$
			Lead Temperature (Soldering, 10 seconds)	300°C	300°C

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions		LF412A			LF412		Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10\,k\Omega$, $T_A = 25°C$			0.5	1.0		1.0	3.0	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\,k\Omega$ (Note 6)			7	10		7	20 (Note 6)	$\mu V/°C$
I_{OS}	Input Offset Current	$V_S = \pm 15V$ (Notes 5 and 7)	$T_j = 25°C$		25	100		25	100	pA
			$T_j = 70°C$			2			2	nA
			$T_j = 125°C$			25			25	nA
I_B	Input Bias Current	$V_S = \pm 15V$ (Notes 5 and 7)	$T_j = 25°C$		50	200		50	200	pA
			$T_j = 70°C$			4			4	nA
			$T_j = 125°C$			50			50	nA
R_{IN}	Input Resistance	$T_j = 25°C$			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 2k$, $T_A = 25°C$		50	200		25	200		V/mV
		Over Temperature		25	200		15	200		V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k$		± 12	± 13.5		± 12	± 13.5		V
V_{CM}	Input Common-Mode Voltage Range			± 16	+ 19.5		± 11	+ 14.5		V
					− 16.5			− 11.5		V
CMRR	Common-Mode Rejection Ratio	$R_S \leq 10k$		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 8)		80	100		70	100		dB
I_S	Supply Current				3.6	5.6		3.6	6.8	mA

AC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	LF412A			LF412			Units
			Min	Typ	Max	Min	Typ	Max	
	Amplifier to Amplifier Coupling	$T_A = 25°C$, f = 1 Hz–20 kHz (Input Referred)		− 120			− 120		dB
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$	10	15		8	15		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$	3	4		2.7	4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1 kHz		25			25		nV/$\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_A = 25°C$, f = 1 kHz		0.01			0.01		pA/$\sqrt{Hz}$

Notes

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 4: These devices are available in both the commercial temperature range $0°C \leq T_A \leq 70°C$ and the military temperature range $-55°C \leq T_A \leq 125°C$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.
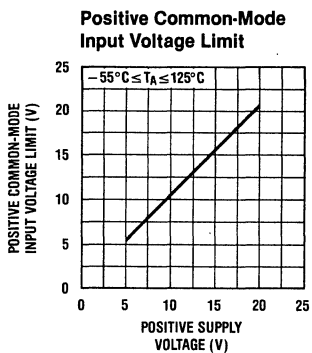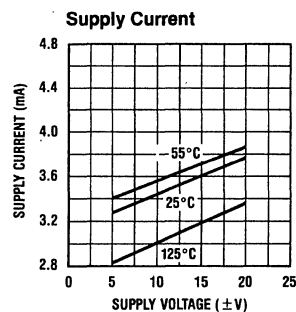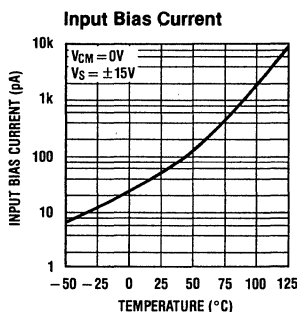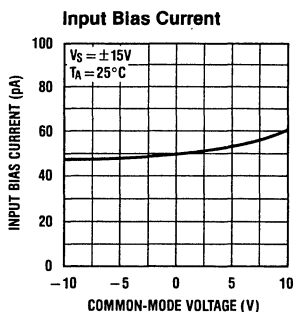
Note 5: Unless otherwise specified, the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF412A and for $V_S = \pm 15V$ for the LF412. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

Note 6: The LF412A is 100% tested to this specification. The LF412 is sample tested on a per amplifier basis to insure at least 90% of the amplifiers meet this specification.

Note 7: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
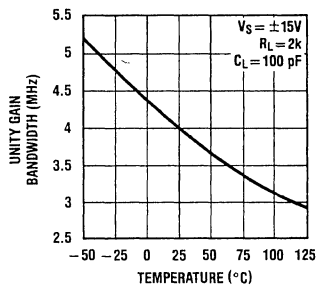
Note 8: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.
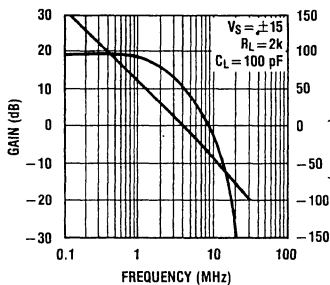
Typical Performance Characteristics

Input Bias Current

Input Bias Current

Supply Current

Positive Common-Mode Input Voltage Limit

Negative Common-Mode Input Voltage Limit

Positive Current Limit

Negative Current Limit

Output Voltage Swing

Output Voltage Swing
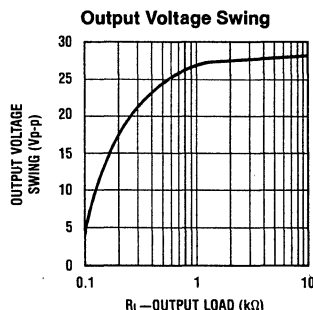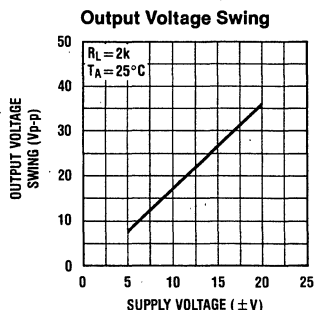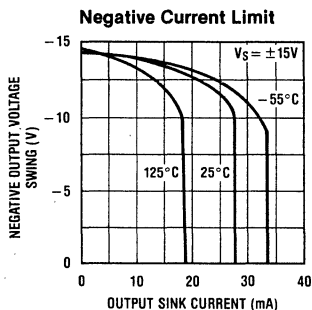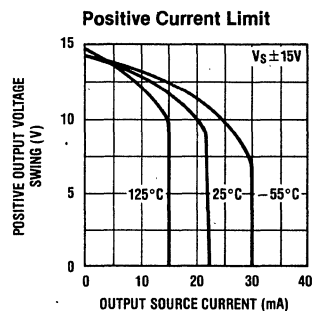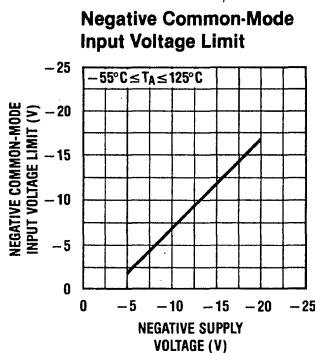
Typical Performance Characteristics (Continued)
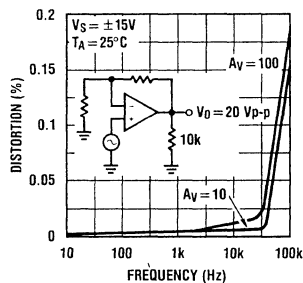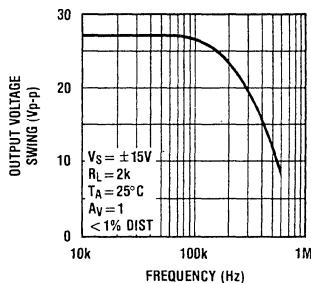
Gain Bandwidth
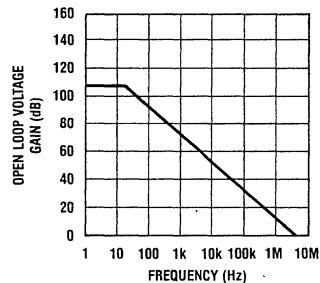
Bode Plot

Slew Rate
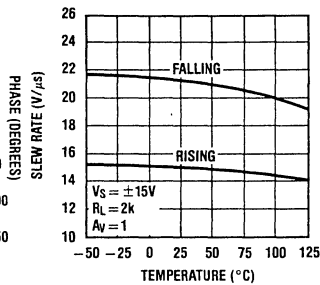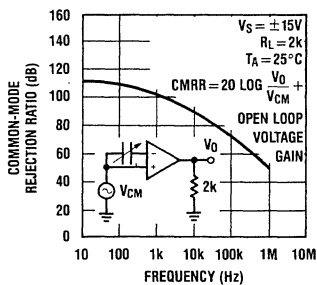
Distortion vs Frequency

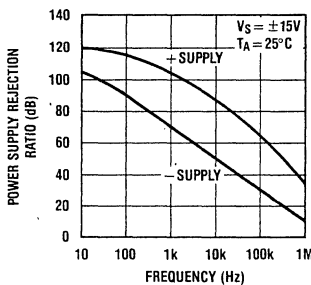### Undistorted Output Voltage Swing

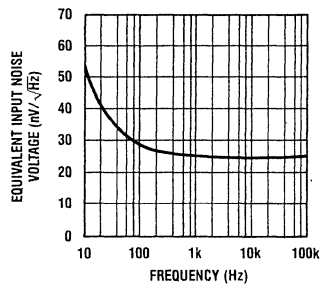### Open Loop Frequency Response
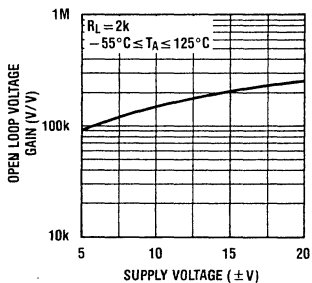
Common-Mode Rejection Ratio
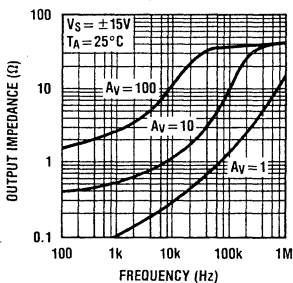
Power Supply Rejection Ratio
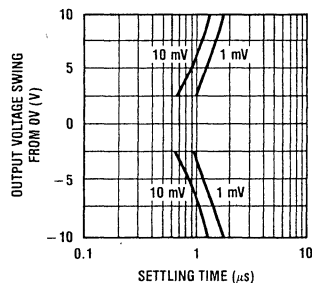
Equivalent Input Noise Voltage

Open Loop Voltage Gain

Output Impedance

Inverter Settling Time

Pulse Response $R_L = 2 k\Omega$, $C_L = 10 pF$
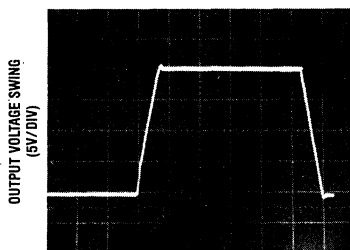
Small Signal Inverting

OUTPUT VOLTAGE SWING (50 mV/DIV)
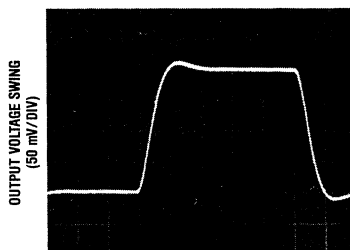
TIME (0.2 μs/DIV)

Small Signal Non-Inverting

OUTPUT VOLTAGE SWING (50 mV/DIV)
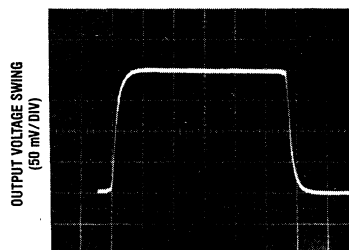
TIME (0.2 μs/DIV)

Large Signal Inverting

OUTPUT VOLTAGE SWING (5V/DIV)

TIME (2 μs/DIV)

Large Signal Non-Inverting

OUTPUT VOLTAGE SWING (5V/DIV)
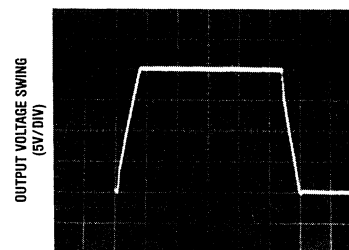
TIME (2 μs/DIV)

Current Limit ($R_L = 100\Omega$)

OUTPUT VOLTAGE SWING (1V/DIV)
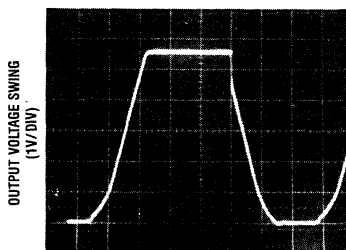
TIME (5 μs/DIV)

Application Hints

The LF412 series of JFET input dual op amps are internally trimmed (BI-FET II™) providing very low input offset voltages and guaranteed input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output, however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Application Hints (Continued)

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.
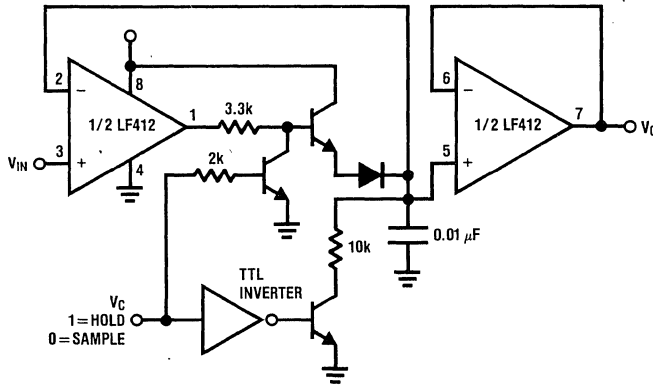
As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the fre-

quency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Application

Single Supply Sample and Hold

Detailed Schematic