How the bi-FET process benefits linear circuits

Op amps that combine bipolar and field-effect transistors on the same chip outperform purely bipolar chips at little extra cost

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☐ The new kid on the block in linear technology is the bi-FET process. Monolithic operational amplifiers built with this mixed process provide broader bandwidth, faster slewing, and higher input impedance than do standard bipolar devices, yet they are selling at only a slight cost premium.

Bi-FET is an appropriate acronym for these linear circuits, which combine bipolar transistors with junction field-effect transistors on one and the same silicon chip. A number of semiconductor manufacturers are already producing bi-FET integrated circuits in standard linear configurations besides op amps: analog switches, instrumentation amps, and even sample-and-hold circuits.

Emerging only a few years ago, bi-FET technology today accounts for about 5% of the total linear IC business. Moreover, the industrial market for linears is expected to double by 1980 and most of this increase should be in bi-FET products. Thus major semiconductor manufacturers are getting on the bandwagon and are turning their attention to innovations in this area.

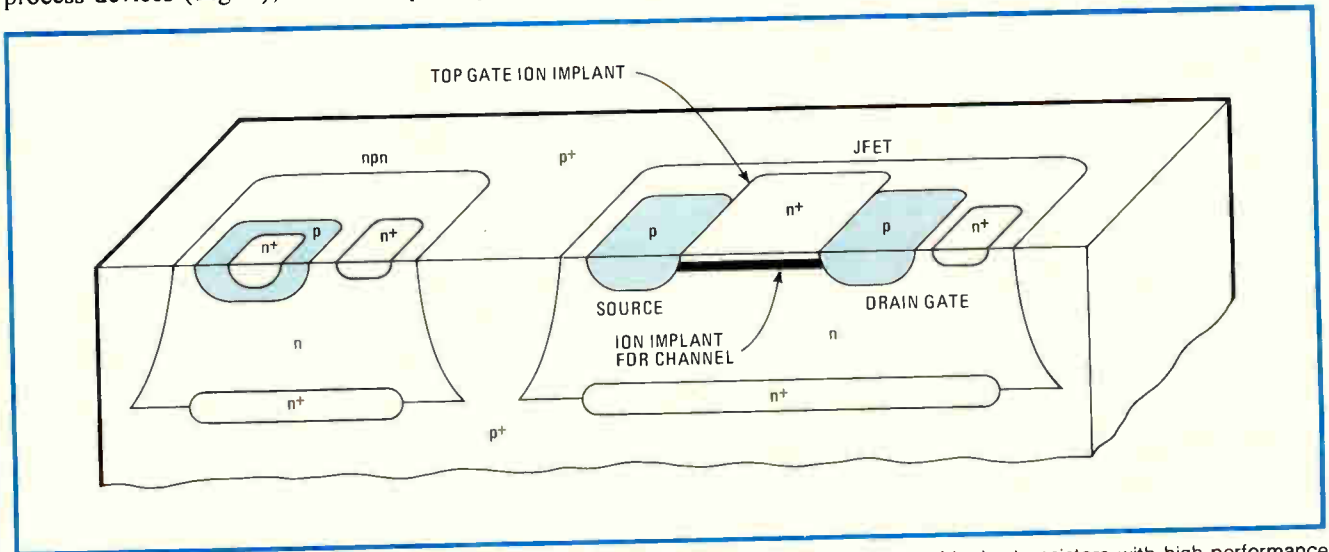
Bi-FET vs bipolar

Ion implantation makes the difference between bi-FET and standard bipolar linear processing. In the mixed-process devices (Fig. 1), one ion implant produces the p channel between the source and drain contacts, which are standard bipolar p-type gate base diffusions. A second implant produces the n-type gate region overlying this channel. The pinch-off voltage of a junction FET is roughly proportional to the total amount of dopant there is in the channel.

With diffusion processes, pinch-off voltage is very hard to control, and matching these voltages in two JFETs is nearly impossible. But implanting the channel virtually permits counting the number of dopant ions for a predictable channel Q, so that control over absolute pinch-off voltage and JFET matching are easily achieved. Besides minimum pinch-off voltage, low-concentration channel implants provide high JFET breakdown voltages.

In many linear circuits, the very low dc input bias current the JFET offers is, by itself, a tremendous advantage over strictly bipolar devices. Another benefit of these transistors—an even more important one in some applications—is the roughly order-of-magnitude improvement in frequency response.

Moreover, in op-amp circuits, slew rate may be improved by a factor of 20, even with no increase in bandwidth. The slew rate of a standard monolithic frequency-compensated op amp is proportional to the ratio of the quiescent bias current to the transconduc-



1. Basic structure. Because of ion implantation, bi-FET circuits can combine high-performance bipolar transistors with high-performance matched JFETs. One implant creates the p channel between source and drain contacts, another the gate region over this channel.

Mixed-process linears: a perspective

Since the first practical devices appeared some three years ago, mixed-process linears have steadily gained ground on their all-bipolar counterparts. These bi-FET and bi-MOS chips are clearly here to stay. About a dozen semiconductor manufacturers are now using the mixed technology for a variety of standard linear circuit functions, and the list is growing. Besides numerous operational amplifiers, the circuit functions include analog multiplexers, comparators, sample-and-hold circuits, analog switches, instrumentation amplifiers, and even the analog portions of data-converter chip sets.

Mixed-process devices combine field-effect transistors with bipolar transistors on the same silicon chip. The FETs most often are front-end devices, the bipolars are in the output stage. A bi-FET device mixes bipolars with p-channel junction FETs, whereas a bi-MOS device combines metal-oxide-silicon FETs with bipolars, a mixture that may even involve complementary MOSFETs.

In terms of input bias current, bandwidth, and slew rate, bi-FET and bi-MOS op amps perform nearly equally. However, bi-FET parts exhibit better noise characteristics and less offset-voltage drift. Bi-MOS devices, on the other hand, can handle inputs over the full range of the supply voltage, so they offer broad common-mode voltage capability. The chips are also processed differently. Bi-FET devices involve an ion-implant add-on, while bi-MOS parts are products of diffusion, requiring an extra masking step.

Because of the performance edge bi-FET technology offers, far more semiconductor manufacturers are making bi-FET chips. In alphabetical order, these vendors include: Advanced Micro Devices, Fairchild, Intersil, Motorola, National Semiconductor, Precision Monolithics, Signetics, Texas Instruments, and the latest entry by Analog Devices. Among the manufacturers of bi-MOS devices are RCA Corp., Harris Semiconductor, Siliconix, and again TI.

For the last year or so, the competition in bi-FET op amps centering on price versus performance has been vigorous. For example, last August, National and TI drastically slashed prices on their amplifier products, so that there is now only a difference of pennies between an economy bi-FET op amp and the industry standard bipolar op amp, the 741. As compared to the 741, which sells for 20 to 25 cents in quantity, TI offers its TL081 devices for 33 cents and National is asking 39 cents for its LF351 units. Moreover, National's higher-performance LF356 part is down to 75 cents, from its initial $2 plus.

But the standard versions of these op amps have fairly high input offset voltage, in the range of 10 to 15 millivolts, although both National and TI do offer selected versions with offset down to 2 or 3 mV. In contrast, besides second-sourcing a better-performing LF356, PMI is making an improved second-generation of bi-FET op amps, designated the OP-15, -16, and -17. These devices boast an input offset voltage of 500 microvolts maximum, and their input bias current is compensated for changes in temperature. Of course, the user pays a premium for these features, but as a result, instead of doubling for every 10°C rise in temperature, as is the usual case with JFETs, the bias current of the PMI chips doubles only approximately every 18°C. (Both National and TI have indicated they will also be making 0.5-mV-offset parts in the near future.)

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tance of the input stages. So the key to obtaining high slew rate is to use first-stage gain elements that have a large ratio of biasing current to transconductance. Compared with bipolar transistors, JFETs require a larger biasing current to obtain the same transconductance, making them the better choice for the input stage.

The monolithic op amp

Unquestionably, standard monolithic bipolar op amps have proliferated through the years, and there now are a relatively large number of different devices available. The reason for this proliferation is the continuing introduction of circuit innovations to correct one or two operational deficiencies at a time. From the first successful monolithic op amp—the 709 (Fig. 2a) and its improved version, the newer popular 741 frequency-compensated unit—bipolar designs have used lateral pnp transistors to solve dc level-shifting problems. Since these transistors are relatively low-frequency devices, they limit overall frequency response. Still, bipolar npn transistors can be biased for good frequency response, but then the input current becomes undesirably large.

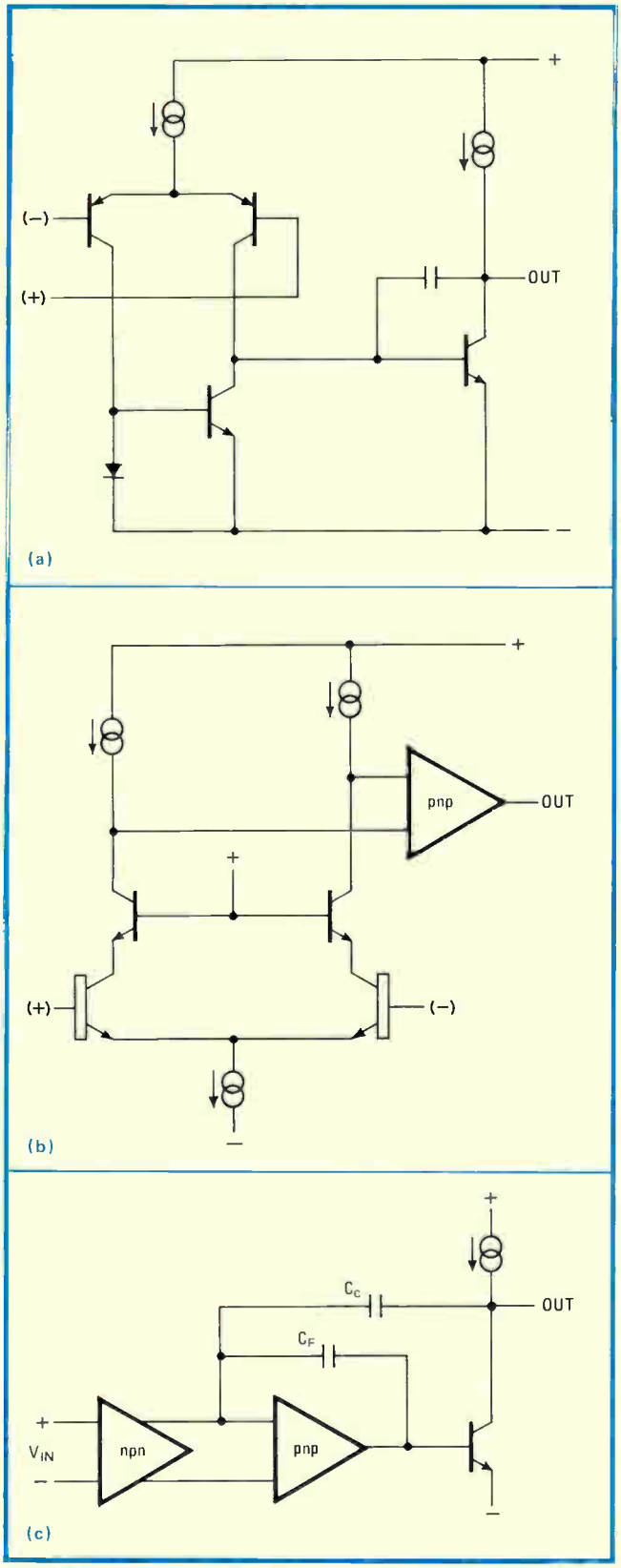
To improve input characteristics, semiconductor makers turned to super-beta npn transistors to come up with the 108-type op amp (Fig. 2b). Although these transistors have low breakdown voltage, they provide a beta as high as 10,000. Therefore, for a small sacrifice in additional circuit complexity to keep off high voltages, these devices are able to serve as excellent input transistors. Unfortunately, though, the lateral pnp transistors are still necessary, so that the speed of the op amp remains essentially unchanged.

The next improvement came with a circuit technique called feedforward, which results in the improved bandwidth and slew rate of the 118-type op amp (Fig. 2c). The idea is to feed the signal around the slow-responding pnp stage. Although this development significantly improves bandwidth, settling time and input bias current are relatively unaffected.

No matter what circuit tricks were tried, only a few parameters at a time could be improved. What was really needed was a high-speed replacement for the lateral pnp transistor, one that did not sacrifice breakdown voltage. The bi-FET process gives just such an active device. What results is an op amp that delivers excellent dc and ac characteristics while offering fast settling and low noise specifications.

The first bi-FET design

The basic design (Fig. 3) of the first viable bi-FET op amp, the LF-356, consists of a differential JFET input stage, followed by a differential bipolar stage for symmetrical bias-current loading. The input transistors are biased at less than I_{DDS} (the zero-bias drain current) to prevent excessive increases in input current should the differential input voltage become large. If a JFET's drain current increases beyond I_{DDS}, the gate-source junction of that device will actually become forward-biased.



2. Evolution. Monolithic bipolar op amps have proliferated because of the evolution of circuit innovations. For example, the 709 (a) incorporates lateral pnp transistors to solve dc level-shifting problems, the 108 (b) has superbeta npn transistors for better input characteristics, and the 118 (c) uses a feedforward technique to improve bandwidth and slew rate.

To simplify biasing in a standard bipolar op amp, a current mirror makes the conversion from a differential to a single-ended stage at the output of the first stage. But this approach does not work with a JFET differential input stage. Such a bipolar current mirror would yield much too large an input offset voltage when the JFET was biased for maximum slew rate. The low transconductance of this transistor actually causes the input to exceed the offset voltage of the mirror.

The biasing solution for a JFET front end is a different circuit approach. For similar biasing, well-matched JFETs also provide well-matched drain currents, so they are useful as current-source loads. A simple gate-source short provides two-terminal current source loads, with the matching depending only on the JFETs. Such diode-connected transistors act as the loads for the input stage, and a common-mode feedback loop biases the sources of the differential input stage. With JFETs, the same device type may be used for both the gain element and its current-source load—something that is out of the question with bipolars.

The common-mode feedback loop optimizes performance for both dc and ac operations. At dc, the 10-picofarad compensation capacitor looks like an open circuit, and the feedback to the sources of the input JFETs is common-mode. For ac inputs, the compensation capacitor will absorb the output current of the first stage. Since there is no place for ac to be absorbed at the other differential output, the common-mode loop must constrain this output current at zero. As a result, the entire differential input voltage is impressed across the gate-source terminals of the noninverting input JFET. This yields gain-doubling, differential-to-single-ended conversion for ac inputs.

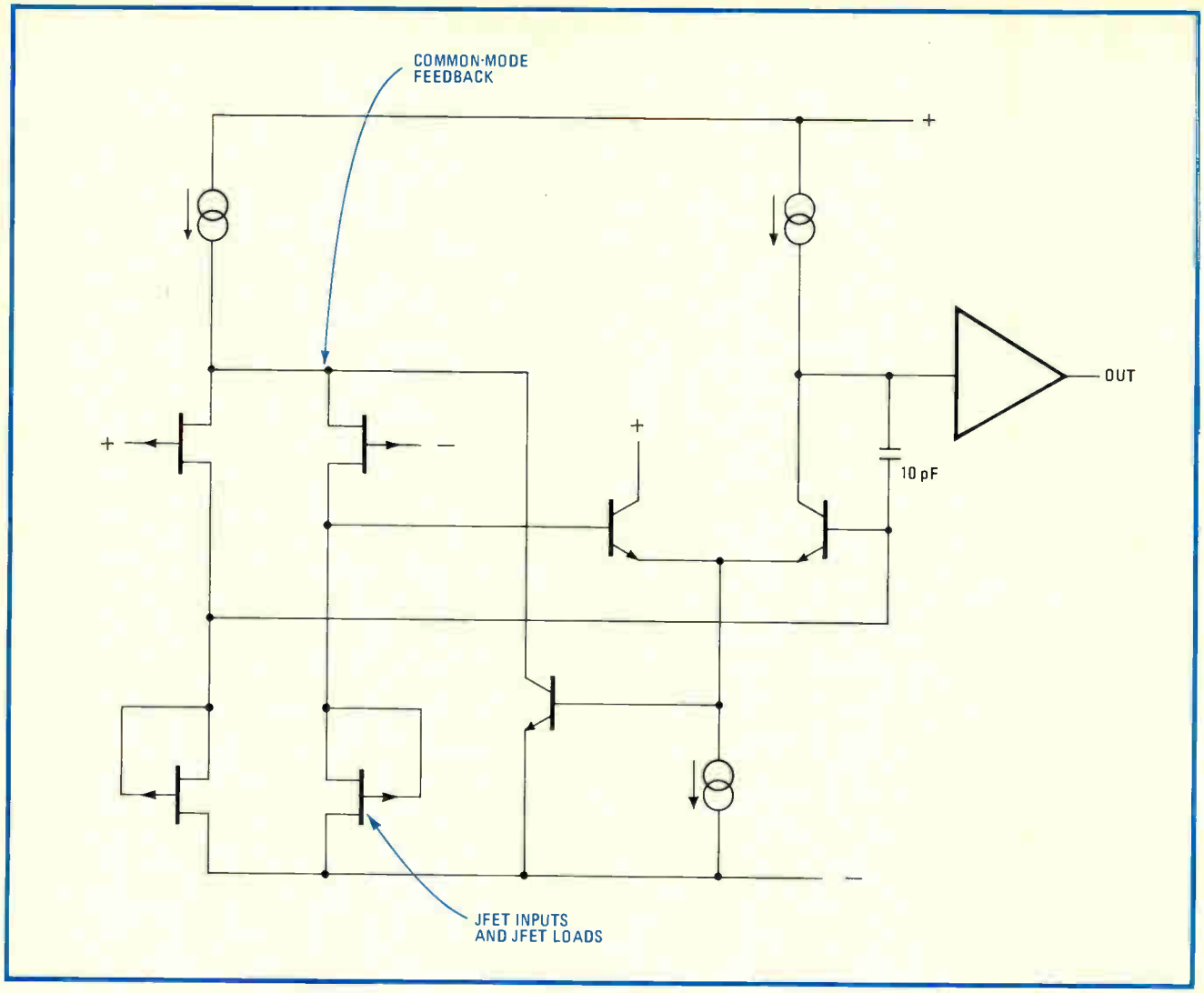
Enhanced stability

To make the stability of the op amp insensitive to large capacitive loads, even up to 10,000 pF, the LF356 contains a wideband composite JFET in its output stage. Many users say they are not driving capacitive loads since they are not working with peak detectors or sample-and-hold circuits. But they may be asking the op amp to drive 50 feet of coaxial cable. At 29 pF per foot, even only a few feet of low-impedance coaxial cable will affect the stability of many op amps.

Another less obvious benefit of the LF356 is its scheme for adjusting input offset voltage. In general, zeroing the input offset voltage of conventional bipolar op amps requires adjusting an external potentiometer. This device shunts the on-chip resistors in the emitters of the current mirror in the first stage. The result of this adjustment is a mismatch in the resistor temperature coefficients, so offset drift is increased. In addition, the signal path is affected, and both gain and common-mode rejection may also be degraded.

The LF356's offset-adjust circuits overcome these problems by using differential JFET currents to modify the dc biasing only. Typically, this technique permits holding offset drift to 0.5 microvolt/°C per millivolt of offset adjustment. The performance of many op amps, monolithic and hybrid, is an order of magnitude worse.

Since the same active devices that contribute to offset



3. High-performance bi-FET. The basic design for the front end of the first bi-FET op amp, the LF356, consists of a differential JFET input stage. A pair of matched JFETs make up this stage, followed by a differential bipolar stage for symmetrical bias-current loading.

voltage also contribute to noise voltage, an input stage designed for low offset voltage tends to produce low noise voltage as well. In the bi-FET op amp, the major contributors to noise voltage are the input JFETs and their JFET current-source loads. The equivalent noise resistance of these devices varies inversely with transconductance. Consequently, it is fortunate that the first-stage transconductance must be high for it to be possible to use a large enough value for the compensation capacitor to obtain effective pole-splitting. Minimizing the input currents of the second stage keeps the 1/f noise corner low, without degrading the frequency performance of the output stage.

A low-cost approach

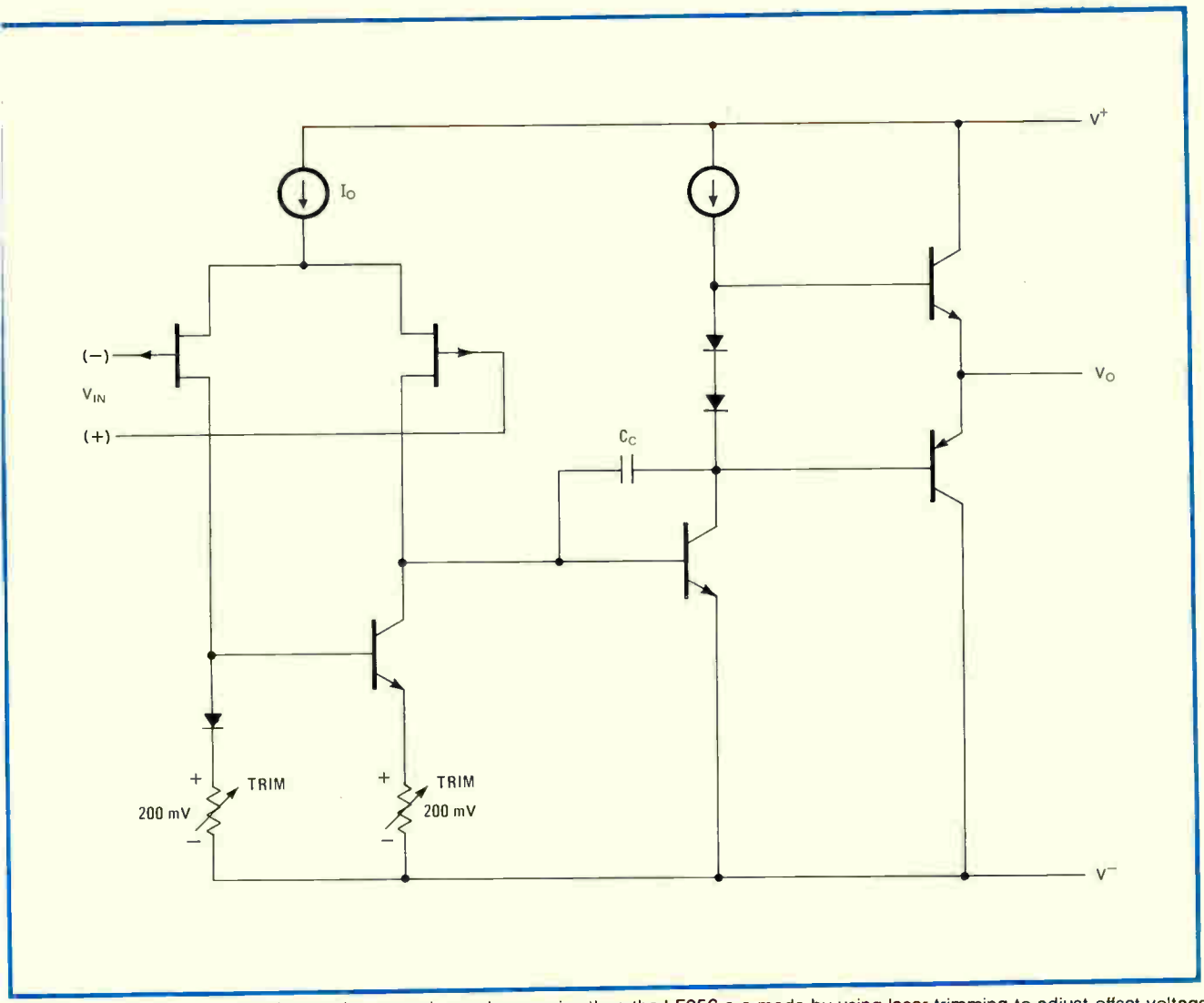
Bi-FET op amps may also be fabricated as less complex, smaller circuits not optimized to achieve low offset voltage. The trick in this case is to use area-consuming JFETs only in the first stage and then to adjust offset by laser-trimming the chip.

One offset-trim method involves opening up metal links across binary-weighted portions of the resistors in the emitters of the current mirror. A larger quiescent voltage is developed across these mirror resistors—by roughly an order of magnitude larger than in a 741 bipolar op amp. As a result, the offset and noise voltage contributions of the bipolar devices in the current mirror are no larger than those of the input JFETs.

What's inside

Figure 4 shows the basic circuitry for a typical low-cost trimmed bi-FET op amp like the LF351 single, LF353 dual, and the LF347 quad devices. When they are run off a constant bias current, their input JFETs have a transconductance that is independent of pinch-off voltage. To keep the bandwidth of the op amp independent of variations in the characteristics of the JFETs, the input bias current is set by a zener voltage and a resistor. Thus, despite their comparatively simple design, these trimmed bi-FET op amps provide large bandwidth, low current drain, short settling time, fast slewing, and the low input bias currents of JFETs.

Because of their broad bandwidth, bi-FET op amps make excellent building blocks for active filters. The



4. Low cost. Bi-FET op amps that are less complex and expensive than the LF356 are made by using laser trimming to adjust offset voltage right on the chip, instead of optimizing the design for low offset as with the LF356. A zener and a resistor set the input bias current.

active-component sensitivities of these filters are inversely proportional to the gain-bandwidth product of the op amps with which they are built. Broadband bi-FET devices, therefore, permit higher frequency operation and higher Q, as well as reduced sensitivities. Further, for low-frequency filters, the benefits of employing smaller-valued capacitors may be realized by impedance scaling, without creating dc voltage-biasing problems.

In data acquisition, an obvious application for a bi-FET op amp is as the output amplifier for a current-output digital-to-analog converter, thereby taking advantage of these devices' fast settling time and dc accuracy.

Another use

A less obvious d-a converter application for a fast-settling op amp is as the driver that keeps the bases of the reference current-source transistors properly biased. As the bits switch, any glitches that occur are coupled back to the output of this driver. The time required by the driver to recover from these abrupt disturbances can limit the settling time of the complete converter.

Moreover, the low cost of trimmed bi-FET devices, brings the advantage of JFET-input amplifiers to inexpensive systems. For example, the large power bandwidth and low noise of these chips make them ideally suited for use in audio applications as RIAA equalization preamps, tone controls, and room equalizers. In addition, even large input voltage swings can be handled with low distortion because of the low transconductance of the JFET input stage. Such performance is especially useful at high frequencies where the reduced open-loop gain of the op amp forces input signals to be larger.

Just a beginning

Undoubtedly, the advent of bi-FET technology is breathing new life into the linear IC world. It gives the circuit designer another tool, providing him with high-performance devices that sell for only slightly more than comparable bipolar parts. The best news of all is that the benefits of bi-FET technology are just the beginning. In the near future, further process innovations and new circuit designs will mean bi-FET op amps with significantly wider bandwidths, higher slew rates, and lower noise voltages. □