CA3140, CA3140A, CA3140B Types Preliminary Data

MOS Operational Amplifiers With MOS/FET Input

The CA3140B, CA3140A, and CA3140 are integrated-circuit operational amplifiers that combine the advantages of high-voltage PMOS transistors with high-voltage bipolar transistors on a single monolithic chip. Because of this unique combination of technologies, this device can now provide designers, for the first time, with the special performance features of the CA3130 COS/MOS Operational Amplifier and the simplicity of the 741 series of industry-standard operational amplifiers.

The CA3140B, CA3140A, and CA3140 PMOS/bipolar operational amplifiers feature gate-protected MOS/FET (PMOS) transistors in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The CA3140B operates at supply voltages, ranging from 4 to 44 volts; the CA3140 and CA3140A, from 4 to 36 volts. These operational amplifiers are internally phase-compensated to achieve stable operation in unity-gain follower operation, and, additionally, have access terminals for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset-voltage nulling.

The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute for single-supply applications. The output stage uses bipolar transistors and includes built-in protection against damage from load-terminal short-circuiting to either supply-rail.

The CA3140 Series have the 8-lead terminal configuration used for the "741" and other industry-standard operational amplifiers. They are supplied in either the standard 8-lead TO-5 style package (T suffix), or in the 8-lead dual-in-line formed-lead TO-5 style package "DIL-CAN" (S suffix). The CA3140B is intended for operation at supply voltages ranging from 4 to 44 volts, and for applications requiring premium-grade specifications and with electrical limits established for operation over the range from −55°C to +125°C. The CA3140A and CA3140 are for operation at supply voltages up to 36 volts (± 18 volts).

The CA3140 and CA3140A can also be operated safely over the temperature range from −55°C to +125°C without malfunctioning, although specification limits for their electrical parameters do not apply when they are operated beyond their specified temperature ranges.

Features:

- MOS/FET Input Stage provides:
  - a) Very high input impedance (Z_{IN}) — 1.5 TΩ typ.
  - b) Very low input current (I_I) — 10 pA typ. at ± 15 V
  - c) Low input offset voltage (V_{IO}) — to 2 mV max.
  - d) Wide common-mode input voltage range (V_{ICR}) — can be swung 0.5 volt below negative rail
  - e) output swing complements input common mode
- Directly replaces industry type 741 in most applications
- Operation from 4-to-44 volts single or dual supplies
- Internally compensated
- Characterized for + 5 volts TTL supply systems with operation down to 4 volts
- Wide bandwidth — 4.5 MHz unity gain at ± 15 V or 30 V; 3.7 MHz at + 5 V
- High slew rate — 9 Volts/μs
- Fast settling time — 1.4 μs typ. to 10 mV with a 10 V p-p signal
- Output swings to within 0.2 volt of negative supply
- Strobable output stage

Applications:

- Ground-referenced single-supply amplifiers in automobile and portable instrumentation
- Sample and hold amplifiers
- Long-duration timers/multivibrators (microseconds — minutes — hours)
- Photocurrent instrumentation
- Peak detectors
- Active filters
- Comparators
- Interface in 5 V TTL systems & other low-supply voltage systems
- All standard operational amplifier applications
- Tone controls
- Function generators
- Power supplies
- Portable instruments
- Intrusion alarm systems

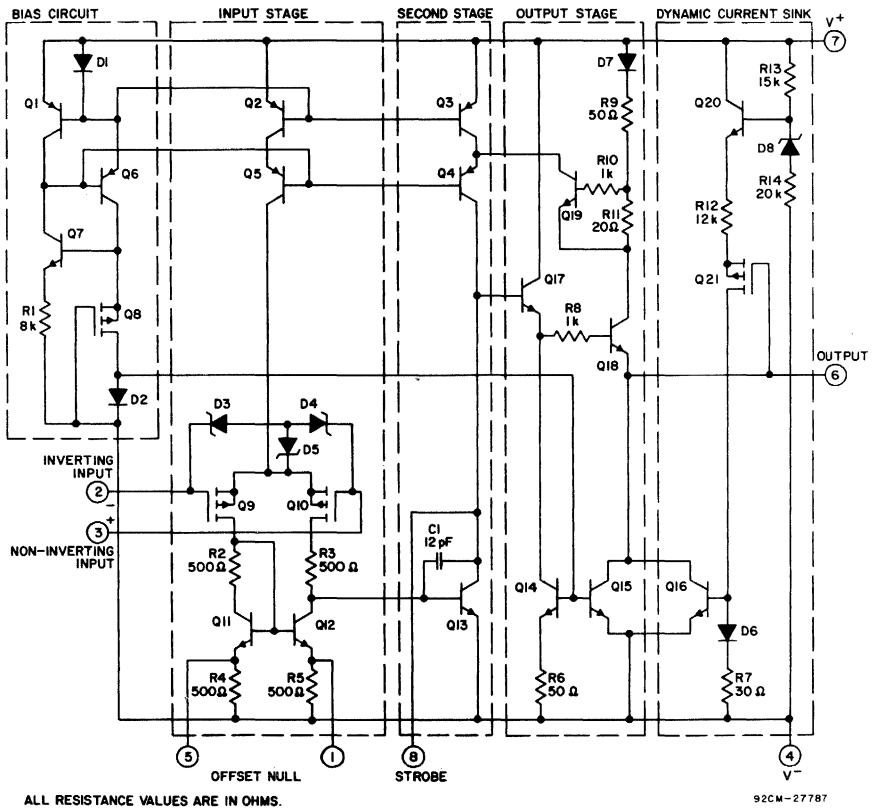

Fig. 1—Schematic diagram of CA3140 series.

CA3140, CA3140A, CA3140B Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

	CA3140, CA3140A	CA3140B
DC SUPPLY VOLTAGE (BETWEEN V^+ AND V^- TERMINALS)	36 V	44 V
DIFFERENTIAL-MODE INPUT VOLTAGE	±8 V	±8 V
COMMON-MODE DC INPUT VOLTAGE	(V^+ +8 V) to (V^- −0.5 V)	
INPUT-TERMINAL CURRENT	1 mA	
DEVICE DISSIPATION:		
WITHOUT HEAT SINK —		
Up to 55°C	630 mW	
Above 55°C	Derate linearly 6.67 mW/°C	
WITH HEAT SINK —		
At 125°C	418 mW	
Below 125°C	Derate linearly 16.7 mW/°C	
TEMPERATURE RANGE:		
OPERATING	−55 to + 125°C	
STORAGE	−65 to + 150°C	
OUTPUT SHORT-CIRCUIT DURATION*	INDEFINITE	
LEAD TEMPERATURE (DURING SOLDERING):		
AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM) FROM CASE FOR 10 SECONDS MAX.	+265°C	

* Short circuit may be applied to ground or to either supply.

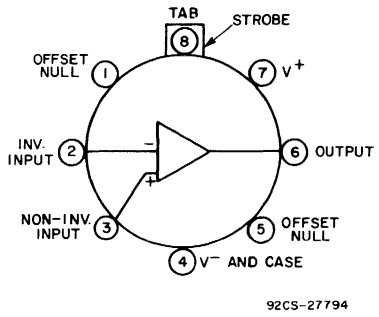

Fig. 2—Functional diagram of the CA3140 series.

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

Characteristic	Test Conditions (V^+ = 15 V, V^- = 15 V, T_A = 25°C (Unless Specified Otherwise)	CA3140B			CA3140A			CA3140			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, V_{IO}		–	0.8	2	–	2	5	–	8	15	mV
Input Offset Current, I_{IO}		–	0.5	10	–	0.5	20	–	0.5	30	pA
Input Current, I_I		–	10	30	–	10	40	–	10	50	pA
Large-Signal Voltage Gain, A_{OL}	V_O=26 V_{p-p}, +12V, −14V, R_L=2 kΩ	50k	100k	–	20k	100k	–	20k	100k	–	V/V
		94	100	–	86	100	–	86	100	–	dB
Common-Mode Rejection Ratio, CMRR		–	20	50	–	32	320	–	32	320	μV/V
		86	94	–	70	90	–	70	90	–	dB
Common-Mode Input Voltage Range, V_{ICR}		−15	−15.5 to 12.5	1.2	−15	−15.5 to 12.5	12	−15	−15.5 to 12.5	11	V
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^+$		–	32	100	–	100	150	–	100	320	μV/V
		80	90	–	76	80	–	76	80	–	dB
Maximum Output Voltage V_{OM}^+	R_L = 2 kΩ	+12	+12.5	–	+12	+12.5	–	+12	+12.5	–	V
Maximum Output Voltage V_{OM}^-	R_L = 2 kΩ	−14	−14.4	–	−14	−14.4	–	−14	−14.4	–	V
Supply Current, I^+		–	4	5.5	–	4	5.5	–	4	5.5	mA
Device Dissipation, P_D		–	120	165	–	120	165	–	120	165	mW
Input Current, I_I	T_A = −55 to +125°C, $V^\pm$ = ±15 V, V_O = 26 V_{p-p}, R_L = 2 kΩ	–	10	30	–	10	–	–	10	–	nA
Input Offset Voltage, V_{IO}		–	1.3	3	–	3	–	–	10	–	mV
Large-Signal Voltage Gain, A_{OL}		20k	100k	–	–	100k	–	–	100k	–	V/V
		86	100	–	–	100	–	–	100	–	dB
Maximum Output Voltage V_{OM}^+	$V^\pm$=±22V	+19	19.5	–	–	–	–	–	–	–	V
Maximum Output Voltage V_{OM}^-		−21	−21.4	–	–	–	–	–	–	–	V
Large Signal Voltage Gain, A_{OL}	R_L=2kΩ, V_O=+19V, −21V	20k	50k	–	–	–	–	–	–	–	V/V
		86	94	–	–	–	–	–	–	–	dB

CA3140, CA3140A, CA3140B Types

CIRCUIT DESCRIPTION

Fig.3 is a block diagram of the CA3140 Series PMOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail. Two class A amplifier stages provide the voltage gain, and a unique class AB amplifier stage provides the current gain necessary to drive low-impedance loads.

A biasing circuit provides control of cascoded constant-current flow circuits in the first and second stages. The CA3140 includes an on-chip phase-compensated capacitor that is sufficient for the unity gain voltage-follower configuration.

Input Stages – The functional circuit diagram of the CA3140 is shown in Fig.2. It consists of a differential-input stage using PMOS field-effect transistors (Q9,Q10) working into a mirror-pair of bipolar transistors (Q11, Q12) functioning as load resistors together with resistors R2 through R5. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base-current drive to the second-stage bipolar transistor (Q13). Offset nulling, when desired, can be effected with a 10-kΩ potentiometer connected across terminals 1 and 5 and with its slider arm connected to terminal 4. Cascode-connected bipolar transistors Q2, Q5 are the constant-current source for the input stage. The base-biasing circuit for the constant-current source is described subsequently. The small diodes D3, D4, D5 provide gate-oxide protection against high-voltage transients, e.g., static electricity.

Second-Stage – Most of the voltage gain in the CA3140 is provided by the second amplifier stage, consisting of bipolar transistor Q13 and its cascode-connected load resistance provided by bipolar transistors Q3, Q4. On-chip phase compensation, sufficient for a majority of the applications is provided by C1. Additional Miller-Effect compensation (roll-off) can be accomplished when desired, by simply connecting a small capacitor between terminals 1 and 8. Terminal 8 is also used to strobe the output stage into quiescence. When terminal 8 is tied to the negative supply rail (terminal 4) by mechanical or electrical means, the output terminal 6 swings low, i.e., approximately to terminal 4 potential.

Output Stage – The CA3140 Series circuits employ a broadband output stage that can sink loads to the negative supply to complement the PMOS input stage. Quiescent current in the emitter-follower cascade circuit (Q17, Q18) is established by transistors (Q15, Q16) whose base-currents are "mirrored" to current flowing through diode D2 in the bias circuit section. When the CA3140 is operating such that output terminal 6 is sourcing current, transistor Q18 functions as an emitter-follower to source current from the V+ bus (terminal 7), via D7, R9, and R11. Under these conditions, the collector potential of Q13 is sufficiently high to permit the necessary flow of base current to emitter follower Q17 which, in turn, drives Q18.

When the CA3140 is operating such that output terminal 6 is sinking current to the V– bus, transistor Q16 is the current-sinking element. Transistor Q16 is mirror-connected to D6, R7, with current fed by way of Q21, R12, and Q20. Transistor Q20, in turn, is biased by current-flow through R13, zener D8, and R14. The dynamic current-sink circuit is controlled by voltage-level sensing. For purposes of explanation, it is assumed that output terminal 6 is quiescently established at the potential mid-point between the V+ and V– supply rails. When output-current sinking-mode operation is required, the collector potential of transistor Q13 is driven below its quiescent level, thereby causing Q17 Q18 to decrease the output voltage at terminal 6. Thus, the gate terminal of PMOS transistor Q21 is displaced toward the V– bus, thereby reducing the channel resistance of Q21. As a consequence, there is an incremental increase in current flow through Q20, R12, Q21, D6, R7, and the base of Q16. As a result, Q16 sinks current from terminal 6 in direct response to the incremental change in output voltage caused by Q18. This sink current flows regardless of load: any excess current is internally supplied by the emitter-follower Q18. Short-circuit protection of the output circuit is provided by Q19, which is driven into conduction by the high voltage drop developed across R11 under output short-circuit conditions. Under these conditions, the collector of Q19 diverts current from Q4 so as to reduce the base-current drive from Q17, thereby limiting current flow in Q18 to the short-circuited load terminal.

Bias Circuit – Quiescent current in all stages (except the dynamic current sink) of the CA3140 is dependent upon bias current flow in R1. The function of the bias circuit is to establish and maintain constant-current flow through D1, Q6, Q8 and D2. D1 is a diode-connected transistor mirror-connected in parallel with the base-emitter junctions of Q1, Q2, and Q3. D1 may be considered as a current-sampling diode that senses the emitter current of Q6 and automatically adjusts the base current of Q6 (via Q1) to maintain a constant current through Q6, Q8, D2. The base-currents in Q2, Q3 are also determined by constant-current flow in D1. Furthermore, current in diode-connected transistor D2 establishes the currents in transistors Q14 and Q15.

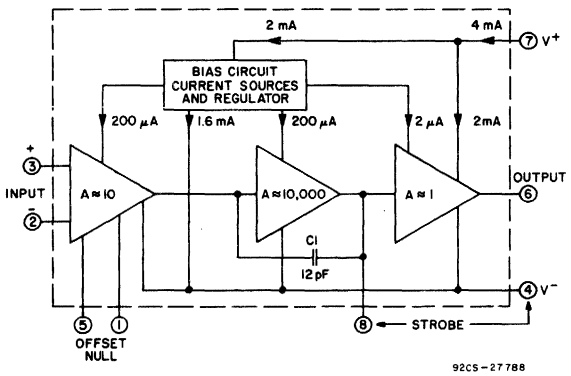

Fig. 3—Block diagram of CA3140 series.