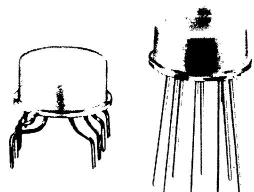
RCA
Solid State
Division

Linear Integrated Circuits

Monolithic Silicon

CA3130BT, CA3130BS
CA3130AT, CA3130AS
CA3130T, CA3130S



8-LEAD TO-5
with Dual-In-Line
Formed Leads
(S suffix)
H-1787

8-LEAD TO-5
(T suffix)
H-1528

COS/MOS Operational Amplifiers

With MOS/FET Input

Features:

- MOS/FET input stage provides:
  very high Z_I = 1.5 TΩ (1.5 x 10^{12} Ω) typ.
  very low I_I = 5 pA typ. at 15 V operation
  2 pA typ. at 5 V operation
- Common-mode input-voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail
- COS/MOS output stage permits signal swing to either (or both) supply rails

} Ideal for single-supply applications

- Low V_{IO}: 2 mV max. (CA3130B)
- Wide BW: 15 MHz typ. (unity-gain crossover)
- High SR: 10 V/μs typ. (unity-gain follower)
- High output current (I_O): 20 mA typ.
- High A_{OL}: 320,000 (110 dB) typ.
- Compensation with single external capacitor

Applications:

- Ground-referenced single-supply amplifiers
- Fast sample-hold amplifiers
- Long-duration timers/monostables
- High-input-impedance comparators
  (ideal interface with digital COS/MOS)
- High-input-impedance wideband amplifiers
- Voltage followers
  (e.g., follower for single-supply D/A converter)
- Voltage regulators
  (permits control of output voltage down to zero volts)
- Peak detectors
- Single-supply full-wave precision rectifiers
- Photo-diode sensor amplifiers

RCA-CA3130T, CA3130S, CA3130AT, CA3130AS, CA-3130BT, and CA3130BS are integrated-circuit operational amplifiers that combine the advantages of both COS/MOS and bipolar transistors on a monolithic chip.

Gate-protected p-channel MOS/FET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

A complementary-symmetry MOS (COS/MOS) transistor pair, capable of swinging the output voltage to within millivolts of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3130 Series circuits operate at supply voltages ranging from 5 to 16 volts, or ±2.5 to ±8 volts when using split supplies. They can be phase compensated with a single external capacitor, and have terminals for adjustment of offset voltage for applications requiring offset-null capability. Terminal provisions are also made to permit strobing of the output stage.

The CA3130 Series is supplied in either the standard 8-lead TO-5-style package (T suffix) or in the 8-lead dual-in-line formed-lead TO-5-style package "DIL-CAN" (S suffix) and operates over the full military-temperature range of −55°C to +125°C. The CA3130B is intended for applications requiring premium-grade specifications and with limits established for: input current, temperature coefficient of input-offset voltage, and gain over the range of −55°C to +125°C. The CA3130A offers superior input characteristics over those of the CA3130.

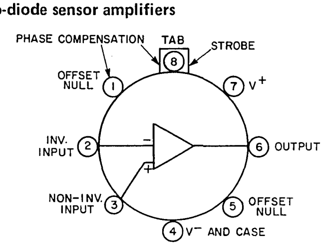


Fig. 1—Functional diagram of the CA3130 Series.

MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY VOLTAGE
(BETWEEN V^+ AND V^- TERMINALS) .... 16 V
DIFFERENTIAL-MODE INPUT VOLTAGE .... ±8 V
COMMON-MODE DC INPUT VOLTAGE .... V^+ to (V^- -0.5 V)
INPUT-TERMINAL CURRENT .... 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK–
UP TO 55°C .... 630 mW
ABOVE 55°C .... Derate linearly 6.67 mW/°C
WITH HEAT SINK–
AT 125°C .... 418 mW
BELOW 125°C .... Increase linearly at 16.7 mW/°C
TEMPERATURE RANGE:
OPERATING .... –55 to +125°C
STORAGE .... –65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION* .... INDEFINITE
LEAD TEMPERATURE (DURING SOLDERING):
AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM)
FROM CASE FOR 10 SECONDS MAX. ....+265°C

*Short circuit may be applied to ground or to either supply.

ELECTRICAL CHARACTERISTICS – For Equipment Design

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V^+=15 V V^-=0 V T_A=25°C (Unless Specified Otherwise)	CA3130B			CA3130A			CA3130			UNITS	FIG. NO.
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Input Offset Voltage	$\|V_{IO}\|$	$V^{\pm}$=±7.5 V	–	0.8	2	–	2	5	–	8	15	mV	–
Input Offset Current	$\|I_{IO}\|$	$V^{\pm}$=±7.5 V	–	0.5	10	–	0.5	20	–	0.5	30	pA	–
Input Current	I_I	$V^{\pm}$=±7.5 V	–	5	20	–	5	30	–	5	50	pA	–
Large-Signal Voltage Gain	A_{OL}	V_O=10 $V_{p\text{-}p}$	100 k	320 k	–	50 k	320 k	–	50 k	320 k	–	V/V	4,5
		R_L=2 kΩ	100	110	–	94	110	–	94	110	–	dB	
Common-Mode Rejection Ratio	CMRR		86	100	–	80	90	–	70	90	–	dB	–
Common-Mode Input-Voltage Range	V_{ICR}		0	–0.5 to 12	10	0	–0.5 to 12	10	0	–0.5 to 12	10	V	–
Power-Supply Rejection Ratio	$\Delta V_{IO}/\Delta V^+$	$V^{\pm}$=±7.5 V	–	32	100	–	32	150	–	32	320	μV/V	–
	$\Delta V_{IO}/\Delta V^-$		–	32	100	–	32	150	–	32	320		
Maximum Output Voltage	V_{OM}^+	R_L=2 kΩ	12	13.3	–	12	13.3	–	12	13.3	–	V	9
	V_{OM}^-		–	0.002	0.01	–	0.002	0.01	–	0.002	0.01		10
	$\|V_{OM}^+\|$	R_L=∞	14.99	15	–	14.99	15	–	14.99	15	–		9
	$\|V_{OM}^-\|$		–	0	0.01	–	0	0.01	–	0	0.01		10
Maximum Output Current: Source	I_{OM}^+	V_O=0 V	12	22	45	12	22	45	12	22	45	mA	9
Sink	I_{OM}^-	V_O=15 V	12	20	45	12	20	45	12	20	45		10
Supply Current	I^+	V_O=7.5 V R_L=∞	–	10	15	–	10	15	–	10	15	mA	7,8
		V_O=0 V R_L=∞	–	2	3	–	2	3	–	2	3		
Input Current	I_I	T_A=–55 to 125°C $V^{\pm}$=±7.5 V▲ V_O=10 $V_{p\text{-}p}$* R_L=2 kΩ*	–	Fig. 11	15	–	Fig. 11	–	–	Fig. 11	–	nA	–
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$		–	5	15	–	10	–	–	10	–	μV/°C	–
Large-Signal Voltage Gain	A_{OL}		50 k	320 k	–	–	320 k	–	–	320 k	–	V/V	5
			94	110	–	–	110	–	–	110	–	dB	

* Applies only to A_{OL}.

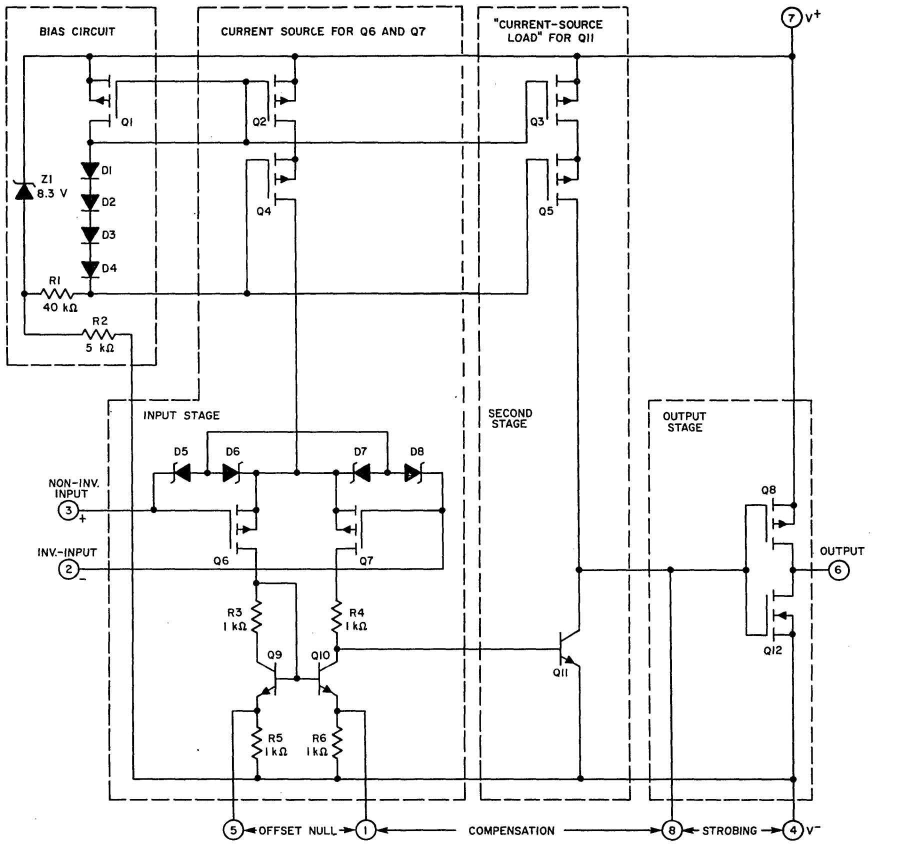
▲ Applies only to I_I and $\Delta V_{IO}/\Delta T$.

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V^+=+7.5 V V^-=−7.5 V T_A=25°C (Unless Specified Otherwise)	CA3130B	CA3130A	CA3130	UNITS	FIG. NO.
Input Offset Voltage Adjustment Range		10 kΩ across Terms. 4 and 5 or 4 and 1	±22	±22	±22	mV	–
Input Resistance	R_I		1.5	1.5	1.5	TΩ	–
Input Capacitance	C_I	f = 1 MHz	4.3	4.3	4.3	pF	–
Equivalent Input Noise	e_n	BW=0.2 MHz R_S=1 MΩ*	23	23	23	μV	14
Unity Gain Crossover Frequency	f_T	C_C = 0	15	15	15	MHz	4,15
		C_C = 47 pF	4	4	4		
Slew Rate: Open Loop	SR	C_C = 0	30	30	30	V/μs	–
Closed Loop		C_C = 56 pF	10	10	10		15
Transient Response: Rise Time	t_r	C_C = 56 pF C_L = 25 pF R_L = 2 kΩ (Voltage Follower)	0.09	0.09	0.09	μs	15
Overshoot			10	10	10	%	15
Settling Time (4 Vp-p Input to <0.1%)			1.2	1.2	1.2	μs	15

* Although a 1-MΩ source is used for this test, the equivalent input noise remains constant for sources of R_S up to 10 MΩ.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V^+ = 5 V V^- = 0 V T_A = 25°C (Unless Specified Otherwise)	CA3130B	CA3130A	CA3130	UNITS	FIG. NO.
Input Offset Voltage	V_{IO}		1	2	8	mV	–
Input Offset Current	I_{IO}		0.1	0.1	0.1	pA	–
Input Current	I_I		2	2	2	pA	–
Common-Mode Rejection Ratio	CMRR		100	90	80	dB	–
Large-Signal Voltage Gain	A_{OL}	V_O = 4 Vp-p R_L = 5 kΩ	100 k	100 k	100 k	V/V	–
			100	100	100	dB	–
Common-Mode Input Voltage Range	V_{ICR}		0 to 2.8	0 to 2.8	0 to 2.8	V	–
Supply Current	I^+	V_O = 5 V, R_L = ∞	300	300	300	μA	7,8
		V_O=2.5 V, R_L = ∞	500	500	500		
Power Supply Rejection Ratio	$\Delta V_{IO}/\Delta V^+$		200	200	200	μV/V	–



NOTE:
DIODES D5 THROUGH D8 PROVIDE GATE-OXIDE PROTECTION FOR MOS/FET INPUT STAGE.

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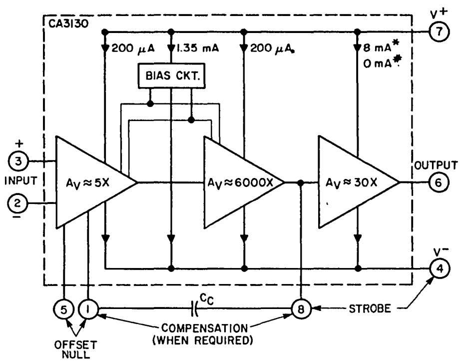
Fig. 2—Schematic diagram of the CA3130 Series.

CIRCUIT DESCRIPTION

Fig. 3 is a block diagram of the CA3130 Series COS/MOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA3130 Series circuits are ideal for single-supply operation. Three Class A amplifier stages, having the individual gain capability and current consumption shown in Fig. 3, provide the total gain of the CA3130. A biasing circuit provides two potentials for common use in the first and second stages. Term. 8 can be used both for phase compensation and to strobe the output stage into quiescence. When Term. 8 is tied to the negative supply rail (Term. 4) by mechanical or electrical means, the output potential at Term. 6 essentially rises to the positive supply-rail potential at Term. 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g., when the amplifier output is used to drive COS/MOS digital circuits in comparator applications).

Input Stages—The circuit of the CA3130 is shown in Fig. 2. It consists of a differential-input stage using PMOS field-effect transistors (Q6, Q7) working into a mirror-pair of bipolar transistors (Q9, Q10) functioning as load resistors together with resistors R3 through R6. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q11). Offset nulling, when desired, can be effected by connecting a 100,000-ohm potentiometer across Terms. 1 and 5 and the potentiometer slider arm to Term. 4. Cascode-connected PMOS



TOTAL SUPPLY VOLTAGE (FOR INDICATED VOLTAGE GAINS) = 15 V
*WITH INPUT TERMINALS BIASED SO THAT TERM. 6 POTENTIAL IS +7.5 V ABOVE TERM. 4.
#WITH OUTPUT TERMINAL DRIVEN TO EITHER SUPPLY RAIL.

92CS-24715

Fig. 3—Block diagram of the CA3130 Series.

transistors Q2, Q4 are the constant-current source for the input stage. The biasing circuit for the constant-current source is subsequently described. The small diodes D5 through D8 provide gate-oxide protection against high-voltage transients, e.g. including static electricity during handling for Q6 and Q7.

Second Stage—Most of the voltage gain in the CA3130 is provided by the second amplifier stage, consisting of bipolar transistor Q11 and its cascode-connected load resistance provided by PMOS transistors Q3 and Q5. The source of bias potentials for these PMOS transistors is subsequently described. Miller-Effect compensation (roll-off) is accomplished by simply connecting a small capacitor between Terms. 1 and 8. A 47-picofarad capacitor provides sufficient compensation for stable unity-gain operation in most applications.

Bias-Source Circuit—At total supply voltages, somewhat above 8.3 volts, resistor R2 and zener diode Z1 serve to establish a voltage of 8.3 volts across the series-connected circuit, consisting of resistor R1, diodes D1 through D4, and PMOS transistor Q1. A tap at the junction of resistor R1 and diode D4 provides a gate-bias potential of about 4.5 volts for PMOS transistors Q4 and Q5 with respect to Term. 7. A potential of about 2.2 volts is developed across diode-connected PMOS transistor Q1 with respect to Term. 7 to provide gate bias for PMOS transistors Q2 and Q3. It should be noted that Q1 is "mirror-connected"† to both Q2 and Q3. Since transistors Q2 and Q3 are twice the size of Q1, the approximate 100-microampere current in Q1 establishes 200-microampere "mirrored" currents in Q2 and Q3 as constant-current sources for the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3 volts, zener diode Z1 becomes non-conductive and the potential, developed across series-connected R1, D1-D4, and Q1, varies directly with variations in supply voltage. Consequently, the gate bias for Q4, Q5 and Q2, Q3 varies in accordance with supply-voltage variations. This variation results in deterioration of the power-supply-rejection ratio (PSRR) at total supply voltages below 8.3 volts. Operation at total supply voltages below about 4.5 volts results in seriously degraded performance.

Output Stage—The output stage consists of a drain-loaded inverting amplifier using COS/MOS transistors operating in the Class A mode. When operating into very high resistance loads, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Fig. 6. Typical op-amp loads are readily driven by the output stage. Because large-signal excursions are non-linear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01 per cent accuracy levels, including the negative supply rail.

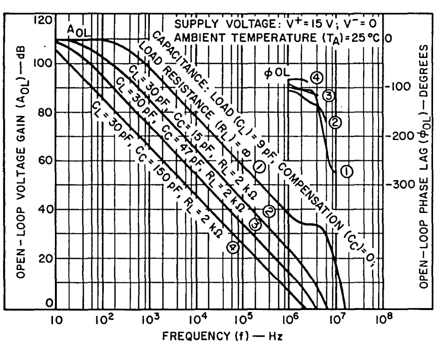


Fig. 4—Open-loop voltage gain and phase shift vs. frequency for various values of C_L, C_C, and R_L.

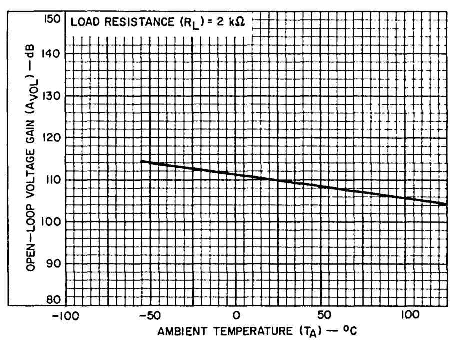


Fig. 5—Open-loop gain vs. temperature.

†For general information on the characteristics of COS/MOS transistor pairs in linear-circuit applications, see File No. 619, data bulletin on CA3600E "COS/MOS Transistor Array."

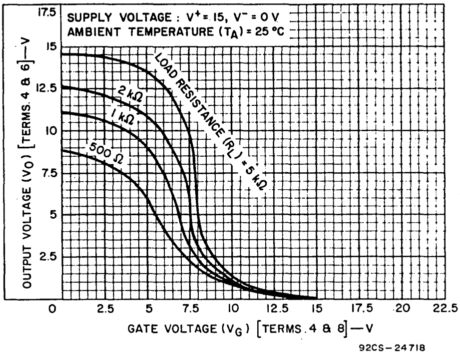


Fig. 6—Voltage transfer characteristics of COS/MOS output stage.

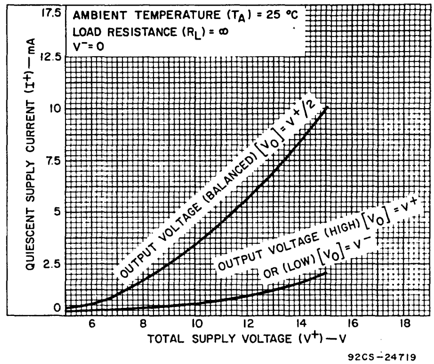


Fig. 7—Quiescent supply current vs. supply voltage.

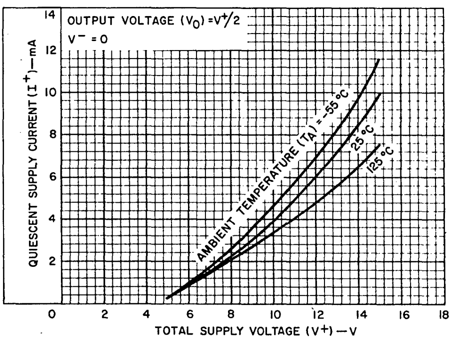


Fig. 8—Quiescent supply current vs. supply voltage at several temperatures.

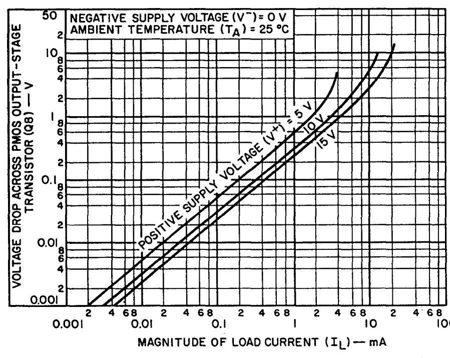


Fig. 9—Voltage across PMOS output transistor (Q8) vs. load current.

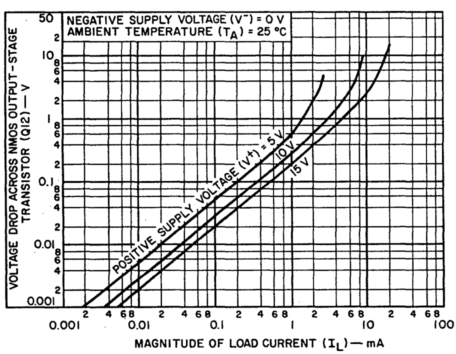


Fig. 10—Voltage across NMOS output transistor (Q12) vs. load current.

HANDLING AND OPERATING CONSIDERATIONS

Handling Considerations

The CA3130 uses MOS field-effect transistors in the input circuit. Because MOS/FET's have extremely high input resistances, they are susceptible to damage when exposed to extremely high static electrical charges. To minimize the possibilities of damaging the input stage transistors, Q6 and Q7, the CA3130 utilizes a protective diode network in the input stage. Nevertheless, it is good practice that the following precautions be observed during handling, testing, and actual operation of the CA3130 devices to minimize exposure to damage-inducing hazards:

1. Soldering-iron tips, metal parts of fixtures, tools, and handling facilities should be grounded.
2. Devices should not be inserted into or removed from circuits with the power ON because transient voltages may cause damage.
3. Signals should not be applied to the input (Terms. 2 and 3) when the device power supply is OFF. Input-terminal currents should not exceed 1 mA.
4. After CA3130 devices have been mounted on circuit boards, proper handling precautions should still be observed if the input terminals are unterminated. It is good practice during board-processing operations to return Terms. 2 and 3 to Term. 4 by jumping the appropriate conductors.

Offset Nulling

Offset-voltage nulling is usually accomplished with a 100,000-ohm potentiometer connected across Terms. 1 and 5 and with the potentiometer slider arm connected to Term. 4. A fine offset-null adjustment usually can be effected with the slider arm positioned in the mid-point of the potentiometer's total range.

Input-Current Variation with Temperature

The input current of the CA3130 Series circuits is typically 5 pA at 25°C. The major portion of this input current is due to leakage current through the gate-protective diodes in the input circuit. As with any semiconductor-junction device, including op amps with a junction-FET input stage, the leakage current approximately doubles for every 10°C increase in temperature. Fig. 11 provides data on the typical variation of input bias current as a function of temperature in the CA3130.

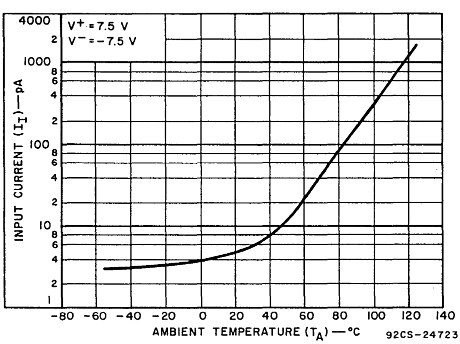


Fig. 11—Input current vs. ambient temperature.

In applications requiring the lowest practical input current and incremental increases in current because of "warm-up" effects, it is suggested that an appropriate heat sink be used with the CA3130. In addition, when "sinking" or "sourcing" significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

Input-Offset-Voltage (V_{IO}) Variation with DC Bias vs. Device Operating Life

It is well known that the characteristics of a MOS/FET device can change slightly when a dc gate-source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA3130 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential dc bias voltage applied across Terms. 2 and 3. Fig. 12 shows typical data pertinent to shifts in offset voltage encountered with CA3130 devices during life testing. The two-volt dc differential voltage example represents conditions when the amplifier output stage is "toggled", e.g., as in comparator applications.

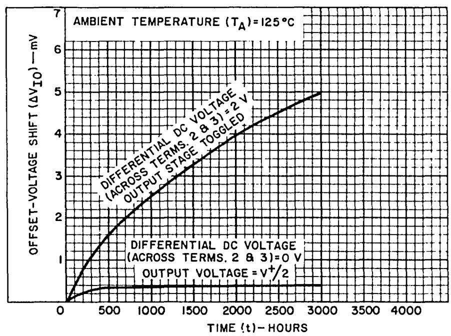


Fig. 12—Typical incremental offset-voltage shift vs. operating life.

Power-Supply Considerations

Because the CA3130 is very useful in single-supply applications, it is pertinent to review some considerations relating to power-supply current consumption under both single and dual-supply service. Figs. 13a and 13b show the CA3130 connected for both dual- and single-supply operation.

Dual-supply operation: When the output voltage at Term. 6 is zero-volts, the currents supplied by the two power supplies are equal. When the gate terminals of Q8 and Q12 are driven increasingly positive with respect to ground, current flow through Q12 (from the negative supply) to the load is increased and current flow through Q8 (from the positive supply) decreases correspondingly. When the gate terminals of Q8 and Q12 are driven increasingly negative with respect to ground, current flow through Q8 is increased and current flow through Q12 is decreased accordingly.

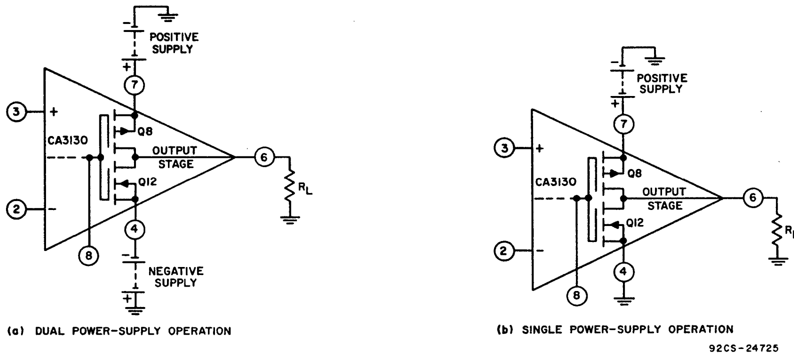


Fig. 13—CA3130 output stage in dual and single power-supply operation.

Single-supply operation: Initially, let it be assumed that the value of R_L is very high (or disconnected), and that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is at $V^+/2$, i.e., the voltage-drops across Q8 and Q12 are of equal magnitude. Fig. 7 shows typical quiescent supply-current vs. supply-voltage for the CA3130 operated under these conditions. Since the output stage is operating as a Class A amplifier, the supply-current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage-transfer characteristics (see Fig. 6). If either Q8 or Q12 are swung out of their linear regions toward cut-off (a non-linear region), there will be a corresponding reduction in supply-current. In the extreme case, e.g., with Term. 8 swung down to ground potential (or tied to ground), NMOS transistor Q12 is completely cut off and the supply-current to series-connected transistors Q8, Q12 goes essentially to zero. The two preceding stages in the CA3130, however, continue to draw modest supply-current (see the lower curve in Fig. 7) even though the output stage is strobed off. Fig. 13a shows a dual-supply arrangement for the output stage that can also be strobed off, assuming $R_L = \infty$, by pulling the potential of Term. 8 down to that of Term. 4.

Let it now be assumed that a load-resistance of nominal value (e.g., 2 kilohms) is connected between Term. 6 and ground in the circuit of Fig. 13b. Let it further be assumed again that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is at $V^+/2$. Since PMOS transistor Q8 must now supply quiescent current to both R_L and transistor Q12, it should be apparent that under these conditions the supply-current must increase as an inverse function of the R_L magnitude. Fig. 9 shows the voltage-drop across PMOS transistor Q8 as a function of load current at several supply-voltages. Fig. 6 shows the voltage-transfer characteristics of the output stage for several values of load resistance.

Wideband Noise

From the standpoint of low-noise performance considerations, the use of the CA3130 is most advantageous in applications where in the source resistance of the input signal is in the order of 1 megohm or more. In this case, the total input-referred noise voltage is typically only 23 μV when the test-circuit amplifier of Fig. 14 is operated at a total supply voltage of 15 volts. This value of total input-referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1 megohm, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.

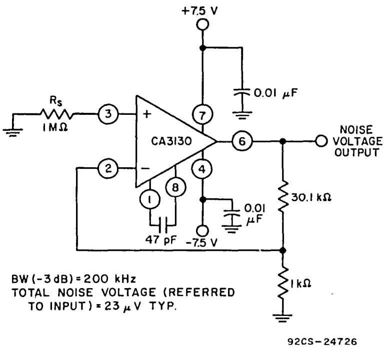
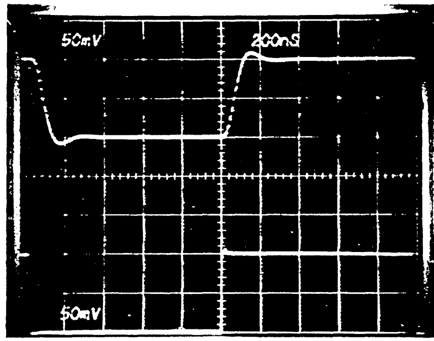
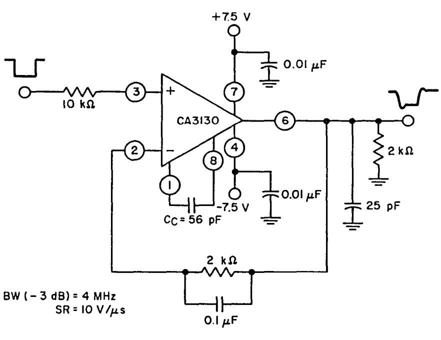


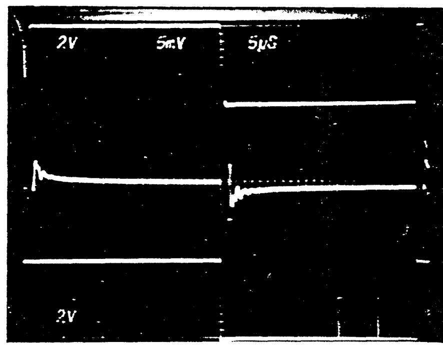
Fig. 14—Test-circuit amplifier (30-dB gain) used for wideband noise measurements.



Top Trace: Output
Bottom Trace: Input

(a) Small-signal response (50 mV/div. and 200 ns/div.)





Top Trace: Output signal (2 V/div. and 5 μs/div.)
Center Trace: Difference signal (5 mV/div. and 5 μs/div.)
Bottom Trace: Input signal (2 V/div. and 5 μs/div.)

(b) Input-output difference signal showing settling time (Measurement made with Tektronix 7A13 differential amplifier)

92CS-24739

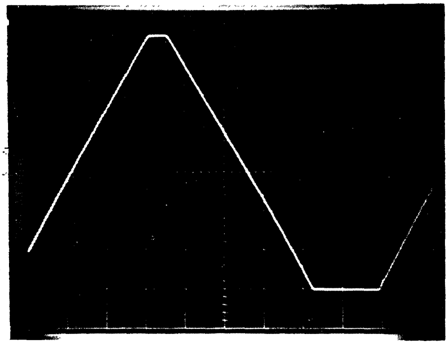
Fig. 15—Split-supply voltage follower with associated waveforms.

TYPICAL APPLICATIONS

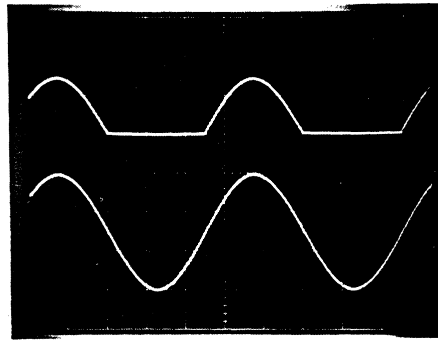
Voltage Followers

Operational amplifiers with very high input resistances, like the CA3130, are particularly suited to service as voltage followers. Fig. 15 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA3130 in a split-supply configuration.

A voltage follower, operated from a single supply, is shown in Fig. 16, together with related waveforms. This follower circuit is linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Fig. 16a with input-signal ramping. The waveforms in Fig. 16b show that the follower does not lose its input-to-output phase-sense, even though the input is being swung 7.5 volts below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Fig. 16b also shows the manner in which the COS/MOS output stage permits the output signal to swing down to the negative supply-rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA3130 in a single-supply voltage-follower application.



(a) Output-waveform with input-signal ramping (2 V/div. and 500 μs/div.)



Top Trace: Output (5 V/div. and 200 μs/div.)
Bottom Trace: Input (5 V/div. and 200 μs/div.)

(b) Output-waveform with ground-reference sine-wave input

92CS-24728

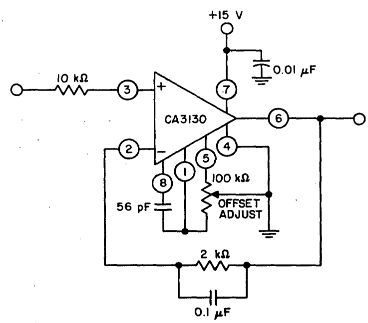


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Fig. 16—Single-supply voltage-follower with associated waveforms. (e.g., for use in single-supply D/A converter; see Fig. 9 in ICAN-6080).

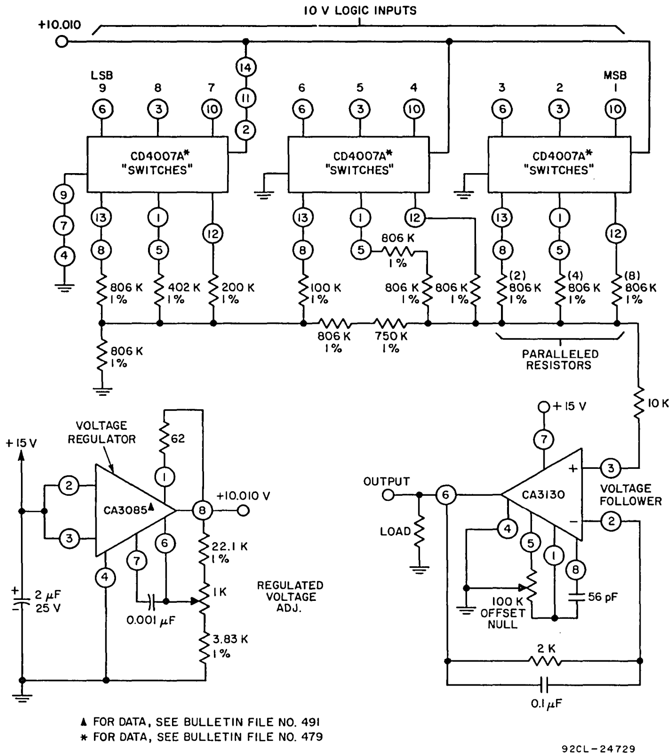
9-BIT COS/MOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC)* is shown in Fig. 17. This system combines the concepts of multiple-switch COS/MOS IC's, a low-cost ladder network of discrete metal-oxide-film resistors, a CA3130 op-amp connected as a follower, and an inexpensive monolithic regulator in a simple single power-supply arrangement. An additional feature of the DAC is that it is readily interfaced with COS/MOS input logic, e.g., 10-volt logic levels are used in the circuit of Fig. 17.

The circuit uses an R/2R voltage-ladder network, with the output potential obtained directly by terminating the ladder arms at either the positive or the negative power-supply terminal. Each CD4007A contains three "inverters", each "inverter" functioning as a single-pole double-throw switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly of one per cent tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000-ohm resistors from the same manufacturing lot.

A single 15-volt supply provides a positive bus for the CA3130 follower amplifier and feeds the CA3085 voltage regulator. A "scale-adjust" function is provided by the regulator output

*"Digital-to-Analog Conversion Using the RCA-CD4007A COS/MOS IC," Application Note ICAN-6080.



BIT	REQUIRED RATIO-MATCH
1	STANDARD
2	±0.1%
3	±0.2%
4	±0.4%
5	±0.8%
6-9	±1% ABS.

ALL RESISTANCES IN OHMS

Fig. 17–9-bit DAC using COS/MOS digital switches and CA3130.

control, set to a nominal 10-volt level in this system. The line-voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with variations of several volts in the supply. The flexibility afforded by the COS/MOS building blocks simplifies the design of DAC systems tailored to particular needs.

Single-Supply, Absolute-Value, Ideal Full-Wave Rectifier

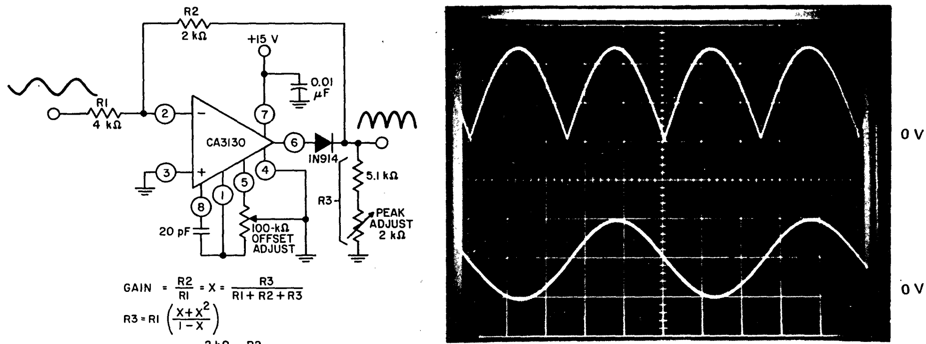
The absolute-value circuit using the CA3130 is shown in Fig. 18. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No. 6) of the inverting amplifier in a negative-going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative-going excursion of the input signal, the CA3130 functions as a normal inverting amplifier with a gain equal to −R2/R1. When the equality of the two equations shown in Fig. 18 is satisfied, the full-wave output is symmetrical.

Peak Detectors

Peak-detector circuits are easily implemented with the CA-3130, as illustrated in Fig. 19 for both the peak-positive and the peak-negative circuit. It should be noted that with large-signal inputs, the bandwidth of the peak-negative circuit is much less than that of the peak-positive circuit. The second stage of the CA3130 limits the bandwidth in this case. Negative-going output-signal excursion requires a positive-going signal excursion at the collector of transistor Q11, which is loaded by the intrinsic capacitance of the associated circuitry in this mode. On the other hand, during a negative-going signal excursion at the collector of Q11, the transistor functions in an active "pull-down" mode so that the intrinsic capacitance can be discharged more expeditiously.

Error-Amplifier in Regulated Power Supplies

The CA3130 is an ideal choice for error-amplifier service in regulated power supplies since it can function as an error-amplifier when the regulated output voltage is required to



GAIN $= \frac{R2}{RI} = X = \frac{R3}{RI + R2 + R3}$

$R3 = RI\left(\frac{X + X^2}{1 - X}\right)$

FOR $X = 0.5$: $\frac{2\,k\Omega}{4\,k\Omega} = \frac{R2}{RI}$

$R3 = 4\,k\Omega\left(\frac{0.75}{0.5}\right) = 6\,k\Omega$

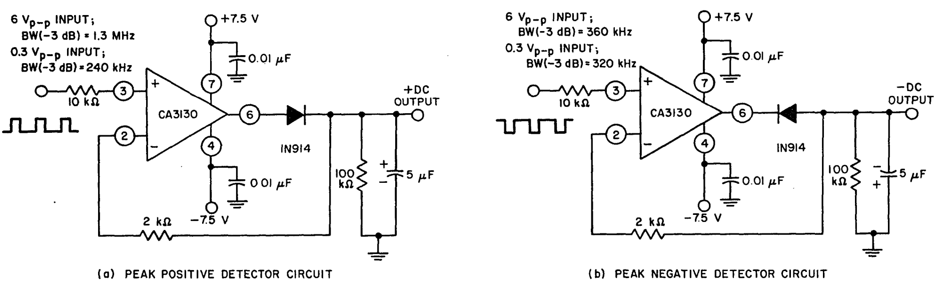
20 V p-p INPUT: BW(-3dB) = 230 kHz, DC OUTPUT (AVG.) = 3.2 V
1 VOLT p-p INPUT: BW(-3dB) = 130 kHz, DC OUTPUT (AVG.) = 160 mV

92CS-24730

Top Trace: Output signal (2 V/div.)
Bottom Trace: Input signal (10 V/div.)
Time base on both traces: 0.2 ms/div.

92CS-24738

Fig. 18—Single-supply, absolute-value, ideal full-wave rectifier with associated waveforms.



92CS-24731

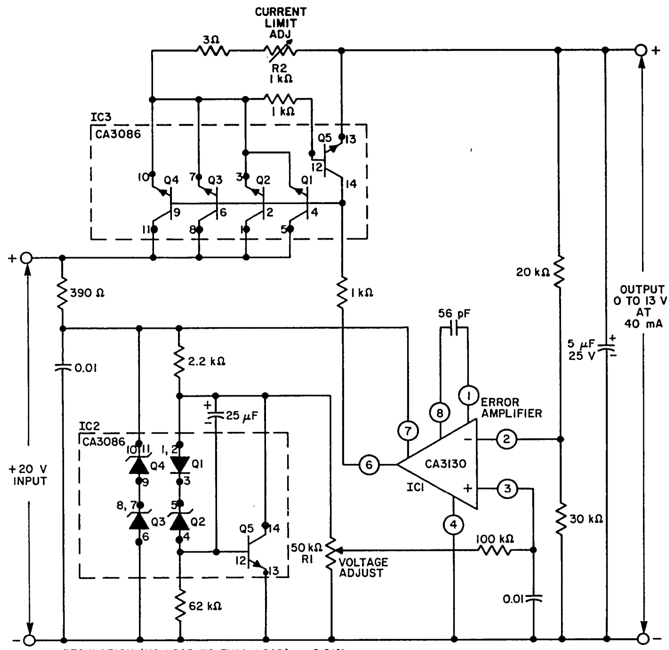
Fig. 19—Peak-detector circuits.

approach zero. Fig. 20 shows the schematic diagram of a 40-mA power-supply capable of providing regulated output voltage by continuous adjustment over the range from 0 to 13 volts. Q3 and Q4 in IC2 (a CA3086 transistor-array IC) function as zeners to provide supply-voltage for the CA3130 comparator (IC1). Q1, Q2, and Q5 in IC2 are configured as a low impedance, temperature-compensated source of adjustable reference voltage for the error amplifier. Transistors Q1, Q2, Q3, and Q4 in IC3 (another CA3086 transistor-array IC) are connected in parallel as the series-pass element. Transistor Q5 in IC3 functions as a current-limiting device by diverting base drive from the series-pass transistors, in accordance with the adjustment of resistor R2.

Fig. 21 contains the schematic diagram of a regulated power-supply capable of providing regulated output voltage by continuous adjustment over the range from 0.1 to 50 volts and currents up to 1 ampere. The error amplifier (IC1) and circuitry associated with IC2 function as previously described, although the output of IC1 is boosted by a discrete transistor (Q4) to provide adequate base drive for the Darlington-connected series-pass transistors Q1, Q2. Transistor Q3 functions in the previously described current-limiting circuit.

Multivibrators

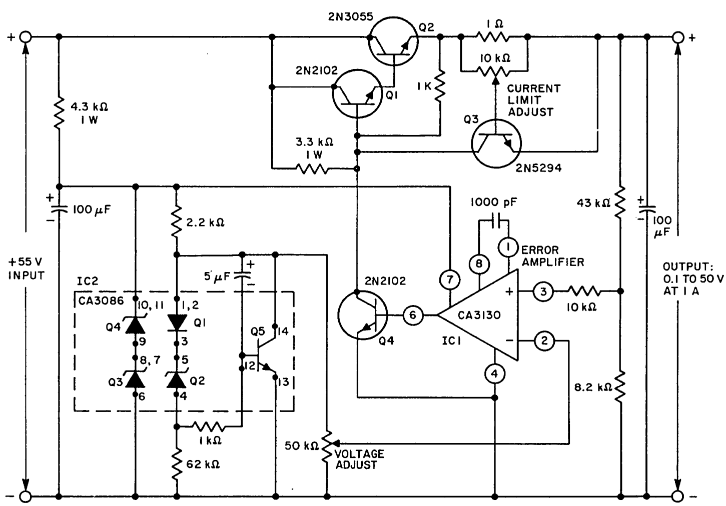
The exceptionally high input resistance presented by the CA3130 is an attractive feature for multivibrator circuit design because it permits the use of timing circuits with high R/C ratios. The circuit diagram of a pulse generator (astable multivibrator), with provisions for independent control of the "on" and "off" periods, is shown in Fig. 22. Resistors R1 and R2 are used to bias the CA3130 to the mid-point of the supply-voltage and R3 is the feedback resistor.



REGULATION (NO LOAD TO FULL LOAD): < 0.01%
INPUT REGULATION: 0.02%/V
HUM AND NOISE OUTPUT: < 25 μV UP TO 100 kHz

92CM-24732

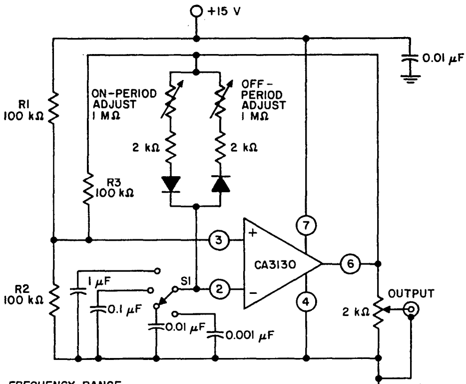
Fig. 20—Voltage regulator circuit (0 to 13 V at 40 mA).



REGULATION (NO LOAD TO FULL LOAD): <0.005%
INPUT REGULATION: <0.01%/V
HUM AND NOISE OUTPUT: <250 μV RMS UP TO 100 kHz

92CM-24734

Fig. 21—Voltage regulator circuit (0.1 to 50 V at 1 A).



FREQUENCY RANGE:

POSITION OF S1	PULSE PERIOD
0.001 μF	4 μs TO 1 ms
0.01 μF	40 μs TO 10 ms
0.1 μF	0.4 ms TO 100 ms
1 μF	4 ms TO 1 s

92CS-24733

Fig. 22—Pulse generator (astable multivibrator) with provisions for independent control of "ON" and "OFF" periods.

Function Generator

Fig. 23 contains the schematic diagram of a function generator using the CA3130 in the integrator and threshold detector functions. This circuit generates a triangular or square-wave output that can be swept over a 1,000,000:1 range (0.1 Hz to 100 kHz) by means of a single control, R1. A voltage-control input is also available for remote sweep-control.

The heart of the frequency-determining system is an operational-transconductance-amplifier (OTA)*, IC1, operated as a voltage-controlled current-source. The output, I_O, is a current applied directly to the integrating capacitor, C1, in the feedback loop of the integrator IC2, using a CA3130, to provide the triangular-wave output. Potentiometer R2 is used to adjust the circuit for slope symmetry of positive-going and negative-going signal excursions.

Another CA3130, IC3, is used as a controlled switch to set the excursion limits of the triangular output from the integrator circuit. Capacitor C2 is a "peaking adjustment" to optimize the high-frequency square-wave performance of the circuit.

Potentiometer R3 is adjustable to perfect the "amplitude symmetry" of the square-wave output signals. Output from the threshold detector is fed back via resistor R4 to the input of IC1 so as to toggle the current source from plus to minus in generating the linear triangular wave.

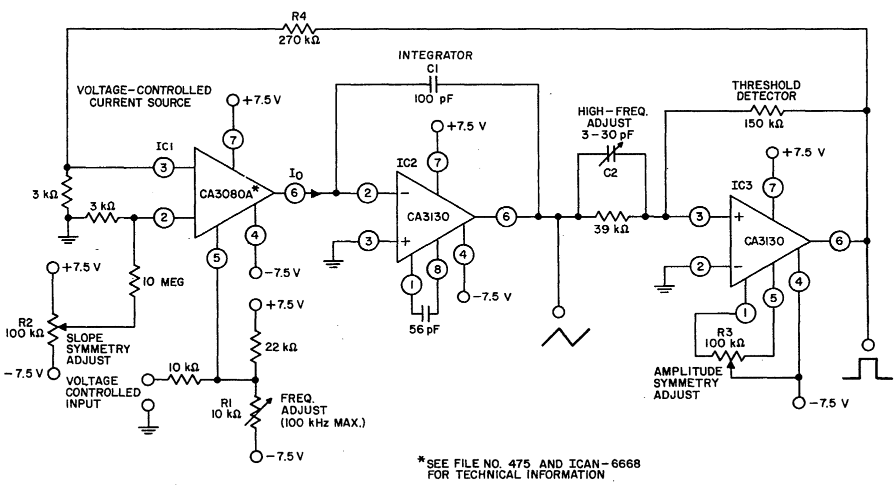


Fig. 23—Function generator (frequency can be varied 1,000,000/1 with a single control).

*See File No. 475 and ICAN-6668.

Operation with Output-Stage Power-Booster

The current-sourcing and -sinking capability of the CA3130 output stage is easily supplemented to provide power-boost capability. In the circuit of Fig. 24, three COS/MOS transistor-pairs in a single CA3600E* IC array are shown parallel connected with the output stage in the CA3130. In the Class A mode of CA3600E shown, a typical device consumes 20 mA of supply current at 15 V operation. This arrangement boosts the current-handling capability of the CA3130 output stage by about 2.5x.

The amplifier circuit in Fig. 24 employs feedback to establish a closed-loop gain of 48 dB. The typical large-signal bandwidth (−3 dB) is 50 kHz.

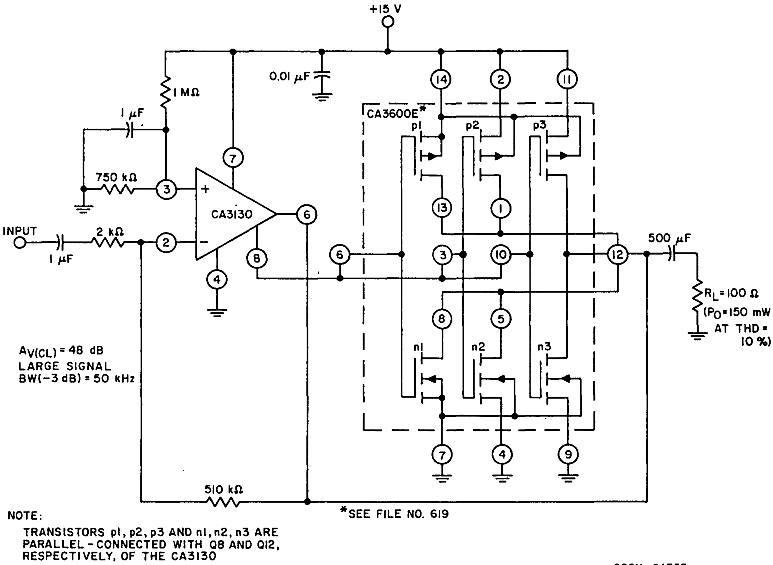


Fig. 24—COS/MOS transistor array (CA3600E) connected as power-booster in the output stage of the CA3130.