555-TYPE INTEGRATED CIRCUITS

The 555 group of i.cs is one of the most popular ever made, with an enormous variety of applications in oscillators and timers. John Linsley Hood explains its internal design and method of operation

by J. L. Linsley Hood

If the 1950s were the decade in which linear electronic circuits, previously implemented using thermionic valves as their active components, were progressively taken over by transistors, then the '60s were the decade in which such circuits, built up from an assembly of discrete components and transistors, were increasingly constructed using one or two simple packages of purpose-built circuitry, containing all the necessary active and passive components in a single lump. The term 'integrated circuit' was coined at this time to describe this packaged assembly of components.

While it was the enormous progress in the field of digital computers; which convinced the i.c. manufacturers of the enormous benefits of scale, it was the consumer market which provided the chance of profitable manufacture away from the computer field.

The realization that there was a large potential market set the design departments of many of the larger semiconductor manufacturers exploring the possibilities for useful functional packages. Clearly, an i.c. functional block which could be used with a relay and a timing capacitor to provide time delays or timing cycles, as, for example, in a washing machine or a darkroom enlarger timer, would have a lot of uses, and several such i.cs were evolved at the end of the 1960s. Of these, by far the most successful was the Signetics 555. A number of manufacturers have copied it in identical form – in the process of what is known as 'second sourcing' – and produced in dual (556), quadruple (558) and c.m.o.s. (ICM7555) versions, along with sundry improved devices having the same pin configurations, such as the LM555C.

With the possible exception of the ubiquitous i.c. operational amplifier, few integrated circuits have had such an appeal to the hobby electronics constructor, with several complete books of circuits having been published showing possible applications for this device. Yet, in spite of this, to most of its users, its method of operation remains needlessly obscure, and many attempted applications founder on inadvertent incompatibilities between the internal and external circuitry.

Circuit description

The 555 is fundamentally intended to give an output voltage waveform, as a 'one-shot' or in a repetitive manner, at a low enough output impedance to operate a reasonably sensitive relay. To simplify calculations for the timing RC chain – in which the time constant RC, in seconds, is the time taken for a capacitor C to charge through resistor R to 63.2% of the applied voltage – the internal voltage switching levels are chosen so that the external timing capacitor charges through about this voltage differential. A simplified block diagram showing the internal arrangement is given in Fig. 1.

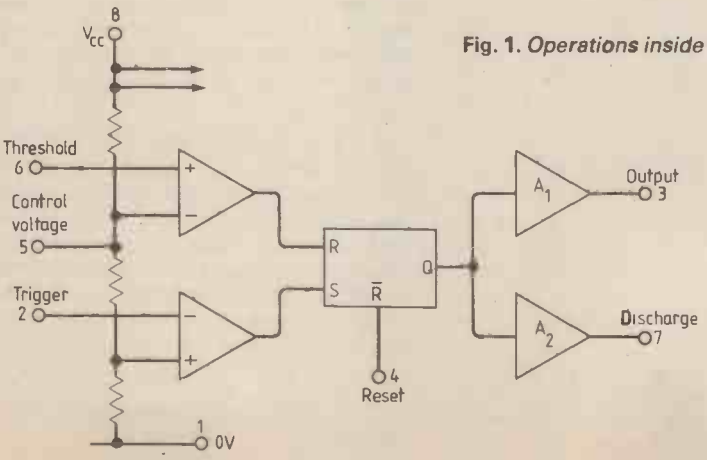
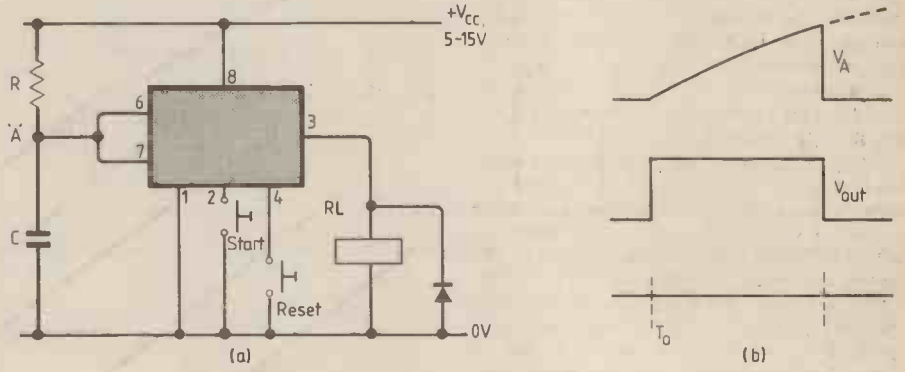


Fig. 1. *Operations inside the 555.*

In this, the heart of the circuit is a bistable 'flip-flop' with an external over-riding reset input R. The two normal inputs are the threshold and the trigger connexions, both of which are fed in through relatively high-impedance buffer amplifiers, connected, respectively, to reference voltages of $\frac{2}{3}V_{cc}$ and $\frac{1}{3}V_{cc}$, derived from the 15k resistor chain. Two buffered outputs from the flip-flop are provided through amplifiers A_1 and A_2, the first of which is a normal 'totem pole' output arrangement, as typically used in t.t.l. logic, to give a fairly low output impedance, and good current-sourcing characteristics. The second output, from A_2, is derived simply from a single transistor 'open collector' stage.

The way in which the 555 would normally be connected to operate as a 'one-shot' timer driving a relay, is shown in Fig. 2(a). In this the threshold input and the discharge (open-collector amplifier) output are joined together, and taken to the junction of timing resistor R and timing capacitor C; the timing cycle is initiated by a momentary operation of a push-switch connected to the trigger input. This sets the Q output from the bistable, and both of the non-inverted outputs from A_1 and A_2, to a high state. In the case of A_1, this will energize the relay RL_1, and in the case of A_2, the result will be that its output becomes an open circuit, so that the timing capacitor C is free to charge up towards the $+V_{cc}$ line.

Fig. 2. *555 as a one-shot relay timer, with manual start and reset.*



Once the Threshold input level has reached $\frac{2}{3}V_{cc}$, the 'reset' input to the bistable, R in Fig. 1, is taken high, when it reverts to its initial state, with A_1 output 'low' – so that the relay is de-energized – and A_2 at a low impedance. This holds the

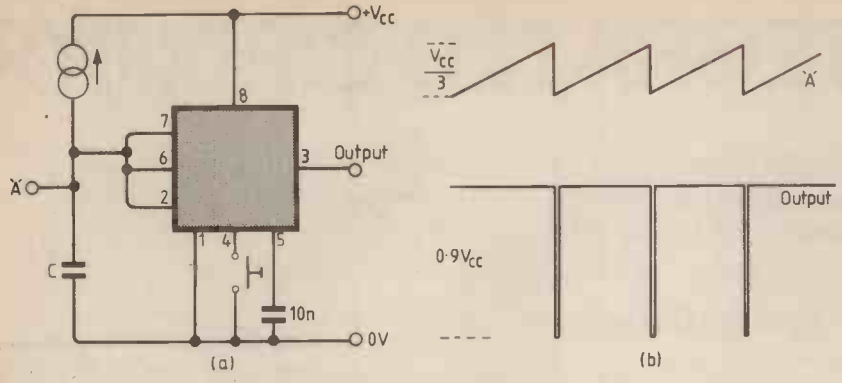


Fig. 3. *Connexion for a free-running oscillator, with a frequency determined by the constant-current source and the value of C..*

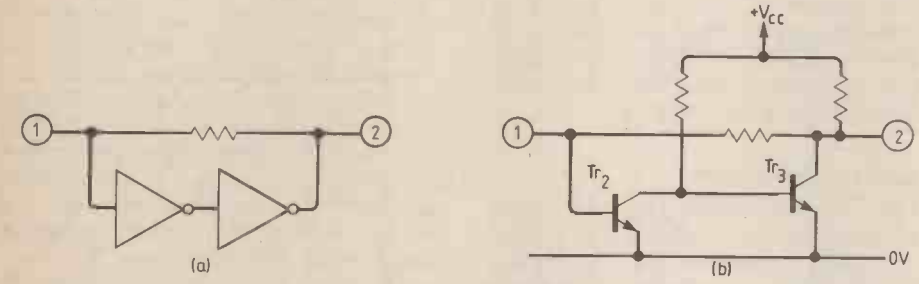


Fig. 4. *Flip-flop block of Fig. 1 in logical form at (a) and in its practical arrangement at (b).*

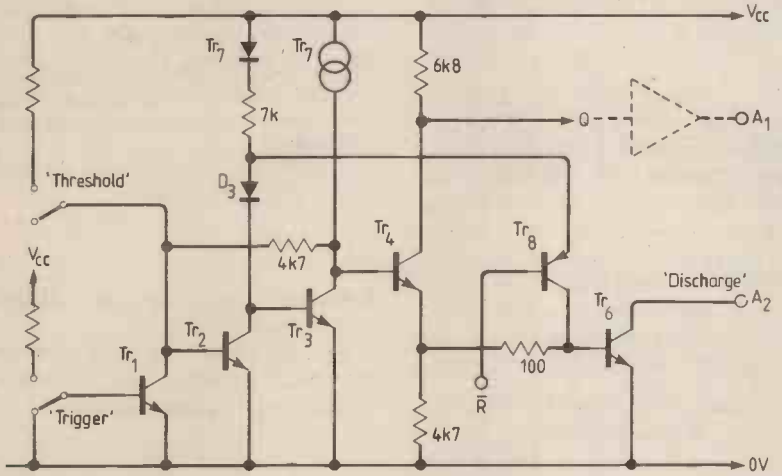


Fig. 5. *Flip-flop (Tr_2 and Tr_3) shown in relation to threshold, trigger and output circuitry.*

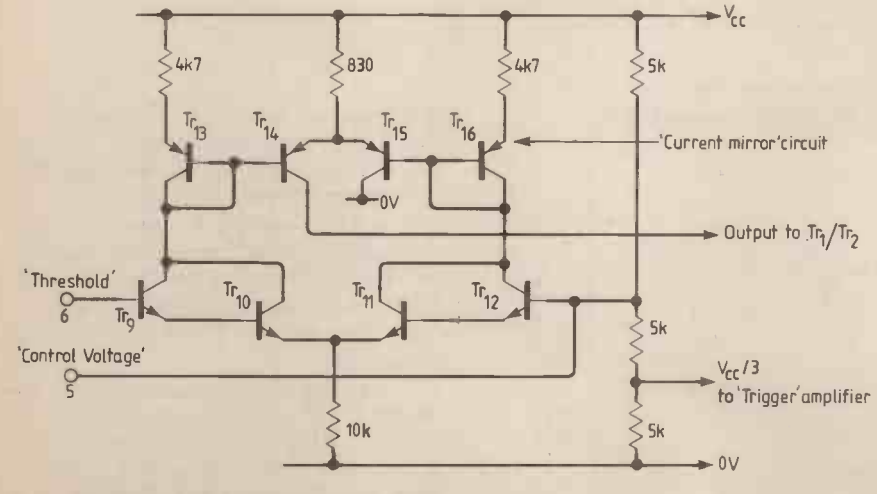


Fig. 6. *Input amplifier for threshold voltage.*

timing capacitor discharged and at a potential close to the 0 volt line level, ready for a further timing cycle to be initiated, by an input at a level less than $\frac{1}{3}V_{cc}$ being applied to the Trigger. The output waveforms are shown in Fig. 2(b).

Since the Trigger input is also taken to the bistable through a impedance buffer amplifier, it is practicable to connect this to the timing circuit as well, without imposing too much of a static load. This will convert the circuit into a 'free-running' sawtooth generator, with an output of $\frac{1}{3}V_{cc}$, as shown in Figs 3(a) and 3(b). Moreover, if the timing resistor R is replaced by an appropriate constant-current source, the output at point A will be a highly linear waveform, suitable for use in a time-base generator, and with a sync. input available at the override reset R of the bistable.

The bistable flip-flop is itself a very simple arrangement, shown schematically in Fig. 4(a) and in its practical form in Fig. 4(b). In this circuit, if the input (1) is taken high, even momentarily, the output will also go high and remain at that state. Similarly, if the input is taken low, the output will also follow, and remain. The fact that the transistor circuit of Tr_2 and Tr_3 can be made to behave like this depends on the characteristic that a transistor turned hard on will have a collector-emitter voltage drop of only some 0.1 to 0.4 volts, depending on construction and I_b and I_c, whereas the minimum voltage necessary at the base, for conduction, will be at least 0.5 volts in a silicon device.

The way in which this circuit is organized, with respect to its output circuitry, and its threshold, trigger, and reset inputs, is shown in Fig. 5. Because the transistor Tr_8, in the reset circuit, acts as a switch directly connected between the positive end of D_3 and the discharge circuit open-collector amplifier, this will cause Tr_3 to be turned off, with Tr_4 and Tr_6 turned on. This will reset both A_1 and A_2 outputs to the low level.

While this input, being connected later in the circuit than the trigger input, will over-ride the trigger signal, if the trigger input is held low, the circuit will revert to the operating condition, with A_1 high and A_2 open circuit, as soon as the reset signal is removed.

The two input amplifiers used in the threshold and trigger circuits, are of similar form, as shown in Figs 6 and 7, using Darlington connected, four-transistor, long-tailed pairs. However, it should be borne in mind, as explained in the first article of this series on the 741, that the integrated circuit manufacturing process does not normally allow the construction of p-n-p transistors, within the i.c., which have a very high current gain, except in the circumstance that their collectors are directly connected to the substrate, (which is normally the 0V line). Since the input p-n-p transistors of the trigger circuit do not meet this condition, they must be of the 'lateral' type, which gives an inferior input impedance to this amplifier to that of the n-p-n input devices

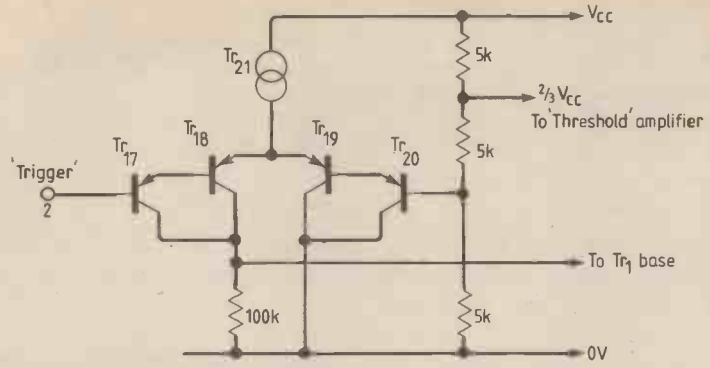


Fig. 7. *Trigger input amplifier, using p-n-p transistors.*

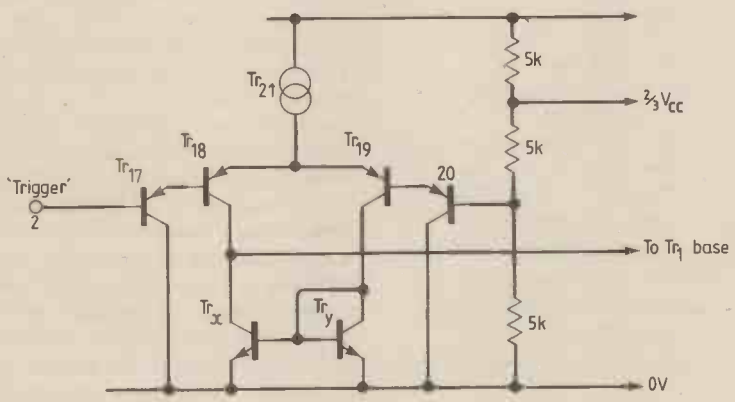


Fig. 8. *Improved trigger amplifier, using higher-gain p-n-p transistors and a current-mirror collector load for Tr_{18}.*

used on the threshold circuit input. To compensate somewhat for this deficiency, the trigger amplifier input circuit is operated at a very low collector current. Nevertheless, the input impedance for this circuit is still some five times lower than for the threshold input. In the National Semiconductor LM555, this circuit is modified, and improved, as shown in Fig. 8, to use a better type of input p-n-p transistor, together with a current mirror collector load (Tr_x and Tr_y).

The complete circuit of the 555 is given in Fig. 9, to show how the separate elements are connected together. Although the circuit is referred to in the data books as linear, because its operation is essentially digital in form, switching rapidly from one stable state to another, there is no need for any of the h.f. compensation of the amplifier elements customary in normal linear devices. This allows very fast rise and fall times at the output, of the order of 100ns, and repetitive operation at frequencies approaching 1MHz.

Typical time delay and free-running frequency graphs are shown, for completeness, in Figs. 10 and 11. □

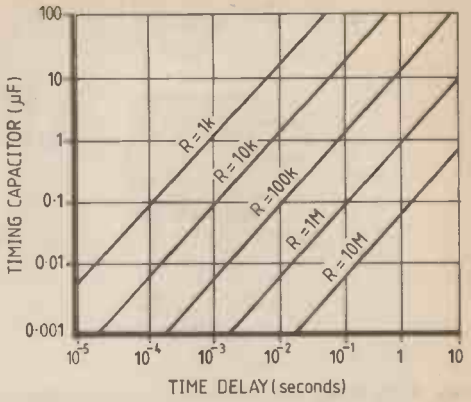


Fig. 10. *Time delay as a function of* R *and* C *in Fig. 1.*

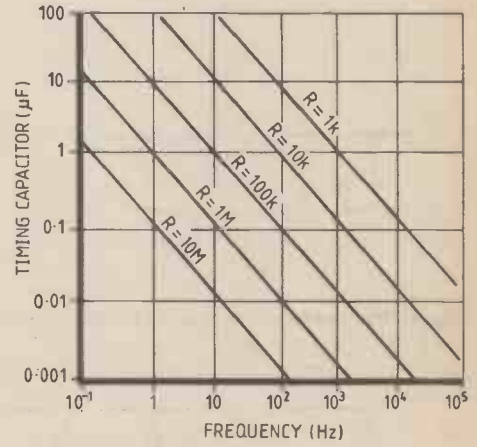


Fig. 11. *Variation of Fig. 3 oscillator frequency with* R *and* C *(constant-I source replaced by* R *if sawtooth linearity not important).*