CA3140, CA3140A, CA3140B Types

BiMOS Operational Amplifiers

With MOS/FET Input, Bipolar Output

The CA3140B, CA3140A, and CA3140 are integrated-circuit operational amplifiers that combine the advantages of high-voltage PMOS transistors with high-voltage bipolar transistors on a single monolithic chip. Because of this unique combination of technologies, this device can now provide designers, for the first time, with the special performance features of the CA3130 COS/MOS operational amplifiers and the versatility of the 741 series of industry-standard operational amplifiers.

The CA3140, CA3140A, and CA3140 BiMOS operational amplifiers feature gate-protected MOS/FET (PMOS) transistors in the input circuit to provide very-high-input impedance, very-low-input current, and high-speed performance. The CA3140B operates at supply voltages from 4 to 44 volts; the CA3140A and CA3140 from 4 to 36 volts (either single or dual supply). These operational amplifiers are internally phase-compensated to achieve stable operation in unity-gain follower operation, and, additionally, have access terminals for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset-voltage nulling.

The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute for single-supply applications. The output stage uses bipolar transistors and includes built-in protection against damage from load-terminal short-circuiting to either supply-rail or to ground.

The CA3140 Series has the same 8-lead terminal pin-out used for the "741" and other industry-standard operational amplifiers. They are supplied in either the standard 8-lead TO-5 style package (T suffix), or in the 8-lead dual-in-line formed-lead TO-5 style package "DIL-CAN" (S suffix). The CA3140 is available in chip form (H suffix). The CA3140A and CA3140 are also available in an 8-lead dual-in-line plastic package (Mini-DIP-E suffix). The CA3140B is intended for operation at supply voltages ranging from 4 to 44 volts, for applications requiring premium-grade specifications and with electrical limits established for operations over the range from −55°C to +125°C. The CA3140A and CA3140 are for operation at supply voltages up to 36 volts (±18 volts). The CA3140 ages up to 36 volts (±18 volts). All types can be operated safely over the temperature range from −55°C to +125°C.

Features:

- MOS/FET Input Stage
  - (a) Very high input impedance (Z_{IN}) − 1.5 TΩ typ.
  - (b) Very low input current (I_I) − 10 pA typ. at ± 15 V
  - (c) Low input-offset voltage (V_{IO}) − to 2 mV max.
  - (d) Wide common-mode input-voltage range (V_{ICR}) − can be swung 0.5 volt below negative supply-voltage rail
  - (e) Output swing complements input common-mode range
  - (f) Rugged input stage − bipolar diode protected
- Directly replaces industry type 741 in most applications
- Includes numerous industry operational amplifier categories such as general-purpose, FET input, wideband (high slew rate)
- Operation from 4-to-44 volts Single or Dual supplies
- Internally compensated
- Characterized for ± 15-volt operation and for TTL supply systems with operation down to 4 volts
- Wide bandwidth − 4.5 MHz unity gain at ± 15 V or 30 V; 3.7 MHz at 5 V
- High voltage-follower slew rate − 9 V/μs
- Fast settling time − 1.4 μs typ. to 10 mV with a 10-V_{p-p} signal
- Output swings to within 0.2 volt of negative supply
- Strobable output stage

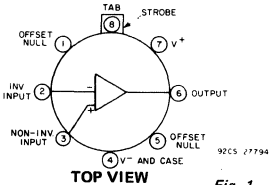
MAXIMUM RATINGS, *Absolute-Maximum Values:*

	CA3140, CA3140A	CA3140B
DC SUPPLY VOLTAGE (BETWEEN V^+ AND V^- TERMINALS)	36 V	44 V
DIFFERENTIAL-MODE INPUT VOLTAGE	±8 V	±8 V
COMMON-MODE DC INPUT VOLTAGE	(V^+ +8 V) to (V^- −0.5 V)	
INPUT-TERMINAL CURRENT	1 mA	
DEVICE DISSIPATION:		
WITHOUT HEAT SINK −		
UP TO 55°C	630 mW	
ABOVE 55°C	Derate linearly 6.67 mW/°C	
WITH HEAT SINK −		
Up to 55°C	1 W	
Above 55°C	Derate linearly 16.7 mW/°C	
TEMPERATURE RANGE:		
OPERATING (ALL TYPES)	−55 to + 125°C	
STORAGE (ALL TYPES)	−65 to +150°C	
OUTPUT SHORT-CIRCUIT DURATION*	INDEFINITE	
LEAD TEMPERATURE (DURING SOLDERING): AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM) FROM CASE FOR 10 SECONDS MAX.	+265°C	

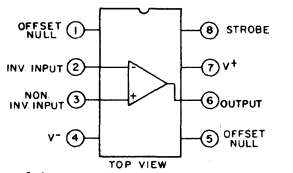
* Short circuit may be applied to ground or to either supply.

Applications:

- Ground-referenced single-supply amplifiers in automobile and portable instrumentation
- Sample and hold amplifiers
- Long-duration timers/multivibrators (microseconds−minutes−hours)
- Photocurrent instrumentation
- Peak detectors
- Active filters
- Comparators
- Interface in 5 V TTL systems & other low-supply voltage systems
- All standard operational amplifier applications
- Function generators
- Tone controls
- Power supplies
- Portable instruments
- Intrusion alarm systems



TOP VIEW
S and T Suffixes



E Suffix

Fig. 1 − Functional diagrams of the CA3140 series.

TYPICAL ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS $V^+ = +15$ V, $V^- = -15$ V, $T_A = 25^oC$		CA3140B (T,S)	CA3140A (T,S,E)	CA3140 (T,S,E)	UNITS
Input Offset Voltage Adjustment Resistor		Typ.Value of Resistor Between Term. 4 and 5 or 4 and 1 to Adjust Max. V_{IO}		43	18	4.7	kΩ
Input Resistance	R_I			1.5	1.5	1.5	TΩ
Input Capacitance	C_I			4	4	4	pF
Output Resistance	R_O			60	60	60	Ω
Equivalent Wideband Input Noise Voltage (See Fig. 39)	e_n	BW = 140 kHz, R_S = 1 MΩ		48	48	48	μV
Equivalent Input Noise Voltage (See Fig.10)	e_n	f = 1 kHz	R_S = 100 Ω	40	40	40	$nV/\sqrt{Hz}$
		f = 10 kHz		12	12	12	
Short-Circuit Current to Opposite Supply	Source I_{OM^+}			40	40	40	mA
	Sink I_{OM^-}			18	18	18	mA
Gain-Bandwidth Product, (See Figs. 5 &18)	f_T			4.5	4.5	4.5	MHz
Slew Rate, (See Fig.6)	SR			9	9	9	V/μs
Sink Current From Terminal 8 To Terminal 4 to Swing Output Low				220	220	220	μA
Transient Response: Rise Time	t_r	R_L = 2 kΩ, C_L = 100 pF		0.08	0.08	0.08	μs
Overshoot (See Fig. 37)				10	10	10	%
Settling Time at 10 V_{p-p}, (See Fig.17)	t_s 1 mV	R_L = 2 kΩ, C_L = 100 pF, Voltage Follower		4.5	4.5	4.5	μs
	t_s 10 mV			1.4	1.4	1.4	

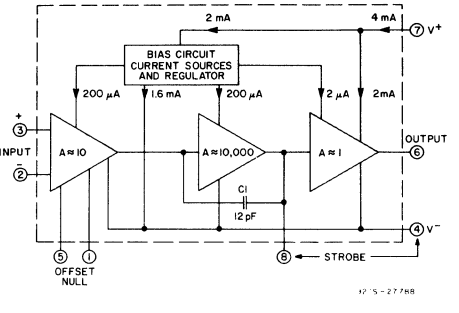


Fig.2 – Block diagram of CA3140 series.

CIRCUIT DESCRIPTION

Fig.2 is a block diagram of the CA3140 Series PMOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail. Two class A amplifier stages provide the voltage gain, and a unique class AB amplifier stage provides the current gain necessary to drive low-impedance loads.

A biasing circuit provides control of cascoded constant-current flow circuits in the first and second stages. The CA3140 includes an on-chip phase-compensating capacitor that is sufficient for the unity gain voltage-follower configuration.

Input Stages – The schematic circuit diagram of the CA3140 is shown in Fig.3. It consists of a differential-input stage using PMOS field-effect transistors (Q9, Q10) working into a mirror pair of bipolar transistors (Q11, Q12) functioning as load resistors together with resistors R2 through R5. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base-current drive to the second-stage bipolar transistor (Q13). Offset nulling, when desired, can be effected with a 10-kΩ potentiometer connected across terminals 1 and 5 and with its slider arm connected to terminal 4. Cascode-connected bipolar transistors Q2, Q5 are the constant-current source for the input stage. The base-biasing circuit for the constant-current source is described subsequently. The small diodes D3, D4, D5 provide gate-oxide protection against high-voltage transients, e.g., static electricity.

Second Stage – Most of the voltage gain in the CA3140 is provided by the second amplifier stage, consisting of bipolar transistor Q13 and its cascode-connected load resistance provided by bipolar transistors Q3, Q4. On-chip phase compensation, sufficient for a majority of the applications is provided by C1. Additional Miller-Effect compensation (roll-off) can be accomplished, when desired, by simply connecting a small capacitor between terminals 1 and 8. Terminal 8 is also used to strobe the output stage into quiescence. When terminal 8 is tied to the negative supply rail (terminal 4) by mechanical or electrical means, the output terminal 6 swings low, i.e., approximately to terminal 4 potential.

Output Stage – The CA3140 Series circuits employ a broadband output stage that can sink loads to the negative supply to complement the capability of the PMOS input stage when operating near the negative rail. Quiescent current in the emitter-follower cascade circuit (Q17, Q18) is established by transistors (Q14, Q15) whose base-currents are "mirrored" to current flowing through diode D2 in the bias circuit section. When the CA3140 is operating such that output terminal 6 is sourcing current, transistor Q18 functions as an emitter-follower to source current from the V+ bus (terminal 7), via D7, R9, and R11. Under these conditions, the collector potential of Q13 is sufficiently high to permit the necessary flow of base current to emitter follower Q17 which, in turn, drives Q18.

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At $V^+ = 15$ V, $V^- = 15$ V, $T_A = 25^oC$ Unless Otherwise Specified

CHARACTERISTIC	LIMITS									UNITS
	CA3140B			CA3140A			CA3140			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$	–	0.8	2	–	2	5	–	5	15	mV
Input Offset Current, $\|I_{IO}\|$	–	0.5	10	–	0.5	20	–	0.5	30	pA
Input Current, I_I	–	10	30	–	10	40	–	10	50	pA
Large-Signal Voltage Gain, A_{OL}● (See Figs. 4,18)	50 k	100 k	–	20 k	100 k	–	20 k	100 k	–	V/V
	94	100	–	86	100	–	86	100	–	dB
Common-Mode Rejection Ratio, CMRR (See Fig.9)	–	20	50	–	32	320	–	32	320	μV/V
	86	94	–	70	90	–	70	90	–	dB
Common-Mode Input-Voltage Range, V_{ICR} (See Fig.20)	−15	−15.5 to +12.5	12	−15	−15.5 to +12.5	12	−15	−15.5 to +12.5	11	V
Power-Supply Rejection Ratio, PSRR $\Delta V_{IO}/\Delta V$ (See Fig.11)	–	32	100	–	100	150	–	100	150	μV/V
	80	90	–	76	80	–	76	80	–	dB
Max. Output Voltage■ V_{OM}^+ (See Figs.13,20) V_{OM}^-	+12	13	–	+12	13	–	+12	13	–	V
	−14	−14.4	–	−14	−14.4	–	−14	−14.4	–	
Supply Current, I^+ (See Fig.7)	–	4	6	–	4	6	–	4	6	mA
Device Dissipation, P_D	–	120	180	–	120	180	–	120	180	mW
Input Current, I_I▲ (See Fig.19)	–	10	30	–	10	–	–	10	–	nA
Input Offset Voltage $\|V_{IO}\|$▲	–	1.3	3	–	3	–	–	10	–	mV
Input Offset Voltage Temp. Drift, $\Delta V_{IO}/\Delta T$	–	5	–	–	6	–	–	8	–	μV/°C
Large-Signal Voltage Gain, A_{OL}▲ (See Figs.4,18)	20 k	100 k	–	–	100 k	–	–	100 k	–	V/V
	86	100	–	–	100	–	–	100	–	dB
Max. Output Voltage,★ V_{OM}^+ V_{OM}^-	+19	+19.5	–	–	–	–	–	–	–	V
	−21	−21.4	–	–	–	–	–	–	–	
Large-Signal Voltage Gain, A_{OL}♦★	20 k	50 k	–	–	–	–	–	–	–	V/V
	86	94	–	–	–	–	–	–	–	dB

● At $V_O = 26V_{p\text{-}p}$, +12V, −14V and $R_L = 2$ kΩ. ■ At $R_L = 2$ kΩ.

▲ At $T_A = -55^oC$ to $+125^oC$, $V^+ = 15$ V, $V^- = 15$ V, $V_O = 26V_{p\text{-}p}$, $R_L = 2$ kΩ.

♦ At $V_O = +19$ V, −21 V, and $R_L = 2$ kΩ. ★ At $V^+ = 22$ V, $V^- = 22$ V.

When the CA3140 is operating such that output terminal 6 is sinking current to the V− bus, transistor Q16 is the current-sinking element. Transistor Q16 is mirror-connected to D6, R7, with current fed by way of Q21, R12, and Q20. Transistor Q20, in turn, is biased by current-flow through R13, zener D8, and R14. The dynamic current-sink is controlled by voltage-level sensing. For purposes of explanation, it is assumed that output terminal 6 is quiescently established at the potential mid-point between the V+ and V− supply rails. When output-current sinking-mode operation is required, the collector potential of transistor Q13 is driven below its quiescent level, thereby causing Q17, Q18 to decrease the output voltage at terminal 6. Thus, the gate terminal of PMOS transistor Q21 is displaced toward the V− bus, thereby reducing the channel resistance of Q21. As a consequence, there is an incremental increase in current flow through Q20, R12, Q21, D6, R7, and the base of Q16. As a result, Q16 sinks current from terminal 6 in direct response to the incremental change in output voltage caused by Q18. This sink current flows regardless of load; any excess current is internally supplied by the emitter-follower Q18. Short-circuit protection of the output circuit is provided by Q19, which is driven into conduction by the high voltage drop developed across R11 under output short-circuit conditions. Under these conditions, the collector of Q19 diverts current from Q4 so as to reduce the base-current drive from Q17, thereby limiting current flow in Q18 to the short-circuited load terminal.

Bias Circuit – Quiescent current in all stages (except the dynamic current sink) of the CA3140 is dependent upon bias current flow in R1. The function of the bias circuit is to establish and maintain constant-current flow through D1, Q6, Q8 and D2. D1 is a diode-connected transistor mirror-connected in parallel with the base-emitter junctions of Q1, Q2, and Q3. D1 may be considered as a current-sampling diode that senses the emitter current of Q6 and automatically adjusts the base current of Q6 (via Q1) to maintain a constant current through Q6, Q8, D2. The base-currents in Q2, Q3 are also determined by constant-current flow D1. Furthermore, current in diode-connected transistor D2 establishes the currents in transistors Q14 and Q15.

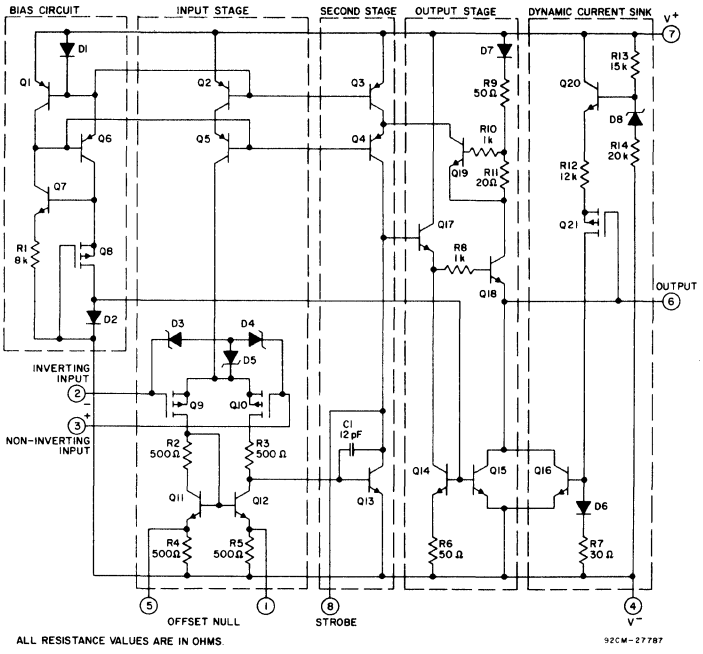


Fig.3 – Schematic diagram of CA3140 series.

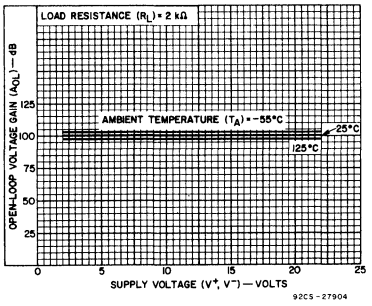


Fig.4 – Open-loop voltage gain vs supply voltage and temperature.

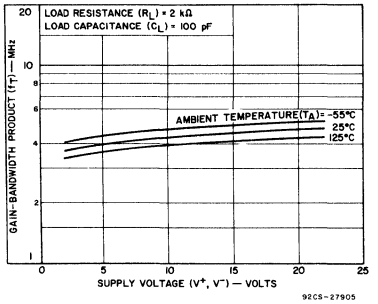


Fig.5 – Gain-bandwidth product vs supply voltage and temperature.

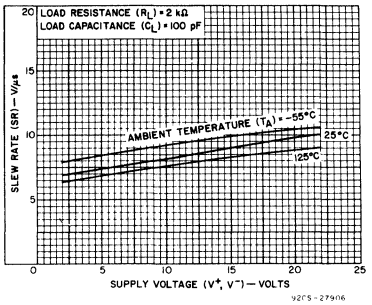


Fig.6 – Slew rate vs supply voltage andtemperature.

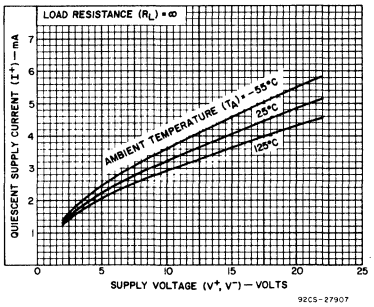


Fig.7 – Quiescent supply current vs supply voltage and temperature.

TYPICAL ELECTRICAL CHARACTERISTICS FOR DESIGN GUIDANCE

At $V^+ = 5$ V, $V^- = 0$ V, $T_A = 25^oC$

CHARACTERISTIC		CA3140B (T,S)	CA3140A (T,S,E)	CA3140 (T,S,E)	UNITS
Input Offset Voltage	$\|V_{IO}\|$	0.8	2	5	mV
Input Offset Current	$\|I_{IO}\|$	0.1	0.1	0.1	pA
Input Current	I_I	2	2	2	pA
Input Resistance		1	1	1	TΩ
Large-Signal Voltage Gain	A_{OL}	100 k	100 k	100 k	V/V
(See Figs.4,18)		100	100	100	dB
Common-Mode Rejection Ratio,	CMRR	20	32	32	μV/V
		94	90	90	dB
Common-Mode Input-Voltage Range	V_{ICR}	−0.5	−0.5	−0.5	V
(See Fig.20)		2.6	2.6	2.6	
Power-Supply Rejection Ratio	$\Delta V_{IO}/\Delta V^+$	32	100	100	μV/V
		90	80	80	dB
Maximum Output Voltage	V_{OM}^+	3	3	3	V
(See Figs.13,20)	V_{OM}^-	0.13	0.13	0.13	
Maximum Output Current:					
Source	I_{OM}^+	10	10	10	mA
Sink	I_{OM}^-	1	1	1	
Slew Rate (See Fig.6)		7	7	7	V/μs
Gain-Bandwidth Product (See Fig.5)	f_T	3.7	3.7	3.7	MHz
Supply Current (See Fig.7)	I^+	1.6	1.6	1.6	mA
Device Dissipation	P_D	8	8	8	mW
Sink Current from Term. 8 to Term. 4 to Swing Output Low		200	200	200	μA

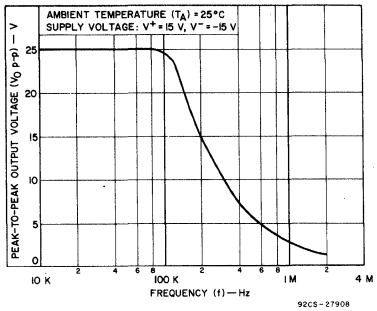


Fig.8 – Maximum output voltage swing vs frequency.

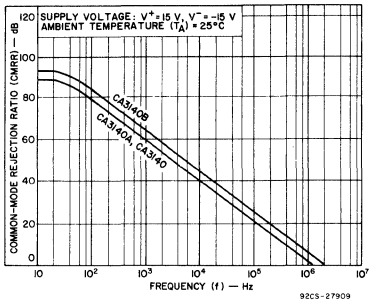


Fig.9 – Common-mode rejection ratio vs frequency.

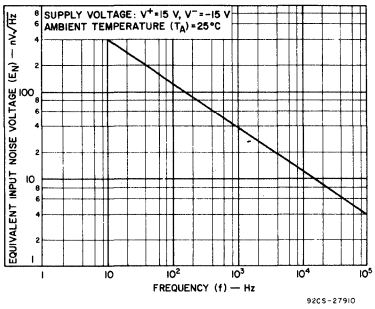


Fig.10 – Equivalent input noise voltage vs frequency.

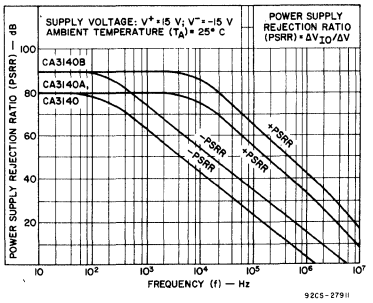


Fig.11 – Power supply rejection ratio vs frequency.

APPLICATIONS CONSIDERATIONS

Wide dynamic range of input and output characteristics with the most desirable high input-impedance characteristic is achieved in the CA3140 by the use of an unique design based upon the PMOS-Bipolar process. Input-common-mode voltage range and output-swing capabilities are complementary, allowing operation with the single supply down to four volts.

The wide dynamic range of these parameters also means that this device is suitable for many single-supply applications, such as, for example, where one input is driven below the potential of terminal 4 and the phase sense of the output signal must be maintained – a most important consideration in comparator applications.

OUTPUT CIRCUIT CONSIDERATIONS

Excellent interfacing with TTL circuitry is easily achieved with a single 6.2-volt zener diode connected to terminal 8 as shown in Fig.12. This connection assures that the maximum output signal swing will not go more positive than the zener voltage minus two base-to-emitter voltage drops within the CA3140. These voltages are independent of the operating supply voltage.

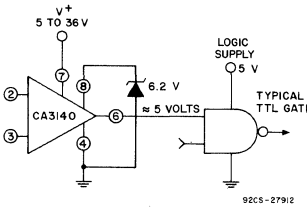


Fig.12 – Zener clamping diode connected to terminals 8 and 4 to limit CA3140 output swing to TTL levels.

Fig.13 shows output current-sinking capabilities of the CA3140 at various supply voltages. Output voltage swing to the negative supply rail permits this device to operate both power transistors and thyristors directly without the need for level-shifting circuitry usually associated with the 741 series of operational amplifiers.

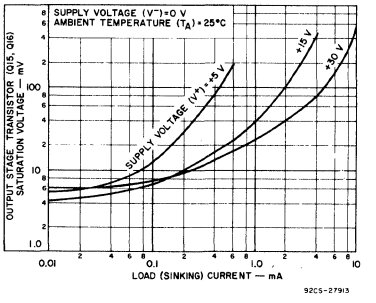


Fig.13 – Voltage across output transistors Q15 and Q16 vs load current.

Fig.16 show some typical configurations. Note that a series resistor, R_L, is used in both cases to limit the drive available to the driven device. Moreover, it is recommended that a series diode and shunt diode be used at the thyristor input to prevent large negative transient surges that can appear at the gate of thyristors, from damaging the integrated circuit.

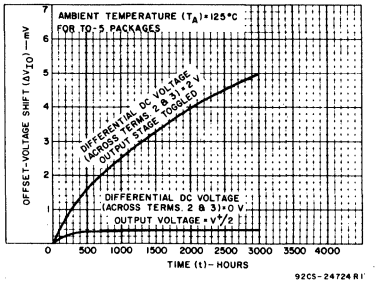


Fig.14 – Typical incremental offset-voltage shift vs operating life.

OFFSET-VOLTAGE NULLING

The input-offset voltage can be nulled by connecting a 10-kΩ potentiometer between terminals 1 and 5 and returning its wiper arm to terminal 4, see Fig.15a. This technique, however, gives more adjustment range than required and therefore, a considerable portion of the potentiometer rotation is not fully utilized. Typical values of series resistors that may be placed at either end of the potentiometer, see Fig.15b, to optimize its utilization range are given in the table "Typical Electrical Characteristics" shown in this bulletin.

An alternate system is shown in Fig.15c. This circuit uses only one additional resistor of approximately the value shown in the table. For potentiometers, in which the resistance does not drop to zero ohms at either end of rotation, a value of resistance 10% lower than the values shown in the table should be used.

LOW-VOLTAGE OPERATION

Operation at total supply voltages as low as 4 volts is possible with the CA3140. A current regulator based upon the PMOS threshold voltage maintains reasonable constant operating current and hence consistent performance down to these lower voltages.

The low-voltage limitation occurs when the upper extreme of the input common-mode voltage range extends down to the voltage at terminal 4. This limit is reached at a total supply voltage just below 4 volts. The output voltage range also begins to extend down to the negative supply rail, but is slightly higher than that of the input. Fig.20 shows these characteristics and shows that with 2-volt dual supplies, the lower extreme of the input common-mode voltage range is below ground potential.

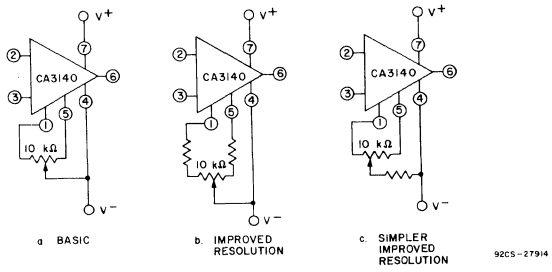


Fig.15 – Three offset-voltage nulling methods.

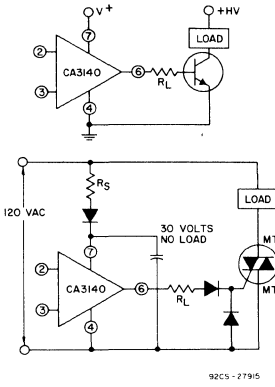


Fig.16 – Methods of utilizing the $V_{CE(sat)}$ sinking-current capability of the CA3140 series.

BANDWIDTH AND SLEW RATE

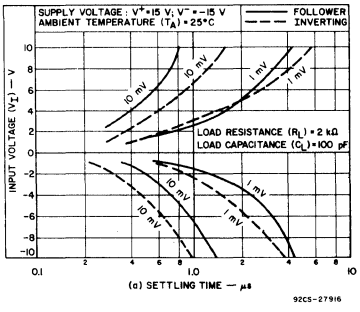
For those cases where bandwidth reduction is desired, for example, broadband noise reduction, an external capacitor connected between terminals 1 and 8 can reduce the open-loop −3 dB bandwidth. The slew rate will, however, also be proportionally reduced by using this additional capacitor. Thus, a 20% reduction in bandwidth by this technique will also reduce the slew rate by about 20%.

Fig.17 shows the typical settling time required to reach 1 mV or 10 mV of the final value for various levels of large signal inputs for the voltage-follower and inverting unity-gain amplifiers. The exceptionally fast settling time characteristics shown in Fig.18 are largely due to the high combination of high gain and wide bandwidth of the CA3140.

INPUT CIRCUIT CONSIDERATIONS

As mentioned previously, the amplifier inputs can be driven below the terminal 4 potential, but a series current-limiting resistor is recommended to limit the maximum input terminal current to less than 1 mA to prevent damage to the input protection circuitry.

Moreover, some current-limiting resistance should be provided between the inverting input and the output when the CA3140 is used as a unity-gain voltage follower. This resistance prevents the possibility of extremely large input-signal transients from forcing a signal through the input-protection network and directly driving the internal constant-current source which could result in positive feedback via the output terminal. A 3.9-kΩ resistor is sufficient.



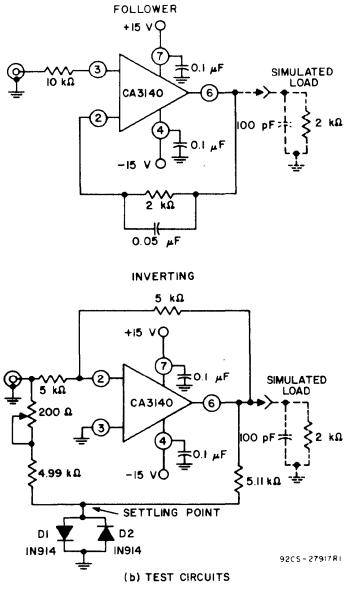


Fig.17 – Input voltage vs settling time.

The typical input current is in the order of 10 pA when the inputs are centered at nominal device dissipation. As the output supplies load current, device dissipation will increase, raising the chip temperature and resulting in increased input current. Fig.19 shows typical input-terminal current versus ambient temperature for the CA3140.

It is well known that MOS/FET devices can exhibit slight changes in characteristics (for example, small changes in input offset voltage) due to the application of large differential input voltages that are sustained over long periods at elevated temperatures.

Both applied voltage and temperature accelerate these changes. The process is reversible and offset voltage shifts of the opposite polarity reverse the offset. Fig.14 shows the typical offset voltage change as a function of various stress voltages at the maximum rating of 125°C (for TO-5); at lower temperatures (TO-5 and plastic), for example, at 85°C, this change in voltage is considerably less. In typical linear applications, where the differential voltage is small and symmetircal, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar a transistor input stage.

SUPER SWEEP FUNCTION GENERATOR

A function generator having a wide tuning range is shown in Fig.21. The 1,000,000/1 adjustment range is accomplished by a single variable potentiometer or by an auxiliary sweeping signal. The CA3140 functions as a non-inverting read-out amplifier of the tri-

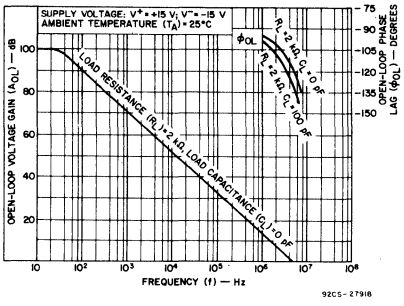


Fig.18 – Open-loop voltage gain and phase lag vs frequency.

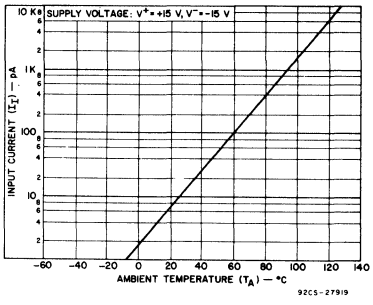


Fig.19 – Input current vs ambient temperature.

angular signal developed across the integrating capacitor network connected to the output of the CA3080A current source.

Buffered triangular output signals are then applied to a second CA3080 functioning as a high-speed hysteresis switch. Output from the switch is returned directly back to the

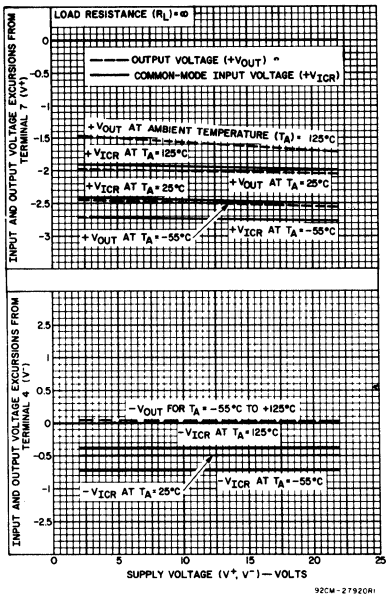


Fig.20 — Output-voltage-swing capability and common-mode input-voltage range vs supply voltage and temperature.

input of the CA3080A current source, thereby, completing the positive feedback loop.

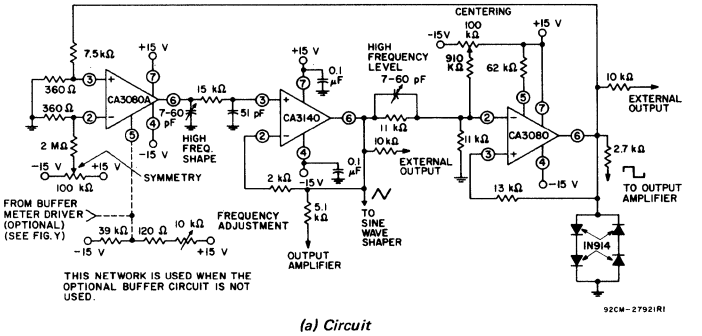
The triangular output level is determined by the four 1N914 level-limiting diodes of the second CA3080 and the resistor-divider network connected to terminal No.2 (input) of the CA3080. These diodes establish the input trip level to this switching stage and, therefore, indirectly determine the amplitude of the output triangle.

Compensation for propagation delays around the entire loop is provided by one adjustment on the input of the CA3080. This adjustment, which provides for a constant generator amplitude output, is most easily made while the generator is sweeping. High-frequency ramp linearity is adjusted by the single 7-to-60 pF capacitor in the output of the CA3080A.

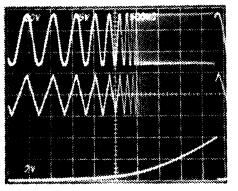
It must be emphasized that only the CA-3080A is characterized for maximum output linearity in the current-generator function.

METER DRIVER AND BUFFER AMPLIFIER

Fig. 22 shows the CA3140 connected as a meter driver and buffer amplifier. Low driving impedance is required of the CA-3080A current source to assure smooth operation of the Frequency Adjustment



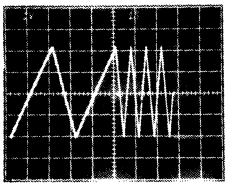
(a) Circuit



TOP TRACE: OUTPUT AT JUNCTION OF 2.7 Ω AND 51 Ω RESISTORS
5 V/DIV AND 500 ms/DIV
CENTER TRACE: EXTERNAL OUTPUT OF TRIANGULAR FUNCTION GENERATOR
2 V/DIV AND 500 ms/DIV
BOTTOM TRACE: OUTPUT OF "LOG" GENERATOR
10 V/DIV AND 500 ms/DIV

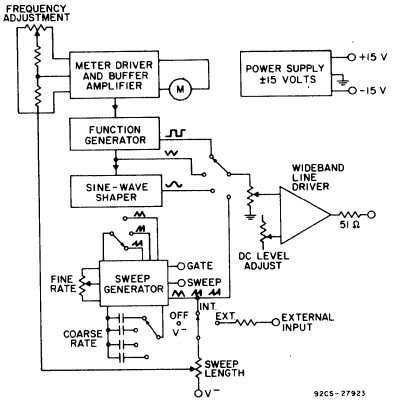
92CS-27922

(b1) Function generator sweeping



92CS-27937

(b2) Function generator with fixed frequencies



(c) Interconnections

1V/DIV and 1 sec/DIV

Three tone test signals, highest frequency ⩾ 0.5 MHz. Note the slight assymmetry at the three-second/cycle signal. This assymmetry is due to slightly different positive and negative integration from the CA3080A and from the pc board and component leakages at the 100-pA level.

Fig.21 — Function generator.

Control. This low-driving impedance requirement is easily met by using a CA3140 connected as a voltage follower. Moreover, a meter may be placed across the input to the CA3080A to give a logarithmic analog indication of the function generators frequency.

Analog frequency readout is readily accomplished by the means described above because the output current of the CA3080A varies approximately one decade for each 60-mV change in the applied voltage, V_{ABC} (voltage between terminals 5 and 4 of the CA3080A of the function generator). Therefore, six decades represent 360-mV change in V_{ABC}.

Now, only the reference voltage must be established to set the lower limit on the meter. The three remaining transistors from the CA3086 Array used in the sweep generator are used for this reference voltage. In addition, this reference generator arrangement tends to track ambient temperature variations, and thus compensates for the effects of the normal negative temperature coefficient of the CA3080A V_{ABC} terminal voltage.

Another output voltage from the reference generator is used to insure temperature tracking of the lower end of the Frequency Adjustment Potentiometer. A large series resistance simulates a current source, assuring similar temperature coefficients at both ends of the Frequency Adjustment Control.

To calibrate this circuit, set the Frequency Adjustment Potentiometer at its low end. Then adjust the Minimum Frequency Calibration Control for the lowest frequency. To

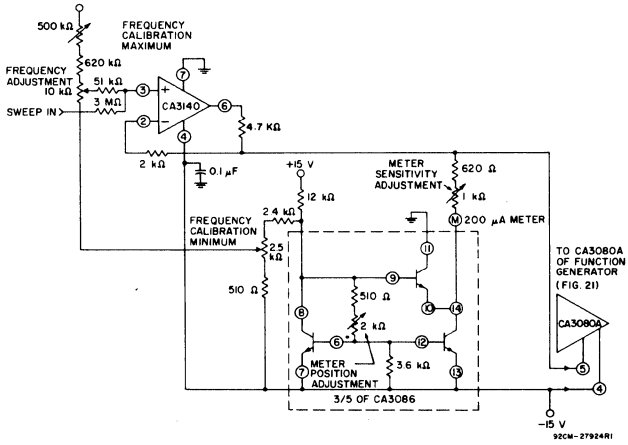


Fig. 22 – Meter driver and buffer amplifier.

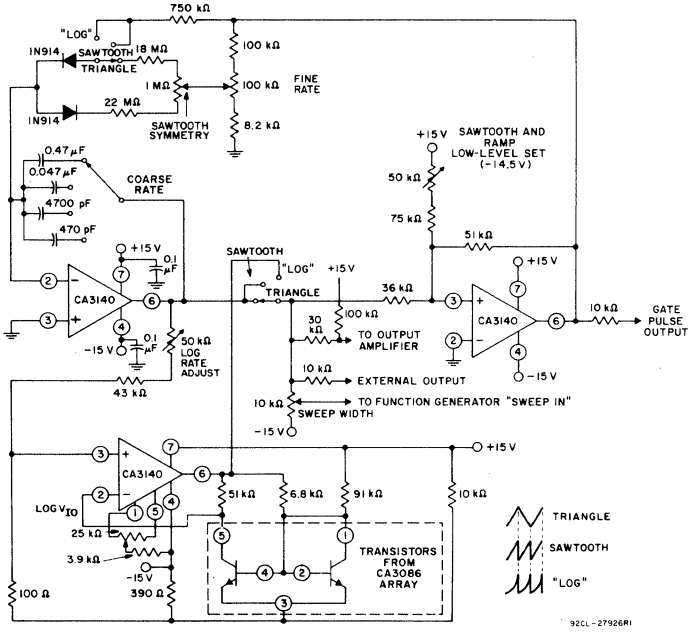


Fig. 24 – Sweeping generator.

establish the upper frequency limit, set the Frequency Adjustment Potentiometer to its upper end and then adjust the Maximum Frequency Calibration Control for the maximum frequency. Because there is interaction among these controls, repetition of the adjustment procedure may be necesary.

Two adjustments are used for the meter. The meter sensitivity control sets the meter-scale width of each decade, while the meter position control adjusts the pointer on the scale with negligible effect on the sensitivity adjustment. Thus, the meter sensitivity adjustment control calibrates the meter so that it deflects 1/6 of full scale for each decade change in frequency.

SINE-WAVE SHAPER

The circuit shown in Fig. 23 uses a CA3140 as a voltage follower in combination with diodes from the CA3019 Array to convert the triangular signal from the function generator to a sine-wave output signal having typically less than 2% THD. The basic zero-crossing slope is established by the 10-kΩ

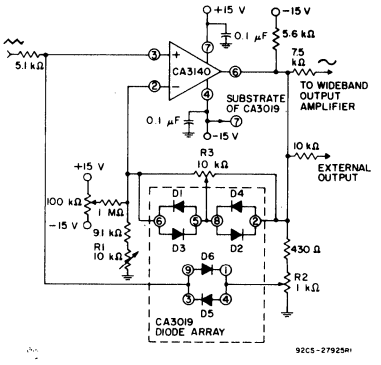


Fig. 23 – Sine-wave shaper.

potentiometer connected between terminals 2 and 6 of the CA3140 and the 9.1-kΩ resistor and 10-kΩ potentiometer from terminal 2 to ground. Two break points are established by diodes D_1 through D_4. Positive feedback via D_5 and D_6 establishes the zero slope at the maximum and minimum levels of the sine wave. This technique is necessary because the voltage-follower configuration approaches unity gain rather than the zero gain required to shape the sine wave at the two extremes.

This circuit can be adjusted most easily with a distortion analyzer, but a good first approximation can be made by comparing the output signal with that of a sine-wave generator. The initial slope is adjusted with the potentiometer R_1, followed by an adjustment of R_2. The final slope is established by adjusting R_3, thereby adding additional segments that are contributed by these diodes. Because there is some interaction among these controls, repetition of the adjustment procedure may be necessarv

SWEEPING GENERATOR

Fig. 24 shows a sweeping generator. Three CA3140's are used in this circuit. One CA3140 is used as an integrator, a second device is used as a hysteresis switch that determines the starting and stopping points of the sweep. A third CA3140 is used as a logarithmic shaping network for the log function. Rates and slopes, as well as sawtooth, triangle, and logarithmic sweeps are generated by this circuit.

WIDEBAND OUTPUT AMPLIFIER

Fig. 25 shows a high-slew-rate, wideband amplifier suitable for use as a 50-ohm transmission-line driver. This circuit, when used in conjunction with the function generator and sine-wave shaper circuits shown in Figs. 21 and 23 provides 18 volts peak-to-peak output open-circuited, or 9 volts peak-to-peak output when terminated in 50 ohms. The slew rate required of this amplifier is 28 volts/μs (18 volts peak-to-peak x π x 0.5 MHz).

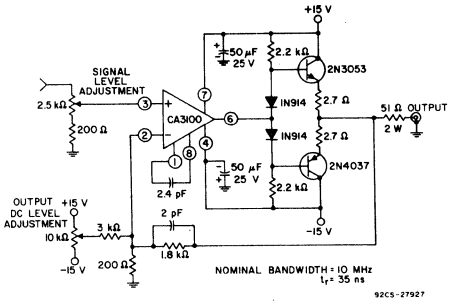


Fig. 25 – Wideband output amplifier.

POWER SUPPLIES

High input-impedance, common-mode capability down to the negative supply and high output-drive current capability are key factors in the design of wide-range output-voltage supplies that use a single input voltage to provide a regulated output voltage that can be adjusted from essentially 0 to 24 volts.

Unlike many regulator systems using comparators having a bipolar transistor-input stage, a high-impedance reference-voltage divider from a single supply can be used in connection with the CA3140 (see Fig. 26).

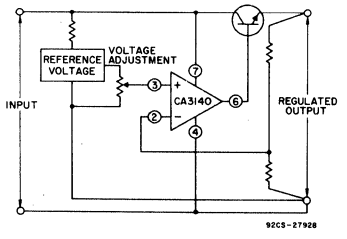


Fig. 26 – Basic single-supply voltage regulator showing voltage-follower configuration.

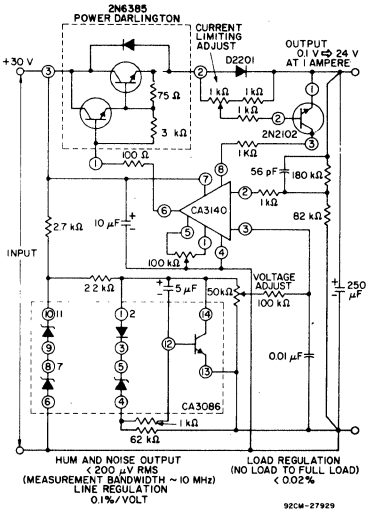


Fig. 27 – Regulated power supply.

In spite of those limitations, the current limiting point can easily be adjusted over the range from 10 mA to 1 ampere with a single adjustment potentiometer. If the temperature stability of the current-limiting

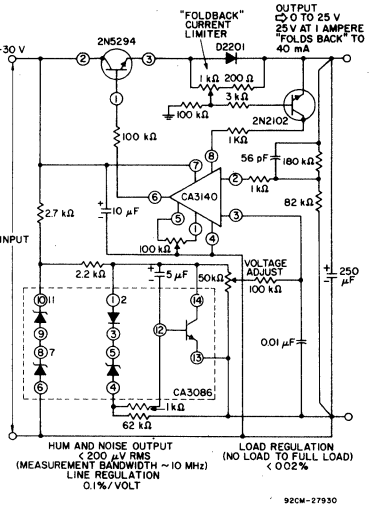
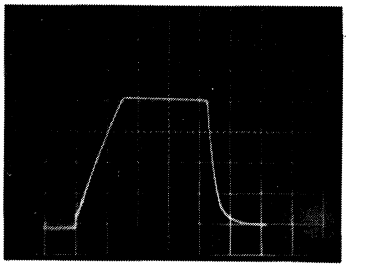
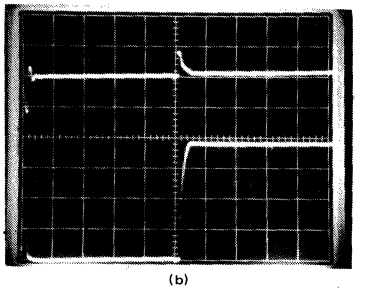


Fig. 28 – Regulated power supply with "foldback" current limiting.



(a)

SUPPLY TURN-ON AND TURN-OFF CHARACTERISTICS
(5 VOLTS / DIV. AND -1 s/DIV.)
92CS-27882



(b)

TRANSIENT RESPONSE
TOP TRACE : OUTPUT VOLTAGE (200 mV/DIV AND 5 µs/DIV)
BOTTOM TRACE : COLLECTOR OF LOAD SWITCHING TRANSISTOR, LOAD = 1 AMPERE (5 VOLTS/DIV AND 5 µs/DIV)
92CS-27881

Fig. 29 – Waveforms of dynamic characteristics of power supply currents shown in Figs. 29 and 30.

Essentially, the regulators, shown in Figs. 27 and 28, are connected as non-inverting power operational amplifiers with a gain of 3.2. An 8-volt reference input yields a maximum output voltage slightly greater than 25 volts. As a voltage follower, when the reference input goes to 0 volts the output will be 0 volts. Because the offset voltage is also multiplied by the 3.2 gain factor, a potentiometer is needed to null the offset voltage.

Series pass transistors with high I_{CBO} levels will also prevent the output voltage from reaching zero because there is a finite voltage drop (V_{CE}sat) across the output of the CA3140 (see Fig.13). This saturation voltage level may indeed set the lowest voltage obtainable.

The high impedance presented by terminal 8 is advantageous in effecting current limiting. Thus, only a small signal transistor is required for the current-limit sensing amplifier. Resistive decoupling is provided for this transistor to minimize damage to it or the CA3140 in the event of unusual input or output transients on the supply-rail.

Figs. 27 and 28, show circuits in which a D2201 high-speed diode is used for the current sensor. This diode was chosen for its slightly higher forward-voltage drop characteristic thus giving greater sensitivity. It must be emphasized that heat sinking of this diode is essential to minimize variation of the current trip point due to internal heating of the diode. That is, 1 ampere at 1 volt forward drop represents one watt which can result in significant regenerative changes in the current trip point as the diode temperature rises. Placing the small-signal reference amplifier in the proximity of the current-sensing diode also helps minimize the variability in the trip level due to the negative temperature coefficient of the diode.

system is a serious consideration, the more usual current-sampling resistor-type of circuitry should be employed.

A power Darlington transistor (in a heat sink TO-3 case), is used as the series-pass element for the conventional current-limiting system, Fig. 27, because high-power Darlington dissipation will be encountered at low output voltage and high currents.

A small heat-sink VERSAWATT transistor is used as the series-pass element in the foldback current system, Fig.28, since dissipation levels will only approach 10 watts. In this system, the D2201 diode is used for current sampling. Foldback is provided by the 3 kΩ and 100 kΩ divider network connected to the base of the current-sensing transistor.

Both regulators, Figs. 27 and 28, provide better than 0.02% load regulation. Because there is constant loop gain at all voltage settings, the regulation also remains constant. Line regulation is 0.1% per volt. Hum and noise voltage is less than 200 μV as read with a meter having a 10-MHz bandwidth.

Fig.31 (a) shows the turn ON and turn OFF characteristics of both regulators. The slow turn-on rise is due to the slow rate of rise of the reference voltage. Fig. 29 (b) shows the transient response of the regulator with the switching of a 20-Ω load at 20 volts output.

TONE CONTROL CIRCUITS

High-slew-rate, wide-bandwidth, high-output voltage capability and high input impedance are all characteristics required of tone-control amplifiers. Two tone control circuits that exploit these characteristics of the CA3140 are shown in Figs. 30 and 31.

The first circuit, shown in Fig. 31, is the Baxandall tone-control circuit which provides unity gain at midband and uses standard linear potentiometers. The high input impedance of the CA3140 makes possible the use of low-cost, low-value, small-size capacitors, as well as reduced load of the driving stage.

Bass treble boost and cut are ± 15 dB at 100 Hz and 10 kHz, respectively. Full peak-to-peak output is available up to at least 20 kHz due to the high slew rate of the CA3140. The amplifier gain is −3 dB down from its "flat" position at 70 kHz.

Fig. 30 shows another tone-control circuit with similar boost and cut specifications. The wideband gain of this circuit is equal to the ultimate boost or cut plus one, which in this case is a gain of eleven. For 20-dB boost and cut, the input loading of this circuit is essentially equal to the value of the resistance from terminal No.3 to ground. A detailed analysis of this circuit is given in "An IC Operational Transconductance Amplifier (OTA) With Power Capability" by L. Kaplan and H. Wittlinger, IEEE Transactions on Broadcast and Television Receivers, Vol. BTR-18, No.3, August, 1972.

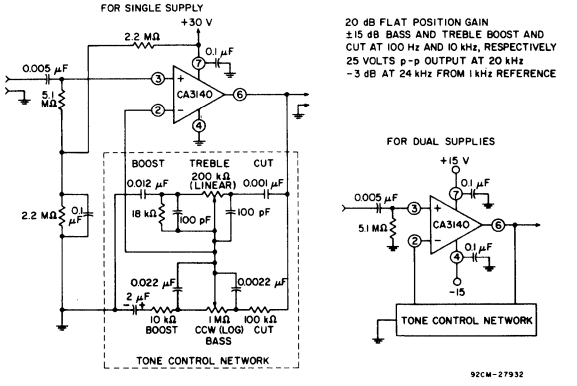


Fig. 30 — Tone control circuit using CA3130 series (20-dB midband gain).

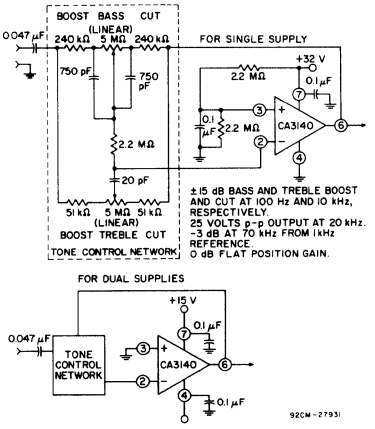


Fig. 31 — Baxandall tone control circuit using CA3140 series.

WIEN BRIDGE OSCILLATOR

Another application of the CA3140 that makes excellent use of its high input-impedance, high-slew-rate, and high-voltage qualities is the Wien Bridge sine-wave oscillator. A basic Wien Bridge oscillator is shown in Fig. 32. When $R_1 = R_2 = R$ and $C_1 = C_2 = C$, the frequency equation reduces to the familiar $f = 1/2\pi RC$ and the gain required for oscillation, A_{OSC} is equal to 3. Note that if C_2 is increased by a factor of four and R_2 is reduced by a factor of four, the gain required for oscillation becomes 1.5, thus permitting a potentially higher operating frequency closer to the gain-bandwidth product of the CA3140.

Oscillator stabilization takes on many forms. It must be precisely set, otherwise the amplitude will either diminish or reach some form of limiting with high levels of distortion. The element, R_S, is commonly replaced with some variable resistance element. Thus, through some control means, the value of R_S is adjusted to maintain constant oscillator output. A FET channel resistance, a thermistor, a lamp bulb, or other device whose resistance is made to increase as the output amplitude is increased are a few of the elements often utilized.

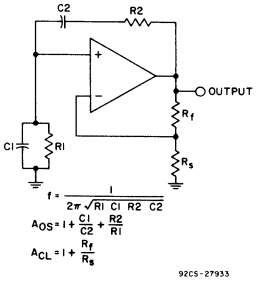


Fig. 32 — Basic Wien bridge oscillator circuit using an operational amplifier.

Fig. 33 shows another means of stabilizing the oscillator with a zener diode shunting the feedback resistor (R_f of Fig. 32). As the output signal amplitude increases, the zener diode impedance decreases resulting in more feedback with consequent reduction in gain; thus stabilizing the amplitude of the output signal. Furthermore, this combination of a monolithic zener diode and bridge rectifier circuit tends to provide a zero temperature coefficient for this regulating system. Because this bridge rectifier system has no time constant, i.e., thermal time constant for the lamp bulb, and RC time constant for filters often used in detector networks, there is no lower frequency limit. For example, with 1-μF polycarbonate capacitors and 22 MΩ for the frequency determining network, the operating frequency is 0.007 Hz.

As the frequency is increased, the output amplitude must be reduced to prevent the output signal from becoming slew-rate limited. An output frequency of 180 kHz will reach a slew rate of approximately 9 volts/μs when its amplitude is 16 volts peak-to-peak.

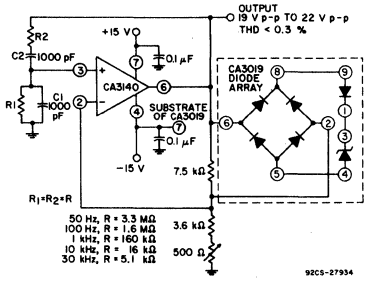


Fig. 33 – Wien bridge oscillator circuit using CA3140 series.

SIMPLE SAMPLE-AND-HOLD SYSTEM

Fig. 34 shows a very simple sample-and-hold system using the CA3140 as the readout amplifier for the storage capacitor. The CA3080A serves as both input buffer amplifier and low feed-through transmission switch.* System offset nulling is accomplished with the CA3140 via its offset nulling terminals. A typical simulated load of 2 kΩ and 30 pF is shown in the schematic.

In this circuit, the storage compensation capacitance (C_1) is only 200 pF. Larger value capacitors provide longer "hold" periods but with slower slew rates. The slew rate

$$\frac{dv}{dt} = \frac{i}{c} = 0.5 \text{ mA}/200 \text{ pF} = 2.5 \text{ V}/\mu\text{s}.$$

* ICAN-6668 "Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers".

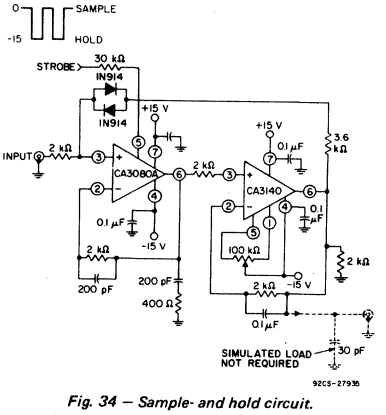
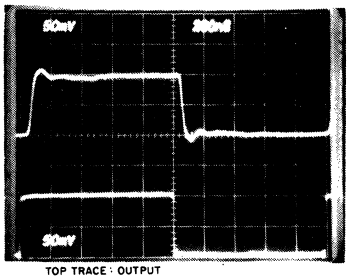
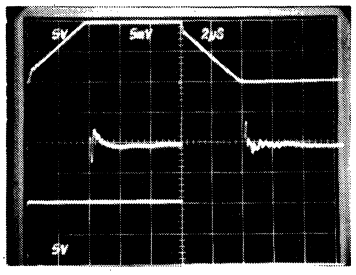


Fig. 34 – Sample- and hold circuit.

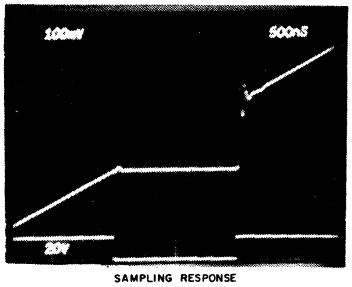
Pulse "droop" during the hold interval is 170 pA/200 pF which is = 0.85 μV/μs; (i.e., 170 pA/200 pF). In this case, 170 pA represents the typical leakage current of the CA3080A when strobed off. If C_1 were increased to 2000 pF, the "hold-droop" rate will decrease to 0.085 μV/μs, but the slew rate would decrease to 0.25 V/μs. The parallel diode network connected between terminal 3 of the CA3080A and terminal 6 of the CA3140 prevents large input-signal feed-through across the input terminals of the CA3080A to the 200 pF storage capacitor when the CA3080A is strobed off. Fig. 35 shows dynamic characteristic waveforms of this sample-and-hold system.



TOP TRACE: OUTPUT
(50 mV/DIV. AND 200 ns/DIV.)
BOTTOM TRACE: INPUT
(50 mV/DIV. AND 200 ns/DIV.)
92CS-27883



LARGE-SIGNAL RESPONSE AND SETTLING TIME
TOP TRACE: OUTPUT SIGNAL
(5 V/DIV. AND 2 μs/DIV.)
BOTTOM TRACE: INPUT SIGNAL
(5 V/DIV. AND 2 μs/DIV.)
CENTER TRACE: DIFFERENCE OF INPUT AND OUTPUT SIGNALS THROUGH TEKTRONIX AMPLIFIER 7A13
(5 mV/DIV. AND 2 μs/DIV.) 92CS-27884



SAMPLING RESPONSE
TOP TRACE: SYSTEM OUTPUT
(100 mV/DIV. AND 500 ns/DIV.)
BOTTOM TRACE: SAMPLING SIGNAL
(20 V/DIV. AND 500 ns/DIV.)
92CS-27885

Fig. 35 – Sample- and hold system dynamic characteristics waveforms.

CURRENT AMPLIFIER

The low input-terminal current needed to drive the CA3140 makes it ideal for use in current-amplifier applications such as the one shown in Fig. 36.• In this circuit, low current is supplied at the input potential as the power supply to load resistor R_L. This load current is increased by the multiplication factor R2/R1, when the load current is monitored by the power supply meter M. Thus, if the load current is 100 nA, with values shown, the load current presented to the supply will be 100 μA; a much easier current to measure in many systems.

Note that the input and output voltages are transferred at the same potential and only the output current is multiplied by the scale factor.

The dotted components show a method of decoupling the circuit from the effects of high output-load capacitance and the potential oscillation in this situation. Essentially, the necessary high-frequency feedback is provided by the capacitor with the dotted series resistor providing load decoupling.

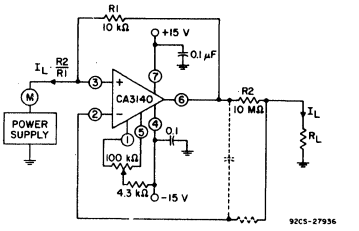


Fig. 36 – Basic current amplifier for low-current measurement systems.

Fig. 37 shows a single-supply, absolute-value, ideal full-wave rectifier with associated waveforms. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No.6) of the inverting amplifier in a negative-going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative-going excursion of the input signal, the CA3140 functions as a normal inverting amplifier with a gain equal to −R2/R1. When the equality of the two equations shown in Fig. 37 is satisfied, the full-wave output is symmetrical.

• "Operational Amplifiers Design and Applications", J. G. Graeme, McGraw-Hill Book Company, page 308 – "Negative Immittance Converter Circuits".

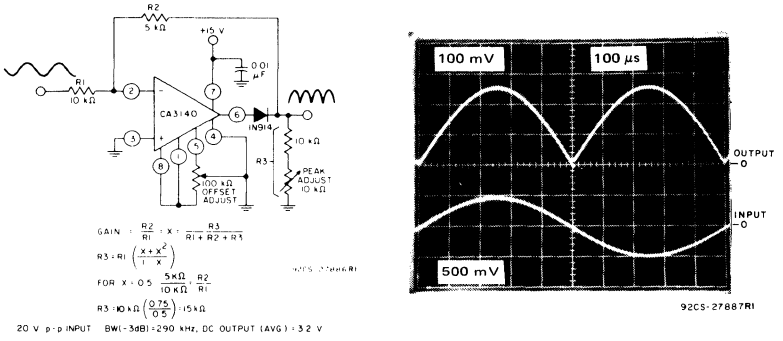


Fig. 37 — Single-supply, absolute-value, ideal full-wave rectifier with associated waveforms.

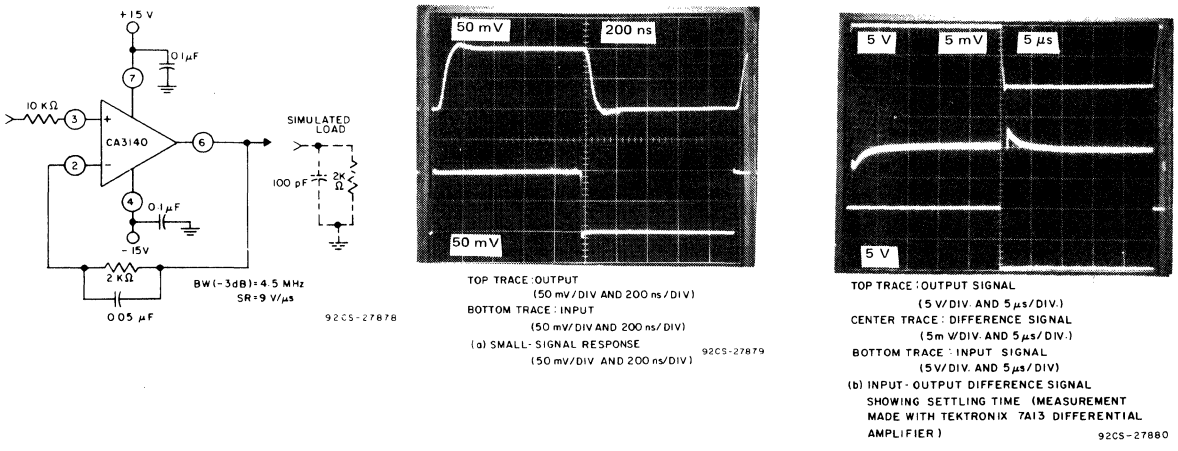


Fig. 38 — Split-supply voltage-follower test circuit and associated waveforms.

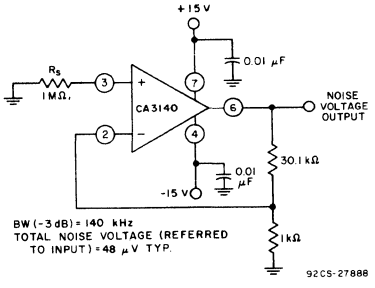
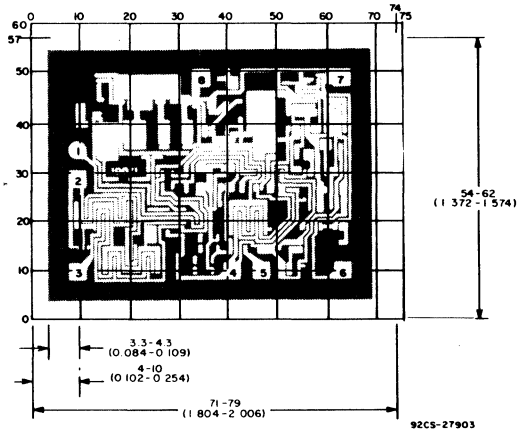


Fig. 39 — Test circuit amplifier (30-dB gain) used for wideband noise measurement.



CA3140H Chip

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).