Better understanding of FET operation yields viable monolithic J-FET op amp

Input current in the nanoampere range, together with low offset voltage, enables a monolithic op amp to do jobs that were once delegated to hybrid devices; the result is to bring higher accuracy within the range of less expensive systems

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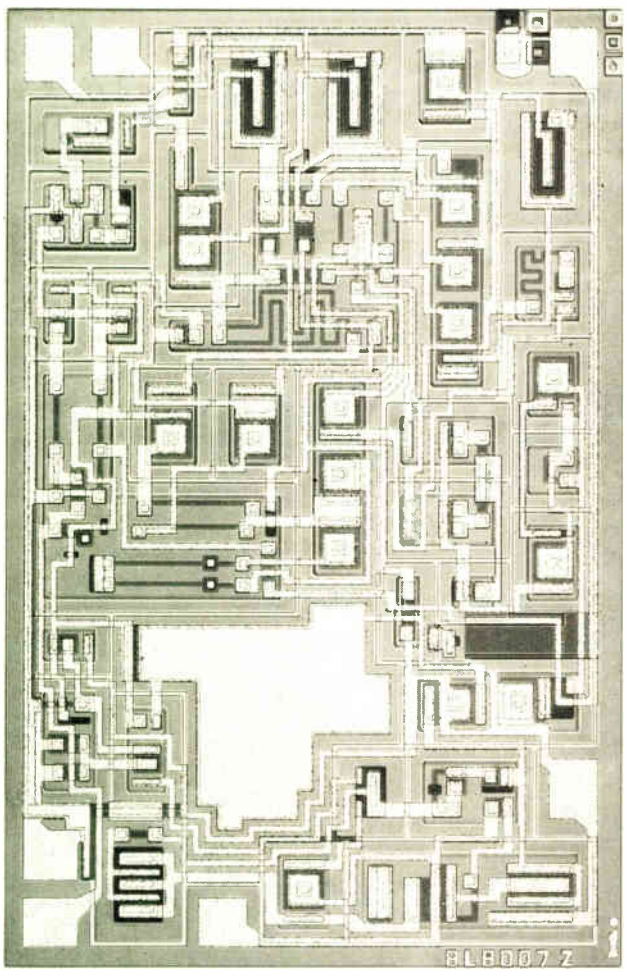
☐ Although monolithic operational amplifiers have been around for almost a decade, the analog designer invariably turns to an expensive hybrid device when he builds a system intended for accurate data acquisition. Usually it's a two-chip design with junction field-effect transistors to provide low input currents. In contrast, the monolithic J-FET approach has always run into problems of excessive input currents, excessive drift, and faulty biasing techniques.

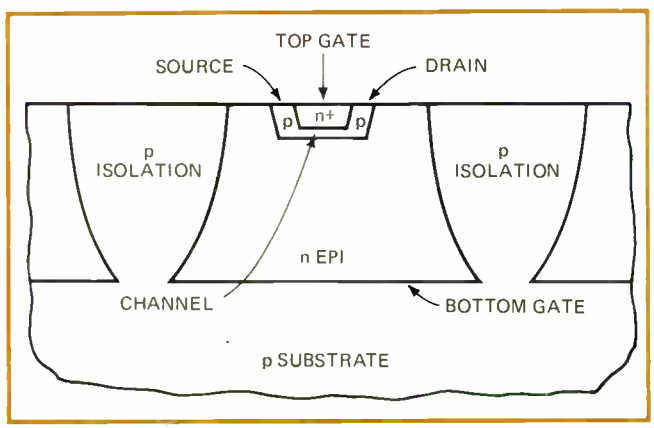
An improved J-FET circuit design, however, results in a monolithic device that combines the input and stability features of the hybrids at about half the hybrid's price. At last the monolithic J-FET-input op amp can take its place alongside such familiar, all-bipolar products as the 741 and the 101A. It should all but replace modules in op amp applications such as log and antilog amplifiers, photocell amplifiers, peak detectors, sample-and-hold circuits, high impedance buffers, and active filters.



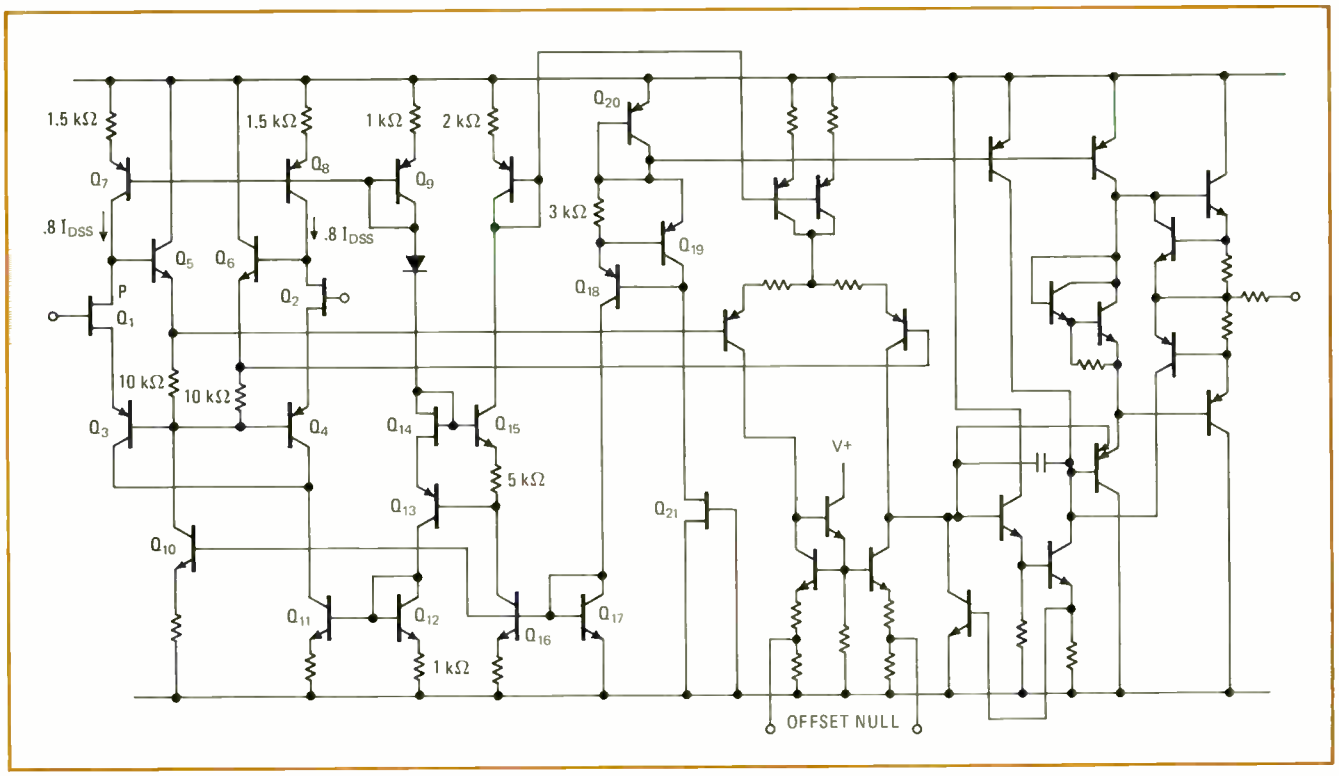
Small draw. Monolithic op amps with field-effect transistors at their input can now compete with hybrid modules in precision amplifier applications. The J-FET inputs, which allow an op amp to operate at extremely low bias currents, are shown in the center on the extreme left of this photomicrograph. A third J-FET (upper left) is used for biasing. The chip, 83 by 54 mils, incorporates designs that minimize input current at high gain, while maintaining stability. Sample-and-hold, log, and photocell circuits will benefit.

Why J-FETs?

The J-FET input can operate with extremely small input currents, plus fairly low offset voltages, which can be nulled to zero. Such conditions allow small signals to be detected with practically no distortion. In two-chip hybrids one chip is used for the input and a second for the rest of the amplifier. This approach separates the touchy input structure from the gain stages of the device, and makes the design of the front end much easier. For a successful monolithic equivalent the trick is to integrate both the J-FET input stage and the bipolar gain



1. Basic J-FET. Junction FET, built with standard p-channel processing, has n-type emitter diffusion and epi collector material which becomes top and bottom gates of the two-gate structure. For high gains and low leakage the back gate must be tied to the source, thus removing the leakage path between back gate and substrate.



2. Getting protection. Schematic of the 8007 shows method of protecting the input stage. Transistors Q_3 and Q_4 protect the input J-FETs from voltages in excess of 6.3 volts. Notice that offset nulling is done in the second pnp stage, minimizing voltage drift in J-FET-input stage

stages onto the same chip without degrading the performance of either.

Unfortunately, integrating J-FETs is no easy job, although many attempts have been made and versions of such a device have been available for about three years. The fundamental problem has been circuit design, resulting from the failure of designers to fully comprehend the nature of the J-FET structure and its relationship to the rest of linear bipolar processing.

Indeed, early monolithic op amps with J-FET inputs suffered from three major problems. Input currents were often too large for many applications, especially charge-storage circuits such as sample-and-hold circuits, peak detectors, and so on. The offset drifted with temperature, especially after initial null setting. And poorly designed bias networks in the front end often resulted in acute manufacturing yield problems.

Integrating J-FETs

In general, the excess input current in any J-FET structure is a function of both the particular FET geometry chosen and the inherent leakage of the process. The most convenient method of making a junction FET, with only minor changes to a standard bipolar process, is to build the p-channel device shown in Fig. 1. Here the base diffusion forms the channel, while the n-type emitter diffusion and the epitaxial collector material become the top and bottom gates respectively.

Unfortunately, a J-FET so formed has several limitations. First, its transconductance—typically 300 micromhos—is inherently lower than that in equivalent discrete devices, but when the device is used as a source follower, the low g_m is no problem. Also, its drain-gate breakdown voltage is only 6.3 volts and to some degree

TABLE 1: OPERATING PARAMETERS OF 8007 OP AMP

Parameter	Typical value
Input bias current	0.3 pA
Input offset voltage	15 mV
Input resistance	10^{12} Ω
Offset voltage drift	20 μV/°C
Common-mode rejection	90 dB
Input voltage range	±12 V
Slew rate	6 V/μs
Output swing	±12 V

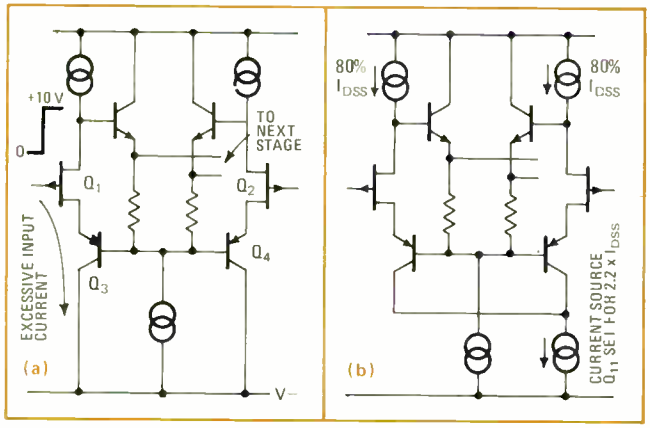
complicates the front-end biasing circuits. Worst of all is the excess gate current that occurs if the two gates are tied together.

At first sight, it is tempting to do this in order to maximize the transconductance, g_m. But the effect is to create a disastrously large gate current. This is because in monolithic form the back-gate-to-substrate junction has a very large surface area, giving rise to excessive leakage currents between it and the negative supply. This leakage current adds to the J-FET-input bias current, which becomes large in its turn and renders the J-FET input ineffective for sensitive measurements.

A better way of achieving low leakage while max-

TABLE 2: AMPLIFIER NOISE COMPARISON

Type	e_n (at 10 Hz)	i_n (at 10 Hz)
8007	300 nV/√Hz	0.01 pA/√Hz
741	25 nV/√Hz	0.7 pA/√Hz



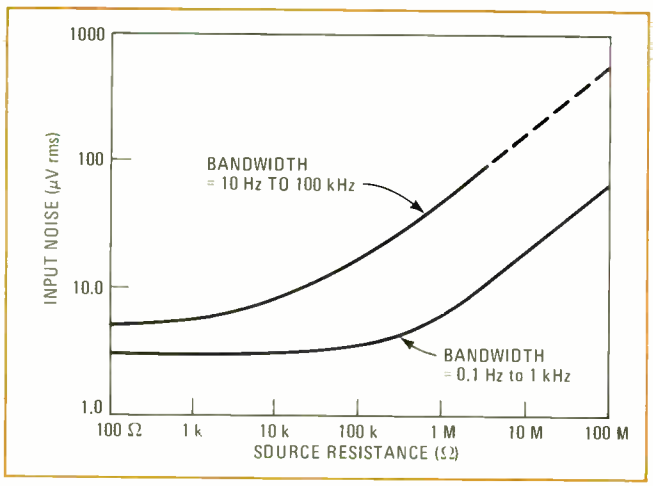
3. Setting limits. The 8007's input stage is protected against high currents should the input transistors break down under fast transient conditions. In other monolithic J-FET op amps, a high-speed 10-V pulse could cause transistors Q_3 and Q_4 to return directly to the negative supply, forcing high current to ground. Shown in (b) is the 8007 answer to this problem—to limit this current with Q_{11}.

imizing transconductance and gain is to tie the back gate to the source, thus removing the back-gate leakage path from the input current. In this case, since the back gate is more lightly doped than the channel, most of the depletion region goes the wrong way, that is, into the gate. The result: a small reduction in g_m (by about only 10%), and most significantly a great reduction in leakage.

Getting the drift down

Once high gains at low input currents are achieved, it's necessary to go after low drifts. Unfortunately, the J-FET has inherently worse drift performance than its bipolar counterpart. However, just as there are design techniques for minimizing the drift of bipolar transistor pairs, so there are equivalent techniques for minimizing the drift of J-FET pairs.

But merely following the bipolar example leads to trouble. In the case of the bipolar transistor pairs, the first-order drift terms can be minimized by mismatching the collector current I_c until the base-to-emitter voltage differential, ΔV_{BE}, equals zero. In the equivalent J-FET



4. Noise. Common to all amplifiers is the increase in noise as the source resistance goes up. The noise structure of the 8007 is shown at two typical bandwidth values.

case, however, mismatching the drain current I_D until the differential in gate-to-source voltage, $_dV_{GS}$, equals zero will result in overwhelmingly large voltage drifts. The key to achieving minimum drift with J-FET pairs is rather to match the drain currents as closely as possible, and to perform the offset nulling in such a manner as not to disturb this match. This means that offset nulling must be implemented in the second stage.

A third design challenge involves biasing the J-FET input stage so as to maximize manufacturing yield without degrading electrical performance. Over a period of months, run-to-run variations in the manufacturing process will produce J-FETs with a range of drain-to-source current (I_{DSS}) from one third the typical value to triple this value, a 9:1 spread.

Now, if an attempt is made to bias the J-FET stage with a fixed current, as was done in some old designs, a value less than $I_{DSS(min)}$ must be selected. If not, some of the devices will be forward-biased. But when this same current is used to bias those J-FETs that are toward the high end of the I_{DSS} range, V_{GS} will be high and the input common-mode range will suffer proportionally. And matters get worse when a wide temperature range is involved.

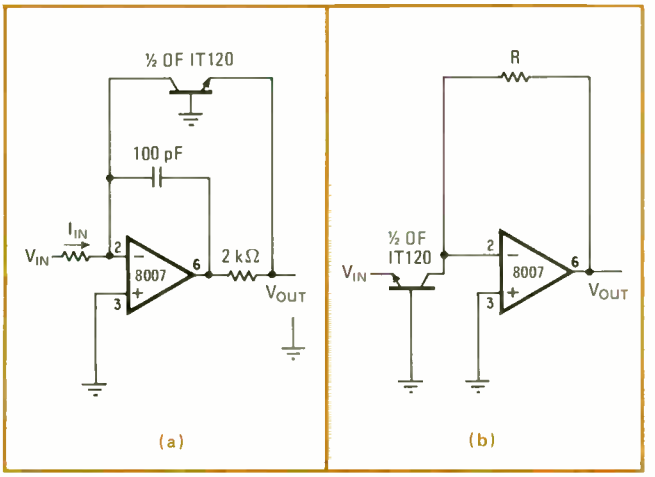
The solution is to bias the J-FET differential stage from another J-FET. The input stage J-FETs are then operated at about 80% I_{DSS}. V_{GS} is always low, thus ensuring an exceptional common-mode range for a J-FET amplifier. There is no danger of forward-biasing the J-FET, and the scheme assures these conditions hold good over wide temperature ranges.

The outcome

These design features have been incorporated into the Intersil monolithic 8007 op amp, shown in Fig. 2. The sensitive input J-FETs, Q_1 and Q_2, are protected from voltages in excess of 2.5 volts (well below breakdown) by the bootstrap loop comprising Q_3, Q_4, Q_5 and Q_6. This loop maintains a fixed drain-to-source voltage across the J-FETs regardless of the input voltage, and also contributes toward the exceptional common-mode rejection of the circuit. Notice that the offset nulling in the pnp gain stage has no effect on the drain current match of the first-stage J-FETs.

A key feature of the circuit is the operation of transistors Q_{14} and Q_{15}, which serve to generate the bias current for the input stage. Q_{14} is a p-channel J-FET connected so as to generate a suitable drain-to-source current. This current is scaled down by about 20% by the resistors in the emitters of Q_7 through Q_9, in this way insuring that transistors Q_1 and Q_2 will not be forward-biased.

Another input feature of the 8007 is the current source Q_{11}, which limits the input current should either Q_1 or Q_2 break down under fast transient conditions. Consider, for example, the effect of a high-speed positive pulse on one input, as shown in Fig. 3a. If the pulse were of sufficient amplitude, and if Q_3 and Q_4 were returned directly to the negative supply, excessive currents could flow through the path indicated in the figure. At best, there is a danger of latch-up—an input J-FET would remain in a breakdown state. The current source shown in Fig. 3b, on the other hand, eliminates



5. Logging it in. In typical log amplifier (a) and antilog amplifier (b), the low bias current of the J-FET op amp increases the sensitivity of the log range. Typically nine decades can be accommodated when a low-leakage IT120 transistor is used with the op amp.

the problem. Here the output stage is of conventional design, being very similar to the stage which is used in the 741.

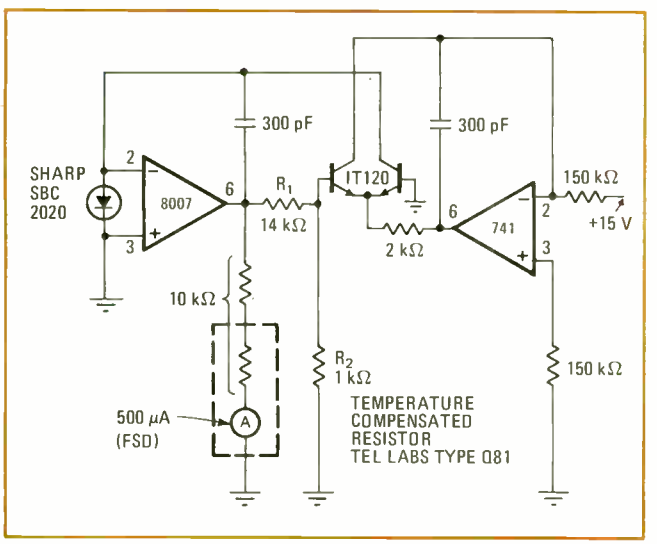
Performance tells the story

The circuit performance of the 8007 is summarized in Table 1. Note particularly that the typical input current is substantially less than 1 picoampere at 25°C, well within the design specifications of even the best J-FET-input modules. Equally important is the 8007's ability to perform with low noise. The total mean-square noise of an operational amplifier for a bandwidth $\Delta f = f_2 - f_1$ is given by

$$e_T^2 = \int_{f_1}^{f_2} e_n^2\, df + R_s^2 \int_{f_1}^{f_2} i_n^2\, df + 4KTR_s\,\Delta f$$

where the critical terms are: the source resistance, R_s; the input noise voltage generator, e_n; and the input noise current generator, i_n.

Typical values of the 8007 for e_n and i_n are compared in Table 2 with figures for the general-purpose 741 op amp. It is clear that for general-purpose applications, where high source resistance (R_s greater than 1 megohm) and low input noise are requirements, the J-FET input is superior to the standard bipolar design. The details of the total input noise of the 8007 as a function of source resistance are shown in Fig. 4.



6. Lightly. Low input current of the J-FET op amp is useful for photocell circuits where microamp sensitivity is required.

One of the 8007's uses

An application which illustrates the advantages of the low input current of the 8007 is the log circuit of Fig. 5a and its antilog counterpart, Fig. 5b. In this setup, a low-leakage discrete transistor, such as the IT120, is connected across the op amp. This transister has accurate logarithmic relationship between V_{BE} and I_C over a remarkably wide range of collector currents—10 decades (0.1 pA to 1 mA) are possible. At the low end of the current range, the accuracy of the circuit is primarily dependent on the ability of the amplifier to function. The 8007 with its picoamp bias currents becomes an ideal choice in this situation.

The photocell amplifier circuit of Fig. 6 can also profit from the 8007's input parameters. In this circuit, a light meter directly displays the log of the light intensity as an exposure value. (An Exposure Value is a photographic term, each unit change in which corresponds to a factor-of-two change in light intensity.) To minimize leakage errors, the silicon cell is operated at zero voltage. Any current drawn by the op amp will directly subtract from the photocell output and show up as an error. This is especially true at low light levels, where the cell current may be only a few tens of picoamps. Thus the picoampere range of the 8007 again makes it a natural choice of photocell circuits.

Another use

An application that relies on the high slew rate of the 8007 is the Wien bridge oscillator, which can be used to generate large signal oscillations over a wide band of frequencies. When general-purpose amplifiers, such as the 741, are used to obtain signals with amplitudes greater than about 100 millivolts, the slew rate (the maximum rate at which the output voltage can change) is the parameter that determines the upper operating frequency. If the amplifier slew rate is less than a critical threshold, distortion will occur. For example, for a sine wave above about 10 kilohertz, an amplifier with 0.6 V/s slew rate (the 741, for example) will not handle a 20-V peak-to-peak signal.

Typically the 8007 has a slew rate of 6V/μs, and thus offers an operating-frequency range that is 10 times the 741's. Indeed, using the 8007 in a typical Wien Bridge oscillator provides a 20-V peak-to-peak output at 40 kHz. In this circuit, the amplitude may simply be controlled by R_1. For smaller output swings, correspondingly higher frequencies can be obtained. □

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