OP-07

ULTRA-LOW OFFSET VOLTAGE OP AMP

GENERAL DESCRIPTION

The OP-07 Series represents a breakthrough in monolithic operational amplifier performance—Vos of 10μV, TC Vos of 0.2μV/°C and long term stability of 0.2μV/month are achieved by a low noise, chopper-less bipolar input transistor amplifier circuit. Complete elimination of external components for offset nulling, frequency compensation and device protection permits extreme miniaturization and optimization of system Mean-Time-Between-Failure Rates in high performance aerospace/defense and industrial applications. Excellent device interchangeability provides reduced system assembly time and eliminates field recalibrations.

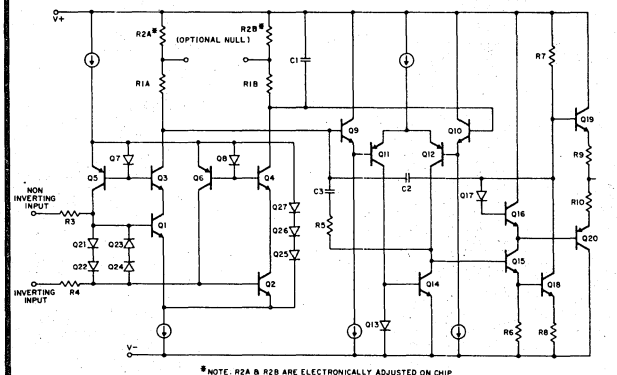
True differential inputs with wide input voltage range and outstanding common mode rejection provide maximum flexibility and performance in high noise environments and non-inverting applications. Low bias currents and extremely high input impedances are maintained over the entire temperature range.

Low cost, high volume production of OP-07 is achieved by electronic adjustment of an on-chip offset trimming network during initial factory testing. The OP-07 provides unparalleled performance for low noise, high accuracy amplification of very low level signals in transducer applications. Other applications include use in stable integrators, precision summing amplifiers for analog computation and test equipment and in ultra-precise voltage threshold detectors and comparators. The OP-07 is recommended as a replacement for modular and monolithic chopper-stabilized amplifiers where reductions in cost, noise, size and power consumption are required. Devices are available in chip form for use in hybrid circuitry. The OP-07 is a direct replacement for 725, 108A/308A, and OP-05 amplifiers; 741-types may be directly replaced by removing the 741's nulling potentiometer.

FEATURES

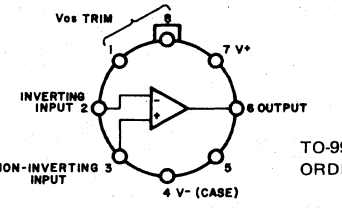
- Ultra-Low Vos . . . . . 10 μV
- Ultra-Low Vos Drift . . . . . 0.2 μV/°C
- Ultra-Stable vs Time . . . . . 0.2 μV/Month
- Ultra-Low Noise . . . . . 0.35 μVp-p
- No External Components Required
- Replaces Chopper amps at Lower Cost
- Single Chip Monolithic Construction
- High Common Mode Input Range . . . . . ±14.0V
- Wide Supply Voltage Range . . . . . ±3V to ±18V
- Fits 725, 108A/308A, 741 Sockets

SIMPLIFIED SCHEMATIC

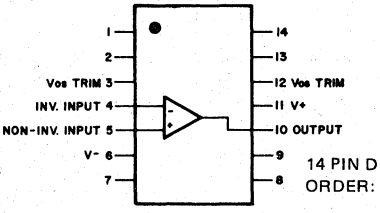


*NOTE: R2A & R2B ARE ELECTRONICALLY ADJUSTED ON CHIP AT FACTORY FOR MINIMUM INPUT OFFSET VOLTAGE.

PIN CONNECTIONS AND ORDERING INFORMATION



TO-99 (J-Suffix)
ORDER: OP-07AJ
OP-07J
OP-07EJ
OP-07CJ



14 PIN DIP (Y-Suffix)
ORDER: OP-07AY
OP-07Y
OP-07EY
OP-07CY

TOP VIEW

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V	Storage Temperature Range	-65°C to +150°C
Internal Power Dissipation (Note 1)	500mW	Operating Temperature Range	
Differential Input Voltage	±30V	OP-07A, OP-07	-55°C to +125°C
Input Voltage (Note 2)	±22V	OP-07E, OP-07C	0°C to +70°C
Output Short Circuit Duration	Indefinite	Lead Temperature Range (Soldering, 60 sec)	300°C

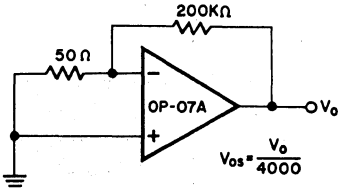
NOTES:

Note 1: Maximum package power dissipation vs. ambient temperature.

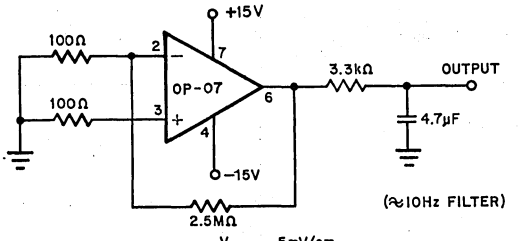
Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1mW/°C
Dual-in-Line (Y)	100°C	10.0mW/°C

Note 2: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

OFFSET VOLTAGE TEST CIRCUIT



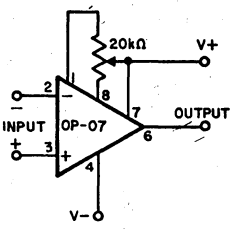
LOW FREQUENCY NOISE TEST CIRCUIT



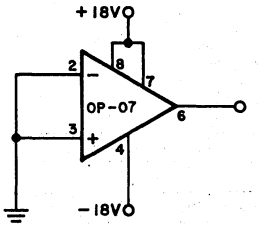
INPUT REFERRED NOISE = $\frac{V_O}{25{,}000} = \frac{5mV/cm}{25{,}000} = 200nV/cm$

SEE NOISE PHOTO-PAGE 6-27

OPTIONAL OFFSET NULLING CIRCUIT



BURN-IN CIRCUIT



APPLICATIONS INFORMATION

OP-07 Series units may be fitted directly to 725, 108A/308A and OP-05 sockets with or without removal of external compensation or nulling components. Additionally, OP-07 may be fitted to unnulled 741-type sockets; however if conventional 741 nulling circuitry is in use, it should be modified or removed to enable proper OP-07 operation. OP-07 offset voltage may be nulled to zero (or other desired setting) through use of a potentiometer (see diagram above).

The OP-07 provides stable operation with load capacitances up to 500pF and ±10V swings; larger capacitances should be decoupled with a 50Ω decoupling resistor. The designer is cautioned that stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

ELECTRICAL CHARACTERISTICS			OP-07A			OP-07			
These specifications apply for $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{os}	(Note 1)	—	10	25	—	30	75	μV
Long Term Input Offset Voltage Stability	V_{os}/Time	(Note 2)	—	0.2	1.0	—	0.2	1.0	μV/Mo
Input Offset Current	I_{os}		—	0.3	2.0	—	0.4	2.8	nA
Input Bias Current	I_B		—	±.7	±2.0	—	±1.0	±3.0	nA
Input Noise Voltage	$e_{np\text{-}p}$	0.1Hz to 10Hz (Note 3)	—	0.35	0.6	—	0.35	0.6	μV p-p
Input Noise Voltage Density	e_n	f_o = 10Hz (Note 3)	—	10.3	18.0	—	10.3	18.0	nV/√Hz
		f_o = 100Hz (Note 3)	—	10.0	13.0	—	10.0	13.0	
		f_o = 1000Hz (Note 3)	—	9.6	11.0	—	9.6	11.0	
Input Noise Current	$i_{np\text{-}p}$	0.1Hz to 10Hz (Note 3)	—	14	30	—	14	30	pA p-p
Input Noise Current Density	i_n	fo = 10Hz (Note 3)	—	0.32	0.80	—	0.32	0.80	pA/√Hz
		fo = 100Hz (Note 3)	—	0.14	0.23	—	0.14	0.23	
		fo = 1000Hz (Note 3)	—	0.12	0.17	—	0.12	0.17	
Input Resistance - Differential Mode	R_{in}		30	80	—	20	60	—	MΩ
Input Resistance - Common Mode	R_{inCM}		—	200	—	—	200	—	GΩ
Input Voltage Range	CMVR		±13.0	±14.0	—	±13.0	±14.0	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm$CMVR	110	126	—	110	126	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	100	110	—	100	110	—	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	300	500	—	200	500	—	V/mV
		$R_L \geq 500\Omega$, $V_O = \pm 0.5V$	150	500	—	150	500	—	
		$V_S = \pm 3V$							
Maximum Output Voltage Swing	V_{oM}	$R_L \geq 10k\Omega$	±12.5	±13.0	—	±12.5	±13.0	—	V
		$R_L \geq 2k\Omega$	±12.0	±12.8	—	±12.0	±12.8	—	
		$R_L \geq 1k\Omega$	±10.5	±12.0	—	±10.5	±12.0	—	
Slewing Rate	SR	$R_L \geq 2k\Omega$	—	0.25	—	—	0.25	—	V/μsec
Closed Loop Bandwidth	BW	$A_{VCL} = +1.0$	—	1.2	—	—	1.2	—	MHz
Open Loop Output Resistance	R_o	$V_o = O$, $I_o = O$	—	60	—	—	60	—	Ω
Power Consumption	Pd		—	75	120	—	75	120	mW
		$V_S = \pm 3V$	—	4	6	—	4	6	
Offset Adjustment Range		$R_p = 20k\Omega$	—	±4	—	—	±4	—	mV
The following specifications apply for $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.									
Input Offset Voltage	V_{os}	(Note 1)	—	25	60	—	60	200	μV
Average Input Offset Voltage Drift									
Without External Trim	TCV_{os}		—	0.2	0.6	—	0.3	1.3	μV/°C
With External Trim	TCV_{osn}	$R_p = 20k\Omega$	—	0.2	0.6	—	0.3	1.3	μV/°C
Input Offset Current	I_{os}		—	0.8	4.0	—	1.2	5.6	nA
Average Input Offset Current Drift	TCI_{os}		—	5	25	—	8	50	pA/°C
Input Bias Current	I_B		—	±1.0	±4.0	—	±2.0	±6.0	nA
Average Input Bias Current Drift	TCI_B		—	8	25	—	13	50	pA/°C
Input Voltage Range	CMVR		±13.0	±13.5	—	±13.0	±13.5	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm$CMVR	106	123	—	106	123	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	94	106	—	94	106	—	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	400	—	150	400	—	V/mV
Maximum Output Voltage Swing	V_{oM}	$R_L \geq 2k\Omega$	±12.0	±12.6	—	±12.0	±12.6	—	V

NOTE 1: Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. Additionally, OP-07A offset voltage is measured five minutes after power supply application at 25°C, -55°C and +125°C.

NOTE 2: Long Term Input Offset Voltage Stability refers to the averaged trend line of Vos vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in Vos during the first 30 operating days are typically 2.5μV — refer to typical performance curves. Parameter is not 100% tested; 90% of units meet this specification.

NOTE 3: Parameter is not 100% tested; 90% of units meet this specification.

ELECTRICAL CHARACTERISTICS			OP-07E			OP-07C			
These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{os}	(Note 1)	—	30	75	—	60	150	µV
Long Term Input Offset Voltage Stability	V_{os}/Time	(Note 2)	—	0.3	1.5	—	0.4	2.0	µV/Mo
Input Offset Current	I_{os}		—	0.5	3.8	—	0.8	6.0	nA
Input Bias Current	I_B		—	±1.2	±4.0	—	±1.8	±7.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)	—	0.35	0.6	—	0.38	0.65	µV p-p
Input Noise Voltage Density	e_n	f_o = 10Hz (Note 3)	—	10.3	18.0	—	10.5	20.0	nV/√Hz
		f_o = 100Hz (Note 3)	—	10.0	13.0	—	10.2	13.5	
		f_o = 1000Hz (Note 3)	—	9.6	11.0	—	9.8	11.5	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 3)	—	14	30	—	15	35	pAp-p
Input Noise Current Density	i_n	f_o = 10Hz (Note 3)	—	0.32	0.80	—	0.35	0.90	pA/√Hz
		f_o = 100Hz (Note 3)	—	0.14	0.23	—	0.15	0.27	
		f_o = 1000Hz (Note 3)	—	0.12	0.17	—	0.13	0.18	
Input Resistance — Differential Mode	R_{in}		15	50	—	8	33	—	MΩ
Input Resistance — Common Mode	R_{inCM}		—	160	—	—	120	—	GΩ
Input Voltage Range	CMVR		±13.0	±14.0	—	±13.0	±14.0	—	V
Common Mode Rejection Ratio	CMRR	V_{cM} = ±CMVR	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	V_s = ±3V to ±18V	94	107	—	90	104	—	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$, V_o = ±10V	200	500	—	120	400	—	V/mV
		$R_L \geq 500\Omega$, V_o = ±.5V, V_s = ±3V	150	500	—	100	400	—	
Maximum Output Voltage Swing	V_{oM}	$R_L \geq 10k\Omega$	±12.5	±13.0	—	±12.0	±13.0	—	V
		$R_L \geq 2k\Omega$	±12.0	±12.8	—	±11.5	±12.8	—	
		$R_L \geq 1k\Omega$	±10.5	±12.0	—	—	±12.0	—	
Slewing Rate	SR	$R_L \geq 2k\Omega$	—	0.25	—	—	0.25	—	V/µsec
Closed Loop Bandwidth	BW	A_{VCL} = +1.0	—	1.2	—	—	1.2	—	MHz
Open Loop Output Resistance	R_o	V_o = 0, I_o = 0	—	60	—	—	60	—	Ω
Power Consumption	P_d		—	75	120	—	80	150	mW
		V_s = ±3V	—	4	6	—	4	8	
Offset Adjustment Range		R_p = 20kΩ	—	±4	—	—	±4	—	mV
The following specifications apply for V_S = ±15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.									
Input Offset Voltage	V_{os}	(Note 1)	—	45	130	—	85	250	µV
Average Input Offset Voltage Drift								(Note 3)	µV/°C
Without External Trim	TCV_{os}	R_p = 20kΩ	—	0.3	1.3	—	0.5	1.8	
With External Trim	TCV_{osn}		—	0.3	1.3	—	0.4	1.6 (Note 3)	
Input Offset Current	I_{os}		—	0.9	5.3	—	1.6	8.0	nA
Average Input Offset Current Drift	TCI_{os}	(Note 3)	—	8	35	—	12	50	pA/°C
Input Bias Current	I_B		—	±1.5	±5.5	—	±2.2	±9.0	nA
Average Input Bias Current Drift	TCI_B	(Note 3)	—	13	35	—	18	50	pA/°C
Input Voltage Range	CMVR		±13.0	±13.5	—	±13.0	±13.5	—	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	103	123	—	97	120	—	dB
Power Supply Rejection Ratio	PSRR	V_s = ±3V to ±18V	90	104	—	86	100	—	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$, V_o = ±10V	180	450	—	100	400	—	V/mV
Maximum Output Voltage Swing	V_{oM}	$R_L \geq 2k\Omega$,	±12.0	±12.6	—	±11.0	±12.6	—	V

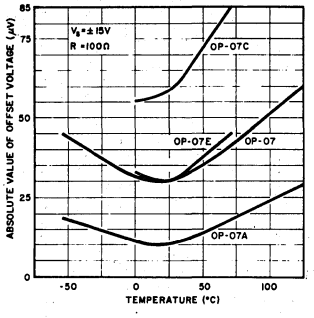
NOTE 1: Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

NOTE 2: Long Term Input Offset Voltage Stability refers to the averaged trend line of Vos vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in Vos during the first 30 operating days are typically 2.5µV — refer to typical performance curve. Parameter is not 100% tested; 90% of units meet this specification.

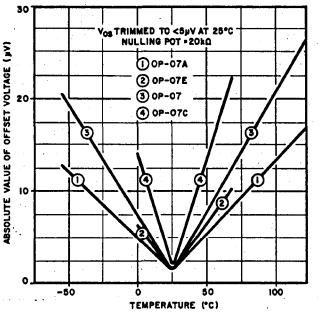
NOTE 3: Parameter is not 100% tested; 90% of units meet this specification.

TYPICAL PERFORMANCE CURVES

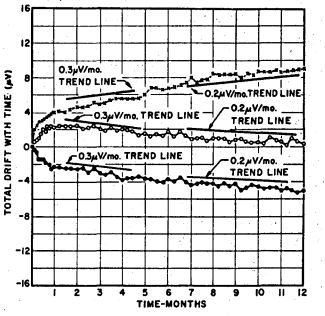
UNTRIMMED OFFSET VOLTAGE VS TEMPERATURE



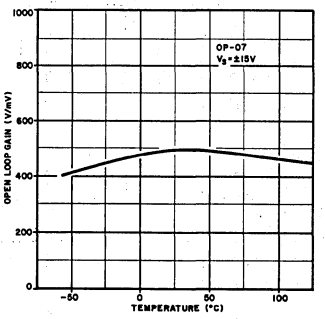
TRIMMED OFFSET VOLTAGE VS TEMPERATURE



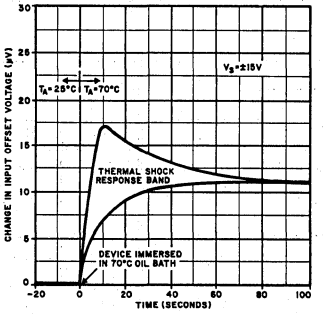
OFFSET VOLTAGE STABILITY VS TIME



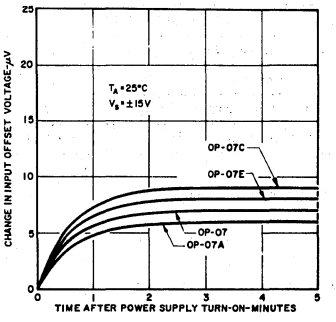
OPEN LOOP GAIN VS TEMPERATURE



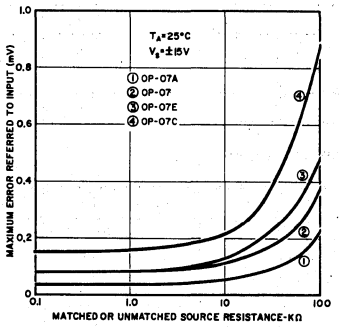
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



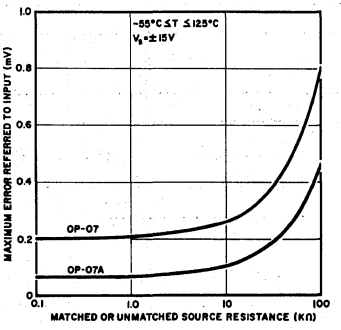
WARM-UP DRIFT



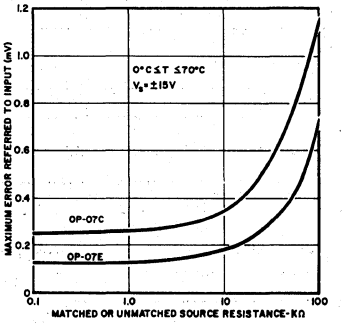
MAXIMUM ERROR VS SOURCE RESISTANCE



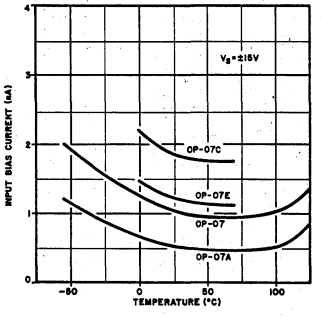
MAXIMUM ERROR VS SOURCE RESISTANCE



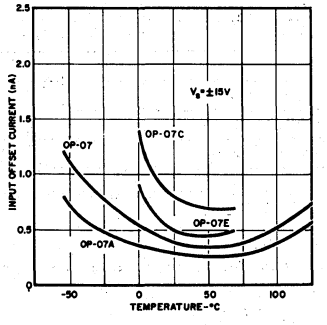
MAXIMUM ERROR VS SOURCE RESISTANCE



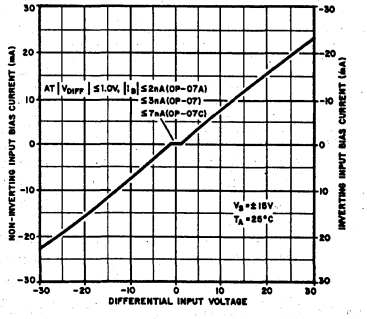
INPUT BIAS CURRENT VS TEMPERATURE



INPUT OFFSET CURRENT VS TEMPERATURE

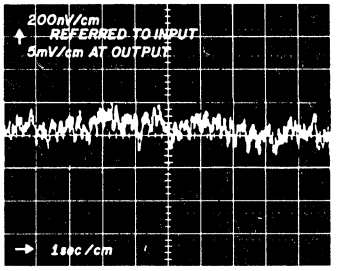


INPUT BIAS CURRENT VS DIFFERENTIAL INPUT VOLTAGE

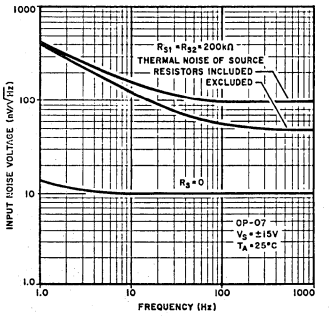


TYPICAL PERFORMANCE CURVES

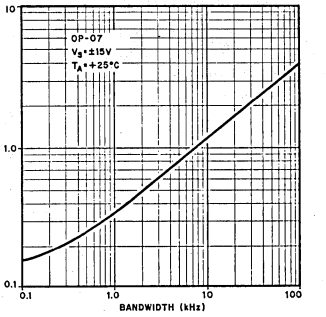
OP-07 LOW FREQUENCY NOISE



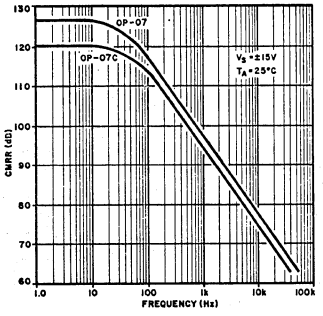
TOTAL INPUT NOISE VOLTAGE VS FREQUENCY



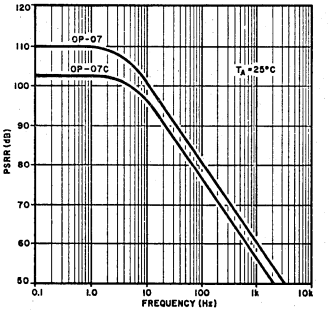
INPUT WIDEBAND NOISE VS BANDWIDTH (.1Hz TO FREQUENCY INDICATED)



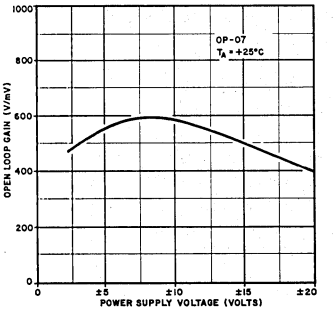
CMRR VS FREQUENCY



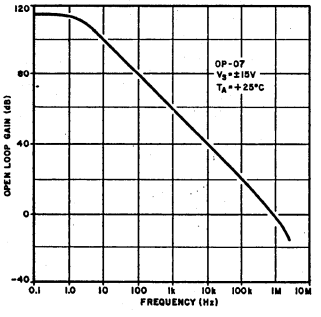
PSRR VS FREQUENCY



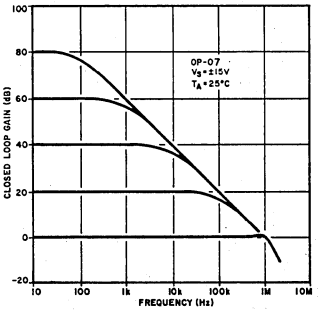
OPEN LOOP GAIN VS POWER SUPPLY VOLTAGE



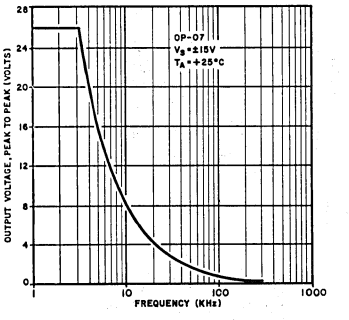
OPEN LOOP FREQUENCY RESPONSE



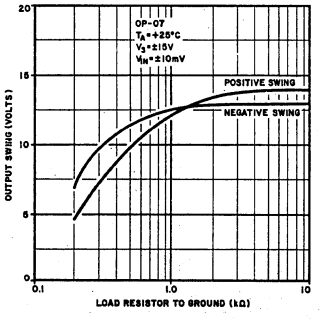
CLOSED LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS



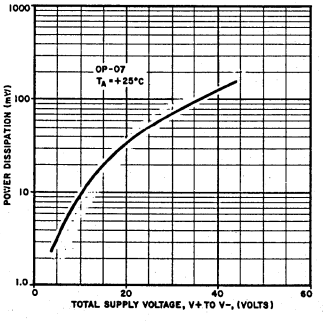
MAXIMUM UNDISTORTED OUTPUT VS FREQUENCY



OUTPUT VOLTAGE VS. LOAD RESISTANCE



POWER CONSUMPTION VS POWER SUPPLY



OUTPUT SHORT-CIRCUIT CURRENT VS TIME