MC3401P

Specifications and Applications Information

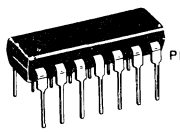
MONOLITHIC QUAD SINGLE-SUPPLY OPERATIONAL AMPLIFIER

These internally compensated operational amplifiers are designed specifically for single positive power supply applications found in industrial control systems and automotive electronics. Each MC3401P device contains four independent amplifiers — making it ideal for applications such as active filters, multi-channel amplifiers, tachometer, oscillator and other similar usages.

- Single-Supply Operation — +5.0 Vdc to +18 Vdc
- Internally Compensated
- Wide Unity Gain Bandwidth — 5.0 MHz typical
- Low Input Bias Current — 50 nA typical
- High Open-Loop Gain — 1000 V/V minimum

MONOLITHIC QUAD OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT

EPITAXIAL PASSIVATED



PLASTIC PACKAGE
CASE 646
(TO-116)

FIGURE 1 — EQUIVALENT CIRCUIT

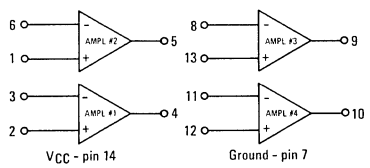


FIGURE 2 — SMALL-SIGNAL TRANSIENT RESPONSE

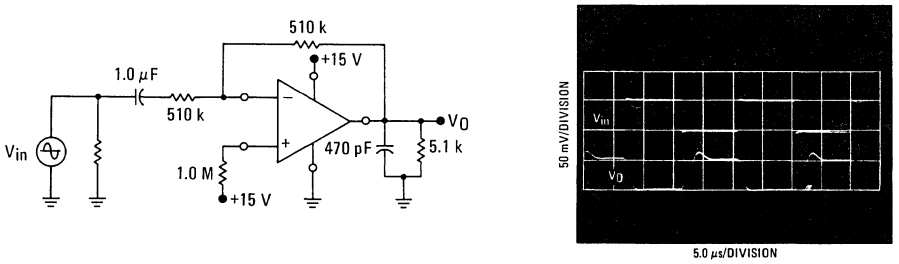


FIGURE 3 — INVERTING AMPLIFIER

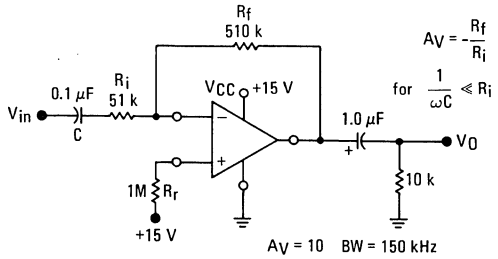
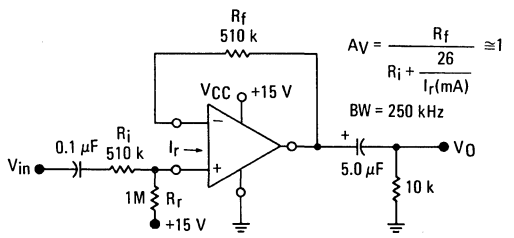


FIGURE 4 — NONINVERTING AMPLIFIER



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Non-inverting Input Current	I_{in}	5.0	mA
Power Dissipation Derate above T_A = +25°C	P_D	625 5.0	mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS [V_{CC} = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C (each amplifier) unless otherwise noted.]

Characteristic	Fig. No.	Note	Symbol	Min	Typ	Max	Unit
Open-Loop Voltage Gain	5,9,10	1	A_{vol}				V/V
T_A = +25°C				1000	2000	–	
0°C ≤ T_A ≤ +75°C				800	–	–	
Quiescent Power Supply Current (Total for four amplifiers)	6,12	2					mAdc
Noninverting inputs open			I_{DO}	–	6.9	10	
Noninverting inputs grounded			I_{DG}	–	7.8	14	
Input Bias Current, R_L = ∞	5	3	I_{IB}				nAdc
T_A = +25°C				–	50	300	
0°C ≤ T_A ≤ +75°C				–	–	500	
Output Current	5	4					mAdc
Source Capability	13		I_{source}	5.0	10	–	
Sink Capability	14		I_{sink}	0.5	1.0	–	
Output Voltage							Vdc
High Voltage	7	5	V_{OH}	13.5	14.2	–	
Low Voltage	7	5	V_{OL}	–	0.03	0.1	
Undistorted Output Swing (0°C < T_A < +75°C)	8	6	$V_{O(p-p)}$	10	13.5	–	$V_{(p-p)}$
Input Resistance	5		R_{in}	0.1	1.0	–	MEG Ω
Slew Rate (C_L = 100 pF, R_L = 5.0 k)			SR	–	0.6	–	V/μs
Unity Gain Bandwidth			BW	–	5.0	–	MHz
Phase Margin			ϕ_m	–	70	–	Degrees
Power Supply Rejection (f = 100 Hz)		7	PSSR	–	55	–	dB
Channel Separation (f = 1.0 kHz)			e_{o1}/e_{o2}	–	65	–	dB

Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

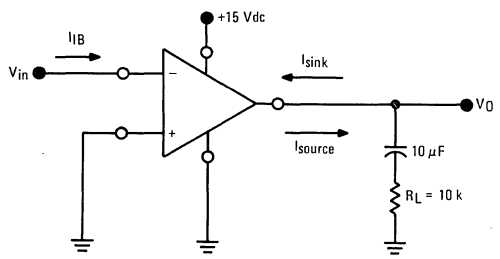
NOTES

1. Open loop voltage gain is defined as the voltage gain from the inverting input to the output.
2. The quiescent current will increase approximately 0.3 mA for each noninverting input which is grounded. Leaving the noninverting input open causes the apparent input bias current to increase slightly (100 nA) at high temperatures.
3. Input bias current can be defined only for the inverting input. The noninverting input is not a true "differential input" – as with a conventional IC operational amplifier. As such this input does not have a requirement for input bias current.
4. Sink current is specified for linear operation. When the device is used as a gate or a comparator (non-linear operation), the sink capability of the device is approximately 5.0 milliamperes.
5. When used as a noninverting amplifier, the minimum output voltage is the V_{BE} of the inverting input transistor.
6. Peak-to-peak restrictions are due to the variations of the quiescent dc output voltage in the standard configuration (Figure 8).
7. Power supply rejection is specified at closed loop unity gain, and therefore indicates the supply rejection of both the biasing circuitry and the feedback amplifier.

SIMPLIFIED TEST CIRCUITS

(V_{CC} = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C
[each amplifier] unless otherwise noted)

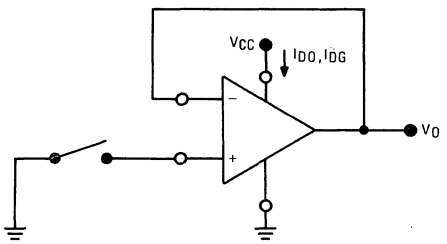
FIGURE 5 – OPEN-LOOP GAIN AND INPUT RESISTANCE (INPUT BIAS CURRENT, OUTPUT CURRENT)



$$R_{in} = \frac{\Delta V_{in}}{\Delta I_{IB}} \quad A_{vol} = -\frac{\Delta V_O}{\Delta V_{in}}$$

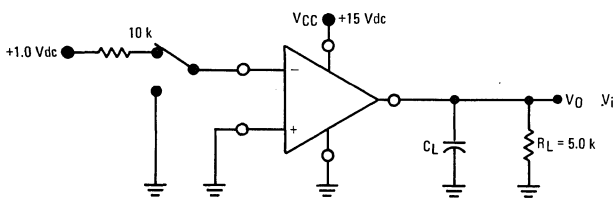
Amplifier must be biased (by V_{in}) in the linear operating region.

FIGURE 6 – QUIESCENT POWER SUPPLY CURRENT



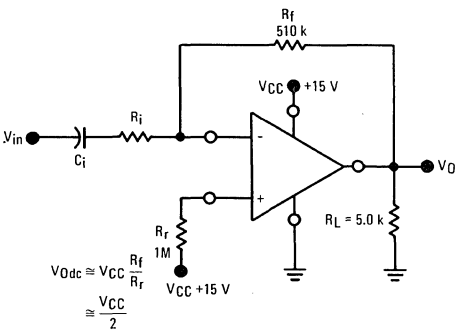
I_{DO} is total supply current with "+" input open.
I_{DG} is total supply current with "+" input grounded.

FIGURE 7 – OUTPUT VOLTAGE SWING



V_{OL} measured with "–" input biased up as shown.
V_{OH} measured with "–" input grounded.

FIGURE 8 – PEAK-TO-PEAK OUTPUT VOLTAGE



$$V_{Odc} \cong V_{CC}\frac{R_f}{R_r} \cong \frac{V_{CC}}{2}$$

for $R_r \cong 2R_f$

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TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C
[each amplifier] unless otherwise noted.)

FIGURE 9 – OPEN-LOOP VOLTAGE GAIN versus FREQUENCY

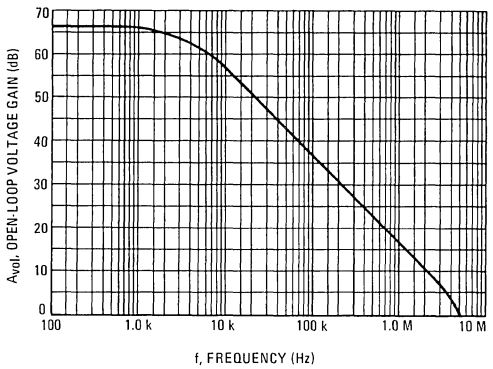


FIGURE 10 – OPEN-LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

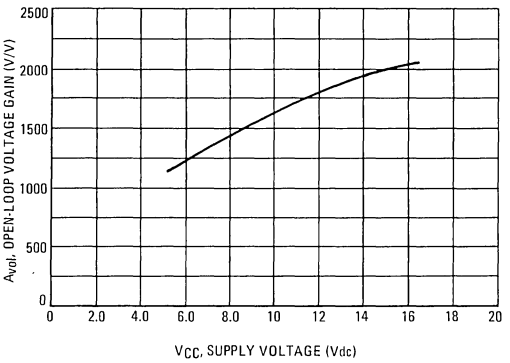


FIGURE 11 – OUTPUT RESISTANCE versus FREQUENCY

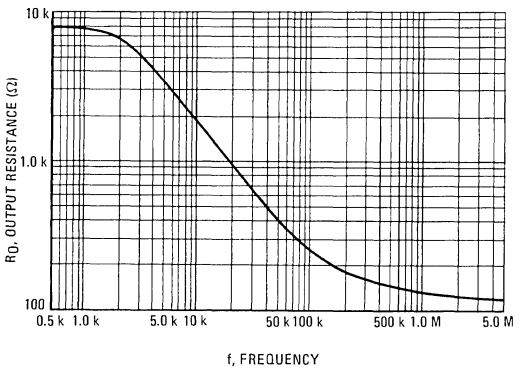


FIGURE 12 – SUPPLY CURRENT versus SUPPLY VOLTAGE

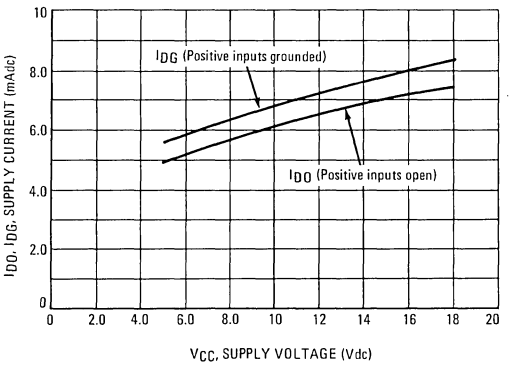


FIGURE 13 – LINEAR SOURCE CURRENT versus SUPPLY VOLTAGE

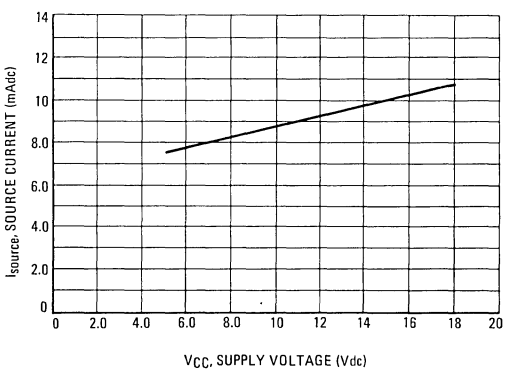
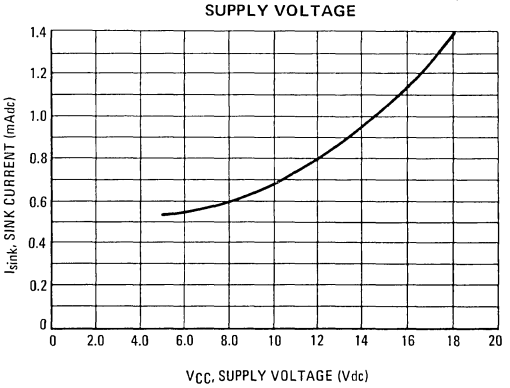


FIGURE 14 – LINEAR SINK CURRENT versus SUPPLY VOLTAGE



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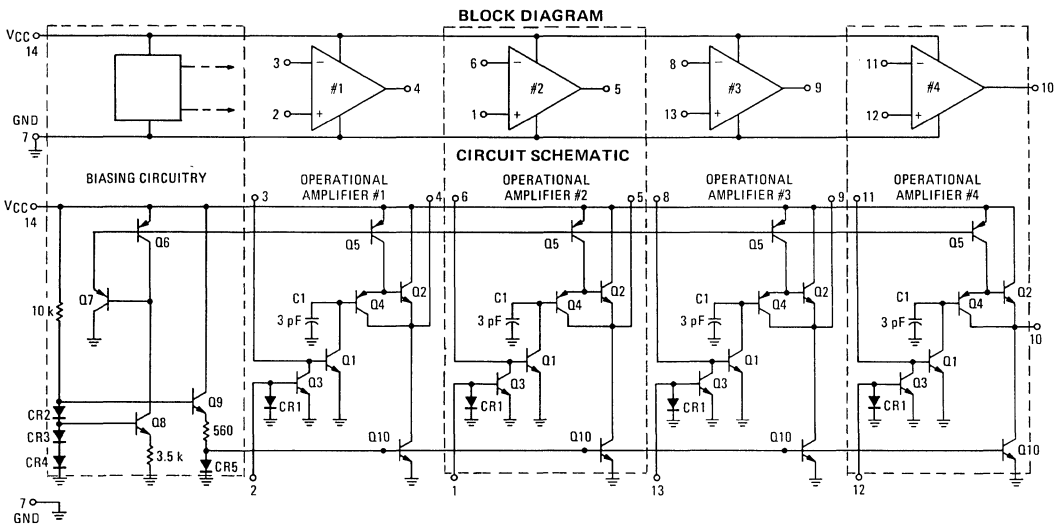
OPERATION AND APPLICATIONS

Basic Amplifier

The basic amplifier is the common emitter stage shown in Figures 15 and 16. The active load I_1 is buffered from the input transistor by a PNP transistor, Q4, and from the output by an NPN transistor, Q2. Q2 is biased class A by the current source I_2. The magnitude of I_2 (specified I_{sink}) is a limiting factor in capacitively coupled linear operation at the output. The sink current of the device can be forced to exceed the specified level with an increase in the distortion appearing at the output. Closed loop stability is maintained by an on-the-chip 3-pF capacitor shown in Figure 18. No external compensation is required.

FIGURE 15



A noninverting input is obtained by adding a current mirror as shown in Figure 17. Essentially all current which enters the noninverting input, I_{in2}, flows through the diode CR1. The voltage drop across CR1 corresponds to this input current magnitude and this same voltage is applied to a matched device, Q3. Thus Q3 is biased to conduct an emitter current equal to I_{in2}. Since the alpha current gain of Q3 $\approx$ 1, its collector current $\approx I_{in2}$ also. In operation this current flows through an external feedback resistor which generates the output voltage signal. For inverting applications, the noninverting input is often used to set the dc quiescent level at the output. Techniques for doing this are discussed in the "Normal Design Procedure" section.

FIGURE 16 – A BASIC GAIN STAGE

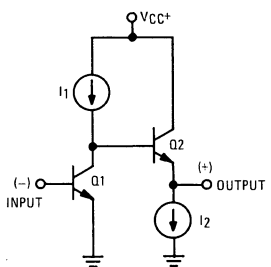
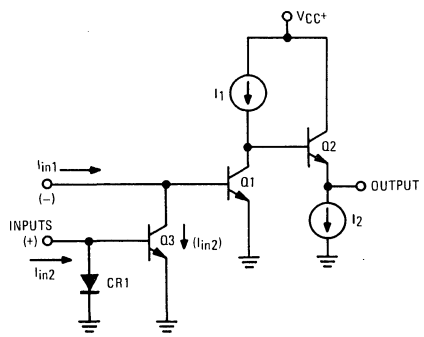


FIGURE 17 – OBTAINING A NONINVERTING INPUT



Biasing Circuitry

The circuitry common to all four amplifiers is shown in Figure 19. The purpose of this circuitry is to provide biasing voltage for the PNP and NPN current sources used in the amplifiers.

The voltage drops across diodes CR2, CR3 and CR4 are used as references. The voltage across resistor R1 is the sum of the drops across CR4 and CR3 minus the V_{BE} of Q8. The PNP current sources (Q5, etc.) are set to the magnitude $V_{BE}/R1$ by transistor Q6. Transistor Q7 reduces base current loading. The voltage across resistor R2 is the sum of the voltage drops across CR2, CR3 and CR4, minus the V_{BE} drops of transistor Q9 and diode CR5. The current thus set is established by CR5 in all the NPN current sources (Q10, etc.). This technique results in current source magnitudes which are relatively independent of the supply voltage.

OPERATION AND APPLICATIONS (continued)

FIGURE 18 – A BASIC OPERATIONAL AMPLIFIER

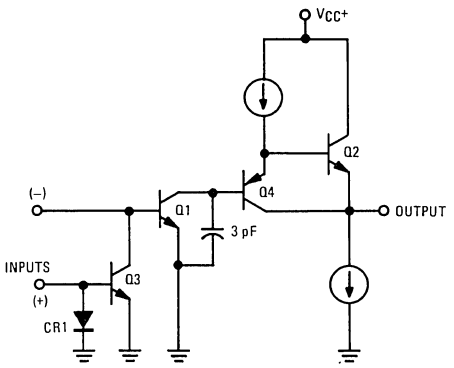
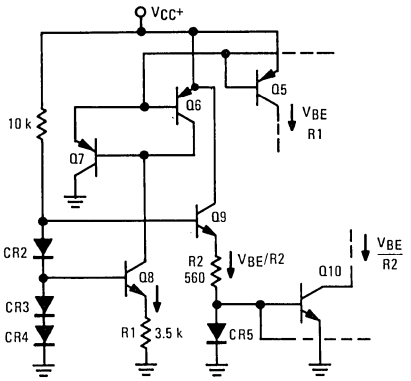


FIGURE 19 – BIASING CIRCUITRY



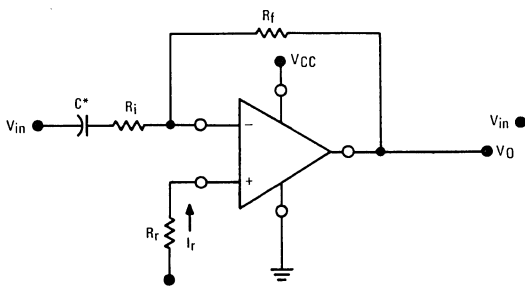
NORMAL DESIGN PROCEDURE

1. Output Q-Point Biasing
   A. A number of techniques may be devised to bias the quiescent output voltage to an acceptable level. However, in terms of loop gain considerations it is usually desirable to use the noninverting input to effect the biasing as shown in Figures 3 and 4. The high impedance of the collector of the noninverting "current mirror" transistor helps to achieve the maximum loop gain for any particular configuration. It is desirable that the noninverting input current be in the 5 μA to 100 μA range.
   B. V_{CC} Reference Voltage (see Figures 3 and 4)
   The noninverting input is normally returned to the V_{CC} voltage (which should be well filtered) through a resistor, R_r, allowing the input current, I_r, to be within the range of 5 μA to 100 μA. Choosing the feedback resistor, R_f, to be equal to ½ R_r will now bias the amplifier output dc level to approximately $\frac{V_{CC}}{2}$. This allows for maximum dynamic range of the output voltage.
   C. Reference Voltage other than V_{CC} (See Figure 20).
   The biasing resistor R_r may be returned to a voltage (V_r) other than V_{CC}. By setting $R_f = R_r$, (still keeping I_r between 5 μA and 100 μA) the output dc level will be equal to V_r. Neglecting error terms, the expression for determining V_{Odc} is:

$$V_{Odc} = \frac{(V_r)\ (R_f)}{R_r} + \left(1 - \frac{R_f}{R_r}\right)\phi$$

   where ϕ is the V_{BE} drop of the input transistors (approximately 0.7 Vdc @ +25°C).
   The error terms not appearing in the above equation can cause the dc operating point to vary up to 20% from the expected value. Error terms are minimized by setting the input current within the range of 5 μA to 100 μA.
2. Gain Determination
   A. Inverting Amplifier
   The amplifier is normally used in the inverting mode. The input may be capacitively coupled to avoid upsetting the dc bias and the output is normally capacitively coupled to eliminate the dc voltage across the load. Note that when the output is capacitively coupled to the load, the value of

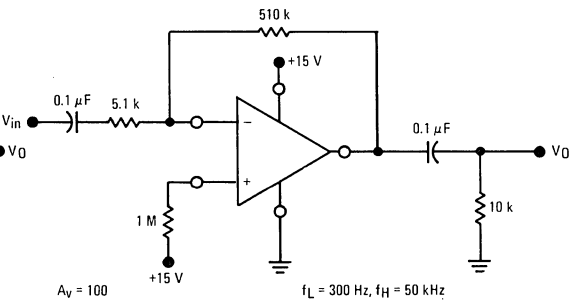
FIGURE 20 – INVERTING AMPLIFIER WITH ARBITRARY REFERENCE



$V_O = \frac{V_r R_f}{R_r} + (1 - \frac{R_f}{R_r})\phi$

*Select for low frequency response.

FIGURE 21 – INVERTING AMPLIFIER WITH A_v = 100 AND $V_r = V_{CC}$



A_v = 100

f_L = 300 Hz, f_H = 50 kHz

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NORMAL DESIGN PROCEDURE (continued)

I_{sink} becomes a limitation with respect to the load driving capabilities of the device. The limitation is less severe if the device is direct coupled. In this configuration, the ac gain is determined by the ratio of R_f to R_i, in the same manner as for a conventional operational amplifier:

$$A_v = -\frac{R_f}{R_i}$$

The lower corner frequency is determined by the coupling capacitors to the input and load resistors. The upper corner frequency will usually be determined by the amplifier internal compensation. The amplifier unity gain bandwidth is typically 5.0 MHz and with the gain roll-off at 20 dB per decade, bandwidth will typically be 500 kHz with 20 dB of closed loop gain or 50 kHz with 40 dB of closed loop gain. The exception to this occurs at low gains where the input resistor selected is large. The pole formed by the amplifier input capacitance, stray capacitance and the input resistor may occur before the closed loop gain intercepts the open loop response curve. The inverting input capacity is typically 3.0 pF.

B. Noninverting Amplifier

Although recommended as an inverting amplifier, the MC 3401P may be used in the noninverting mode (see Figure 4). The amplifier gain in this configuration is subject to the same error terms that affect the output Q point biasing so the gain may deviate as much as ±20% from that expected. In addition, the resistance of the input diode must be included in the value of the input resistor. This resistance is approximately $\frac{26}{I_r}$ ohms, where I_r is input current in milliamperes. The noninverting gain expression is given by:

$$A_v = \frac{R_f}{R_i + \frac{26}{I_r\,(mA)}} \quad \pm 20\%.$$

The bandwidth of the noninverting configuration for a given R_f value is essentially independent of the gain chosen. For R_f = 510 kΩ the bandwidth will be in excess of 200 kHz for noninverting gains of 1, 10, or 100. This is a result of the loop gain remaining constant for these gains since the input resistor is effectively isolated from the feedback loop.

TYPICAL APPLICATIONS

FIGURE 22 – AMPLIFIER AND DRIVER FOR A 50-OHM LINE

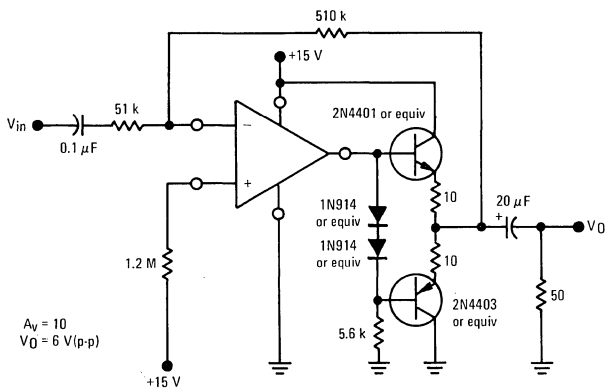
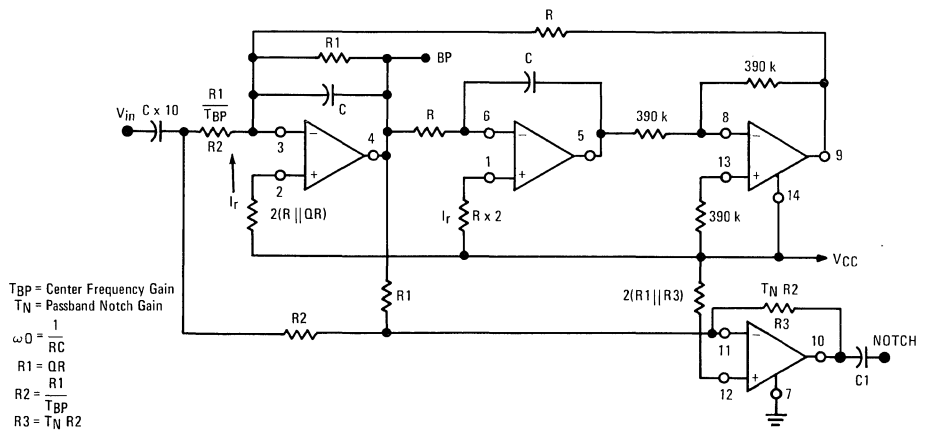


FIGURE 23 – BASIC BANDPASS AND NOTCH FILTER



TYPICAL APPLICATIONS (continued)

FIGURE 24 – BANDPASS AND NOTCH FILTER

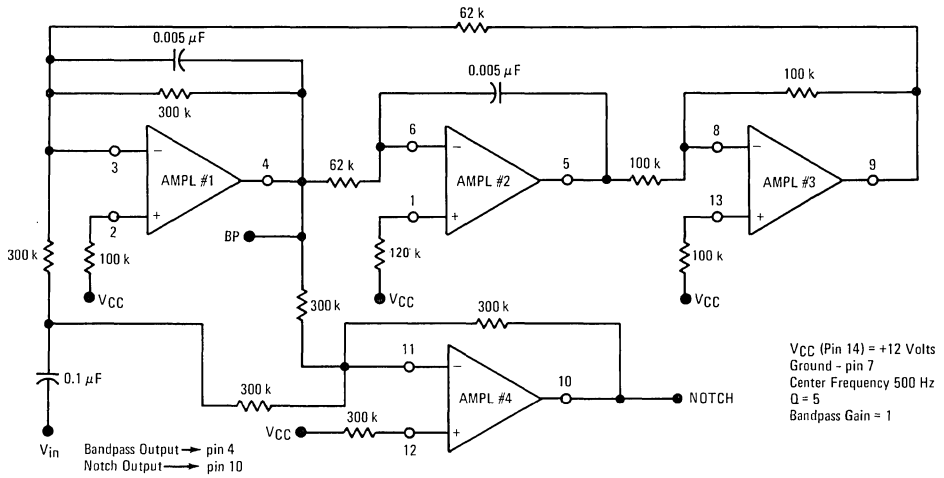
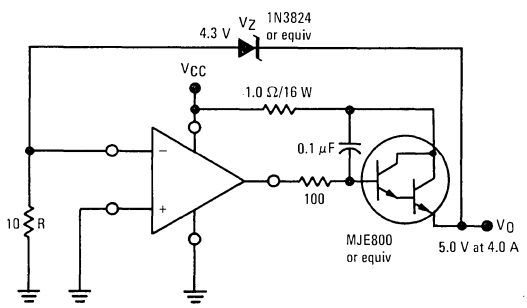


FIGURE 25 – VOLTAGE REGULATOR

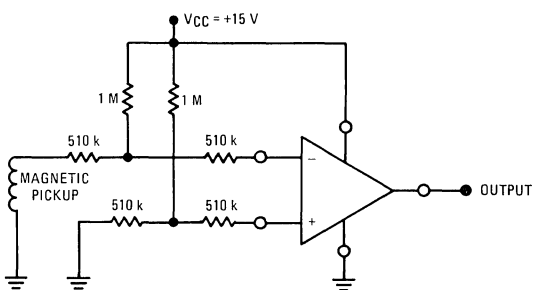


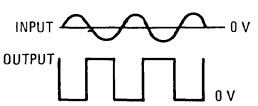
$V_O = V_Z + 0.6$ Vdc

NOTE 1: R is used to bias the zener.

NOTE 2: If the Zener TC is positive, and equal in magnitude to the negative TC of the input to the operational amplifier (≈ 2.0 mV/°C), the output is zero-TC. A 7.0-Volt Zener will give approximately zero-TC.

FIGURE 26 – ZERO CROSSING DETECTOR





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