The Leaky Semicolon

Compositional Semantic Dependencies for Relaxed-Memory Concurrency

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Program logics and semantics tell us that when executing $(S_1; S_2)$ starting in state s_0, we execute S_1 in s_0 to arrive at s_1, then execute S_2 in s_1 to arrive at the final state s_2. This is, of course, an abstraction. Processors execute instructions out of order, due to pipelines and caches, and compilers reorder programs even more dramatically. All of this reordering is meant to be unobservable in single-threaded code, but is observable in multi-threaded code. A formal attempt to understand the resulting mess is known as a "relaxed memory model." The relaxed memory models that have been proposed to date either fail to address sequential composition directly, overly restrict processors and compilers, or permit nonsense thin-air behaviors which are unobservable in practice.

To support sequential composition while targeting modern hardware, we propose using preconditions and families of predicate transformers. When composing $(S_1; S_2)$, the predicate transformers used to validate the preconditions of events in S_2 are chosen based on the semantic dependencies from events in S_1 to events in S_2. We apply this approach to two existing memory models: "Modular Relaxed Dependencies" for C11 and "Pomsets with Preconditions."

CCS Concepts: • **Theory of computation → Parallel computing models**; *Preconditions.*

Additional Key Words and Phrases: Concurrency, Relaxed Memory Models, Multi-Copy Atomicity, ARMv8, Pomsets, Preconditions, Temporal Safety Properties, Thin-Air Reads, Compiler Optimizations

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1 INTRODUCTION

Sequentiality is a *leaky abstraction* [Spolsky 2002]. For example, sequentiality tells us that when executing $(r_1 := x\,;\, y := r_2)$, the assignment $r_1 := x$ is executed before $y := r_2$. Thus, one might reasonably expect that the final value of r_1 is independent of the initial value of r_2. In most modern languages, however, this fails to hold when the program is run concurrently with $(s := y\,;\, x := s)$, which copies y to x.

In certain cases it is possible to ban concurrent access using separation [O'Hearn 2007], or to accept inefficient implementation in order to obtain sequential consistency [Marino et al. 2015]. When these approaches are not available, however, we are left with an enormous gap in our understanding of one of the most basic elements of computing: the humble semicolon. Until recently, existing approaches either

- did not bother tracking dependencies, allowing "thin air" executions — as in C and C++ [Batty et al. 2015],
- tracked dependencies conservatively, using syntax, requiring inefficient implementation of relaxed access [Boehm and Demsky 2014; Kavanagh and Brookes 2018; Lahav et al. 2017;

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Vafeiadis and Narayan 2013]— a non-starter for safe languages like Java, and an unacceptable cost for low-level languages like C,

- computed dependencies using non-compositional operational models over alternate worlds [Chakraborty and Vafeiadis 2019; Cho et al. 2021; Jagadeesan et al. 2010; Kang et al. 2017; Lee et al. 2020; Manson et al. 2005]—these models validate many compiler optimizations, but fail to validate temporal safety properties (see §A.1).

Recently, two denotational models have been proposed that compute sequential dependencies semantically. Paviotti et al. [2020] defined Modular Relaxed Dependencies (MRD-C11), which use event structures to calculate dependencies for C11, targeting the Intermediate Memory Model (IMM) [Podkopaev et al. 2019]. Jagadeesan et al. [2020] defined Pomsets with Preconditions (PwP), which use preconditions and logic to calculate dependencies for a Java-like language targeting multicopy-atomic (MCA) hardware, such as Arm8 [Pulte et al. 2018]. However, neither paper treated sequential composition as a first-class citizen. MRD-C11 encoded sequential composition using continuation-passing, and PwP used prefixing, adding one event at a time on the left. In both cases, adding an event requires perfect knowledge of the future.

In this paper, we show that PwP can be extended with *families of predicate transformers* (PwT) to calculate sequential dependencies in a way that is *compositional* and *direct*: *compositional* in that the denotation of $(S_1 ; S_2)$ can be computed from the denotation of S_1 and the denotation of S_2, and *direct* in that these can be calculated independently. The definition is associative: the denotation of $((S_1 ; S_2) ; S_3)$ is the same as the denotation of $(S_1 ; (S_2 ; S_3))$. It also validates expected laws concerning the interaction of sequencing and conditional execution.

To manage complexity, we have layered the definitions. After an overview and discussion of related work, we define sequential dependencies in §4. We then add concurrency. In §5, we define PwT-MCA, which provides a Java-like model for MCA hardware, similar to that of Jagadeesan et al. [2020]; §6 summarizes the results for this model. In §7, we define PwT-C11, which models C11, adapting the approach of Paviotti et al. [2020]; §8 describes a tool for automatic evaluation of litmus tests. In §9, we extend the semantics to include additional features, such as address calculation and RMWs.

2 OVERVIEW

This paper is about the interaction of two of the fundamental building blocks of computing: sequential composition and mutable state. One would like to think that these are well-worn topics, where every issue has been settled, but this is not the case.

2.1 Sequential Composition

Introductory programmers are taught *sequential abstraction*: that the program $S_1 ; S_2$ executes S_1 before S_2. Since the late 1960s, we've been able to explain this using logic [Hoare 1969]. In Dijkstra's [1975] formulation, we think of programs as *predicate transformers*, where predicates describe the state of memory in the system. In the calculus of weakest preconditions, programs map postconditions to preconditions. We recall the definition of $wp_S(\psi)$ for loop-free code below (where r–s range over thread-local *registers* and M–N range over side-effect-free *expressions*).

(D1) $wp_{\texttt{skip}}(\psi) = \psi$
(D2) $wp_{r := M}(\psi) = \psi[M/r]$
(D3) $wp_{S_1;S_2}(\psi) = wp_{S_1}(wp_{S_2}(\psi))$
(D4) $wp_{\texttt{if}(M)\{S_1\}\texttt{else}\{S_2\}}(\psi) = ((M{\neq}0) \Rightarrow wp_{S_1}(\psi)) \land ((M{=}0) \Rightarrow wp_{S_2}(\psi))$

For this language, the Hoare triple $\{\phi\}\ S\ \{\psi\}$ holds exactly when $\phi \Rightarrow wp_S(\psi)$. This is an elegant explanation of sequential computation in a sequential context. Note that D2 is sound because a read from a thread-local register must be fulfilled by a preceding write in the same thread. In a concurrent context, with shared variables (x–z), the obvious generalization

(D2a) $wp_{x := M}(\psi) = \psi[M/x]$
(D2b) $wp_{r := x}(\psi) = \psi[x/r]$

is unsound! In particular, a read from a shared memory location may be fulfilled by a write in another thread, invalidating D2b. (We assume that expressions do *not* include shared variables.)

In this paper we answer the following question: what does sequential composition mean in a concurrent context? An acceptable answer must satisfy several desiderata:

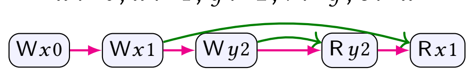
(1) it should not impose too much order, overconstraining the implementation,
(2) it should not impose too little order, allowing bogus executions, and
(3) it should be *compositional* and *direct*, as described in §1.

Memory models differ in how they navigate between desiderata 1 and 2. In one direction there are both more valid compiler optimizations and also more potentially dubious executions, in the other direction, less of both. To understand the tradeoffs, one must first understand the underlying hardware and compilers.

2.2 Memory Models

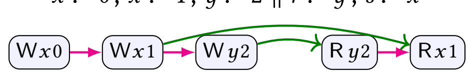
For single-threaded programs, memory can be thought of as you might expect: programs write to, and read from, memory references. This can be thought of as a total order of reads and writes (pink arrows $\rightarrow$), where each read has a matching *fulfilling* write (green arrows $\longrightarrow$), for example:

$$x := 0\,;\; x := 1\,;\; y := 2\,;\; r := y\,;\; s := x$$



This model naturally extends to the case of shared-memory concurrency, leading to a *sequentially consistent* semantics [Lamport 1979], in which *program order* inside a thread implies a total *causal order* between read and write events, for example (where ; has higher precedence than ||):

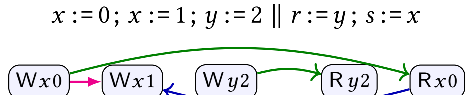
$$x := 0\,;\; x := 1\,;\; y := 2 \parallel r := y\,;\; s := x$$



Unfortunately, this model does not compile efficiently to commodity hardware, resulting in a 37–73% increase in CPU time on Arm8 [Liu et al. 2019] and, hence, in power consumption. Developers of software and compilers have therefore been faced with a difficult trade-off, between an elegant model of memory, and its impact on resource usage (such as size of data centers, electricity bills and carbon footprint). Unsurprisingly, many have chosen to prioritize efficiency over elegance.

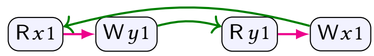
This has led to *relaxed memory models*, in which the requirement of sequential consistency is weakened to only apply *per-location* and not globally over the whole program. This allows executions that are inconsistent with program order, such as:

$$x := 0\,;\; x := 1\,;\; y := 2 \parallel r := y\,;\; s := x$$



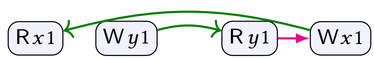
In such models, the causal order between events is important, and includes control and data dependencies, to avoid paradoxical "out of thin air" examples such as:

$$r := x\,;\ \mathtt{if}(r)\{y := 1\} \parallel s := y\,;\ x := s$$



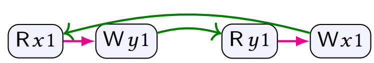
This candidate execution forms a cycle in causal order, so is disallowed, but this depends crucially on the control dependency from $(\mathsf{R}\,x1)$ to $(\mathsf{W}\,y1)$, and the data dependency from $(\mathsf{R}\,y1)$ to $(\mathsf{W}\,x1)$. If either is missing, then this execution is acyclic and hence allowed. For example dropping the control dependency results in:

$$r := x\,;\ y := 1 \parallel s := y\,;\ x := s$$



While syntactic dependency calculation suffices for hardware models, it is not preserved by common compiler optimizations. For example, if we calculate control dependencies syntactically, then there is a dependency from $(\mathsf{R}\,x1)$ to $(\mathsf{W}\,y1)$, and therefore a cycle in, the candidate execution:

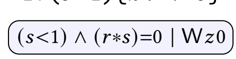
$$r := x\,;\ \mathtt{if}(r)\{y := 1\}\,\mathtt{else}\,\{y := 1\} \parallel s := y\,;\ x := s$$



A compiler may lift the assignment $y := 1$ out of the conditional, thus removing the dependency.

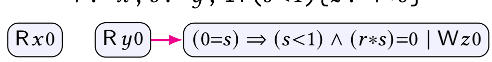
To address this, Jagadeesan et al. [2020] introduced *Pomsets with Preconditions (*PwP*)*, where events are labeled with logical formulae. Nontrivial preconditions are introduced by store actions (modeling data dependencies) and conditionals (modeling control dependencies):

$$\mathtt{if}(s{<}1)\{z := r{*}s\}$$

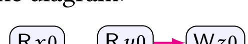


Preconditions are discharged by being ordered after a read (we assume the usual precedence for logical operators—$\neg$, $\wedge$, $\vee$, $\Rightarrow$):

$$r := x\,;\ s := y\,;\ \mathtt{if}(s{<}1)\{z := r{*}s\} \qquad (\dagger)$$



Note that there is dependency order from $(\mathsf{R}\,y0)$ to $(\mathsf{W}\,z0)$ so the precondition for $(\mathsf{W}\,z0)$ only has to be satisfied assuming the hypothesis $(0{=}s)$. There is no matching order from $(\mathsf{R}\,x0)$ to $(\mathsf{W}\,z0)$ which is why we do not assume the hypothesis $(0{=}r)$. Nonetheless, the precondition on $(\mathsf{W}\,z0)$ is a tautology, and so can be elided in the diagram:



2.3 Predicate Transformers For Relaxed Memory

Pomsets with Preconditions show how the logical approach to sequential dependency calculation can be mixed into a relaxed memory model. However, Jagadeesan et al. do not provide a model of sequential composition. Instead, their model uses *prefixing*, which requires that the model is built from right to left: events are prepended one at a time, with perfect knowledge of the future. This makes reasoning about sequential program fragments difficult. For example, Jagadeesan et al. state the equivalence allowing reordering independent writes as follows,

$$[\![x := M\,;\ y := N\,;\ S]\!] = [\![y := N\,;\ x := M\,;\ S]\!] \quad \text{if } x \neq y$$

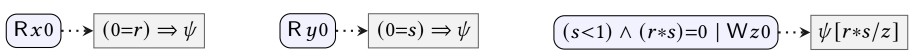
where S is the entire future computation! By formalizing sequential composition, we can show:

$$[\![x := M ; y := N]\!] = [\![y := N ; x := M]\!] \quad \text{if } x \neq y$$

Then the equivalence holds in any context.

Predicate transformers are a good fit for logical models of dependency calculation, since both are concerned with preconditions and how they are transformed by sequential composition. Our first attempt is to associate a predicate transformer with each pomset. We visualize this in diagrams by showing how ψ is transformed, for example:

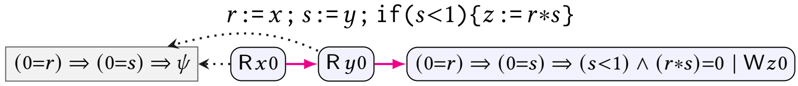
$r := x$ $\qquad$ $s := y$ $\qquad$ $\texttt{if}(s<1)\{z := r*s\}$



The predicate transformer from the write matches Dijkstra's D2a. For the reads, however, D2b defines the transformer of $r := x$ to be $\psi[x/r]$, which is equivalent to $(x{=}r) \Rightarrow \psi$ under the assumption that registers are assigned at most once. Instead, we use $(0{=}r) \Rightarrow \psi$, reflecting the fact that 0 may come from a concurrent write. The obligation to find a matching write is moved from the sequential semantics of *substitution* and *implication* to the concurrent semantics of *fulfillment*.

For a sequentially consistent semantics, sequential composition is straightforward: we apply each predicate transformer to the preconditions of subsequent events, composing the predicate transformers. (In subsequent diagrams, we only show predicate transformers for reads.)

$r := x ; s := y ; \texttt{if}(s<1)\{z := r*s\}$



This model works for the sequentially consistent case, but needs to be weakened for the relaxed case. The key observation of this paper is that rather than working with one predicate transformer, we should work with a *family* of predicate transformers, indexed by sets of events.

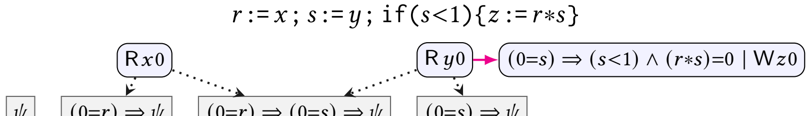
For example, for single-event pomsets, there are two predicate transformers, since there are two subsets of any one-element set. The *independent* transformer is indexed by the empty set, whereas the *dependent* transformer is indexed by the singleton. We visualize this by including more than one transformed predicate, with an edge leading to the dependent one. For example:

$r := x$ $\qquad$ $s := y$

The model of sequential composition then picks which predicate transformer to apply to an event's precondition by picking the one indexed by all the events before it in causal order.

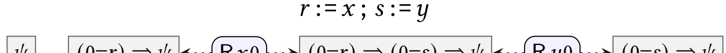
For example, we can recover the expected semantics for (†) by choosing the predicate transformer which is independent of $(\mathsf{R}\,x\,0)$ but dependent on $(\mathsf{R}\,y\,0)$, which is the transformer which maps ψ to $(0{=}s) \Rightarrow \psi$.

$r := x ; s := y ; \texttt{if}(s<1)\{z := r*s\}$



In the diagram, the dotted lines indicate set inclusion into the index of the transformer-family. As a sanity check, we can see that sequential composition is associative in this case, since it does not matter whether we associate to the left, with intermediate step:

$r := x ; s := y$



or to the right, with intermediate step:

$$s := y;\ \mathtt{if}(s<1)\{z := r*s\}$$

$$\boxed{\psi} \qquad \boxed{(0{=}s) \Rightarrow \psi} \dashleftarrow \boxed{\mathsf{R}\,y0} \rightarrow \boxed{(0{=}s) \Rightarrow (s<1) \land (r*s){=}0 \mid \mathsf{W}\,z0}$$

This is an instance of the general result that sequential composition forms a monoid.

3 RELATED WORK

Marino et al. [2015] argue that the "silently shifting semicolon" is sufficiently problematic for programmers that concurrent languages should guarantee sequential abstraction, despite the performance penalties. In this paper, we take the opposite approach. We have attempted to find the most intellectually tractable model that encompasses all of the messiness of relaxed memory.

There are few prior studies of relaxed memory that include sequential composition and/or precise calculation of semantic dependencies. Jagadeesan et al. [2020] give a denotational semantics, using prefixing rather than sequential compositions. Paviotti et al. [2020] give a denotational semantics, calculating dependencies using event structures rather than logic. They give the semantics of sequential composition in continuation passing style, whereas we give it in direct style. This paper provides a general technique for computing sequential dependencies and applies it to these two approaches. We provide a detailed comparison with [Jagadeesan et al. 2020] in §A.2.

Kavanagh and Brookes [2018] define a semantics using pomsets without preconditions. Instead, their model uses syntactic dependencies, thus invalidating many compiler optimizations. They also require a fence after every relaxed read on Arm8. Pichon-Pharabod and Sewell [2016] use event structures to calculate dependencies, combined with an operational semantics that incorporates program transformations. This approach seems to require whole-program analysis.

Other studies of relaxed memory can be categorized by their approach to dependency calculation. Hardware models use syntactic dependencies [Alglave et al. 2014]. Many software models do not bother with dependencies at all [Batty et al. 2011; Cox 2016; Watt et al. 2020, 2019]. Others have strong dependencies that disallow compiler optimizations and efficient implementation, typically requiring fences for every relaxed read on Arm [Boehm and Demsky 2014; Dolan et al. 2018; Jeffrey and Riely 2016; Lahav et al. 2017; Lamport 1979]. Many of the most prominent models are operational, whole-program models based on speculative execution [Chakraborty and Vafeiadis 2019; Cho et al. 2021; Jagadeesan et al. 2010; Kang et al. 2017; Lee et al. 2020; Manson et al. 2005]. We provide a detailed comparison with these approaches in §A.1.

Other work in relaxed memory has shown that tooling is especially useful to researchers, architects, and language specifiers, enabling them to build intuitions experimentally [Alglave et al. 2014; Batty et al. 2011; Cooksey et al. 2019; Paviotti et al. 2020]. Unfortunately, it is not obvious that tools can be built for all thin-air free models, the calculation of Pichon-Pharabod and Sewell [2016] does not have a termination proof for an arbitrary input, and the enormous state space for the operational models of Kang et al. [2017] and Chakraborty and Vafeiadis [2019] is a daunting prospect for a tool builder – and as yet no tool exists for automatically evaluating these models. We describe a tool, PwTer, for automatically evaluating PwT in §8.

4 SEQUENTIAL SEMANTICS

After some preliminaries (§4.1–4.2), we define the basic model and establish some basic properties (§4.3 and Fig. 1). We then explain the model using examples (§4.4–4.9). We encourage readers to skim the definitions and then skip to §4.4, coming back as needed.

4.1 Preliminaries

The syntax is built from

- a set of *values* $\mathcal{V}$, ranged over by v, w, ℓ, k,
- a set of *registers* $\mathcal{R}$, ranged over by r, s,
- a set of *expressions* $\mathcal{M}$, ranged over by M, N, L.

Memory references are tagged values, written $[\ell]$. Let $\mathcal{X}$ be the set of memory references, ranged over by x, y, z. We require that

- values and registers are disjoint,
- values include at least the constants 0 and 1,
- expressions include at least registers and values,
- expressions do *not* include references: $M[N/x] = M$.

We model the following language.

$$\mu, \nu \ ::= \mathsf{rlx} \mid \mathsf{rel} \mid \mathsf{acq} \mid \mathsf{sc}$$

$$S \ ::= \ r := M \mid r := [L]^{\mu} \mid [L]^{\mu} := M \mid \mathsf{F}^{\mu} \mid \mathtt{skip} \mid S_1 ; S_2 \mid \mathtt{if}(M)\{S_1\}\mathtt{else}\{S_2\} \mid S_1 \mathbin{+\!\!\!\!\shortmid\!\!\!\shortmid\!\!\!\!\!\to} S_2$$

Access modes, μ, are relaxed (rlx), release (rel), acquire (acq), and sequentially consistent (sc). Let expressions ($r := M$) only affect thread-local state and thus do not have a mode. Reads ($r := [L]^{\mu}$) support rlx, acq, sc. Writes ($[L]^{\mu} := r$) support rlx, rel, sc. Fences (F^{μ}) support rel, acq, sc. In examples, the default mode for reads and writes is rlx—we systematically drop the annotation.

Commands, aka *statements*, S, include memory accesses at a given mode, as well as the usual structural constructs. Following [Ferreira et al. 1996], $\mathbin{+\!\!\!\!\shortmid\!\!\!\shortmid\!\!\!\!\!\to}$ denotes parallel composition, preserving thread state on the right after a join. In examples and sublanguages without join, we use the symmetric $\parallel$ operator.

We use common syntax sugar, such as *extended expressions*, $\mathbb{M}$, which include memory locations. For example, if $\mathbb{M}$ includes a single occurrence of x, then $y := \mathbb{M}; S$ is shorthand for $r := x;$ $y := \mathbb{M}[r/x]; S$. Each occurrence of x in an extended expression corresponds to an separate read. We also write $\mathtt{if}(M)\{S\}$ as shorthand for $\mathtt{if}(M)\{S\}\mathtt{else}\{\mathtt{skip}\}$.

Throughout §1–8 we require that

- each register is assigned at most once in a program.

In §9, we drop this restriction, requiring instead that

- there are registers $\mathcal{S}_{\mathcal{E}} = \{s_e \mid e \in \mathcal{E}\}$, that do not appear in programs: $S[N/s_e] = S$.

The semantics is built from the following.

- a set of *events* $\mathcal{E}$, ranged over by e, d, c, and subsets ranged over by E, D, C,
- a set of *logical formulae* Φ, ranged over by ϕ, ψ, θ,
- a set of *actions* $\mathcal{A}$, ranged over by a, b,
- a family of *quiescence symbols* Q_x, indexed by location.

We require that

- formulae include tt, ff, Q_x, and the equalities ($M{=}N$) and ($x{=}M$),
- formulae are closed under $\neg$, $\wedge$, $\vee$, $\Rightarrow$, and substitutions $[M/r]$, $[M/x]$, $[\phi/\mathsf{Q}_x]$,
- there is a relation $\models$ between formulae, capturing entailment,
- $\models$ has the expected semantics for $=$, $\neg$, $\wedge$, $\vee$, $\Rightarrow$ and substitutions $[M/r]$, $[M/x]$, $[\phi/\mathsf{Q}_x]$,
- there is a subset of $\mathcal{A}$, distinguishing *read* actions,
- there are four binary relations over $\mathcal{A} \times \mathcal{A}$: *delays* and *matches* $\subseteq$ *blocks* $\subseteq$ *overlaps*.

Logical formulae include equations over registers and memory references, such as ($r{=}s{+}1$) and ($x{=}1$). We use expressions as formulae, coercing M to $M{\neq}0$.

We write $\phi \equiv \psi$ when $\phi \vDash \psi$ and $\psi \vDash \phi$. We say ϕ is a *tautology* if $\mathsf{tt} \vDash \phi$. We say ϕ is *unsatisfiable* if $\phi \vDash \mathsf{ff}$, and *satisfiable* otherwise.

4.2 Actions in This Paper

In this paper, we let actions be reads and writes and fences:

$$a, b \ ::= \ \mathsf{W}^{\mu}xv \ \mid \ \mathsf{R}^{\mu}xv \ \mid \ \mathsf{F}^{\mu}$$

We use shorthand when referring to actions. In definitions, we drop elements of actions that are existentially quantified. In examples, we drop elements of actions, using defaults. Let $\sqsubseteq$ be the smallest order over access and fence modes such that $\mathsf{rlx} \sqsubseteq \mathsf{rel} \sqsubseteq \mathsf{sc}$ and $\mathsf{rlx} \sqsubseteq \mathsf{acq} \sqsubseteq \mathsf{sc}$. We write $(\mathsf{W}^{\sqsupseteq\mathsf{rel}})$ to stand for either $(\mathsf{W}^{\mathsf{rel}})$ or $(\mathsf{W}^{\mathsf{sc}})$, and similarly for the other actions and modes.

Definition 4.1. Actions (R) are *read* actions.
We say a *matches* b if $a = (\mathsf{W}xv)$ and $b = (\mathsf{R}xv)$.
We say a *blocks* b if $a = (\mathsf{W}x)$ and $b = (\mathsf{R}x)$, regardless of value.
We say a *overlaps* b if they access the same location, regardless of whether they read or write.
Let $\bowtie_{\mathsf{co}}$ capture write-write, read-write coherence: $\bowtie_{\mathsf{co}} = \{(\mathsf{W}x, \mathsf{W}x),\ (\mathsf{R}x, \mathsf{W}x),\ (\mathsf{W}x, \mathsf{R}x)\}$.
Let $\ltimes_{\mathsf{sync}}$ capture conflict due to synchronization:[1] $\ltimes_{\mathsf{sync}} = \{(a, \mathsf{W}^{\sqsupseteq\mathsf{rel}}),\ (a, \mathsf{F}^{\sqsupseteq\mathsf{rel}}),\ (\mathsf{R}, \mathsf{F}^{\sqsupseteq\mathsf{acq}}),\ (\mathsf{R}^{\sqsupseteq\mathsf{acq}}, b),\ (\mathsf{F}^{\sqsupseteq\mathsf{acq}}, b),\ (\mathsf{F}^{\sqsupseteq\mathsf{rel}}, \mathsf{W}),\ (\mathsf{W}^{\sqsupseteq\mathsf{rel}}x, \mathsf{W}x)\}$.
Let $\bowtie_{\mathsf{sc}}$ capture conflict due to sc access: $\bowtie_{\mathsf{sc}} = \{(\mathsf{W}^{\mathsf{sc}}, \mathsf{W}^{\mathsf{sc}}),\ (\mathsf{R}^{\mathsf{sc}}, \mathsf{W}^{\mathsf{sc}}),\ (\mathsf{W}^{\mathsf{sc}}, \mathsf{R}^{\mathsf{sc}}),\ (\mathsf{R}^{\mathsf{sc}}, \mathsf{R}^{\mathsf{sc}})\}$.
We say a *delays* b if $a \bowtie_{\mathsf{co}} b$ or $a \ltimes_{\mathsf{sync}} b$ or $a \bowtie_{\mathsf{sc}} b$.

4.3 PwT: Pomsets with Predicate Transformers

Predicate transformers are functions on formulae that preserve logical structure, providing a natural model of sequential composition. The definition comes from Dijkstra [1975]:

Definition 4.2. A *predicate transformer* is a function $\tau : \Phi \longrightarrow \Phi$ such that
(x1) $\tau(\psi_1 \wedge \psi_2) \equiv \tau(\psi_1) \wedge \tau(\psi_2)$,
(x2) $\tau(\psi_1 \vee \psi_2) \equiv \tau(\psi_1) \vee \tau(\psi_2)$,
(x3) if $\phi \vDash \psi$, then $\tau(\phi) \vDash \tau(\psi)$.

We consistently use ψ as the parameter of predicate transformers. Note that substitutions ($\psi[M/r]$ and $\psi[M/x]$) and implications on the right ($\phi \Rightarrow \psi$) are predicate transformers.

As discussed in §1, predicate transformers suffice for sequentially consistent models, but not relaxed models, where dependency calculation is crucial. For dependency calculation, we use a *family* of predicate transformers, indexed by sets of events. In sequential composition, we will use $\tau^{\downarrow e}$ as the predicate transformer applied to event e where $d \in (\downarrow e)$ if $d < e$.

Definition 4.3. A *family of predicate transformers* over E consists of a predicate transformer τ^D for each $D \subseteq \mathcal{E}$, such that if $C \cap E \subseteq D$ then $\tau^C(\psi) \vDash \tau^D(\psi)$.
We write $\tau(\psi)$ as an abbreviation of $\tau^E(\psi)$.

In a family of predicate transformers, the transformer of a smaller set must entail the transformer of a larger set. Thus bigger sets are *better* and $\tau(\psi)$—the transformer of the biggest set—is the *best*. (Note that the definition is written to be insensitive to events outside E.)

In sequential composition, adding more order can only increase the size of $\downarrow e$. Following Def. 4.3, the larger $\downarrow e$ is, the better, at least in terms of satisfying preconditions. Thus more order means weaker preconditions.

Definition 4.4. A *pomset with predicate transformers* (PwT) is a tuple $(E, \lambda, \kappa, \tau, \checkmark, <)$ where

[1] Symmetry would suggest that we include $(\mathsf{R}x, \mathsf{R}^{\sqsupseteq\mathsf{acq}}x)$, but this is not sound for Arm8.

(M1) $E \subseteq \mathcal{E}$ is a set of *events*,
(M2) $\lambda : E \to \mathcal{A}$ defines a *label* for each event,
(M3) $\kappa : E \to \Phi$ defines a *precondition* for each event,
(M4) $\tau : 2^{\mathcal{E}} \to \Phi \to \Phi$ is a *family of predicate transformers* over E,
(M5) $\checkmark : \Phi$ is a *termination condition*, such that
(M5a) $\checkmark \vDash \tau(\mathrm{tt})$,
(M6) $< \subseteq E \times E$, is a strict partial order capturing *causality*,

A PwT is *complete* if
(C3) $\kappa(e)$ is a tautology (for every $e \in E$), (C5) $\checkmark$ is a tautology.

Let P range over pomsets, and $\mathcal{P}$ over sets of pomsets. We give the semantics of programs $[\![\cdot]\!]$ in Fig. 1. The model has 6 components, which can be daunting at first glance. To aid the reader, we use consistent numbering throughout. For example, item 6 always refers to the order relation.

The core of the model is a pomset, which includes a set of events (M1), a labeling (M2), and an order (M6). As usual, we write $d \le e$ to mean $d < e$ or $d = e$. On top of this basic structure, M3–M5 add a layer of logic. For each pomset, M5 provides a termination condition. For each event in a pomset, M3 provides a precondition. For each set of events in a pomset, M4 provides a predicate transformer. Sequential dependency is calculated by κ'_2 in the semantics of sequential composition.

Before discussing the details of the model, we note that the semantics satisfies the expected monoid laws and is closed with respect to *augmentation*. Augments include more order and stronger formulae; in examples, we typically consider pomsets that are augment-minimal. One intuitive reading of augment closure is that adding order can only cause preconditions to weaken.

Lemma 4.5. *(a)* $\mathcal{P} = (\mathcal{P}\,;\,\mathit{SKIP}) = (\mathit{SKIP}\,;\,\mathcal{P})$.
(b) $(\mathcal{P}_1\,;\,\mathcal{P}_2)\,;\,\mathcal{P}_3 = \mathcal{P}_1\,;\,(\mathcal{P}_2\,;\,\mathcal{P}_3)$.

Proof. Straightforward calculation. (a) requires M5a for the termination condition in $(\mathcal{P}\,;\,\mathit{SKIP})$. (b) requires both conjunction closure (X1, for the termination condition) and disjunction closure (X2, for the predicate transformers themselves). □

Lemma 4.6. *(d)* $\texttt{if}(\phi)\{\texttt{if}(\psi)\{\mathcal{P}\}\} = \texttt{if}(\phi \land \psi)\{\mathcal{P}\}$.
(e) $\texttt{if}(\phi)\{\mathcal{P}_1\,;\,\mathcal{P}_3\}\,\texttt{else}\,\{\mathcal{P}_2\,;\,\mathcal{P}_3\} \supseteq \texttt{if}(\phi)\{\mathcal{P}_1\}\,\texttt{else}\,\{\mathcal{P}_2\}\,;\,\mathcal{P}_3$.
(f) $\texttt{if}(\phi)\{\mathcal{P}_1\,;\,\mathcal{P}_2\}\,\texttt{else}\,\{\mathcal{P}_1\,;\,\mathcal{P}_3\} \supseteq \mathcal{P}_1\,;\,\texttt{if}(\phi)\{\mathcal{P}_2\}\,\texttt{else}\,\{\mathcal{P}_3\}$.
(g) $\texttt{if}(\phi)\{\mathcal{P}\}\,\texttt{else}\,\{\mathcal{P}\} \supseteq \mathcal{P}$.
(h) $\texttt{if}(\phi)\{\mathcal{P}_1\}\,\texttt{else}\,\{\mathcal{P}_2\} \supseteq \mathcal{P}_1$ *if* ϕ *is a tautology.*
(i) $\texttt{if}(\phi)\{\mathcal{P}_1\}\,\texttt{else}\,\{\mathcal{P}_2\} = \texttt{if}(\phi)\{\mathcal{P}_1\};\,\texttt{if}(\neg\phi)\{\mathcal{P}_2\}$.
(j) $\texttt{if}(\phi)\{\mathcal{P}_1\}\,\texttt{else}\,\{\mathcal{P}_2\} = \texttt{if}(\neg\phi)\{\mathcal{P}_2\};\,\texttt{if}(\phi)\{\mathcal{P}_1\}$.

Proof. Straightforward calculation. □

In §9.5, we refine the semantics to validate the reverse inclusions for (e), (f), and (g). In §9.2, we refine the semantics to validate the reverse inclusion for (h). As discussed in §5.1, for PwT-MCA, (i) and (j) are inclusions, rather than equations; we show how to restore them to equations in §A.7

Definition 4.7. P_2 is an *augment* of P_1 if all fields are equal except, perhaps, the order, where we require $<_2 \supseteq <_1$.

Lemma 4.8. *If* $P_1 \in [\![S]\!]$ *and* P_2 *augments* P_1 *then* $P_2 \in [\![S]\!]$.

Proof. Induction on the definition of $[\![\cdot]\!]$. □

If $P \in \mathit{SKIP}$ then $E = \emptyset$ and $\tau^D(\psi) \equiv \psi$ and $\checkmark \equiv \mathsf{tt}$.

If $P \in \mathit{SEQ}(\mathcal{P}_1, \mathcal{P}_2)$ then $(\exists P_1 \in \mathcal{P}_1)\ (\exists P_2 \in \mathcal{P}_2)$
let $\kappa'_2(e) = \tau_1^{\downarrow e}(\kappa_2(e))$, where $\downarrow e = \{c \mid c < e\}$,

(s1) $E = (E_1 \cup E_2)$,
(s2) $\lambda = (\lambda_1 \cup \lambda_2)$,
(s3a) if $e \in E_1 \setminus E_2$ then $\kappa(e) \equiv \kappa_1(e)$,
(s3b) if $e \in E_2 \setminus E_1$ then $\kappa(e) \equiv \kappa'_2(e)$,
(s3c) if $e \in E_1 \cap E_2$ then $\kappa(e) \equiv \kappa_1(e) \vee \kappa'_2(e)$,
(s4) $\tau^D(\psi) \equiv \tau_1^D(\tau_2^D(\psi))$,
(s5) $\checkmark \equiv \checkmark_1 \wedge \tau_1(\checkmark_2)$,
(s6) $< \supseteq <_1 \cup <_2$.

If $P \in \mathit{IF}(\phi, \mathcal{P}_1, \mathcal{P}_2)$ then $(\exists P_1 \in \mathcal{P}_1)\ (\exists P_2 \in \mathcal{P}_2)$

(i1) $E = (E_1 \cup E_2)$,
(i2) $\lambda = (\lambda_1 \cup \lambda_2)$,
(i3a) if $e \in E_1 \setminus E_2$ then $\kappa(e) \equiv \phi \wedge \kappa_1(e)$,
(i3b) if $e \in E_2 \setminus E_1$ then $\kappa(e) \equiv \neg\phi \wedge \kappa_2(e)$,
(i3c) if $e \in E_1 \cap E_2$ then $\kappa(e) \equiv (\phi \wedge \kappa_1(e)) \vee (\neg\phi \wedge \kappa_2(e))$,
(i4) $\tau^D(\psi) \equiv (\phi \wedge \tau_1^D(\psi)) \vee (\neg\phi \wedge \tau_2^D(\psi))$,
(i5) $\checkmark \equiv (\phi \wedge \checkmark_1) \vee (\neg\phi \wedge \checkmark_2)$,
(i6) $< \supseteq <_1 \cup <_2$.

If $P \in \mathit{LET}(r, M)$ then $E = \emptyset$ and $\tau^D(\psi) \equiv \psi[M/r]$ and $\checkmark \equiv \mathsf{tt}$.

If $P \in \mathit{WRITE}(x, M, \mu)$ then $(\exists v \in \mathcal{V})$

(w1) $|E| \leqslant 1$,
(w2) $\lambda(e) = \mathsf{W}^\mu x v$,
(w3) $\kappa(e) \equiv M{=}v$,
(w4a) if $E \neq \emptyset$ then $\tau^D(\psi) \equiv \psi[M/x][M{=}v/\mathsf{Q}_x]$,
(w4b) if $E = \emptyset$ then $\tau^D(\psi) \equiv \psi[M/x][\mathsf{ff}/\mathsf{Q}_x]$,
(w5a) if $E \neq \emptyset$ then $\checkmark \equiv M{=}v$,
(w5b) if $E = \emptyset$ then $\checkmark \equiv \mathsf{ff}$.

If $P \in \mathit{READ}(r, x, \mu)$ then $(\exists v \in \mathcal{V})$

(r1) $|E| \leqslant 1$,
(r2) $\lambda(e) = \mathsf{R}^\mu x v$,
(r3) $\kappa(e) \equiv \mathsf{Q}_x$,
(r4a) if $e \in E \cap D$ then $\tau^D(\psi) \equiv v{=}r \Rightarrow \psi$,
(r4b) if $e \in E \setminus D$ then $\tau^D(\psi) \equiv (v{=}r \vee x{=}r) \Rightarrow \psi$,
(r4c) if $E = \emptyset$ then $\tau^D(\psi) \equiv \psi$,
(r5a) if $E \neq \emptyset$ or $\mu \sqsubseteq \mathsf{rlx}$ then $\checkmark \equiv \mathsf{tt}$,
(r5b) if $E = \emptyset$ and $\mu \sqsupseteq \mathsf{acq}$ then $\checkmark \equiv \mathsf{ff}$.

$$
\begin{aligned}
[\![r := M]\!] &= \mathit{LET}(r, M) & [\![\mathtt{skip}]\!] &= \mathit{SKIP} \\
[\![r := x^\mu]\!] &= \mathit{READ}(r, x, \mu) & [\![S_1\,;\,S_2]\!] &= \mathit{SEQ}([\![S_1]\!], [\![S_2]\!]) \\
[\![x^\mu := M]\!] &= \mathit{WRITE}(x, M, \mu) & [\![\mathtt{if}(M)\{S_1\}\,\mathtt{else}\,\{S_2\}]\!] &= \mathit{IF}(M{\neq}0, [\![S_1]\!], [\![S_2]\!])
\end{aligned}
$$

Fig. 1. PwT Semantics

4.4 Pomsets and Complete Pomsets

Ignoring the logic, the definitions are straightforward. Reads and writes map to pomsets with at most one event. skip maps to the empty pomset. Note only that $[\![x := 1]\!]$ can write any value v; the fact that v must be 1 is captured in the logic.

The structural rules combine pomsets: *SEQ* and *IF* perform a union, inheriting labeling and order from the two sides. We say that $d \in E_1$ and $e \in E_2$ *coalesce* if $d = e$.

As a trivial consequence of using union rather than disjoint union, s1 validates *mumbling* [Brookes 1996] by coalescing events. For example $[\![x := 1\,;\, x := 1]\!]$ includes the singleton pomset $\boxed{\mathsf{W}x1}$. From this it is easy to see that $[\![x := 1\,;\, x := 1]\!] \supseteq [\![x := 1]\!]$ is a valid refinement. It is equally obvious that

$[\![x := 1]\!] \not\supseteq [\![x := 1\,;\; x := 1]\!]$ is not a valid refinement, since the latter includes a two-element pomset, but the former does not.[2]

In complete pomsets, c5 requires that ✓ is a tautology, capturing termination. In *WRITE*, w5b ensures that all writes are included in complete pomsets. This also ensures $[\![x := 1]\!] \not\supseteq [\![\texttt{if}(M)\{x := 1\}]\!]$, since $[\![\texttt{if}(M)\{x := 1\}]\!]$ includes the empty set with termination condition $\neg M$, but $[\![x := 1]\!]$ can only include the empty set with termination condition ff.

In addition, w5a ensures that complete pomsets do not include bogus writes. Suppose $P \in [\![x := 1]\!]$. As we noted above, P can include $(1{=}v \mid \mathsf{W}xv)$, for any value v. In complete pomsets, however, w5a requires that ✓ implies $1{=}v$. In this case, m3a would filter the pomset, since preconditions must be satisfiable. However, unsatisfiable writes can be become satisfiable via merging:

$$\begin{array}{ccc} x := 1 & x := 2 & \texttt{if}(M)\{x := 3\} \\ \boxed{\mathsf{W}x1} & \boxed{2{=}3 \mid \mathsf{W}x3} & \boxed{M \mid \mathsf{W}x3} \end{array}$$

By merging, the semantics allows the following:

$$\begin{array}{c} x := 1\,;\; x := 2\,;\; \texttt{if}(M)\{x := 3\} \\ \boxed{\mathsf{W}x1} \quad \boxed{M \mid \mathsf{W}x3} \end{array}$$

This pomset is incomplete, however, since ✓ $\equiv 2{=}3$.

In *READ*, ✓ depends on the mode. r5b ensures that all acquiring reads are included in complete pomsets. Instead r5a states that relaxed reads are optional: ✓ is alway true for relaxed reads. From this, it is easy to see that $[\![r := x]\!] \supseteq [\![\texttt{skip}]\!]$ is a valid refinement (where the default mode is rlx).

Ignoring predicate transformers, the *SEQ* rule s5 takes ✓ to be $✓_1 \wedge ✓_2$. This is as expected: the program terminates if both subprograms terminate.

In $\mathit{IF}(\phi, \mathcal{P}_1, \mathcal{P}_2)$, the termination condition (i5) is $(\phi \wedge ✓_1) \vee (\neg\phi \wedge ✓_2)$: the program terminates as long as the "true" branch terminates. Thus $[\![\texttt{if}(\texttt{tt})\{x := 1\}\,\texttt{else}\,\{y := 1\}]\!]$ contains a complete pomset with exactly one event: $(\mathsf{W}x1)$. To construct this pomset, we take the singleton from the left and the empty set from the right. This is a general principle: for code that contributes no events at top-level, use the empty set.

4.5 Preconditions, Predicate Transformers, and Data Dependencies

Preconditions are used to calculate dependencies. They also determine which events can appear in a pomset. In a complete pomset, c3 requires that every precondition $\kappa(e)$ is a tautology. Using w3, $[\![x := 2]\!]$ cannot include a complete pomset with event $(\mathsf{W}x3)$, since $2{=}3$ is not a tautology. The symbols Q_x that occur in r3 and w4 serve similar purpose. We defer discussion of these until §4.8.

Preconditions are discharged during sequential composition by applying predicate transformers τ_1 from the left to preconditions $\kappa_2(e)$ on the right. The specific rules are s3b and s3c, which use the transformed predicate $\kappa_2'(e) = \tau_1^{\downarrow e}(\kappa_2(e))$, where $\downarrow e = \{c \mid c < e\}$ is the set of events that precede e in causal order. We call $\downarrow e$ the *dependent set* for e. Then $E \setminus (\downarrow e)$ is the *independent set*.

Before looking at the details, it is useful to have a high-level view of how nontrivial preconditions and predicate transformers are introduced. (We discuss address dependencies in §9.3.)

Preconditions are introduced in:

(i3) for control dependencies,
(w3) for data dependencies on writes.

Predicate transformers are introduced in:

(r4a) for reads in the dependent set,
(r4b) for reads in the independent set,
(w4) for writes.

The rules track dependencies. We discuss data dependencies (w3) here and control dependencies (i3) in §4.6. Unless otherwise noted, we assume pomsets are *complete* and *augment-minimal*.

[2]These are distinguished by the context: $[-] \parallel r := x\,;\; x := 2\,;\; s := x\,;\; \texttt{if}(r{=}s)\{z := 1\}$.

A simple example of a data dependency is a pomset $P \in [\![r := x\,;\, y := r]\!]$. If P is complete, it must have two events. Then *SEQ* requires that there are $P_1 \in [\![r := x]\!]$ and $P_2 \in [\![y := r]\!]$ of the form:

$$\begin{array}{cc} r := x & y := r \\ \boxed{(x{=}r \lor v{=}r) \Rightarrow \psi}\ \ (\mathsf{R}\,x\,v)^{d} \dashrightarrow \boxed{v{=}r \Rightarrow \psi} & \boxed{\psi[r/y]}\ \ (r{=}w \mid \mathsf{W}\,y\,w)^{e} \dashrightarrow \boxed{\psi[r/y]} \end{array} \qquad (\dagger\dagger)$$

First we consider the case that $v = w$. For example if $v = w = 1$, we have:

$$\boxed{(x{=}r \lor 1{=}r) \Rightarrow \psi}\ \ (\mathsf{R}\,x\,1)^{d} \dashrightarrow \boxed{1{=}r \Rightarrow \psi} \qquad \boxed{\psi[r/y]}\ \ (r{=}1 \mid \mathsf{W}\,y\,1)^{e} \dashrightarrow \boxed{\psi[r/y]}$$

For the read, the dependent transformer $\tau_1^{\{d\}}$ is $1{=}r \Rightarrow \psi$; the independent transformer $\tau_1^{\emptyset}$ is $(x{=}r \lor 1{=}r) \Rightarrow \psi$. These are determined by R4a and R4b, respectively. For the write, both $\tau_2^{\{e\}}$ and $\tau_2^{\emptyset}$ are $\psi[r/y]$, as are determined by W4. Combining these into a single pomset, we have:

$$\begin{array}{c} r := x\,;\, y := r \\ \boxed{(x{=}r \lor 1{=}r) \Rightarrow \psi[r/y]}\ \ (\mathsf{R}\,x\,1)^{d} \dashrightarrow \boxed{1{=}r \Rightarrow \psi[r/y]} \qquad (\phi \mid \mathsf{W}\,y\,1)^{e} \end{array}$$

By S4, predicate transformers are determined by composition; thus $\tau^D(\psi)$ is $\tau_1^D(\tau_2^D(\psi))$. Since the transformer does not depend on whether the write is included, we do not draw dependencies for the write in the diagram.

Turning to the precondition ϕ on the write, recall that in order for e to participate in a top-level pomset, the precondition ϕ must be a tautology at top-level. There are two possibilities.

- If $d < e$ then we apply the dependent transformer and $\phi \equiv (1{=}r \Rightarrow r{=}1)$, a tautology.
- If $d \not< e$ then we apply the independent transformer and $\phi \equiv ((x{=}r \lor 1{=}r) \Rightarrow r{=}1)$. Under the assumption that r is bound, this is logically equivalent to $(x{=}1)$. (We make this more precise in §9.2.)

Eliding transformers, the two outcomes are:

$$\begin{array}{cc} r := x\,;\, y := r & r := x\,;\, y := r \\ (\mathsf{R}\,x\,1)^{d} \rightarrow (\mathsf{W}\,y\,1)^{e} & (\mathsf{R}\,x\,1)^{d} \quad (x{=}1 \mid \mathsf{W}\,y\,1)^{e} \end{array}$$

The independent case on the right can only participate in a top-level pomset if the precondition $(x{=}1)$ is discharged. To do so, we must prepend a pomset P_0 that writes 1 to x:

$$\begin{array}{cc} x := 1 & x := 1\,;\, r := x\,;\, y := r \\ \boxed{\psi[1/x]}\ \ (1{=}1 \mid \mathsf{W}\,x\,1)^{c} \dashrightarrow \boxed{\psi[1/x]} & (1{=}1 \mid \mathsf{W}\,x\,1)^{c} \quad (\mathsf{R}\,x\,1)^{d} \quad (1{=}1 \mid \mathsf{W}\,y\,1)^{e} \end{array}$$

Here we apply the predicate transformer $\tau_0^{\emptyset}$ to $(x{=}1)$, resulting in the tautology $(1{=}1)$.

Now suppose that $v \neq w$ in $(\dagger\dagger)$. Again there are two possibilities. Taking $v{=}0$ and $w{=}1$:

$$\begin{array}{cc} r := x\,;\, y := r & r := x\,;\, y := r \\ (\mathsf{R}\,x\,0)^{d} \rightarrow (0{=}r \Rightarrow r{=}1 \mid \mathsf{W}\,y\,1)^{e} & (\mathsf{R}\,x\,0)^{d} \quad ((x{=}r \lor 0{=}r) \Rightarrow r{=}1 \mid \mathsf{W}\,y\,1)^{e} \end{array}$$

Assuming that r is bound, both preconditions on e are unsatisfiable.

If a write is independent of a read, then clearly no order is imposed between them. For example, the precondition of e is a tautology in:

$$\begin{array}{c} r := x\,;\, y := 1 \\ \boxed{(x{=}r \lor 0{=}r) \Rightarrow \psi[r/y]}\ \ (\mathsf{R}\,x\,0)^{d} \dashrightarrow \boxed{0{=}r \Rightarrow \psi[r/y]} \qquad ((x{=}r \lor 0{=}r) \Rightarrow 1{=}1 \mid \mathsf{W}\,y\,1)^{e} \end{array}$$

4.6 Control Dependencies

In $\mathit{IF}(\phi, \mathcal{P}_1, \mathcal{P}_2)$, the predicate transformer (I4) is $(\phi \land \tau_1^D(\psi)) \lor (\neg\phi \land \tau_2^D(\psi))$, which is the disjunctive equivalent of Dijkstra's conjunctive formulation: $(\phi \Rightarrow \tau_1^D(\psi)) \land (\neg\phi \Rightarrow \tau_2^D(\psi))$.

This semantics validates dead code elimination: if $M{\neq}0$ is a tautology then $[\![\texttt{if}(M)\{S_1\}\,\texttt{else}\,\{S_2\}]\!] \supseteq [\![S_1]\!]$. The reverse inclusion does not hold.

For events from E_1, I3a requires $\phi \land \kappa_1(e)$. For events from E_2, I3b requires $\neg\phi \land \kappa_2(e)$. For coalescing events in $E_1 \cap E_2$, I3c requires $(\phi \land \kappa_1(e)) \lor (\neg\phi \land \kappa_2(e))$. This semantics allows common code to be lifted out of a conditional, validating the transformation $[\![\texttt{if}(M)\{S\}\,\texttt{else}\,\{S\}]\!] \supseteq [\![S]\!]$.

By allowing events to coalesce, I3c ensures that control dependencies are calculated semantically. For example, consider $P \in [\![\texttt{if}(r{=}1)\{y := r\}\,\texttt{else}\,\{y := 1\}]\!]$, which is build from $P_1 \in [\![y := r]\!]$ and $P_2 \in [\![y := 1]\!]$ such as:

$$y := r \qquad\qquad y := 1 \qquad\qquad \texttt{if}(r{=}1)\{y := r\}\,\texttt{else}\,\{y := 1\}$$

$$\boxed{r{=}1 \mid \mathsf{W}\,y\,1}^{e} \qquad \boxed{1{=}1 \mid \mathsf{W}\,y\,1}^{e} \qquad \boxed{(r{=}1 \Rightarrow r{=}1) \land (r{\neq}1 \Rightarrow 1{=}1) \mid \mathsf{W}\,y\,1}^{e}$$

Here, the precondition in the combined pomset is a tautology, independent of r.

Control dependencies are eliminated in the same way as data dependencies. For example:

$$r := x \qquad\qquad \texttt{if}(r{=}1)\{y := 1\}$$

$$\boxed{(x{=}r \lor v{=}r) \Rightarrow \psi}\; \boxed{\mathsf{R}\,x\,v}^{d} \dashrightarrow \boxed{v{=}r \Rightarrow \psi} \qquad \boxed{\tau_2^{\emptyset}(\psi)}\; \boxed{r{=}1 \mid \mathsf{W}\,y\,w}^{e} \dashrightarrow \boxed{\tau_2^{\{e\}}(\psi)}$$

where $\tau_2^{\emptyset}(\psi) \equiv \tau_2^{\{e\}}(\psi) \equiv (r{=}1 \land \psi[1/y]) \lor (r{\neq}1 \land \psi)$. As for (††), there are two possibilities:

$$r := x\,;\ \texttt{if}(r{=}1)\{y := 1\} \qquad\qquad r := x\,;\ \texttt{if}(r{=}1)\{y := 1\}$$

$$\boxed{\mathsf{R}\,x\,1}^{d} \rightarrow \boxed{1{=}r \Rightarrow r{=}1 \mid \mathsf{W}\,y\,1}^{e} \qquad\qquad \boxed{\mathsf{R}\,x\,1}^{d} \quad \boxed{(x{=}r \lor 1{=}r) \Rightarrow r{=}1 \mid \mathsf{W}\,y\,1}^{e}$$

4.7 A Refinement: No Dependencies into Reads

To avoid stalling the CPU pipeline unnecessarily, hardware does not enforce control dependencies between reads. To support if-closure (§9.5), software models must not distinguish control dependencies from other dependencies. Thus, we are forced to drop all dependencies into reads. To achieve this, we modify the definition of κ_2' in Fig. 1.

$$\kappa_2'(e) = \begin{cases} \tau_1(\kappa_2(e)) & \text{if } \lambda(e) \text{ is a read} \\ \tau_1^{\downarrow e}(\kappa_2(e)) & \text{otherwise, where } {\downarrow}e = \{c \mid c < e\} \end{cases}$$

Thus reads always use the "best" transformer, τ_1. In order for non-reads to get a good transformer, they need to add order.

Throughout the remainder of the paper, we use this definition. (The lack of dependencies into reads is one of the factors complicating downset closure; see §A.6 for a discussion.)

4.8 A Subtlety: Local Invariant Reasoning

Two aspects of Fig. 1 that are fairly obscure: First, R4b introduces locations into formula, in order to track the local state of memory. This is necessary to support local invariant reasoning as in JMM Causality Test Case 1 (TC1) [Pugh 2004]. Second, R3 introduces symbols Q_x to ensure that local state is tracked accurately. Consider TC1:

$$x := 0;\ (r := x\,;\ \texttt{if}(r{\geqslant}0)\{y := 1\} \parallel x := y)$$

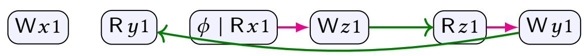
$$\boxed{\mathsf{W}\,x\,0} \quad \boxed{\mathsf{R}\,x\,1} \quad \boxed{\phi \mid \mathsf{W}\,y\,1} \rightarrow \boxed{\mathsf{R}\,y\,1} \rightarrow \boxed{\mathsf{W}\,x\,1} \tag{TC1}$$

In order to allow this execution, the precondition ϕ must be a tautology. Using R4b and W4a, the precondition is $((1{=}r \lor x{=}r) \Rightarrow r{\geqslant}0)[0/x]$ which is $((1{=}r \lor 0{=}r) \Rightarrow r{\geqslant}0)$ which is indeed a tautology.

Intuitively, R4b says that, to be independent of the read action, subsequent preconditions must be tautological under both $[v/r]$ and $[x/r]$. Here v is the value read, and x tracks the "local state" of the variable. This idea is borrowed from [Jagadeesan et al. 2020], which includes further examples. (See §4.9 for a discussion of Skolemization.) [Todo: Local invariant reasoning requires that we track the state of variables in the logic, not just registers. This is one reason we use predicate transformers rather than simple postconditions.]

To see that Q_x is necessary to constrain this use of local state, consider the following example from [Paviotti et al. 2020, §6.3]:

$$x:=1;\, r:=y;\, \mathtt{if}(r)\{s:=x;\, \mathtt{if}(s)\{z:=1\}\}\,\mathtt{else}\,\{x:=0;\, s:=x;\, \mathtt{if}(s)\{z:=1\}\} \parallel \mathtt{if}(z)\{y:=1\}$$



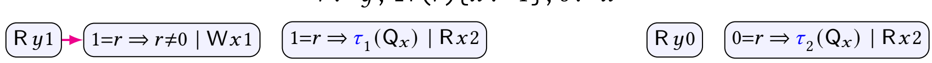
Note that the two branches of the conditional are the same after the first assignment in the else branch. Without Q_x, the precondition ϕ is tt, which is a tautology, and the execution is allowed, resulting in a violation of DRF-SC. To construct this pomset, we have chosen the empty pomset for $[\![x:=0]\!]$. The constraints on complete pomsets do not filter out this pomset, since $x:=0$ is in the false-branch of the conditional. The problem here is that we have forgotten the local state of x in the false-branch of the execution. Nonetheless, we are using the subsequent read.

With Q_x, the precondition of ϕ is ff. Intuitively, Q_x requires that the most recent prior write to x must be in the pomset in order to read x.

Q_x also guarantees initialization in complete pomsets: (C3) requires tautologies, which means that all variables must be initialized sequentially in order to get rid of Q_x.

The use of Q_x is not too restrictive. As a sanity check, consider the following pomsets,

$$r:=y;\, \mathtt{if}(r)\{x:=1\};\, s:=x$$



where $\tau_1(\psi) = (r{\neq}0 \wedge \psi[1/x][1{=}1/\mathsf{Q}_x]) \vee (r{=}0 \wedge \psi)$ and $\tau_2(\psi) = (r{\neq}0 \wedge \psi[1/x][\mathsf{ff}/\mathsf{Q}_x]) \vee (r{=}0 \wedge \psi)$ are the predicate transformers for the conditional writes, using W4a and W4b respectively. The executions are complete since all preconditions are tautologies.

4.9 Associativity and Skolemization

The predicate transformers we have chosen for R4a and R4b are different from the ones used traditionally, which are written using substitution. Attempting to write R4a and R4b in this style we would have (as in [Jagadeesan et al. 2020]):

(R4a′) if $E \neq \emptyset$ and $(E \cap D) \neq \emptyset$ then $\tau^D(\psi) \equiv \psi[v/r]$,

(R4b′) if $E \neq \emptyset$ and $(E \cap D) = \emptyset$ then $\tau^D(\psi) \equiv \psi[v/r] \wedge \psi[x/r]$.

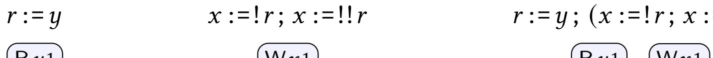
Sadly, this definition fails associativity.

Consider the following, eliding transformers for the writes ("!" represents logical negation):

$$r:=y \qquad\qquad x:=!r \qquad\qquad x:=!!r$$

Coalescing the writes and associating to the right, we have the following, since $(r{=}0 \vee r{\neq}0) \equiv \mathsf{tt}$:

$$r:=y \qquad\qquad x:=!r;\, x:=!!r \qquad\qquad r:=y;\, (x:=!r;\, x:=!!r)$$



The precondition of $(\mathsf{W}x1)$ is a tautology. Associating to the left and the coalescing, instead:

$$r := y\,;\, x := !r \qquad\qquad x := !!r \qquad\qquad (r := y\,;\, x := !r)\,;\, x := !!r$$

$$\boxed{\mathsf{R}\,y1} \;\; \boxed{1{=}0 \land y{=}0 \mid \mathsf{W}x1} \qquad\qquad \boxed{r{\neq}0 \mid \mathsf{W}x1} \qquad\qquad \boxed{\mathsf{R}\,y1} \;\; \boxed{\phi \mid \mathsf{W}x1}$$

The precondition $\phi \equiv (1{=}0 \land y{=}0) \lor (1{\neq}0 \land y{\neq}0)$, which is equivalent to $y{\neq}0$, which is not a tautology. This pomset can never be complete due to the bogus write of $(x := !r)$, which will show up in the termination condition $(1{=}0)$. Nevertheless, this is a problem, since associativity must hold for incomplete pomsets.

Our solution is to Skolemize, replacing substitution by implication, with uniquely chosen registers. Using Fig. 1, we compute a tautology in the example above: $\phi \equiv ((y{=}r \lor 1{=}r) \Rightarrow r{=}0) \lor (r{\neq}0)$.

The proof of associativity requires that predicate transformers distribute through disjunction (Def. 4.2). The attempt to define predicate transformers using substitution fails for R4c because the predicate transformer $\tau(\psi) = (\forall r)\psi$ does not distribute through disjunction: $\tau(\psi_1 \lor \psi_2) = (\forall r)(\psi_1 \lor \psi_2) \neq ((\forall r)(\psi_1)) \lor ((\forall r)(\psi_2)) = \tau(\psi_1) \lor \tau(\psi_2)$. Since $\tau(\psi) = (\forall r)\psi$ does not distribute through disjunction, we use $\tau(\psi) = \psi$ instead (which trivially distributes through disjunction). This change means we cannot use substitution, since ψ does not imply $\psi[v/r]$. Fortunately, Skolemizing solves this problem, since ψ implies $(r{=}v) \Rightarrow \psi$.

5 PwT-MCA: POMSETS WITH PREDICATE TRANSFORMERS FOR MCA

We derive a model of concurrent computation by adding *parallel composition* and *reads-from* to Fig. 1. To model coherence and synchronization, we add *delay* to the rule for sequential composition. For MCA architectures, it is sufficient to encode delay in the pomset order. The resulting model, PwT-MCA$_1$, supports optimal lowering for relaxed access on Arm8, but requires extra synchronization for acquiring reads.

A variant, PwT-MCA$_2$, supports optimal lowering for all access modes on Arm8. To achieve this, PwT-MCA$_2$ drops the global requirement that *reads-from* implies pomset order (M7c). The models are the same, except for *internal reads*, where a thread reads its own write.

The lowering proofs can be found in §B. The proofs use recent alternative characterizations of Arm8 [Alglave et al. 2021].

5.1 PwT-MCA1

We define PwT-MCA$_1$ by extending Def. 4.4 and Fig. 1. The definition uses several relations over actions—matches, blocks and delays—as well a distinguished set of read actions; see §4.2.

Definition 5.1. A PwT-MCA$_1$ is a PwT (Def. 4.4) equipped with a relation rf such that

- (M7) $\mathsf{rf} \subseteq E \times E$ is an injective relation capturing *reads-from*, such that
  - (M7a) if $d \xrightarrow{\mathsf{rf}} e$ then $\lambda(d)$ matches $\lambda(e)$,
  - (M7b) if $d \xrightarrow{\mathsf{rf}} e$ and $\lambda(c)$ blocks $\lambda(e)$ then either $c \leq d$ or $e \leq c$,
  - (M7c) if $d \xrightarrow{\mathsf{rf}} e$ then $d < e$.

A PwT-MCA is *complete* if

- (C3) (C5) as in Def. 4.4,
- (C7) if $\lambda(e)$ is a read then there is some $d \xrightarrow{\mathsf{rf}} e$.

If $P \in \mathit{PAR}(\mathcal{P}_1, \mathcal{P}_2)$ then $(\exists P_1 \in \mathcal{P}_1)\ (\exists P_2 \in \mathcal{P}_2)$

- (P1) $E = (E_1 \uplus E_2)$,
- (P2) $\lambda = (\lambda_1 \cup \lambda_2)$,
- (P3a) if $e \in E_1$ then $\kappa(e) \equiv \kappa_1(e)$,
- (P3b) if $e \in E_2$ then $\kappa(e) \equiv \kappa_2(e)$,
- (P4) $\tau^D(\psi) \equiv \tau_2^D(\psi)$,
- (P5) $\checkmark \equiv \checkmark_1 \land \checkmark_2$,
- (P6) $< \supseteq (<_1 \cup <_2)$,
- (P7) $\mathsf{rf} \supseteq (\mathsf{rf}_1 \cup \mathsf{rf}_2)$.

If $P \in \mathit{SEQ}(\mathcal{P}_1, \mathcal{P}_2)$ then $(\exists P_1 \in \mathcal{P}_1)\ (\exists P_2 \in \mathcal{P}_2)$

(s1) (s2) (s3) (s4) (s5) (s6) as in Fig. 1, (s7) $\mathsf{rf} \supseteq (\mathsf{rf}_1 \cup \mathsf{rf}_2)$.
(s6a) if $\lambda_1(d)$ delays $\lambda_2(e)$ then $d \leq e$,

If $P \in \mathit{IF}(\phi, \mathcal{P}_1, \mathcal{P}_2)$ then $(\exists P_1 \in \mathcal{P}_1)\ (\exists P_2 \in \mathcal{P}_2)$
(I1) (I2) (I3) (I4) (I5) (I6) as in Fig. 1, (I7) $\mathsf{rf} \supseteq (\mathsf{rf}_1 \cup \mathsf{rf}_2)$.

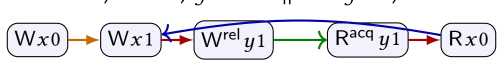
Let $[\![S_1 \mathbin{+\!\!\!\!\!\!\;\rightarrow} S_2]\!] = \mathit{PAR}([\![S_1]\!], [\![S_2]\!])$. We write $[\![\cdot]\!]_{\mathsf{mca1}}$ for the semantic function when it is unclear from context.

In complete pomsets, rf must pair every read with a matching write (C7). The requirements M7a, M7b, and M7c guarantee that reads are *fulfilled*, as in [Jagadeesan et al. 2020, §2.7].

The semantic rules are mostly straightforward: Parallel composition is disjoint union, and all constructs respect reads-from. The monoid laws (Lemma 4.5) extend to parallel composition, with `skip` as right unit only due to the asymmetry of P4.

Only s6a requires explanation. From Def. 4.1, recall that a *delays* b if $a \bowtie_{\mathsf{co}} b$ or $a \ltimes_{\mathsf{sync}} b$ or $a \bowtie_{\mathsf{sc}} b$. s6a guarantees that sequential order is enforced between conflicting accesses of the same location ($\bowtie_{\mathsf{co}}$), into a release and out of an acquire ($\ltimes_{\mathsf{sync}}$), and between SC accesses ($\bowtie_{\mathsf{sc}}$). Combined with the fulfillment requirements (M7a, M7b and M7c), these ensure coherence, publication, subscription and other idioms. For example, consider the following:[3]

$$x := 0;\ x := 1;\ y^{\mathsf{rel}} := 1 \parallel r := y^{\mathsf{acq}};\ s := x \qquad (\text{PUB})$$



The execution is disallowed due to the cycle. All of the order shown is required at top-level: The intra-thread order comes from s6a: $(\mathsf{W}x0) \rightarrow (\mathsf{W}x1)$ is required by $\bowtie_{\mathsf{co}}$. $(\mathsf{W}x1) \rightarrow (\mathsf{W}^{\mathsf{rel}}y1)$ and $(\mathsf{R}^{\mathsf{acq}}y1) \rightarrow (\mathsf{R}x0)$ are required by $\ltimes_{\mathsf{sync}}$. The cross-thread order is required by fulfillment: C7 requires that all top-level reads are in the image of $\xrightarrow{\mathsf{rf}}$. M7a ensures that $(\mathsf{W}^{\mathsf{rel}}y1) \xrightarrow{\mathsf{rf}} (\mathsf{R}^{\mathsf{acq}}y1)$, and M7c subsequently ensures that $(\mathsf{W}^{\mathsf{rel}}y1) < (\mathsf{R}^{\mathsf{acq}}y1)$. The *antidependency* $(\mathsf{R}x0) \rightarrow (\mathsf{W}x1)$ is required by M7b. (Alternatively, we could have $(\mathsf{W}x1) \rightarrow (\mathsf{W}x0)$, again resulting in a cycle.)

The semantics gives the expected results for store buffering and load buffering, as well as litmus tests involving fences and SC access. The model of coherence is weaker than C11, in order to support common subexpression elimination, and stronger than Java, in order to support local reasoning about data races. For further examples, see §D and [Jagadeesan et al. 2020, §3.1].

Lemmas 4.5 and 4.6 mostly hold for PwT-MCA$_1$. The exceptions are items (i) and (j), which become inclusions. For example, (i) becomes:

$$\texttt{if}(\phi)\{\mathcal{P}_1\}\,\texttt{else}\,\{\mathcal{P}_2\} \supseteq \texttt{if}(\phi)\{\mathcal{P}_1\};\ \texttt{if}(\neg\phi)\{\mathcal{P}_2\}$$

The culprit is delay, which introduces order regardless of whether preconditions are disjoint. As an example, $[\![\texttt{if}(r)\{x := 1\}\,\texttt{else}\,\{x := 2\}]\!]$ has an execution with $(r{=}0 \mid \mathsf{W}x2) \rightarrow (r{\neq}0 \mid \mathsf{W}x1)$, (using augmentation), whereas $[\![\texttt{if}(r)\{x := 1\};\ \texttt{if}(!r)\{x := 2\}\}]\!]$ has no such execution.

For further discussion, see §A.7.

[3]We use different colors for arrows representing order:

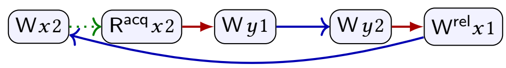
- $d \rightarrow e$ arises from $\bowtie_{\mathsf{co}}$ (s6a),
- $d \rightarrow e$ arises from $\ltimes_{\mathsf{sync}}$ or $\bowtie_{\mathsf{sc}}$ (s6a),
- $d \rightarrow e$ arises from control/data/address *dependency* (s3, definition of $\kappa'_2(d)$),
- $d \rightarrow e$ arises from *reads-from* (M7a),
- $d \rightarrow e$ arises from *blocking* (M7b).

In PwT-MCA$_2$, it is possible for rf to contradict $<$. In this case, we use a dotted arrow for rf: $d \dashrightarrow e$ indicates that $e < d$.

5.2 PwT-MCA2

Lowering PwT-MCA1 to Arm8 requires a full fence after every acquiring read. To see why, consider the following attempted execution, where the final values of both x and y are 2.

$$x := 2;\ r := x^{\mathsf{acq}};\ y := r{-}1 \parallel y := 2;\ x^{\mathsf{rel}} := 1$$



The execution is allowed by Arm8, but disallowed by PwT-MCA$_1$, due to the cycle.

Arm8 allows the execution because the read of x is internal to the thread. This aspect of Arm8 semantics is difficult to model locally. To capture this, we found it necessary to drop M7c and relax s6a, adding local constraints on rf to *PAR*, *SEQ* and *IF*. Rather than ensuring that there is no *global* blocker for a sequentially fulfilled read (M7c), we require only that there is no *thread-local* blocker (s6b). For PwT-MCA$_2$, internal reads don't necessarily contribute to order, and thus the above execution is allowed.

Definition 5.2. A PwT-MCA$_2$ is a PwT (Def. 4.4) equipped with an injective relation rf that satisfies requirements M7a and M7b of Def. 5.1.

A PwT-MCA$_2$ is *complete* if it satisfies C3, C5, and C7—this is the same as for PwT-MCA$_1$.

If $P \in PAR(\mathcal{P}_1, \mathcal{P}_2)$ then $(\exists P_1 \in \mathcal{P}_1)\ (\exists P_2 \in \mathcal{P}_2)$

(P1) (P2) (P3) (P4) (P5) (P6) (P7) as in Def. 5.1,

(P6a) if $d \in E_1$, $e \in E_2$ and $d \xrightarrow{\mathsf{rf}} e$ then $d < e$,

(P6b) if $d \in E_1$, $e \in E_2$ and $e \xrightarrow{\mathsf{rf}} d$ then $e < d$,

(P7a) $\mathsf{rf}_i = \mathsf{rf} \cap (E_i \times E_i)$, for $i \in \{1, 2\}$.

If $P \in SEQ(\mathcal{P}_1, \mathcal{P}_2)$ then $(\exists P_1 \in \mathcal{P}_1)\ (\exists P_2 \in \mathcal{P}_2)$

(S1) (S2) (S3) (S4) (S5) (S6) (S7) as in Def. 5.1,

(S6a) if $\lambda_1(d)$ delays $\lambda_2(e)$ then either $d \xrightarrow{\mathsf{rf}} e$ or $d \leq e$,

(S6b) if $\lambda_1(c)$ blocks $\lambda_2(e)$ and $d \xrightarrow{\mathsf{rf}} e$ then $c \leq d$,

(S7a) $\mathsf{rf}_i = \mathsf{rf} \cap (E_i \times E_i)$, for $i \in \{1, 2\}$.

If $P \in IF(\phi, \mathcal{P}_1, \mathcal{P}_2)$ then $(\exists P_1 \in \mathcal{P}_1)\ (\exists P_2 \in \mathcal{P}_2)$

(I1) (I2) (I3) (I4) (I5) (I6) (I7) as in Def. 5.1,

(I7a) $\mathsf{rf}_i = \mathsf{rf} \cap (E_i \times E_i)$, for $i \in \{1, 2\}$.

A PwT-MCA$_2$ need not satisfy requirement M7c, and thus we may have $d \xrightarrow{\mathsf{rf}} e$ and $e < d$.

[Todo: Example using s6a and s6b. To make space, Lemma 5.3 could move to appendix.]

With the weakening of s6a, we must be careful not to allow spurious pairs to be added to the rf relation. Thus we add P7a, S7a, and I7a. For example, I7a ensure that $[\![\texttt{if}(b)\{r := x \parallel x := 1\}\texttt{else}\ \{r := x;\ x := 1\}]\!]$ does not include $(\mathsf{R}\,x\,1) \rightarrow (\mathsf{W}\,x\,1)$, taking rf from the left and $<$ from the right.

As a consequence of dropping M7c, sequential rf must be validated during pomset construction, rather than post-hoc. In §7, we show how to construct program order (po) for complete pomsets using phantom events (π). Using this construction, the following lemma gives a post-hoc verification technique for rf.

Lemma 5.3. *If $P \in [\![S]\!]_{\mathsf{mca2}}$ is complete, then for every $d \xrightarrow{\mathsf{rf}} e$ either*

- *external fulfillment: $d < e$ and if $\lambda(c)$ blocks $\lambda(e)$ then either $c \leq d$ or $e \leq c$, or*
- *internal fulfillment: $(\exists d' \in \pi^{-1}(d))\ (\exists e' \in \pi^{-1}(e))\ d' \xrightarrow{\mathsf{po}} e'$ and $(\nexists c')\ \kappa(c)$ is a tautology and $\lambda(c)$ blocks $\lambda(e)$ and $d' \xrightarrow{\mathsf{po}} c \xrightarrow{\mathsf{po}} e'$.*

These mimic the *external consistency* requirements of Arm8 [Alglave et al. 2021].

6 PwT-MCA RESULTS

PwP [Jagadeesan et al. 2020] is a novel memory model, intended to serve as a semantic basis for a Java-like language, where all access is safe. PwT-MCA generalizes PwP, making several small but significant changes. As a result, we have had to re-prove most of the theorems from PwP.

In §B, we show that PwT-MCA$_1$ supports the optimal lowering of relaxed accesses to Arm8 and that PwT-MCA$_2$ supports the optimal lowering of *all* accesses to Arm8. The proofs are based on two recent characterizations of Arm8 [Alglave et al. 2021]. For PwT-MCA$_1$, we use *External Global Consistency*. For PwT-MCA$_2$, we use *External Consistency*.

In §C, we prove sequential consistency for local-data-race-free programs. The proof uses *program order*, which we construct for C11 in §7. The same construction works for PwT-MCA. (This proof assumes there are no RMW operations.)

The semantics validates many peephole optimizations, such as the standard reorderings on relaxed access:

$$\llbracket r := x\,;\, s := y \rrbracket = \llbracket s := y\,;\, r := x \rrbracket \qquad \text{if } r \neq s$$
$$\llbracket x := M;\, y := N \rrbracket = \llbracket y := N;\, x := M \rrbracket \qquad \text{if } x \neq y$$
$$\llbracket x := M;\, s := y \rrbracket = \llbracket s := y\,;\, x := M \rrbracket \qquad \text{if } x \neq y \text{ and } s \notin \mathsf{id}(M)$$

Here $\mathsf{id}(S)$ is the set of locations and registers that occur in S. Using augmentation closure, the semantics also validates roach-motel reorderings [Sevčík 2008]. For example, on read/write pairs:

$$\llbracket x^{\mu} := M;\, s := y \rrbracket \supseteq \llbracket s := y\,;\, x^{\mu} := M \rrbracket \qquad \text{if } x \neq y \text{ and } s \notin \mathsf{id}(M)$$
$$\llbracket x := M;\, s := y^{\mu} \rrbracket \supseteq \llbracket s := y^{\mu}\,;\, x := M \rrbracket \qquad \text{if } x \neq y \text{ and } s \notin \mathsf{id}(M)$$

Notably, the semantics does *not* validate read introduction. When combined with case analysis (§9.5), read introduction can break temporal reasoning. This combination is allowed by speculative operational models. See §A.1 for a discussion.

Prop. 6.1 of [Jagadeesan et al. 2020] establishes a compositional principle for proving that programs validate formula in past-time temporal logic. The principal is based entirely on the pomset order relation. It's proof, and all of the no-thin-air examples in [Jagadeesan et al. 2020, §6] hold equally for the models described here.

7 PWT-C11: POMSETS WITH PREDICATE TRANSFORMERS FOR C11

PwT can be used to generate semantic dependencies to prohibit thin-air executions of C11, while preserving optimal lowering for relaxed access. We follow the approach of Paviotti et al. [2020], using our semantics to generate C11 candidate executions with a dependency relation, then applying the rules of RC11 [Lahav et al. 2017]. The No-Thin-Air axiom of RC11 is overly restrictive, requiring that $\mathsf{rf} \cup \mathsf{po}$ be acyclic. Instead, we require that $\mathsf{rf} \cup <$ is acyclic. This is a more precise categorisation of thin-air behavior, and it allows aggressive compiler optimizations that would be erroneously forbidden by RC11's original No-Thin-Air axiom.

The chief difficulty is instrumenting our semantics to generate program order, for use in the various axioms of C11.

Definition 7.1. A PwT-PO is a PwT (Def. 4.4) equipped with relations π and po such that

(M8) $\pi : (E \longrightarrow E)$ is an idempotent function capturing *merging*, such that
let $R = \{e \mid \pi(e){=}e\}$ be *real* events, let $\overline{R} = (E \setminus R)$ be *phantom* events,
let $S = \{e \mid \forall d.\ \pi(d){=}e \Rightarrow d{=}e\}$ be *simple* events, let $\overline{S} = (E \setminus S)$ be *compound* events,
(M8a) $\lambda(e) = \lambda(\pi(e))$, (M8b) if $e \in \overline{S}$ then $\kappa(e) \vDash \bigvee_{\{c \in \overline{R} \mid \pi(c)=e\}} \kappa(c)$.

(M9) $\mathsf{po} \subseteq (S \times S)$ is a partial order capturing *program order*.

A PwT-PO is *complete* if

(c3) if $e \in R$ then $\kappa(e)$ is a tautology, (c5) $\checkmark$ is a tautology.

Since π is idempotent, we have $\pi(\pi(e)) = \pi(e)$. Equivalently, we could require $\pi(e) \in R$.

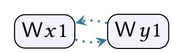
We use π to partition events E in two ways: we distinguish *real* events R from *phantom* events $\overline{R}$; we distinguish *simple* events S from *compound* events $\overline{S}$. From idempotency, it follows that all phantom events are simple ($\overline{R} \subseteq S$) and all compound events are real ($\overline{S} \subseteq R$). In addition, all phantom events map to compound events (if $e \in \overline{R}$ then $\pi(e) \in \overline{S}$).

Lemma 7.2. *If P is a* PwT *then there is a* PwT-po *P'' that conservatively extends it.*

Proof. The proof strategy is as follows: We extend the semantics of Fig. 1 with po. The obvious definition gives us a preorder rather than a partial order. To get a partial order, we replay the semantics without merging to get an *unmerged* pomset P'; the construction also produces the map π. We then construct P'' as the union of P and P', using the dependency relation from P.

We extend the semantics with po as follows. For pomsets with at most one event, po is the identity. For sequential composition, $\text{po} = \text{po}_1 \cup \text{po}_2 \cup E_1 \times E_2$. For the conditional, $\text{po} = \text{po}_1 \cup \text{po}_2$. By construction, po is a pre-order, which may include cycles due to coalescing. For example:

$\texttt{if}(r)\{x := 1;\ y := 1\}\texttt{else}\{y := 1;\ x := 1\}$



To find an acyclic po', we replay the construction of P to get P'. When building P', we require disjoint union in s1 and i1: $E' = E_1' \uplus E_2'$. If and event is unmerged in P (*i.e.* $e \in E_1 \uplus E_2$) then we choose the same event name for E' in P'. If an event is merged in P (*i.e.* $e \in E_1 \cap E_2$) then we choose fresh event names—e_1' and e_2'—and extend π accordingly: $\pi(e_1') = \pi(e_2') = e$. In P', we take $\leq' = \text{po}'$.

To arrive at P'', we take (1) $E'' = E \cup E'$, (2) $\lambda'' = \lambda \cup \lambda'$, (3a) if $e \in E$ then $\kappa''(e) = \kappa(e)$, (3b) if $e \in E' \setminus E$ then $\kappa''(e) = \kappa'(e)$, (4) $\tau''^{D} = \tau^{(\pi^{-1}(D))}$, (5) $\checkmark'' = \checkmark$, (6) $d <'' e$ exactly when $\pi(d) < \pi(e)$, (7) $\text{po}'' = \text{po}'$, and (8) π'' is the constructed merge function. □

Definition 7.3. For a PwT-po, let $\text{extract}(P)$ be the projection of P onto the set $\{e \in E_1 \mid e \text{ is simple and } \kappa_1(e) \text{ is a tautology}\}$.

By definition, $\text{extract}(P)$ includes the simple events of P whose preconditions are tautologies. These are already in program order, as per item 7 of the proof. The dependency order is derived from the real events using π, as per item 6.

The following lemma shows that if P is *complete*, then $\text{extract}(P)$ includes at least one simple event for every compound event in P.

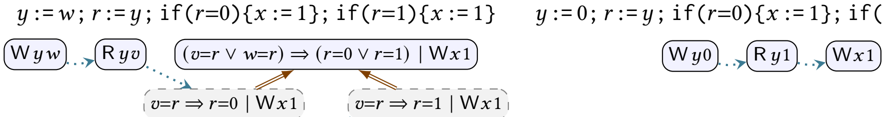
Lemma 7.4. *If P is a complete* PwT-po *with compound event e, then there is a phantom event $c \in \pi^{-1}(e)$ such that $\kappa(c)$ is a tautology.*

Proof. Immediate from m8b. □

A pomset in the image of extract is a *candidate execution.*

As an example, consider Java Causality Test Case 6. Taking $w = 0$ and $v = 1$, the PwT-po on the left below produces the candidate execution on the right. In diagrams, we visualize po using a dotted arrow ⇢, and π using a double arrow ⟹.

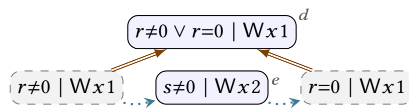
$y := w;\ r := y;\ \texttt{if}(r{=}0)\{x := 1\};\ \texttt{if}(r{=}1)\{x := 1\}$ $y := 0;\ r := y;\ \texttt{if}(r{=}0)\{x := 1\};\ \texttt{if}(r{=}1)\{x := 1\}$



We write $[\![\cdot]\!]^{\mathsf{po}}$ for the semantic function defined by applying the construction of Lemma 7.2 to the base semantics of 1.

The dependency calculation of $[\![\cdot]\!]^{\mathsf{po}}$ is sufficient for c11; however, it ignores synchronization and coherence completely.

$$\texttt{if}(r)\{x := 1\};\ \texttt{if}(s)\{x := 2\};\ \texttt{if}(!r)\{x := 1\}$$



(‡)

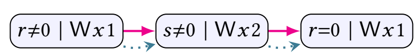
Adding a pair of reads to complete the pomset, we can extract the following candidate execution.

$$r := y;\ s := z;\ \texttt{if}(r)\{x := 1\};\ \texttt{if}(s)\{x := 2\};\ \texttt{if}(!r)\{x := 1\}$$

It is somewhat surprising that the writes are independent of both reads!

In PwT-mca, delay stops the merge in (‡).

$$\texttt{if}(r)\{x := 1\};\ \texttt{if}(s)\{x := 2\};\ \texttt{if}(!r)\{x := 1\}$$



It is possible to mimic this in c11, without introducing extra dependencies: one can filter executions post-hoc using the relation $\sqsubseteq$, defined as follows:

$$\pi(d) \sqsubseteq \pi(e) \text{ if } d \xrightarrow{\mathsf{po}} e \text{ and } \lambda(d) \text{ delays } \lambda(e).$$

In (‡), we have both $d \sqsubseteq e$ and $e \sqsubseteq d$. To rule out this execution, it suffices to require that $\sqsubseteq$ is a partial order.

Program (‡) shows that the definition of semantic dependency is up for debate in c11, and the International Standard Organisation's C++ concurrency subgroup acknowledges that semantic dependency (sdep) would address the Out-of-Thin-Air problem: *Prohibiting executions that have cycles in* rf ∪ sdep *can therefore be expected to prohibit Out-of-Thin-Air behaviors* [McKenney et al. 2016]. PwT-c11 resolves program structure into a dependency relation—not a complex state—that is precise and easily adjusted. As refinements are made to c11, PwT-c11 can accommodate these and test them automatically.

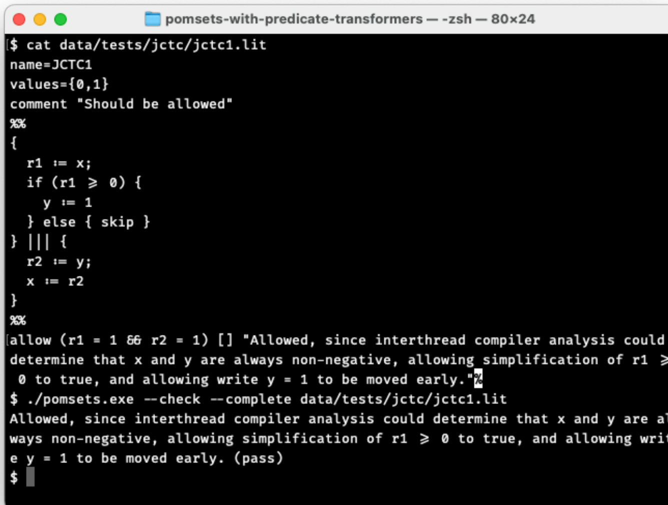
8 PwTer: AUTOMATIC LITMUS TEST EVALUATOR

PwTer automatically and exhaustively calculates the allowed outcomes of litmus tests for the PwT, PwT-po, and PwT-c11 models. It is built in OCaml, and uses Z3 [De Moura and Bjørner 2008] to judge the truth of predicates constructed by the models. PwTer obviates the need for error-prone hand evaluation.

PwTer allows several modes of evaluation: it can evaluate the rules of Fig. 1, implementing PwT; it can generate program order according to §7, implementing PwT-po; and similar to mrd-c11 [Paviotti et al. 2020], it can construct C11-style pre-executions and filter them according to the rules of rc11 as described in §7. Finally, PwTer also allows us to toggle the complete check of 4.4, providing an interface for understanding how fragments of code might compose by exposing preconditions and termination conditions that are not yet tautologies. We show PwTer in action in Fig. 2. PwTer will be made open source upon publication.

9 REFINEMENTS AND ADDITIONAL FEATURES

In the paper so far, we have assumed that registers are assigned at most once. We have done this primarily for readability. In the first subsection below, we drop this assumption, instead using



```
pomsets-with-predicate-transformers — -zsh — 80×24
$ cat data/tests/jctc/jctc1.lit
name=JCTC1
values={0,1}
comment "Should be allowed"
%%
{
  r1 := x;
  if (r1 ≥ 0) {
    y := 1
  } else { skip }
} ||| {
  r2 := y;
  x := r2
}
%%
allow (r1 = 1 && r2 = 1) [] "Allowed, since interthread compiler analysis could
determine that x and y are always non-negative, allowing simplification of r1 ≥
 0 to true, and allowing write y = 1 to be moved early."%
$ ./pomsets.exe --check --complete data/tests/jctc/jctc1.lit
Allowed, since interthread compiler analysis could determine that x and y are al
ways non-negative, allowing simplification of r1 ≥ 0 to true, and allowing writ
e y = 1 to be moved early. (pass)
$
```

Fig. 2. Example output of PwTer, validating TC1 [Pugh 2004].

substitution to rename registers. We use the set $\mathcal{S}_{\mathcal{E}} = \{s_e \mid e \in \mathcal{E}\}$. By assumption (§4.1), these registers do not appear in programs: $S[N/s_e] = S$. The resulting semantics satisfies redundant read elimination.

Our approach to register recycling allows us to define a criterion for eliminating certain types of useless pomsets (§9.2).

In the remainder of this section we consider several mostly-orthogonal features: address calculation, if-closure, fences, and read-modify-write operations. Address calculation and if-closure do have some interaction, and we spell out the combined semantics in §A.4.

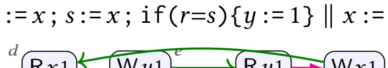
It is worth pointing out that address calculation and if-closure only affect the semantics of read and write. Fences introduce new trivial actions. RMWs require more infrastructure in order to ensure atomicity while compiling to Arm8 using load-exclusive and store-exclusive.

These extensions preserve all of the program transformation discussed thus far, and apply equally to the various semantics we have discussed: PwT, PwT-MCA$_1$, PwT-MCA$_2$, and PwT-C11. The results discussed in §6 also apply equally, with the exception of RMWs: we have not proven DRF-SC or Arm8 lowering for RMWs.

9.1 Register Recycling and Redundant Read Elimination

JMM Test Case 2 [Pugh 2004] states the following execution should be allowed "since redundant read elimination could result in simplification of $r{=}s$ to true, allowing $y := 1$ to be moved early."

$$r := x\,;\ s := x\,;\ \mathtt{if}(r{=}s)\{y := 1\} \parallel x := y \tag{TC2}$$



Under the semantics of Fig. 1, the precondition of e in the independent case is

$$(1{=}r \lor x{=}r) \Rightarrow (1{=}s \lor r{=}s) \Rightarrow (r{=}s), \tag{$*$}$$

which is equivalent to $(x{=}r) \Rightarrow (1{=}s) \Rightarrow (r{=}s)$, which is not a tautology, and thus Fig. 1 requires order from d to e in order to complete the pomset.

This execution is allowed, however, if we rename registers using a map from event names to register names. By using this renaming, coalesced events must choose the same register name. In the above example, the precondition of e in the independent case becomes

$$(1{=}s_e \vee x{=}s_e) \Rightarrow (1{=}s_e \vee s_e{=}s_e) \Rightarrow (s_e{=}s_e), \tag{$**$}$$

which is a tautology. In $(**)$, the first read resolves the nondeterminism in both the first and the second read. Given the choice of event names, the outcome of the second read is predetermined! In $(*)$, the second read remains nondeterministic, even in the case that the events are destined to coalesce.

Definition 9.1. Let $[\![\cdot]\!]$ be defined as in Fig. 1, changing R4 of *READ*:

(R4a) if $e \in E \cap D$ then $\tau^D(\psi) \equiv v{=}s_e \Rightarrow \psi[s_e/r]$,
(R4b) if $e \in E \setminus D$ then $\tau^D(\psi) \equiv (v{=}s_e \vee x{=}s_e) \Rightarrow \psi[s_e/r]$,
(R4c) if $E = \emptyset$ then $(\forall s)\ \tau^D(\psi) \equiv \psi[s/r]$.

With this semantics, it is straightforward to see that redundant load elimination is sound:

$$[\![r := x^\mu ;\ s := x^\mu]\!] \supseteq [\![r := x^\mu ;\ s := r]\!]$$

As a further example, consider [Sevčík and Aspinall 2008, Fig. 5], referenced in [Paviotti et al. 2020, §6.4]. Consider the case where the reads are merged, both seeing 1:

$$r := y ;\ \texttt{if}(r{=}1)\{s := y ;\ x := s\}\,\texttt{else}\,\{x := 1\} \qquad \boxed{\mathsf{R}\,y1} \quad \boxed{\phi \mid \mathsf{W}x1}$$

In order to independent of both reads, we take the precondition ϕ to be:

$$(1{=}r \vee y{=}r) \Rightarrow [r{=}1 \wedge \big((1{=}s \vee y{=}s) \Rightarrow s{=}1\big)] \vee [r{\neq}1]$$

Then collapsing r and s and substituting the initial value of y (say 0), we have a tautology:

$$(1{=}r \vee 0{=}r) \Rightarrow [r{=}1 \wedge \big((1{=}r \vee 0{=}r) \Rightarrow r{=}1\big)] \vee [r{\neq}1]$$

9.2 Register Consistency

If a precondition is false, you can be pretty sure it's useless. In this subsection, we develop a criterion for eliminating such useless pomsets.

To achieve this, we would like to bolt a requirement into the definition of pomsets in order to weed out the useless ones. Something like this:

(M3a′) $\kappa(e)$ is satisfiable.

For associativity, (M3a′) would in turn require

(X4′) $\tau(\mathsf{ff}) \equiv \mathsf{ff}$.

Dijkstra [1975] requires exactly X4′. Problem solved! Unfortunately, our transformer for read actions (R4a) does not obey X4′, since ff is not equivalent to $v{=}r \Rightarrow \mathsf{ff}$.

In this subsection, we refine these requirements into ones that do hold. The main insight is to pull values for registers from the labels of pomset itself. Thus, we define θ_λ to capture the *register state* of a pomset.

Definition 9.2. Let $\theta_\lambda = \bigwedge_{\{(e,v)\in(E\times\mathcal{V}) \mid \lambda(e)=(\mathsf{R}\,v)\}}(s_e{=}v)$ where $E = \mathsf{dom}(\lambda)$.
We say that ϕ is *λ-consistent* if $\phi \wedge \theta_\lambda$ is satisfiable. We say that it is *λ-inconsistent* otherwise.

Using this, we define the constraint on predicate transformers that we want. We also need to update the definition of predicate transformer families to carry the labeling.

Definition 9.3. A λ*-predicate transformer* is a function $\tau : \Phi \to \Phi$ such that

(x3) (x1) (x2) as in Def. 4.2,

(x4) if ψ is λ-inconsistent then $\tau(\psi)$ is λ-inconsistent.

A *family of* λ*-predicate transformers* over consists of a λ-predicate transformer τ^D for each $D \subseteq \mathcal{E}$, such that if $C \cap E \subseteq D$ then $\tau^C(\psi) \vDash \tau^D(\psi)$.

(M4) $\tau : 2^{\mathcal{E}} \to \Phi \to \Phi$ is a *family of* λ*-predicate transformers*,

Given these definitions, we can add the following requirement to the model, which enables us to prune pomsets that include λ-inconsistent preconditions and termination conditions.

(M3a) $\kappa(e)$ is λ-consistent, (M5b) $\checkmark$ is λ-consistent.

With this modification, dead-code elimination (Lemma 4.6h) can be changed from an inclusion to an equation:

$$\texttt{if}(\phi)\{\mathcal{P}_1\}\,\texttt{else}\,\{\mathcal{P}_2\} = \mathcal{P}_1 \text{ if } \phi \text{ is a tautology.}$$

9.3 Address Calculation

Inevitably, address calculation complicates the definitions of *WRITE* and *READ*.

Definition 9.4. If $P \in \mathit{WRITE}(L, M, \mu)$ then $(\exists \ell \in \mathcal{V})\ (\exists v \in \mathcal{V})$

(w1) if $|E| \leqslant 1$,

(w2) $\lambda(e) = \mathsf{W}^{\mu}[\ell]v$,

(w3) $\kappa(e) \equiv L{=}\ell \wedge M{=}v$,

(w4a) if $E \neq \emptyset$ then $\tau^D(\psi) \equiv (L{=}\ell) \Rightarrow \psi[M/[\ell]][M{=}v/\mathsf{Q}_{[\ell]}]$,

(w4b) if $E = \emptyset$ then $(\forall k)\ \tau^D(\psi) \equiv (L{=}k) \Rightarrow \psi[M/[k]][\mathsf{ff}/\mathsf{Q}_{[k]}]$,

(w5a) if $E \neq \emptyset$ then $\checkmark \equiv L{=}\ell \wedge M{=}v$,

(w5b) if $E = \emptyset$ then $\checkmark \equiv \mathsf{ff}$.

If $P \in \mathit{READ}(r, L, \mu)$ then $(\exists \ell \in \mathcal{V})\ (\exists v \in \mathcal{V})$

(R1) if $|E| \leqslant 1$,

(R2) $\lambda(e) = \mathsf{R}^{\mu}[\ell]v$

(R3) $\kappa(e) \equiv L{=}\ell \wedge \mathsf{Q}_{[\ell]}$,

(R4a) if $e \in E \cap D$ then $\tau^D(\psi) \equiv (L{=}\ell \Rightarrow v{=}s_e) \Rightarrow \psi[s_e/r]$,

(R4b) if $e \in E \setminus D$ then $\tau^D(\psi) \equiv ((L{=}\ell \Rightarrow v{=}s_e) \vee (L{=}\ell \Rightarrow [\ell]{=}s_e)) \Rightarrow \psi[s_e/r]$,

(R4c) if $E = \emptyset$ then $(\forall s)\ \tau^D(\psi) \equiv \psi[s/r]$,

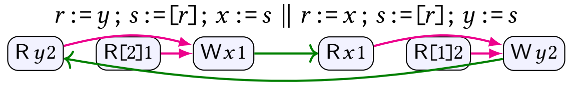
(R5a) if $E \neq \emptyset$ or $\mu \sqsubseteq \mathsf{rlx}$ then $\checkmark \equiv \mathsf{tt}$.

(R5b) if $E = \emptyset$ and $\mu \sqsupseteq \mathsf{acq}$ then $\checkmark \equiv \mathsf{ff}$.

[Todo: Perhaps move this to §D and put TC12 here.]

The combination of read-read independency (§4.7) and address calculation is somewhat delicate. Consider the following program, from [Jagadeesan et al. 2020, §5], where initially $x = 0$, $y = 0$, $[0] = 0, [1] = 2$, and $[2] = 1$. It should only be possible to read 0, disallowing the attempted execution below:

$$r := y\,;\ s := [r]\,;\ x := s \parallel r := x\,;\ s := [r]\,;\ y := s$$



This execution would become possible, however, if we were to replace $(L{=}\ell \Rightarrow v{=}s_e)$ by $(v{=}s_e)$ in R4a. In this case, $(\mathsf{R}\,y2)$ would not necessarily be dependency ordered before $(\mathsf{W}\,x1)$.

9.4 Fences and Read-Modify-Write Operations

The semantics of fences is straightforward. Let $[\![\mathsf{F}^{\mu}]\!] = \mathit{FENCE}(\mu)$, where if $P \in \mathit{FENCE}(\mu)$ then

(F1) $|E| \leqslant 1$,

(F2) $\lambda(e) = \mathsf{F}^{\mu}$,

(F3) $\kappa(e) \equiv \mathsf{tt}$,

(F4) $\tau^D(\psi) \equiv \psi$,

(F5a) if $E \neq \emptyset$ then $\checkmark \equiv \mathsf{tt}$,

(F5b) if $E = \emptyset$ then $\checkmark \equiv \mathsf{ff}$.

This semantics is identical to that of [Jagadeesan et al. 2020]; see there for examples.

RMW operations are more complex. To support RMWs, we add a relation $\xrightarrow{\mathsf{rmw}} \subseteq E \times E$ that relates the read of a successful RMW to the succeeding write.

Definition 9.5. Extend the definition of a pomset as follows.

(M10) rmw : $E \rightarrow E$ is a partial function capturing read-modify-write *atomicity*, such that
- (M10a) if $d \xrightarrow{\text{rmw}} e$ then $\lambda(e)$ blocks $\lambda(d)$,
- (M10b) if $d \xrightarrow{\text{rmw}} e$ then $d < e$,
- (M10c) if $\lambda(c)$ overlaps $\lambda(d)$ and $d \xrightarrow{\text{rmw}} e$ then $c < e$ implies $c \leq d$ and $d < c$ implies $e \leq c$.

Extend the definition of *SEQ*, *IF* and *PAR* to include:

(S10) (I10) (P10) rmw = (rmw$_1$ ∪ rmw$_2$),

To define specific operations, we extend the syntax:

$$S \ ::= \ \cdots \ | \ r := \mathsf{CAS}^{\mu,\nu}([\![L]\!], M, N) \ | \ r := \mathsf{FADD}^{\mu,\nu}([\![L]\!], M) \ | \ r := \mathsf{EXCHG}^{\mu,\nu}([\![L]\!], M)$$

We require that r does not occur in L. The corresponding semantic functions are as follows.

Definition 9.6. Let *READ′* be defined as for *READ*, adding the constraint:

(R4d) if $(E \cap D) = \emptyset$ then $\tau^D(\psi) \equiv \psi$.

If $P \in \mathit{FADD}(r, x, M, \mu, \nu)$ then $P \in \mathit{SEQ}(\mathit{READ}'(r, x, \mu), \mathit{WRITE}(x, r{+}M, \nu))$ and
If $P \in \mathit{EXCHG}(r, x, M, \mu, \nu)$ then $P \in \mathit{SEQ}(\mathit{READ}'(r, x, \mu), \mathit{WRITE}(x, M, \nu))$ and
If $P \in \mathit{CAS}(r, x, M, N, \mu, \nu)$ then
$P \in \mathit{SEQ}(\mathit{READ}'(r, x, \mu), \mathit{IF}(r{=}M, \mathit{WRITE}(x, N, \nu), \mathit{SKIP}))$ and

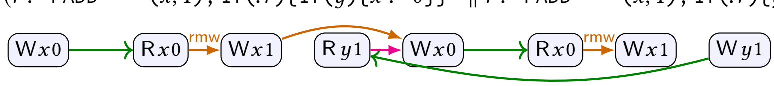
(U10) if $\lambda(e)$ is a write then there is a read $\lambda(d)$ such that $\kappa(e) \vDash \kappa(d)$ and $d \xrightarrow{\text{rmw}} e$.

$$[\![r := \mathsf{CAS}^{\mu,\nu}(x, M, N)]\!] = \mathit{CAS}(r, x, M, N, \mu, \nu)$$
$$[\![r := \mathsf{FADD}^{\mu,\nu}(x, M)]\!] = \mathit{FADD}(r, x, M, \mu, \nu)$$
$$[\![r := \mathsf{EXCHG}^{\mu,\nu}(x, M)]\!] = \mathit{EXCHG}(r, x, M, \mu, \nu)$$

This definition ensures atomicity and supports lowering to Arm load/store exclusive operations. See [Jagadeesan et al. 2020] for examples.

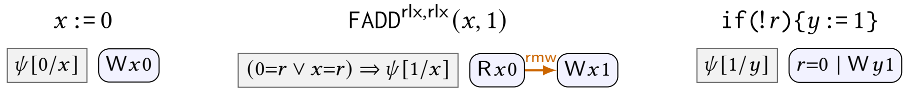
One subtlety of the definition is that we use *READ′* rather than *READ*. Thus, for RMW operations, the independent case for a read is the same as the empty case. To see why this should be, consider the relaxed variant of the CDRF example from [Lee et al. 2020], using *READ* rather than *READ′*.

$$x := 0;\ (r := \mathsf{FADD}^{\mathsf{rlx},\mathsf{rlx}}(x, 1);\ \mathtt{if}(!r)\{\mathtt{if}(y)\{x := 0\}\} \ \ \|\ r := \mathsf{FADD}^{\mathsf{rlx},\mathsf{rlx}}(x, 1);\ \mathtt{if}(!r)\{y := 1\})$$



A write should only be visible to one FADD instruction, but here the write of 0 is visible to two. This is allowed because no order is required from (Rx0) to (Wy1) in the last thread. To see why, consider the independent transformers of the last thread and initializer:

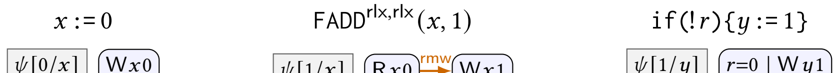
$x := 0$ $\qquad$ $\mathsf{FADD}^{\mathsf{rlx},\mathsf{rlx}}(x, 1)$ $\qquad$ $\mathtt{if}(!r)\{y := 1\}$



After sequencing, the precondition of (Wy1) is a tautology: $(0{=}r \vee 0{=}r) \Rightarrow r{=}0$.

By including R4d, *READ′* constrains the independent predicate transformer of the FADD:

$x := 0$ $\qquad$ $\mathsf{FADD}^{\mathsf{rlx},\mathsf{rlx}}(x, 1)$ $\qquad$ $\mathtt{if}(!r)\{y := 1\}$



After sequencing, the precondition of (Wy1) is $r{=}0$, which is *not* a tautology. This forces any top-level pomset to include dependency order from (Rx0) to (Wy1).

9.5 If-Closure

In order to model sequential composition, we must allow inconsistent predicates in a single pomset, unlike PwP [Jagadeesan et al. 2020]. For example, if $S = (x := 1)$, then the semantics Fig. 1 does *not* allow:

$$\texttt{if}(M)\{x := 1\};\ S;\ \texttt{if}(\neg M)\{x := 1\}$$

$$\boxed{\mathsf{W}x1} \rightarrow \boxed{\mathsf{W}x1}$$

However, if $S = (\texttt{if}(\neg M)\{x := 1\};\ \texttt{if}(M)\{x := 1\})$, then it *does* allow the execution. Looking at the initial program:

$$\begin{array}{ccc} \texttt{if}(M)\{x := 1\} & x := 1 & \texttt{if}(\neg M)\{x := 1\} \\ \boxed{M \mid \mathsf{W}x1} & \boxed{\mathsf{W}x1} & \boxed{\neg M \mid \mathsf{W}x1} \end{array}$$

The difficulty is that the middle action can coalesce either with the right action, or the left, but not both. Thus, we are stuck with some non-tautological precondition. Our solution is to allow a pomset to contain many events for a single action, as long as the events have disjoint preconditions.

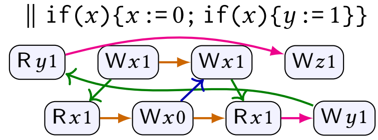
Def. 9.7 allows the execution, by splitting the middle command:

$$\begin{array}{ccc} \texttt{if}(M)\{x := 1\} & x := 1 & \texttt{if}(\neg M)\{x := 1\} \\ {}^{d}\boxed{M \mid \mathsf{W}x1} & {}^{d}\boxed{\neg M \mid \mathsf{W}x1}\quad {}^{e}\boxed{M \mid \mathsf{W}x1} & {}^{e}\boxed{\neg M \mid \mathsf{W}x1} \end{array}$$

Coalescing events gives the desired result.

This is not simply a theoretical question; it is observable. For example, the semantics of Fig. 1 does not allow the following, since it must add order in the first thread from the read of y to one of the writes to x.

$$r := y;\ \texttt{if}(r)\{x := 1\};\ x := 1;\ \texttt{if}(\neg r)\{x := 1\};\ z := r$$
$$\parallel\ \texttt{if}(x)\{x := 0;\ \texttt{if}(x)\{y := 1\}\}$$



Definition 9.7. Let $E \subseteq \mathcal{E}$ and $\theta : E \to \Phi$ and $\Omega \in \Phi$. We say that θ *partitions* Ω if (1) if $\theta_e \wedge \theta_d$ is satisfiable then $e = d$, (2) $\Omega \equiv \bigvee_{e\in E} \theta_e$.

If $P \in \mathit{WRITE}(x, M, \mu)$ then $(\exists v : E \to \mathcal{V})\ (\exists \theta : E \to \Phi)\ (\exists \Omega \in \{\mathsf{tt}, \mathsf{ff}\})$

- (w1) θ partitions Ω,
- (w2) $\lambda(e) = \mathsf{W}^{\mu} x v_e$,
- (w3) $\kappa(e) \equiv \theta_e \wedge M{=}v_e$,
- (w4) $\tau^D(\psi) \equiv \bigwedge_{e\in E}(\theta_e \Rightarrow \psi[M/x][M{=}v_e/\mathsf{Q}_x])$ $\wedge \neg\Omega \Rightarrow \psi[M/x][\mathsf{ff}/\mathsf{Q}_x]$
- (w5) $\checkmark \equiv \Omega \wedge \bigwedge_{e\in E}(\theta_e \Rightarrow M{=}v_e)$.

If $P \in \mathit{READ}(r, x, \mu)$ then $(\exists v : E \to \mathcal{V})\ (\exists \theta : E \to \Phi)\ (\exists \Omega \in \{\mathsf{tt}, \mathsf{ff}\})$

- (R1) θ partitions Ω,
- (R2) $\lambda(e) = \mathsf{R}^{\mu} x v_e$
- (R3) $\kappa(e) \equiv \theta_e \wedge \mathsf{Q}_x$,
- (R4) $(\forall s)\tau^D(\psi) \equiv \bigwedge_{e\in E\cap D}(\theta_e \Rightarrow v_e{=}s_e \Rightarrow \psi[s_e/r])$ $\wedge \bigwedge_{e\in E\setminus D}(\theta_e \Rightarrow (v_e{=}s_e \vee x{=}s_e) \Rightarrow \psi[s_e/r])$ $\wedge \neg\Omega \Rightarrow \psi[s/r]$
- (R5a) if $\mu \sqsubseteq \mathsf{rlx}$ then $\checkmark \equiv \mathsf{tt}$,
- (R5b) if $\mu \sqsupseteq \mathsf{acq}$ then $\checkmark \equiv \Omega$.

The definition allows multiple events to represent a single action, each with a disjoint precondition. The predicate transformers are derived from those defined for the conditional.

This modification validates Lemma 4.6e, f, and g as equations.

We show how to combine address calculation and if-closure in §A.4.

10 CONCLUSIONS

This paper is the first to present a direct denotational semantics for sequential composition in a relaxed memory model that can be efficiently compiled to modern CPUs. We extract from this model a semantic dependency relation and use it to build PwT-C11, a solution to the Out-of-Thin-Air problem in C11, and PwT-MCA, a model for Java-like languages.

We have not treated loops in this model, though we expect that the usual approach of showing continuity for all the semantic operations with respect to set inclusion would go through. Paviotti et al. [2020] use step-indexing to account for loops; a similar approach could be applied here.

PwT-MCA does not validate access elimination: store-forwarding and dead-write-removal are unsound. We expect that these can be validated by allowing events with different labels to merge.

PwT-MCA_1 is a simpler model than PwT-MCA_2, but requires fences on acquiring reads for Arm8. It would be illuminating to find out what the performance penalty is for these fences.

PwT does not validate read introduction, whereas speculative operational semantics do. Recent work shows a tension between read introduction and compositional reasoning for temporal safety properties (see §A.1). Nonetheless, read introduction is ubiquitous is some compilers. It would be interesting to know if there is a performance penalty for banning read introduction.

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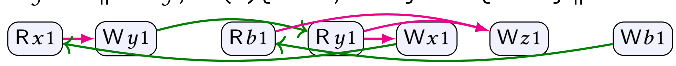
A DISCUSSION

A.1 Comparison to "Promising Semantics" [POPL 2017]

Recently, Cho et al. [2021] showed that certain combinations of compiler optimizations are inconsistent with local DRF guarantees. All of the examples that prove inconsistency have the same shape: they combine read introduction and case analysis (aka, if-closure). Effectively, this turns one read into two, where different conditional branches can be taken for the two copies of the read. This is reminiscent of the type of *bait and switch* behavior noted by Jagadeesan et al. [2020]: the promising semantics (PS) [Kang et al. 2017] and related models [Chakraborty and Vafeiadis 2019; Jagadeesan et al. 2010; Manson et al. 2005], fail to validate compositional reasoning of temporal properties. Consider example OOTA4 from [Jagadeesan et al. 2020]:

$$y := x \parallel r := y;\ \mathtt{if}(b)\{x := r;\ z := r\}\,\mathtt{else}\,\{x := 1\} \parallel b := 1$$

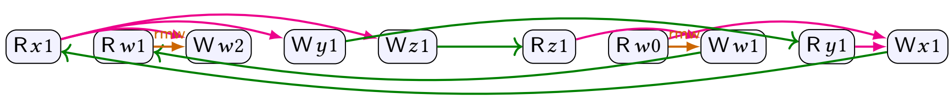


(OOTA4)

Under all variants of PwT, this outcome is disallowed, due to the cycle involving x and y.[4] Under PS, this outcome is allowed by baiting with the `else` branch, then switching to the `then` branch, based on a coin flip (b).

Cho et al. [2021] introduce more complex examples to show that the promising semantics fails LDRF-SC.[5] Here is one, dubbed LDRF-FAIL-PS.

$$\mathtt{if}(x)\{\mathtt{FADD}(w,1);\ y := 1;\ z := 1\} \parallel \mathtt{if}(z)\{\mathtt{if}(!\mathtt{FADD}(w,1))\{x := y\}\}\,\mathtt{else}\,\{x := 1\}$$



Again, all variants of PwT disallow the outcome due to the cycle involving x and y. It is allowed by PS by baiting the second thread with $x := 1$ in the `else` branch, then switching to the `then` branch. This shows some some structural resemblance to OOTA4, with z replacing b.

Cho et al. argue that the outcome of LDRF-FAIL-PS is inevitable due to compiler optimizations. The examples crucially involve the following sequence of operations:

- read introduction,
- if introduction, branching on the read just introduced.

We believe this combination of optimizations is unsound. This is obviously the case in C11: read introduction may cause undefined behavior (UB), due to the possible introduction of a data race.

The situation is more delicate in LLVM. The short version of the story is that load-hoisting followed by case analysis is unsound in LLVM, without freeze. This happens because:

- read introduction may result in the undefined value **undef**, due to the possible introduction of a data race [Chakraborty and Vafeiadis 2017], and
- branching on an undefined value in LLVM results in UB.

LLVM delays UB using the undefined value. This allows LLVM to perform optimizations such as load hoisting, where $\mathtt{if}(C)\{r := x\}$ is rewritten to $s := x;\ r := C?s : r$. Despite this, other optimizations regularly performed by LLVM are unsound [Lee et al. 2017]. An example is loop switching, where $\mathtt{while}(C_1)\{\mathtt{if}(C_2)\{S_1\}\,\mathtt{else}\,\{S_2\}\}$ is rewritten to $\mathtt{if}(C_2)\{\mathtt{while}(C_1)\{S_1\}\}\,\mathtt{else}\,\{\mathtt{while}$

[4] All of the reads in OOTA4 are cross-thread, so there is no difference between PwT-MCA$_1$ and PwT-MCA$_2$. For PwT-C11, there is a cycle in $\mathsf{rf} \cup <$.

[5] Cho et al. [2021] show that by restricting RMW-store reorderings, one can establish LDRF-SC for PS. We speculate that no such restriction is required for PwT. (We did not treat RMWs in our proof of LDRF-SC.)

$(C_1)\{S_2\}\}$. Freeze was introduced in LLVM in order to make such optimizations sound by allowing branch on frozen **undef** to give nondeterministic choice rather than UB. In the RFC for freeze, Lopes [2016] says: *"Note that having branch on poison not trigger* UB *has its own problems. We believe this is a good tradeoff."* LDRF-FAIL-PS demonstrates a concrete problem with this tradeoff. Other compilers, such as Compcert, are more conservative [Lee et al. 2017, §9].

Thus, the difference between PS and PwT can be understood in terms of the valid program transformations. PS allows reads to be introduced, with subsequent case analysis on the value read. PwT validates case analysis, but invalidates read introduction.

Allowing executions such as OOTA4 and LDRF-FAIL-PS also invalidates compositional reasoning for temporal safety properties (see §6).

These differences highlight the subtle tensions between compiler optimizations and program logics that are revealed by relaxed memory models. It is not possible to have everything one wants. Thus, one is forced to choose which optimizations and reasoning principles are most important.[6]

Finally, we note that it is possible that PS is properly weaker than PwT.

A.2 Comparison to "Pomsets with Preconditions" [OOPSLA 2020]

PwT-MCA is closely related to PwP model of [Jagadeesan et al. 2020]. The major difference is that PwT-MCA supports sequential composition. In the remainder of this section, we discuss other differences. We also point out some errors in [Jagadeesan et al. 2020], all of which have been confirmed by the authors.

Substitution. PwP uses substitution rather than Skolemizing. Indeed our use of Skolemization is motivated by disjunction closure for predicate transformers, which do not appear in PwP. In Fig. 1, we gave the semantics of read for nonempty pomsets as:

(R4a) if $(E \cap D) \neq \emptyset$ then $\tau^D(\psi) \equiv v{=}r \Rightarrow \psi$,
(R4b) if $(E \cap D) = \emptyset$ then $\tau^D(\psi) \equiv (v{=}r \lor x{=}r) \Rightarrow \psi$.

In PwP, the definition is roughly as follows:

(R4a′) if $(E \cap D) \neq \emptyset$ then $\tau^D(\psi) \equiv \psi[v/r][v/x]$,
(R4b′) if $(E \cap D) = \emptyset$ then $\tau^D(\psi) \equiv \psi[v/r][v/x] \land \psi[x/r]$

The use of conjunction in R4b′ causes disjunction closure to fail because the predicate transformer $\tau(\psi) = \psi' \land \psi''$ does not distribute through disjunction, even assuming that the prime operations do:[7] $\tau(\psi_1 \lor \psi_2) = (\psi_1' \lor \psi_2') \land (\psi_1'' \lor \psi_2'') \neq (\psi_1' \land \psi_1'') \lor (\psi_2' \land \psi_2'') = \tau(\psi_1) \lor \tau(\psi_2)$. See also §4.9.

The substitutions collapse x and r, allowing local invariant reasoning (LIR), as required by JMM causality test case 1, discussed in §4.8. Without Skolemizing it is necessary to substitute $[x/r]$, since the reverse substitution $[r/x]$ is useless when r is bound—compare with §A.5. As discussed below (Downset closure), including this substitution affects the interaction of LIR and downset closure.

Removing the substitution of $[x/r]$ in the independent case has a technical advantage: we no longer require *extended* expressions (which include memory references), since substitutions no longer introduce memory references.

[6] Another example is the tension between load hoisting—forbidden in C11 but allowed by LLVM—and common subexpression elimination over an acquiring lock—allowed by C11 but forbidden by LLVM [Chakraborty and Vafeiadis 2017].
[7] $(\psi_1 \lor \psi_2)' = (\psi_1' \lor \psi_2')$ and $(\psi_1 \lor \psi_2)'' = (\psi_1'' \lor \psi_2'')$.

The substitution $[x/r]$ does not work with Skolemization, even for the dependent case, since we lose the unique marker for each read. In effect, this forces all reads of a location to see the same values. Using this definition, consider the following:

$$r := x;\ s := x;\ \texttt{if}(r{<}s)\{y := 1\}$$

$$\boxed{\mathsf{R}x1} \quad \boxed{\mathsf{R}x2} \rightarrow \boxed{1{=}x \Rightarrow 2{=}x \Rightarrow x{<}x \mid \mathsf{W}y1}$$

Although the execution seems reasonable, the precondition on the write is not a tautology.

Downset closure. PwP enforces downset closure in the prefixing rule. Even without this, downset closure would be different for the two semantics, due to the use of substitution in PwP. Consider the final pomset in the last example of §A.6 under the semantics of this paper, which elides the middle read event:

$$x := 0;\ r := x;\ \texttt{if}(r{\geqslant}0)\{y := 1\}$$

$$\boxed{\mathsf{W}x0} \qquad \boxed{r{\geqslant}0 \mid \mathsf{W}y1}$$

In PwP, the substitution $[x/r]$ is performed by the middle read regardless of whether it is included in the pomset, with the subsequent substitution of $[0/x]$ by the preceding write, we have $[x/r][0/x]$, which is $[0/r][0/x]$, resulting in:

$$\boxed{\mathsf{W}x0} \qquad \boxed{0{\geqslant}0 \mid \mathsf{W}y1}$$

Consistency. PwP imposes *consistency*, which requires that for every pomset P, $\bigwedge_e \kappa(e)$ is satisfiable. Associativity requires that we allow pomsets with inconsistent preconditions. Consider a variant of the example from §9.5.

$$\texttt{if}(M)\{x := 1\} \qquad \texttt{if}(!M)\{x := 1\} \qquad \texttt{if}(M)\{y := 1\} \qquad \texttt{if}(!M)\{y := 1\}$$

$$\boxed{M \mid \mathsf{W}x1} \qquad \boxed{\neg M \mid \mathsf{W}x1} \qquad \boxed{M \mid \mathsf{W}y1} \qquad \boxed{\neg M \mid \mathsf{W}y1}$$

Associating left and right, we have:

$$\texttt{if}(M)\{x := 1\};\ \texttt{if}(!M)\{x := 1\} \qquad \texttt{if}(M)\{y := 1\};\ \texttt{if}(!M)\{y := 1\}$$

$$\boxed{\mathsf{W}x1} \qquad \boxed{\mathsf{W}y1}$$

Associating into the middle, instead, we require:

$$\texttt{if}(M)\{x := 1\} \qquad \texttt{if}(!M)\{x := 1\};\ \texttt{if}(M)\{y := 1\} \qquad \texttt{if}(!M)\{y := 1\}$$

$$\boxed{M \mid \mathsf{W}x1} \qquad \boxed{\neg M \mid \mathsf{W}x1}\ \boxed{M \mid \mathsf{W}y1} \qquad \boxed{\neg M \mid \mathsf{W}y1}$$

Joining left and right, we have:

$$\texttt{if}(M)\{x := 1\};\ \texttt{if}(!M)\{x := 1\};\ \texttt{if}(M)\{y := 1\};\ \texttt{if}(!M)\{y := 1\}$$

$$\boxed{\mathsf{W}x1} \quad \boxed{\mathsf{W}y1}$$

Causal Strengthening. PwP imposes *causal strengthening*, which requires for every pomset P, if $d < e$ then $\kappa(e) \vDash \kappa(d)$. Associativity requires that we allow pomsets without causal strengthening. Consider the following.

$$\texttt{if}(M)\{r := x\} \qquad y := r \qquad \texttt{if}(!M)\{s := x\}$$

$$\boxed{M \mid \mathsf{R}x1} \qquad \boxed{r{=}1 \mid \mathsf{W}y1} \qquad \boxed{\neg M \mid \mathsf{R}x1}$$

Associating left, with causal strengthening:

$$\texttt{if}(M)\{r := x\};\ y := r \qquad \texttt{if}(!M)\{s := x\}$$

$$\boxed{M \mid \mathsf{R}x1} \rightarrow \boxed{M \mid \mathsf{W}y1} \qquad \boxed{\neg M \mid \mathsf{R}x1}$$

Finally, merging:

$$\mathtt{if}(M)\{r:=x\};\ y:=r;\ \mathtt{if}(!M)\{s:=x\}$$

$$\boxed{\mathsf{R}\,x\,1} \rightarrow \boxed{M \mid \mathsf{W}\,y\,1}$$

Instead, associating right:

$$\mathtt{if}(M)\{r:=x\} \qquad\qquad y:=r;\ \mathtt{if}(!M)\{s:=x\}$$

$$\boxed{M \mid \mathsf{R}\,x\,1} \qquad\qquad \boxed{r{=}1 \mid \mathsf{W}\,y\,1}\quad \boxed{\neg M \mid \mathsf{R}\,x\,1}$$

Merging:

$$\mathtt{if}(M)\{r:=x\};\ y:=r;\ \mathtt{if}(!M)\{s:=x\}$$

$$\boxed{\mathsf{R}\,x\,1} \rightarrow \boxed{\mathsf{W}\,y\,1}$$

With causal strengthening, the precondition of $\mathsf{W}\,y\,1$ depends upon how we associate. This is not an issue in PwP, which always associates to the right.

One use of causal strengthening is to ensure that address dependencies do not introduce thin air reads. Associating to the right, the intermediate state of the example in §9.3 is:

$$s:=[r];\ x:=s$$

$$\boxed{r{=}2 \mid \mathsf{R}[2]1} \rightarrow \boxed{(r{=}2 \Rightarrow 1{=}s) \Rightarrow s{=}1 \mid \mathsf{W}\,x\,1}$$

In PwP, we have, instead:

$$s:=[r];\ x:=s$$

$$\boxed{r{=}2 \mid \mathsf{R}[2]1} \rightarrow \boxed{r{=}2 \wedge [2]{=}1 \mid \mathsf{W}\,x\,1}$$

Without causal strengthening, the precondition of $(\mathsf{W}\,x\,1)$ would be simply $[2]{=}1$. The treatment in this paper, using implication rather than conjunction, is more precise.

Internal Acquiring Reads. The proof of compilation to Arm in PwP assumes that all internal reads can be eliminated. However, this is not the case for acquiring reads. For example, PwP disallows the following execution, where the final values of x is 2 and the final value of y is 2. This execution is allowed by Arm8 and TSO.

$$x:=2;\ r:=x^{\mathsf{acq}};\ s:=y \parallel y:=2;\ x^{\mathsf{rel}}:=1$$

$$\boxed{\mathsf{W}\,x\,2} \rightarrow \boxed{\mathsf{R}^{\mathsf{acq}}\,x\,2} \rightarrow \boxed{\mathsf{R}\,y\,0} \rightarrow \boxed{\mathsf{W}\,y\,2} \rightarrow \boxed{\mathsf{W}^{\mathsf{rel}}\,x\,1}$$

We discuss two approaches to this problem in §B.

Redundant Read Elimination. Contrary to the claim, redundant read elimination fails for PwP. We discuss redundant read elimination in §9.1. Consider JMM Causality Test Case 2, which we describe there.

$$r:=x;\ s:=x;\ \mathtt{if}(r{=}s)\{y:=1\} \parallel x:=y$$

$$\boxed{\mathsf{R}\,x\,1} \quad \boxed{\mathsf{R}\,x\,1} \quad \boxed{\mathsf{W}\,y\,1} \rightarrow \boxed{\mathsf{R}\,y\,1} \rightarrow \boxed{\mathsf{W}\,x\,1}$$

Under the semantics of PwP, we have

$$r:=x;\ s:=x;\ \mathtt{if}(r{=}s)\{y:=1\}$$

$$\boxed{\mathsf{R}\,x\,1} \quad \boxed{\mathsf{R}\,x\,1} \quad \boxed{1{=}1 \wedge 1{=}x \wedge x{=}1 \wedge x = x \mid \mathsf{W}\,y\,1}$$

The precondition of ($\mathsf{W}y1$) is *not* a tautology, and therefore redundant read elimination fails. (It is a tautology in $r := x;\ s := r;\ \mathtt{if}(r{=}s)\{y := 1\}$.) PwP(§3.1) incorrectly stated that the precondition of ($\mathsf{W}y1$) was $1{=}1 \land x{=}x$.

A.3 Comparison with Sequential Predicate Transformers

We compare traditional transformers to the dependent-case transformers of Fig. 1.

All programs in our language are strongly normalizing, so we need not distinguish strong and weak correctness. In this setting, the Hoare triple $\{\phi\}\ S\ \{\psi\}$ holds exactly when $\phi \Rightarrow wp_S(\psi)$.

Hoare triples do not distinguish thread-local variables from shared variables. Thus, the assignment rule applies to all types of storage. The rules can be written as on the left below:

$$
\begin{aligned}
wp_{x:=M}(\psi) &= \psi[M/x] & \qquad \tau_{x:=M}(\psi) &= \psi[M/x] \\
wp_{r:=M}(\psi) &= \psi[M/r] & \qquad \tau_{r:=M}(\psi) &= \psi[M/r] \\
wp_{r:=x}(\psi) &= x{=}r \Rightarrow \psi & \qquad \tau_{r:=x}(\psi) &= v{=}r \Rightarrow \psi \quad \text{where } \lambda(e) = \mathsf{R}xv
\end{aligned}
$$

Here we have chosen an alternative formulation for the read rule, which is equivalent to the more traditional $\psi[x/r]$, as long as registers are assigned at most once in a program. Our predicate transformers for the dependent case are shown on the right above. Only the read rule differs from the traditional one.

For programs where every register is bound and every read is fulfilled, our dependent transformers are the same as the traditional ones. Thus, when comparing to weakest preconditions, let us only consider totally-ordered executions of our semantics where every read could be fulfilled by prepending some writes. For example, we ignore pomsets of $x := 2;\ r := x$ that read 1 for x.

For example, let S_i be defined:

$$
S_1 = s := x;\ x := s{+}r \qquad S_2 = x := t;\ S_1 \qquad S_3 = t := 2;\ r := 5;\ S_2
$$

The following pomset appears in the semantics of S_2. A pomset for S_3 can be derived by substituting $[2/t, 5/r]$. A pomset for S_1 can be derived by eliminating the initial write.

$$x := t;\ s := x;\ x := s{+}r$$

$$
(t{=}2 \mid \mathsf{W}x2) \rightarrow (\mathsf{R}x2) \rightarrow (2{=}s \Rightarrow (s{+}r){=}7 \mid \mathsf{W}x7) \dashrightarrow \boxed{2{=}s \Rightarrow \psi[s{+}r/x]}
$$

The predicate transformers are:

$$
\begin{aligned}
wp_{S_1}(\psi) &= x{=}s \Rightarrow \psi[s{+}r/x] & \qquad \tau_{S_1}(\psi) &= 2{=}s \Rightarrow \psi[s{+}r/x] \\
wp_{S_2}(\psi) &= t{=}s \Rightarrow \psi[s{+}r/x] & \qquad \tau_{S_2}(\psi) &= 2{=}s \Rightarrow \psi[s{+}r/x] \\
wp_{S_3}(\psi) &= 2{=}s \Rightarrow \psi[s{+}5/x] & \qquad \tau_{S_3}(\psi) &= 2{=}s \Rightarrow \psi[s{+}5/x]
\end{aligned}
$$

A.4 Combining Address Calculation and If-Closure

Def. 9.4 is naive with respect to merging events. Consider the following example:

$$[r] := 0;\ [0] := !r \qquad\qquad [r] := 0;\ [0] := !r$$

$$
\overset{c}{(r{=}1 \mid \mathsf{W}[1]0)} \quad \overset{d}{(r{=}1 \mid \mathsf{W}[0]0)} \qquad\qquad \overset{d}{(r{=}0 \mid \mathsf{W}[0]0)} \rightarrow \overset{e}{(r{=}0 \mid \mathsf{W}[0]1)}
$$

Merging, we have:

$$\mathtt{if}(M)\{[r] := 0;\ [0] := !r\}\,\mathtt{else}\,\{[r] := 0;\ [0] := !r\}$$

$$
\overset{c}{(r{=}1 \mid \mathsf{W}[1]0)} \quad \overset{d}{(r{=}0 \lor r{=}1 \mid \mathsf{W}[0]0)} \rightarrow \overset{e}{(r{=}0 \mid \mathsf{W}[0]1)}
$$

The precondition of $\mathsf{W}[0]0$ is a tautology; however, this is not possible for ($[r] := 0;\ [0] := !r$) alone, using Def. 9.4.

Def. A.1, enables this execution using if-closure. Under this semantics, we have:

$$[r] := 0 \qquad\qquad\qquad\qquad [0] := !r$$

$$^{c}\boxed{r{=}1 \mid \mathsf{W}[1]0} \quad ^{d}\boxed{r{=}0 \mid \mathsf{W}[0]0} \qquad\qquad ^{d}\boxed{r{=}1 \mid \mathsf{W}[0]0} \quad ^{e}\boxed{r{=}0 \mid \mathsf{W}[0]1}$$

Sequencing and merging:

$$[r] := 0\,;\ [0] := !r$$

$$^{c}\boxed{r{=}1 \mid \mathsf{W}[1]0} \quad ^{d}\boxed{r{=}0 \lor r{=}1 \mid \mathsf{W}[0]0} \rightarrow {}^{e}\boxed{r{=}0 \mid \mathsf{W}[0]1}$$

The precondition of $(\mathsf{W}[0]0)$ is a tautology, as required.

Definition A.1. If $P \in \mathit{WRITE}(L, M, \mu)$ then $(\exists \ell : E \to \mathcal{V})\ (\exists v : E \to \mathcal{V})\ (\exists \theta : E \to \Phi)\ (\exists \Omega \in \{\mathsf{tt}, \mathsf{ff}\})$

- (w1) θ partitions Ω,
- (w2) $\lambda(e) = \mathsf{W}^{\mu}[\ell]v_e$,
- (w3) $\kappa(e) \equiv \theta_e \land L{=}\ell_e \land M{=}v_e$,
- (w4) $(\forall k)\tau^{D}(\psi) \equiv \bigwedge_{e\in E}(\theta_e \Rightarrow (L{=}\ell) \Rightarrow \psi[M/x][M{=}v_e/\mathsf{Q}_x])$
  $\land \neg\Omega \Rightarrow (L{=}k) \Rightarrow \psi[M/x][\mathsf{ff}/\mathsf{Q}_x]$
- (w5) $\checkmark \equiv \Omega \land \bigwedge_{e\in E}(\theta_e \Rightarrow L{=}\ell_e \land M{=}v_e)$.

If $P \in \mathit{READ}(r, L, \mu)$ then $(\exists \ell : E \to \mathcal{V})\ (\exists v : E \to \mathcal{V})\ (\exists \theta : E \to \Phi)\ (\exists \Omega \in \{\mathsf{tt}, \mathsf{ff}\})$

- (r1) θ partitions Ω,
- (r2) $\lambda(e) = \mathsf{R}^{\mu}[\ell]v_e$
- (r3) $\kappa(e) \equiv \theta_e \land L{=}\ell_e \land \mathsf{Q}_{[\ell]}$,
- (r4) $(\forall s)\tau^{D}(\psi) \equiv \bigwedge_{e\in E\cap D}(\theta_e \Rightarrow (L{=}\ell_e \Rightarrow v_e{=}s_e) \Rightarrow \psi[s_e/r])$
  $\land \bigwedge_{e\in E\setminus D}(\theta_e \Rightarrow ((L{=}\ell_e \Rightarrow v_e{=}s_e) \lor (L{=}\ell_e \Rightarrow [\ell]{=}s_e)) \Rightarrow \psi[s_e/r])$
  $\land \neg\Omega \Rightarrow \psi[s/r]$,
- (r5a) if $\mu \sqsubseteq \mathsf{rlx}$ then $\checkmark \equiv \mathsf{tt}$,
- (r5b) if $\mu \sqsupseteq \mathsf{acq}$ then $\checkmark \equiv \Omega$.

A.5 Substitutions

In *READ*, it is also possible to collapse x and r via substitution:

- (r4a′) if $(E \cap D) \neq \emptyset$ then $\tau^{D}(\psi) \equiv v{=}r \Rightarrow \psi[r/x]$,
- (r4b′) if $E \neq \emptyset$ and $(E \cap D) = \emptyset$ then $\tau^{D}(\psi) \equiv (v{=}r \lor x{=}r) \Rightarrow \psi[r/x]$,
- (r4c′) if $E = \emptyset$ then $\tau^{D}(\psi) \equiv \psi[r/x]$,

Perhaps surprisingly, this semantics is incomparable with that of Fig. 1. Consider the following:

$$\texttt{if}(r \land s\ \mathsf{even})\{y := 1\};\ \texttt{if}(r \land s)\{z := 1\}$$

$$\boxed{r \land s\ \mathsf{even} \mid \mathsf{W}y1} \quad \boxed{r \land s \mid \mathsf{W}z1}$$

Prepending $(s := x)$, we get the same result regardless of whether we substitute $[s/x]$, since x does not occur in either precondition. Here we show the independent case:

$$s := x\,;\ \texttt{if}(r \land s\ \mathsf{even})\{y := 1\};\ \texttt{if}(r \land s)\{z := 1\}$$

$$\boxed{\mathsf{R}x2} \quad \boxed{(2{=}s \lor x{=}s) \Rightarrow (r \land s\ \mathsf{even}) \mid \mathsf{W}y1} \quad \boxed{(2{=}s \lor x{=}s) \Rightarrow (r \land s) \mid \mathsf{W}z1}$$

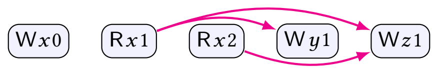
Since the preconditions mention x, prepending $(r := x)$, we now get different results depending on whether we perform the substitution. Without any substitution, we have:

$$r := x\,;\ s := x\,;\ \texttt{if}(r \land s\ \mathsf{even})\{y := 1\};\ \texttt{if}(r \land s)\{z := 1\}$$

$$\boxed{\mathsf{R}x1} \quad \boxed{\mathsf{R}x2} \quad \boxed{1{=}r \Rightarrow (2{=}s \lor x{=}s) \Rightarrow (r \land s\ \mathsf{even}) \mid \mathsf{W}y1} \quad \boxed{1{=}r \Rightarrow (2{=}s \lor x{=}s) \Rightarrow (r \land s) \mid \mathsf{W}z1}$$

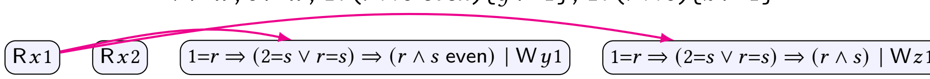
Prepending $(x := 0)$, which substitutes $[0/x]$, the precondition of $(\mathsf{W}y1)$ becomes $(1{=}r \Rightarrow (2{=}s \lor 0{=}s) \Rightarrow (r \land s\ \mathsf{even}))$, which is a tautology, whereas the precondition of $\mathsf{W}z1$ becomes $(1{=}r \Rightarrow$

$(2{=}s \vee 0{=}s) \Rightarrow (r \wedge s))$, which is not. In order to be top-level, $(\mathsf{W}z1)$ must be dependency ordered after $(\mathsf{R}x2)$; in this case the precondition becomes $(1{=}r \Rightarrow 2{=}s \Rightarrow (r \wedge s))$, which is a tautology.

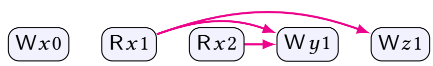


The situation reverses with the substitution $[r/x]$:

$$r := x\,;\ s := x\,;\ \mathtt{if}(r \wedge s \text{ even})\{y := 1\};\ \mathtt{if}(r \wedge s)\{z := 1\}$$



Prepending $(x := 0)$:



The dependency has changed from $(\mathsf{R}x2) \rightarrow (\mathsf{W}z1)$ to $(\mathsf{R}x2) \rightarrow (\mathsf{W}y1)$. The resulting sets of pomsets are incomparable.

Thinking in terms of hardware, the difference is whether reads update the cache, thus clobbering preceding writes. With $[r/x]$, reads clobber the cache, whereas without the substitution, they do not. Since most caches work this way, the model with $[r/x]$ is likely preferred for modeling hardware. However, this substitution only makes sense in a model with read-read coherence and read-read dependencies, which is not the case for Arm8.

A.6 Downset Closure

We would like the semantics to be closed with respect to *downsets*. Downsets include a subset of initial events, similar to *prefixes* for strings.

Definition A.2. P_2 is an *downset* of P_1 if

(1) $E_2 \subseteq E_1$,
(2) $(\forall e \in E_2)\ \lambda_2(e) = \lambda_1(e)$,
(3) $(\forall e \in E_2)\ \kappa_2(e) \equiv \kappa_1(e)$,
(4) $(\forall e \in E_2)\ \tau_2^D(e) \equiv \tau_1^D(e)$,
(5) $\checkmark_2 \vDash \checkmark_1$,
(6a) $(\forall d \in E_2)\ (\forall e \in E_2)\ d <_2 e$ iff $d <_1 e$,
(6b) $(\forall d \in E_1)\ (\forall e \in E_2)$ if $d <_1 e$ then $d \in E_2$,
(7) $(\forall d \in E_2)\ (\forall e \in E_2)\ d \ \mathsf{rf}_2\ e$ iff $d \ \mathsf{rf}_1\ e$.

Downset closure fails due to for two reasons. The key property is that the empty set transformer should behave the same as the independent transformer.

First, downset closure fails for read-read independency §4.7. Consider

$$r := x\,;\ \mathtt{if}(!r)\{s := y\}$$

$\boxed{\mathsf{R}x0}$ $\boxed{\mathsf{R}y0}$

The semantics of this program includes the singleton pomset $(\mathsf{R}x0)$, but not the singleton pomset $(\mathsf{R}y0)$. To get $(\mathsf{R}x0)$, we combine:

$r := x$	$\mathtt{if}(!r)\{s := y\}$
$\boxed{\mathsf{R}x0}$	$\emptyset$

Attempting to get $(\mathsf{R}y0)$, we instead get:

$r := x$	$\mathtt{if}(!r)\{s := y\}$
$\emptyset$	$\boxed{r{=}0 \mid \mathsf{R}y0}$

Since r appears only once in the program, this pomset cannot contribute to a top-level pomset.

Second, the semantics is not downset closed because the independency reasoning of R4b is only applicable for pomsets where the ignored read is present! Revisiting JMM causality test case 1 from the end of §4.6:

$$x := 0 \qquad\qquad r := x \qquad\qquad \texttt{if}(r \geqslant 0)\{y := 1\};\ z := r$$

$$\boxed{\mathsf{W}x0} \qquad\qquad \boxed{\mathsf{R}x1} \qquad\qquad \boxed{r{\geqslant}0 \mid \mathsf{W}y1} \quad \boxed{r{=}1 \mid \mathsf{W}z1}$$

$$\boxed{\psi[0/x]} \qquad\qquad \boxed{(1{=}r \vee x{=}r) \Rightarrow \psi}$$

$$x := 0;\ r := x;\ \texttt{if}(r \geqslant 0)\{y := 1\};\ z := r$$

$$\boxed{\mathsf{W}x0} \rightarrow \boxed{\mathsf{R}x1} \quad \boxed{(1{=}r \vee 0{=}r) \Rightarrow r{\geqslant}0 \mid \mathsf{W}y1} \quad \boxed{1{=}r \Rightarrow r{=}1 \mid \mathsf{W}z1}$$

The precondition of $(\mathsf{W}y1)$ is a tautology.

Taking the empty set for the read, however, the precondition of $(\mathsf{W}y1)$ is not a tautology:

$$x := 0;\ r := x;\ \texttt{if}(r \geqslant 0)\{y := 1\};\ z := r$$

$$\boxed{\mathsf{W}x0} \qquad \boxed{r{\geqslant}0 \mid \mathsf{W}y1} \quad \boxed{r{=}1 \mid \mathsf{W}z1}$$

One way to deal with the second issue would be to allow general access elimination to merge $(\mathsf{W}x0)$ and $(\mathsf{R}x0)$:

$$x := 0;\ r := x;\ \texttt{if}(r \geqslant 0)\{y := 1\};\ z := r$$

$$\boxed{\mathsf{W}x0} \qquad \boxed{(0{=}r \vee 0{=}r) \Rightarrow r{\geqslant}0 \mid \mathsf{W}y1} \quad \boxed{r{=}1 \mid \mathsf{W}z1}$$

We leave the elaboration of this idea to future work.

A.7 Logical Encoding of Delay for PwT-MCA

In this subsection, we develop a logical encoding of delay, which can replace s6a in PwT-MCA$_1$. It is not obvious how to repeat this trick for PwT-MCA$_2$, due to thread-local reads-from and thread-local blockers (s6a and s6b in Def. 5.2).

As motivation, note that PwT-MCA satisfies only one direction of Lemma 4.6(i)–(j)

(i) $\texttt{if}(\phi)\{\mathcal{P}_1\}\texttt{else}\{\mathcal{P}_2\} \supseteq \texttt{if}(\phi)\{\mathcal{P}_1\};\ \texttt{if}(\neg\phi)\{\mathcal{P}_2\}$.
(j) $\texttt{if}(\phi)\{\mathcal{P}_1\}\texttt{else}\{\mathcal{P}_2\} \supseteq \texttt{if}(\neg\phi)\{\mathcal{P}_2\};\ \texttt{if}(\phi)\{\mathcal{P}_1\}$.

In order to validate the reverse inclusions, we could require that s6a not impose order when $\kappa_1(d) \wedge \kappa_2(e)$ is unsatisfiable. Thus, following on §9.2, we would also like this:

(s6b′) if $\lambda_1(d)$ delays $\lambda_2(e)$ and $\kappa_1(d) \wedge \kappa'_2(e)$ is λ-consistent then $d \leq e$.

However, (s6b′) fails associativity. Example where $\theta_\lambda = (r{=}0)$

$$r := y \qquad\qquad \texttt{if}(r \parallel s)\{x := 1\} \qquad\qquad \texttt{if}(!s)\{x := 2\}$$

$$\boxed{\mathsf{R}y0} \qquad\qquad \boxed{r{\neq}0 \vee s{\neq}0 \mid \mathsf{W}x1} \qquad\qquad \boxed{s{=}0 \mid \mathsf{W}x2}$$

Associating right, order is required since $((r{\neq}0 \vee s{\neq}0) \wedge s{=}0)$ is satisfiable (take $r{=}1$ and $s{=}0$):

$$r := y \qquad\qquad \texttt{if}(r \parallel s)\{x := 1\};\ \texttt{if}(!s)\{x := 2\}$$

$$\boxed{\mathsf{R}y0} \qquad\qquad \boxed{r{\neq}0 \vee s{\neq}0 \mid \mathsf{W}x1} \rightarrow \boxed{s{=}0 \mid \mathsf{W}x2}$$

$$r := y;\ \texttt{if}(r \parallel s)\{x := 1\};\ \texttt{if}(!s)\{x := 2\}$$

$$\boxed{\mathsf{R}y0} \rightarrow \boxed{r{=}0 \Rightarrow (r{\neq}0 \vee s{\neq}0) \mid \mathsf{W}x1} \rightarrow \boxed{s{=}0 \mid \mathsf{W}x2}$$

Associating left, order is not required between the writes since ($s{\neq}0 \land s{=}0$) is unsatisfiable:

$$r:=y;\ \mathtt{if}(r \parallel s)\{x:=1\} \qquad\qquad \mathtt{if}(!s)\{x:=2\}$$

$$\boxed{\mathsf{R}\,y0} \rightarrow \boxed{r{=}0 \Rightarrow (r{\neq}0 \lor s{\neq}0) \mid \mathsf{W}x1} \qquad\qquad \boxed{s{=}0 \mid \mathsf{W}x2}$$

$$r:=y;\ \mathtt{if}(r \parallel s)\{x:=1\};\ \mathtt{if}(!s)\{x:=2\}$$

$$\boxed{\mathsf{R}\,y0} \rightarrow \boxed{r{=}0 \Rightarrow (r{\neq}0 \lor s{\neq}0) \mid \mathsf{W}x1} \quad \boxed{s{=}0 \mid \mathsf{W}x2}$$

This motivates the logic-based presentation of delay.

In the data model, we require additional symbols: Q_{sc}, $\mathsf{Q}^{x}_{\mathsf{ro}}$, and $\mathsf{Q}^{x}_{\mathsf{wo}}$. We refer to these collectively as *quiescence symbols*.

We update the Def. 4.4 of complete pomset to substitute true for every quiescence symbol (notation $[\mathsf{tt}/\mathsf{Q}]$):

Definition A.3. A PwT is *complete* if

(c3) $\kappa(e)[\mathsf{tt}/\mathsf{Q}]$ is a tautology, (c5) $\checkmark[\mathsf{tt}/\mathsf{Q}]$ is a tautology.

We define some helper notation:

Definition A.4. Let $\mathsf{Q}^{*}_{\mathsf{ro}} = \bigwedge_y \mathsf{Q}^{y}_{\mathsf{ro}}$, and similarly for $\mathsf{Q}^{*}_{\mathsf{wo}}$.
Let formulae $\mathsf{Q}^{\mathsf{S}x}_{\mu}$, $\mathsf{Q}^{\mathsf{L}x}_{\mu}$, and $\mathsf{Q}^{\mathsf{F}}_{\mu}$ be defined:

$$\begin{array}{lll}
\mathsf{Q}^{\mathsf{S}x}_{\mathsf{rlx}} = \mathsf{Q}^{x}_{\mathsf{ro}} \land \mathsf{Q}^{x}_{\mathsf{wo}} & \mathsf{Q}^{\mathsf{L}x}_{\mathsf{rlx}} = \mathsf{Q}^{x}_{\mathsf{wo}} & \mathsf{Q}^{\mathsf{F}}_{\mathsf{rel}} = \mathsf{Q}^{*}_{\mathsf{ro}} \land \mathsf{Q}^{*}_{\mathsf{wo}} \\
\mathsf{Q}^{\mathsf{S}x}_{\mathsf{rel}} = \mathsf{Q}^{*}_{\mathsf{ro}} \land \mathsf{Q}^{*}_{\mathsf{wo}} & \mathsf{Q}^{\mathsf{L}x}_{\mathsf{acq}} = \mathsf{Q}^{x}_{\mathsf{wo}} & \mathsf{Q}^{\mathsf{F}}_{\mathsf{acq}} = \mathsf{Q}^{*}_{\mathsf{ro}} \\
\mathsf{Q}^{\mathsf{S}x}_{\mathsf{sc}} = \mathsf{Q}^{*}_{\mathsf{ro}} \land \mathsf{Q}^{*}_{\mathsf{wo}} \land \mathsf{Q}_{\mathsf{sc}} & \mathsf{Q}^{\mathsf{L}x}_{\mathsf{sc}} = \mathsf{Q}^{x}_{\mathsf{wo}} \land \mathsf{Q}_{\mathsf{sc}} & \mathsf{Q}^{\mathsf{F}}_{\mathsf{sc}} = \mathsf{Q}^{*}_{\mathsf{ro}} \land \mathsf{Q}^{*}_{\mathsf{wo}} \land \mathsf{Q}_{\mathsf{sc}}
\end{array}$$

Let $[\phi/\mathsf{Q}^{*}_{\mathsf{ro}}]$ substitute ϕ for every $\mathsf{Q}^{y}_{\mathsf{ro}}$, and similarly for $\mathsf{Q}^{*}_{\mathsf{wo}}$.
Let substitutions $[\phi/\mathsf{Q}^{\mathsf{S}x}_{\mu}]$, $[\phi/\mathsf{Q}^{\mathsf{L}x}_{\mu}]$, and $[\phi/\mathsf{Q}^{\mathsf{F}}_{\mu}]$ be defined:

$$\begin{array}{lll}
[\phi/\mathsf{Q}^{\mathsf{S}x}_{\mathsf{rlx}}] = [\phi/\mathsf{Q}^{x}_{\mathsf{wo}}] & [\phi/\mathsf{Q}^{\mathsf{L}x}_{\mathsf{rlx}}] = [\phi/\mathsf{Q}^{x}_{\mathsf{ro}}] & [\phi/\mathsf{Q}^{\mathsf{F}}_{\mathsf{rel}}] = [\phi/\mathsf{Q}^{*}_{\mathsf{wo}}] \\
[\phi/\mathsf{Q}^{\mathsf{S}x}_{\mathsf{rel}}] = [\phi/\mathsf{Q}^{x}_{\mathsf{wo}}] & [\phi/\mathsf{Q}^{\mathsf{L}x}_{\mathsf{acq}}] = [\phi/\mathsf{Q}^{*}_{\mathsf{ro}}, \phi/\mathsf{Q}^{*}_{\mathsf{wo}}] & [\phi/\mathsf{Q}^{\mathsf{F}}_{\mathsf{acq}}] = [\phi/\mathsf{Q}^{*}_{\mathsf{ro}}, \phi/\mathsf{Q}^{*}_{\mathsf{wo}}] \\
[\phi/\mathsf{Q}^{\mathsf{S}x}_{\mathsf{sc}}] = [\phi/\mathsf{Q}^{x}_{\mathsf{wo}}, \phi/\mathsf{Q}_{\mathsf{sc}}] & [\phi/\mathsf{Q}^{\mathsf{L}x}_{\mathsf{sc}}] = [\phi/\mathsf{Q}^{*}_{\mathsf{ro}}, \phi/\mathsf{Q}^{*}_{\mathsf{wo}}, \phi/\mathsf{Q}_{\mathsf{sc}}] & [\phi/\mathsf{Q}^{\mathsf{F}}_{\mathsf{sc}}] = [\phi/\mathsf{Q}^{*}_{\mathsf{ro}}, \phi/\mathsf{Q}^{*}_{\mathsf{wo}}, \phi/\mathsf{Q}_{\mathsf{sc}}]
\end{array}$$

Update the following rules from Fig. 1. (The change is similar for address calculation and if-closure.)

(w3) $\kappa(e) \equiv M{=}v \land \mathsf{Q}^{\mathsf{S}x}_{\mu}$,
(w4a) if $E \neq \emptyset$ then $\tau^{D}(\psi) \equiv \psi[M/x][(M{=}v \land \mathsf{Q}^{\mathsf{S}x}_{\mu})/\mathsf{Q}^{\mathsf{S}x}_{\mu}]$,
(w4b) if $E = \emptyset$ then $\tau^{D}(\psi) \equiv \psi[M/x][\mathsf{ff}/\mathsf{Q}^{\mathsf{S}x}_{\mu}]$,
(r3) $\kappa(e) \equiv \mathsf{Q}^{\mathsf{L}x}_{\mu}$,
(r4a) if $e \in E \cap D$ then $\tau^{D}(\psi) \equiv v{=}r \Rightarrow \psi$,
(r4b) if $e \in E \setminus D$ then $\tau^{D}(\psi) \equiv (v{=}r \lor x{=}r) \Rightarrow \psi[\mathsf{ff}/\mathsf{Q}^{\mathsf{L}x}_{\mu}]$,
(r4c) if $E = \emptyset$ then $\tau^{D}(\psi) \equiv \psi[\mathsf{ff}/\mathsf{Q}^{\mathsf{L}x}_{\mu}]$,
(f3) $\kappa(e) \equiv \mathsf{Q}^{\mathsf{F}x}_{\mu}$,
(f4a) if $E \neq \emptyset$ then $\tau^{D}(\psi) \equiv \psi$,
(f4b) if $E = \emptyset$ then $\tau^{D}(\psi) \equiv \psi[\mathsf{ff}/\mathsf{Q}^{\mathsf{F}x}_{\mu}]$.

The quiescence formulae indicate what must precede an event. For example, all preceding accesses must be ordered before a releasing write, whereas only writes on x must be ordered before a releasing read on x.

The quiescence substitutions update quiescence symbols in subsequent code. For subsequent independent code, w3 and r3 substitute false. In complete pomsets, we substitute true for . For example, we substitute ff for $\mathsf{Q}^{\mathsf{S}x}_{\mathsf{rel}}$ in the independent case for a releasing write; this ensures that subsequent writes to x follow the releasing write in top-level pomsets. Similarly, we substitute ff

$x := M$

$\boxed{\psi[M/x][\mathsf{ff}/\mathsf{Q}^x_{\mathsf{wo}}]}$

$M{=}v \land \mathsf{Q}^x_{\mathsf{ro}} \land \mathsf{Q}^x_{\mathsf{wo}} \mid \mathsf{W}\,x\,v$

$\boxed{\psi[M/x][(M{=}v \land \mathsf{Q}^x_{\mathsf{wo}})/\mathsf{Q}^x_{\mathsf{wo}}]}$

$r := x$

$\boxed{(v{=}r \lor x{=}r) \Rightarrow \psi[\mathsf{ff}/\mathsf{Q}^x_{\mathsf{ro}}]}$

$\mathsf{Q}^x_{\mathsf{wo}} \mid \mathsf{R}\,x\,v$

$\boxed{v{=}r \Rightarrow \psi}$

$\mathsf{F}^{\mathsf{rel}}$

$\boxed{\psi[\mathsf{ff}/\mathsf{Q}^*_{\mathsf{wo}}]}$

$\mathsf{Q}^*_{\mathsf{ro}} \land \mathsf{Q}^*_{\mathsf{wo}} \mid \mathsf{F}^{\mathsf{rel}}$

$\boxed{\psi}$

$x^{\mathsf{rel}} := M$

$\boxed{\psi[M/x][\mathsf{ff}/\mathsf{Q}^x_{\mathsf{wo}}]}$

$M{=}v \land \mathsf{Q}^*_{\mathsf{ro}} \land \mathsf{Q}^*_{\mathsf{wo}} \mid \mathsf{W}^{\mathsf{rel}}\,x\,v$

$\boxed{\psi[M/x][(M{=}v \land \mathsf{Q}^x_{\mathsf{wo}})/\mathsf{Q}^x_{\mathsf{wo}}]}$

$r := x^{\mathsf{acq}}$

$\boxed{(v{=}r \lor x{=}r) \Rightarrow \psi[\mathsf{ff}/\mathsf{Q}^*_{\mathsf{ro}}][\mathsf{ff}/\mathsf{Q}^*_{\mathsf{wo}}]}$

$\mathsf{Q}^x_{\mathsf{wo}} \mid \mathsf{R}^{\mathsf{acq}}\,x\,v$

$\boxed{v{=}r \Rightarrow \psi}$

$\mathsf{F}^{\mathsf{acq}}$

$\boxed{\psi[\mathsf{ff}/\mathsf{Q}^*_{\mathsf{ro}}][\mathsf{ff}/\mathsf{Q}^*_{\mathsf{wo}}]}$

$\mathsf{Q}^*_{\mathsf{ro}} \mid \mathsf{R}^{\mathsf{acq}}\,x\,v$

$\boxed{\psi}$

$x^{\mathsf{sc}} := M$

$\boxed{\psi[M/x][\mathsf{ff}/\mathsf{Q}^x_{\mathsf{wo}}][\mathsf{ff}/\mathsf{Q}_{\mathsf{sc}}]}$

$M{=}v \land \mathsf{Q}^*_{\mathsf{ro}} \land \mathsf{Q}^*_{\mathsf{wo}} \land \mathsf{Q}_{\mathsf{sc}} \mid \mathsf{W}^{\mathsf{sc}}\,x\,v$

$\boxed{\psi[M/x][(M{=}v \land \mathsf{Q}^x_{\mathsf{wo}})/\mathsf{Q}^x_{\mathsf{wo}}][(M{=}v \land \mathsf{Q}_{\mathsf{sc}})/\mathsf{Q}_{\mathsf{sc}}]}$

$r := x^{\mathsf{sc}}$

$\boxed{(v{=}r \lor x{=}r) \Rightarrow \psi[\mathsf{ff}/\mathsf{Q}^*_{\mathsf{ro}}][\mathsf{ff}/\mathsf{Q}^*_{\mathsf{wo}}][\mathsf{ff}/\mathsf{Q}_{\mathsf{sc}}]}$

$\mathsf{Q}^x_{\mathsf{wo}} \land \mathsf{Q}_{\mathsf{sc}} \mid \mathsf{R}^{\mathsf{sc}}\,x\,v$

$\boxed{v{=}r \Rightarrow \psi}$

F^{sc}

$\boxed{\psi[\mathsf{ff}/\mathsf{Q}^*_{\mathsf{ro}}][\mathsf{ff}/\mathsf{Q}^*_{\mathsf{wo}}][\mathsf{ff}/\mathsf{Q}_{\mathsf{sc}}]}$

$\mathsf{Q}^*_{\mathsf{ro}} \land \mathsf{Q}^*_{\mathsf{wo}} \land \mathsf{Q}_{\mathsf{sc}} \mid \mathsf{F}^{\mathsf{sc}}$

$\boxed{\psi}$

Fig. 3. The Effect of Quiescence for Each Access Mode

for $\mathsf{Q}^{\mathsf{L}x}_{\mathsf{acq}}$ in the independent case for an acquiring write; this ensures that all subsequent accesses follow the acquiring read in top-level pomsets.

Fig. 3 shows the effect of quiescence for each access mode.

Example A.5. The definition enforces publication. Consider:

$x := 1$

$\boxed{\psi[1/x][\mathsf{ff}/\mathsf{Q}^x_{\mathsf{wo}}]}$

$1{=}v \land \mathsf{Q}^x_{\mathsf{ro}} \land \mathsf{Q}^x_{\mathsf{wo}} \mid \mathsf{W}\,x\,v$

$\boxed{\psi[1/x]}$

$x^{\mathsf{rel}} := 1$

$\boxed{\psi[1/y][\mathsf{ff}/\mathsf{Q}^x_{\mathsf{wo}}]}$

$1{=}v \land \mathsf{Q}^*_{\mathsf{ro}} \land \mathsf{Q}^*_{\mathsf{wo}} \mid \mathsf{W}^{\mathsf{rel}}\,x\,v$

$\boxed{\psi[1/y]}$

Since $\mathsf{Q}^*_{\mathsf{wo}}[\mathsf{ff}/\mathsf{Q}^x_{\mathsf{wo}}]$ is ff, we must introduce order to get a satisfiable precondition for $(\mathsf{W}\,y\,1)$.

Example A.6. The definition enforces subscription. Consider:

$r := y^{\mathsf{acq}}$

$\boxed{(1{=}r \lor y{=}r) \Rightarrow \psi[\mathsf{ff}/\mathsf{Q}^*_{\mathsf{ro}}][\mathsf{ff}/\mathsf{Q}^*_{\mathsf{wo}}]}$

$\mathsf{Q}^y_{\mathsf{wo}} \mid \mathsf{R}^{\mathsf{acq}}\,y\,v$

$\boxed{v{=}r \Rightarrow \psi}$

$r := x$

$\boxed{(1{=}r \lor x{=}r) \Rightarrow \psi[\mathsf{ff}/\mathsf{Q}^x_{\mathsf{ro}}]}$

$\mathsf{Q}^x_{\mathsf{wo}} \mid \mathsf{R}\,x\,v$

$\boxed{v{=}r \Rightarrow \psi}$

Since $\mathsf{Q}^x_{\mathsf{wo}}[\mathsf{ff}/\mathsf{Q}^*_{\mathsf{wo}}]$ is ff, we must introduce order to get a satisfiable precondition for $(\mathsf{W}\,y\,1)$.

Example A.7. Even in its logical form, s6b′ is incompatible with the ability to strengthen preconditions using augment closure, which is allowed in [Jagadeesan et al. 2020]. Consider the following.

$\mathtt{if}(r)\{x := 2\}$ $\quad$ $x := 1$ $\quad$ $x := 2$ $\quad$ $\mathtt{if}(!r)\{x := 1\}$

$r{\neq}0 \mid \mathsf{W}\,x\,2$ $\quad$ $\mathsf{W}\,x\,1$ $\quad$ $\mathsf{W}\,x\,2$ $\quad$ $r{=}0 \mid \mathsf{W}\,x\,1$

If $r{=}0$ then x is 1, 2, 1. If $r{\neq}0$ then x is 2, 1, 2. Augmenting the middle preconditions and then using sequential composition, we have:

$$\begin{array}{ccc} \texttt{if}(r)\{x := 2\} & x := 1;\ x := 2 & \texttt{if}(!r)\{x := 1\} \\ \boxed{r{\neq}0 \mid \mathsf{W}x2} & \boxed{r{\neq}0 \mid \mathsf{W}x1}\ \ \boxed{r{=}0 \mid \mathsf{W}x2} & \boxed{r{=}0 \mid \mathsf{W}x1} \end{array}$$

Note that s6b′ does not require any order between the two writes of the middle pomset. Merging left and right, we have:

$$\texttt{if}(r)\{x := 2\};\ x := 1;\ x := 2;\ \texttt{if}(!r)\{x := 1\}$$
$$\boxed{\mathsf{W}x2} \rightarrow \boxed{\mathsf{W}x1}$$

As shown by the following single-threaded code, allowing this outcome would violate DRF-SC.

$$y := 1;\ r := y;\ \texttt{if}(r)\{x := 2\};\ x := 1;\ x := 2;\ \texttt{if}(!r)\{x := 1\}$$
$$\boxed{\mathsf{W}y1} \rightarrow \boxed{\mathsf{R}y1} \quad \boxed{\mathsf{W}x2} \rightarrow \boxed{\mathsf{W}x1}$$

This is one reason that we use *weakest* preconditions, rather than preconditions.

The same problem does not occur due to if-closure:

$$\begin{array}{ccc} \texttt{if}(r)\{x := 2\} & x := 1;\ x := 2 & \texttt{if}(!r)\{x := 1\} \\ \boxed{r{\neq}0 \mid \mathsf{W}x2} & \boxed{r{\neq}0 \mid \mathsf{W}x1}\ \ \boxed{r{=}0 \mid \mathsf{W}x2} & \boxed{r{=}0 \mid \mathsf{W}x1} \\ & \boxed{r{=}0 \mid \mathsf{W}x1}\ \ \boxed{r{\neq}0 \mid \mathsf{W}x2} & \end{array}$$

Merging left and right, we have

$$\texttt{if}(r)\{x := 2\};\ x := 1;\ x := 2;\ \texttt{if}(!r)\{x := 1\}$$
$$\boxed{\mathsf{W}x2} \rightleftarrows \boxed{r{=}0 \mid \mathsf{W}x1} \quad \boxed{r{\neq}0 \mid \mathsf{W}x2} \rightleftarrows \boxed{\mathsf{W}x1}$$

A.8 Is Coherence/Delay Compatible with If-closure and Dead-Write-Removal?

This paper has a "High-level abstraction for efficient computation"

With if-closure, the following equation should hold:

$$\begin{aligned} &[\![\texttt{if}(r)\{x := 2\};\ x := 1;\ x := 2;\ \texttt{if}(!r)\{x := 1\};\ x := 3]\!] \\ =&[\![\texttt{if}(!r)\{x := 1\};\ x := 2;\ x := 1;\ \texttt{if}(r)\{x := 2\};\ x := 3]\!] \end{aligned}$$

Using dead write removal, these can be refined, respectively, to:

$$\begin{aligned} &[\![x := 1;\ x := 2;\ x := 3]\!] \\ \neq&[\![x := 2;\ x := 1;\ x := 3]\!] \end{aligned}$$

What has become of coherence?

B LOWERING PwT-MCA TO ARM

For simplicity, we restrict to top-level parallel composition.

B.1 Arm executions

Our description of Arm8 follows Alglave et al. [2021], adapting the notation to our setting.

Definition B.1. An *Arm8 execution graph*, G, is tuple $(E, \lambda, \mathsf{poloc}, \mathsf{lob})$ such that

(A1) $E \subseteq \mathcal{E}$ is a set of events,

(A2) $\lambda : E \rightarrow \mathcal{A}$ defines a label for each event,

(A3) $\mathsf{poloc} \subseteq E{\times}E$, is a per-thread, per-location total order, capturing *per-location program order*,

(A4) lob $\subseteq E \times E$, is a per-thread partial order capturing *locally-ordered-before*, such that
  (A4a) poloc $\cup$ lob is acyclic.

The definition of lob is complex. Comparing with our definition of sequential composition, it is sufficient to note that lob includes

(L1) read-write dependencies, required by S3,
(L2) synchronization delay of $\ltimes_{\mathsf{sync}}$, required by S6a,
(L3) sc access delay of $\bowtie_{\mathsf{sc}}$, required by S6a,
(L4) write-write and read-to-write coherence delay of $\bowtie_{\mathsf{co}}$, required by S6a,

and that lob does *not* include

(L5) read-read control dependencies, required by S3,
(L6) write-to-read order of rf, required by M7c,
(L7) write-to-read coherence delay of $\bowtie_{\mathsf{co}}$, required by S6a.

Definition B.2. Execution G is (co, rf, gcb)-*valid*, under *External Global Consistency* (EGC) if

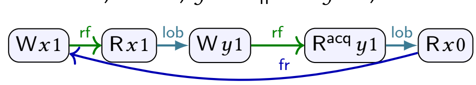
(A5) co $\subseteq E \times E$, is a per-location total order on writes, capturing *coherence*,
(A6) rf $\subseteq E \times E$, is a relation, capturing *reads-from*, such that
  (A6a) rf is surjective and injective relation on $\{e \in E \mid \lambda(e)$ is a read$\}$,
  (A6b) if $d \xrightarrow{\mathsf{rf}} e$ then $\lambda(d)$ matches $\lambda(e)$,
  (A6c) poloc $\cup$ co $\cup$ rf $\cup$ fr is acyclic, where $e \xrightarrow{\mathsf{fr}} c$ if $e \xleftarrow{\mathsf{rf}} d \xrightarrow{\mathsf{co}} c$, for some d,
(A7) gcb $\supseteq$ (co $\cup$ rf) is a linear order such that
  (A7a) if $d \xrightarrow{\mathsf{rf}} e$ and $\lambda(c)$ blocks $\lambda(e)$ then either $c \xrightarrow{\mathsf{gcb}} d$ or $e \xrightarrow{\mathsf{gcb}} c$,
  (A7b) if $e \xrightarrow{\mathsf{lob}} c$ then either $e \xrightarrow{\mathsf{gcb}} c$ or $(\exists d)\ d \xrightarrow{\mathsf{rf}} e$ and $d \xrightarrow{\mathsf{poloc}} e$ but not $d \xrightarrow{\mathsf{lob}} c$.

Execution G is (co, rf, cb)-*valid* under *External Consistency* (EC) if

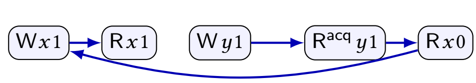
(A5) and (A6), as for EGC,
(A8) cb $\supseteq$ (co $\cup$ lob) is a linear order such that if $d \xrightarrow{\mathsf{rf}} e$ then either
  (A8a) $d \xrightarrow{\mathsf{cb}} e$ and if $\lambda(c)$ blocks $\lambda(e)$ then either $c \xrightarrow{\mathsf{cb}} d$ or $e \xrightarrow{\mathsf{cb}} c$, or
  (A8b) $d \xleftarrow{\mathsf{cb}} e$ and $d \xrightarrow{\mathsf{poloc}} e$ and $(\nexists c)\ \lambda(c)$ blocks $\lambda(e)$ and $d \xrightarrow{\mathsf{poloc}} c \xrightarrow{\mathsf{poloc}} e$.

Alglave et al. [2021] show that EGC and EC are both equivalent to the standard definition of Arm8. They explain EGC and EC using the following example, which is allowed by Arm8.[8]

$$x := 1;\ r := x;\ y := r \parallel 1 := y^{\mathsf{acq}};\ s := x$$

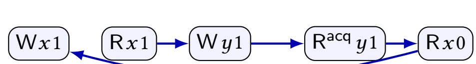


EGC drops lob-order in the first thread using A7b, since (Wx1) is not lob-ordered before (Wy1).



(gcb)

EC drops rf-order in the first thread using A8b.



(cb)

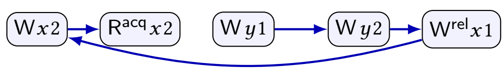
[8] We have changed an address dependency in the first thread to a data dependency.

B.2 Lowering PwT-MCA1 to Arm

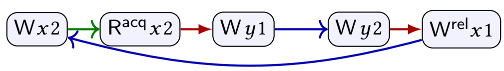
The optimal lowering for Arm8 is unsound for PwT-MCA$_1$. The optimal lowering maps relaxed access to `ldr`/`str` and non-relaxed access to `ldar`/`stlr` [Podkopaev et al. 2019]. In this section, we consider a suboptimal strategy, which lowers non-relaxed reads to (`dmb.sy; ldar`). Significantly, we retain the optimal lowering for relaxed access. In the next section we recover the optimal lowering by adopting an alternative semantics for M7c and S6a.

To see why the optimal lowering fails, consider the following attempted execution, where the final values of both x and y are 2.

$$x := 2;\ r := x^{\mathsf{acq}};\ y := r{-}1 \parallel y := 2;\ x^{\mathsf{rel}} := 1$$



(gcb)

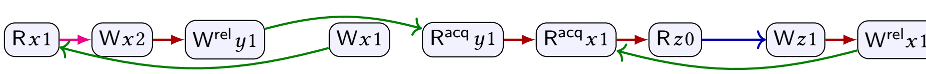


(<)

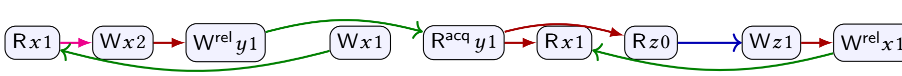
This attempted execution is allowed by Arm8, but disallowed by our semantics.

If the read of x in the execution above is changed from acquiring to relaxed, then our semantics allows the gcb execution, using the independent case for the read and satisfying the precondition of (Wy1) by prepending (Wx2). It may be tempting, therefore, to adopt a strategy of *downgrading* acquires in certain cases. Unfortunately, it is not possible to do this locally without invalidating important idioms such as publication. For example, consider that (R$^{\mathsf{ra}}x$1) is *not* possible for the second thread in the following attempted execution, due to publication of (Wx2) via y:

$$x := x+1;\ y^{\mathsf{rel}} := 1 \parallel x := 1;\ \mathtt{if}(y^{\mathsf{acq}}\ \&\&\ x^{\mathsf{acq}})\{s := z\} \parallel z := 1;\ x^{\mathsf{rel}} := 1$$



Instead, if the read of x is relaxed, then the publication via y fails, and (Rx1) in the second thread is possible.



Using the suboptimal lowering for acquiring reads, our semantics is sound for Arm. The proof uses the characterization of Arm using EGC.

Theorem B.3. *Suppose G_1 is $(\mathsf{co}_1, \mathsf{rf}_1, \mathsf{gcb}_1)$-valid for S under the suboptimal lowering that maps non-relaxed reads to* (`dmb.sy; ldar`). *Then there is a top-level pomset $P_2 \in [\![S]\!]$ such that $E_2 = E_1$, $\lambda_2 = \lambda_1$, $\mathsf{rf}_2 = \mathsf{rf}_1$, and $\leq_2 = \mathsf{gcb}_1$.*

Proof. First, we establish some lemmas about Arm8.

Lemma B.4. *Suppose G is $(\mathsf{co}, \mathsf{rf}, \mathsf{gcb})$-valid. Then $\mathsf{gcb} \supseteq \mathsf{fr}$.*

Proof. Using the definition of fr from A6c, we have $e \xleftarrow{\mathsf{rf}} d \xrightarrow{\mathsf{co}} c$, and therefore $\lambda(c)$ blocks $\lambda(e)$. Applying A7a, we have that either $c \xrightarrow{\mathsf{gcb}} d$ or $e \xrightarrow{\mathsf{gcb}} c$. Since gcb includes co, we have $d \xrightarrow{\mathsf{gcb}} c$, and therefore it must be that $e \xrightarrow{\mathsf{gcb}} c$. ◻

Lemma B.5. *Suppose G is $(\mathsf{co}, \mathsf{rf}, \mathsf{gcb})$-valid and $c \xrightarrow{\mathsf{poloc}} e$, where $\lambda(c)$ blocks $\lambda(e)$. Then $c \xrightarrow{\mathsf{gcb}} e$.*

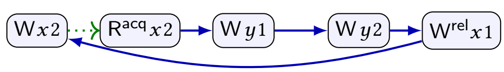
Proof. By way of contradiction, assume $e \xrightarrow{\mathsf{gcb}} c$. If $c \xrightarrow{\mathsf{rf}} e$ then by A7 we must also have $c \xrightarrow{\mathsf{gcb}} e$, contradicting the assumption that gcb is a total order. Otherwise that there is some $d \neq c$ such that $d \xrightarrow{\mathsf{rf}} e$, and therefore $d \xrightarrow{\mathsf{gcb}} e$. By transitivity, $d \xrightarrow{\mathsf{gcb}} c$. By the definition of fr, we have $e \xrightarrow{\mathsf{fr}} c$. But this contradicts A6c, since $c \xrightarrow{\mathsf{poloc}} e$. ◻

We show that all the order required in the pomset is also required by Arm8. M7b holds since cb_1 is consistent with co_1 and fr_1. As noted above, lob includes the order required by s3 and s6a. We need only show that the order removed from A7b can also be removed from the pomset. In order for A7b to remove order from e to c, we must have $d \xrightarrow{\mathsf{rf}} e$ and $d \xrightarrow{\mathsf{poloc}} e$ but not $d \xrightarrow{\mathsf{lob}} c$. Because of our suboptimal lowering, it must be that e is a relaxed read; otherwise the `dmb.sy` would require $d \xrightarrow{\mathsf{lob}} c$. Thus we know that s6a does not require order from e to c. By chaining R4b and W4, any dependence on the read can by satisfied without introducing order in s3. □

B.3 Lowering PwT-MCA2 to Arm

We can achieve optimal lowering for Arm by weakening the semantics of sequential composition slightly. In particular, we must lose M7c, which states that $d \xrightarrow{\mathsf{rf}} e$ implies $d < e$. Revisiting the example in the last subsection, we essentially mimic the EC characterization:

$$x := 2;\ r := x^{\mathsf{acq}};\ y := r{-}1 \parallel y := 2;\ x^{\mathsf{rel}} := 1$$



(cb)

Here the rf relation *contradicts* order! We have both $(\mathsf{W}x2) \dashrightarrow (\mathsf{R}^{\mathsf{acq}}x2)$ and $(\mathsf{W}x2) \xleftarrow{\mathsf{cb}} (\mathsf{R}^{\mathsf{acq}}x2)$.

We first show that EC-validity is unchanged if we assume $\mathsf{cb} \supseteq \mathsf{fr}$:

LEMMA B.6. *Suppose G is EC-valid via $(\mathsf{co}, \mathsf{rf}, \mathsf{cb})$. Then there a permutation cb' of cb such that G is EC-valid via $(\mathsf{co}, \mathsf{rf}, \mathsf{cb}')$ and $\mathsf{cb}' \supseteq \mathsf{fr}$, where fr is defined in A6c.*

PROOF. Suppose $e \xrightarrow{\mathsf{fr}} c$. By definition of fr, $e \xleftarrow{\mathsf{rf}} d \xrightarrow{\mathsf{co}} c$, for some d. We show that either (1) $e \xrightarrow{\mathsf{cb}} c$, or (2) $c \xrightarrow{\mathsf{cb}} e$ and we can reverse the order in cb' to satisfy the requirements.

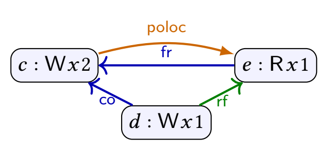
If A8a applies to $d \xrightarrow{\mathsf{rf}} e$, then $e \xrightarrow{\mathsf{cb}} c$, since it cannot be that $c \xrightarrow{\mathsf{co}} d$.

Suppose A8b applies to $d \xrightarrow{\mathsf{rf}} e$ and c is from a different thread than e. Because it is a different thread, we cannot have $e \xrightarrow{\mathsf{lob}} c$, and therefore we can choose $c \xrightarrow{\mathsf{cb}} e$ in cb'.

Suppose A8b applies to $d \xrightarrow{\mathsf{rf}} e$ and c is from the same thread as e. Applying A6c to $e \xrightarrow{\mathsf{fr}} c$, it cannot be that $c \xrightarrow{\mathsf{poloc}} e$. Since poloc is a per-thread-and-per-location total order, it must be that $e \xrightarrow{\mathsf{poloc}} c$. Applying A4a, we cannot have $e \xrightarrow{\mathsf{lob}} c$, and therefore we can choose $c \xrightarrow{\mathsf{cb}} e$ in cb'. □

Here is a contradictory non-example illustrating the last case of the proof:

$$x := 2;\ r := x \parallel x := 1$$



THEOREM B.7. *Suppose G_1 is EC-valid for S via $(\mathsf{co}_1, \mathsf{rf}_1, \mathsf{cb}_1)$ and that $\mathsf{cb}_1 \supseteq \mathsf{fr}_1$. Then there is a top-level pomset $P_2 \in [\![S]\!]$ such that $E_2 = E_1$, $\lambda_2 = \lambda_1$, $\mathsf{rf}_2 = \mathsf{rf}_1$, and $\leq_2 = \mathsf{cb}_1$.*

PROOF. We show that all the order required in the pomset is also required by Arm8. M7b holds since cb_1 is consistent with co_1 and fr_1. s6b follows from A8b. As noted above, lob includes the order required by s3 and s6a. □

C LDRF-SC FOR PwT-MCA

In this appendix, we establish a DRF-SC for PwT-MCA$_2$. We prove an *external* result, where the notion of *data-race* is independent of the semantics itself. Since every PwT-MCA$_2$ is also a PwT-MCA$_1$, the result also applies there. Our result is also *local*. Using Dolan et al.'s [2018] notion of *Local Data Race Freedom (LDRF)*.

We do not address PwT-C11. The internal DRF-SC result for C11 [Batty 2015] does not rely on dependencies and thus applies to PwT-C11. In internal DRF-SC, data-races are defined using the semantics of the language itself. Using the notion of dependency defined here, it should be possible to prove an stronger external result for c11, similar to that of [Lahav et al. 2017]—we leave this as future work.

Jagadeesan et al. [2020] prove LDRF-SC for Pomsets with Preconditions (PwP). PwT-MCA generalizes PwP to account for sequential composition. Most of the machinery of LDRF-SC, however, has little to do with sequential semantics. Thus, we have borrowed heavily from the text of [Jagadeesan et al. 2020]; indeed, we have copied directly from the LaTeX source, which is publicly available. We indicate substantial changes or additions using a change-bar on the right.

There are several changes:

- PwP imposes several conditions that we have dropped: *consistency*, *causal strengthening*, *downset closure* (see §A.2).
- PwP allows preconditions that are stronger than the weakest precondition.
- PwP imposes M7c (rf implies $<$) and thus is similar to PwT-MCA$_1$. PwT-MCA$_2$ is a weaker model that is new to this paper.
- PwP did not provide an accurate account of program order for merged actions. We use Lemma 7.2 to correct this deficiency.

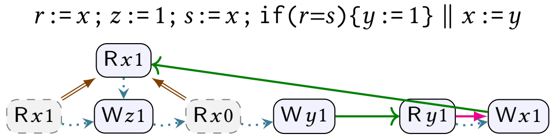
The first two items require us to define gen differently, below.

The result requires that locations are properly initialized. We assume a sufficient condition: that programs have the form "$x_1 := v_1 ; \cdots x_n := v_n ; S$" where every location mentioned in S is some x_i. To simplify the definition of *happens-before*, we ban fences and RMWs.

To state the theorem, we require several technical definitions. The reader unfamiliar with [Dolan et al. 2018] may prefer to skip to the examples in the proof sketch, referring back as needed.

Program Order. Let $[\![\cdot]\!]^{\mathsf{po}}_{\mathsf{mca2}}$ be defined by applying the construction of Lemma 7.2 to $[\![\cdot]\!]_{\mathsf{mca2}}$. We consider only *complete* pomsets. For these, we derive program order on compound events as follows. By Lemma 7.4, if there is a compound event e, then there is a phantom event $c \in \pi^{-1}(e)$ such that $\kappa(c)$ is a tautology. If there is exactly one tautology, we identify e with c in program order. If there is more than one tautology, Lemma C.1, below, shows that it suffices to pick an arbitrary one—we identify e with the $c \in \pi^{-1}(e)$ that is minimal in program order. For example, consider JMM causality test case 2, with an added write to z:

$$r := x ; z := 1 ; s := x ; \texttt{if}(r{=}s)\{y := 1\} \parallel x := y$$



(‡‡)

Data Race. Data races are defined using *program* order (po), not *pomset* order ($<$).

Because we ban fences and RMWs, we can adopt the simplest definition of *synchronizes-with* (sw): Let $d \xrightarrow{\mathsf{sw}} e$ exactly when d fulfills e, d is a release, e is an acquire, and $\neg(d \xrightarrow{\mathsf{po}} e)$.

Let $\mathsf{hb} = (\mathsf{po} \cup \mathsf{sw})^+$ be the *happens-before* relation.

Let $L \subseteq \mathcal{X}$ be a set of locations. We say that d *has an L-race with* e (notation $d \overset{L}{\rightsquigarrow} e$) when (1) at least one is relaxed, (2) at least one is a write, (3) they access the same location in L, and (4) they are unordered by hb: neither $d \xrightarrow{\mathsf{hb}} e$ nor $e \xrightarrow{\mathsf{hb}} d$.

Generators. We say that $P' \in \nabla(\mathcal{P})$ if there is some $P \in \mathcal{P}$ such that P is *complete* (Def. 5.1) and P' is a *downset* of P (Def. A.2).

Let P be *augmentation-minimal* in $\mathcal{P}$ if $P \in \mathcal{P}$ and there is no $P{\neq}P'{\in}\mathcal{P}$ such that P augments P'.

Let $\mathrm{gen}[\![S]\!] = \{P \in \nabla[\![S]\!]^{\mathsf{po}}_{\mathsf{mca2}} \mid P \text{ is augmentation-minimal in } \nabla[\![S]\!]^{\mathsf{po}}_{\mathsf{mca2}}\}$.

Extensions. We say that P' *S-extends* P if $P \neq P' \in \mathrm{gen}[\![S]\!]$ and P is a downset of P'.

Similarity. We say that P' *is e-similar to P* if they differ at most in (1) pomset order adjacent to e, (2) the value associated with event e, if it is a read, and (3) the addition and removal of read events po-after e.

Stability. We say that P is *L-stable in S* if (1) $P \in \text{gen}[\![S]\!]$, (2) P is po-convex (nothing missing in program order), (3) there is no S-extension of P with a *crossing* L-race: that is, there is no $d \in E$, no P' S-extending P, and no $e \in E' \setminus E$ such that $d \overset{L}{\rightsquigarrow} e$. The empty pomset is L-stable.

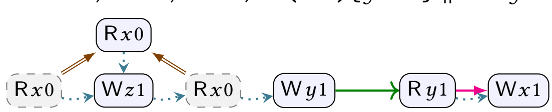
Sequentiality. Let $\lessdot_L = <_L \cup \text{po}$, where $<_L$ is the restriction of $<$ to events that access locations in L. We say that P' is *L-sequential after P* if (1) P' is po-convex, (2) $\lessdot_L$ is acyclic in $E' \setminus E$.

Simplicity. We say that P' is *L-simple after P* if all of the events in $E' \setminus E$ that access locations in L are *simple* (Def. 7.1).

Lemma C.1. *Suppose $P' \in gen[\![S]\!]$ and P is L-sequential after P. Let P'' be the restriction of P' that is L-simple after P (throwing out compound L-events after P). Then $P'' \in gen[\![S]\!]$.*

As a negative example, note that (‡‡) is not L-sequential—in fact there is no execution of the program that results in the simple events of (‡‡): without merging the reads, there would be a dependency $(\mathsf{R}x1) \rightarrow (\mathsf{W}y1)$. L-sequential executions of this code must read 0 for x:

$$r := x\,;\, z := 1\,;\, s := x\,;\, \texttt{if}(r{=}s)\{y := 1\} \parallel x := y$$



Theorem C.2. *Let P be L-stable in S. Let P' be a S-extension of P that is L-sequential after P. Let P'' be a S-extension of P' that is po-convex, such that no subset of E'' satisfies these criteria. Then either (1) P'' is L-sequential and L-simple after P or (2) there is some S-extension P''' of P' and some $e \in (E'' \setminus E')$ such that (a) P''' is e-similar to P'', (b) P''' is L-sequential and L-simple after P, and (c) $d \overset{L}{\rightsquigarrow} e$, for some $d \in (E'' \setminus E)$.*

The theorem provides an inductive characterization of *Sequential Consistency for Local Data-Race Freedom (SC-LDRF)*: Any extension of a L-stable pomset is either L-sequential, or is e-similar to a L-sequential extension that includes a race involving e.

Proof Sketch. We show L-sequentiality. L-simplicity then follows from Lemma C.1.

In order to develop a technique to find P''' from P'', we analyze pomset order in generation-minimal top-level pomsets. First, we note that $<_*$ (the transitive reduction $<$) can be decomposed into three disjoint relations. Let ppo $= (<_* \cap \text{po})$ denote *preserved* program order, as required by sequential composition and conditional. The other two relations are cross-thread subsets of $(<_* \setminus \text{po})$: rfe (reads-from-external) orders writes before reads, satisfying P6; cae (coherence-after-external) orders read and write accesses before writes, satisfying M7b. (Within a thread, S6 induces order that is included in ppo.)

Using this decomposition, we can show the following.

Lemma C.3. *Suppose $P'' \in gen[\![S]\!]$ has an external read $d \xrightarrow{\text{rf}''} e$ that is maximal in (ppo ∪ rfe). Further suppose that there another write d' that could fulfill e. Then there exists an e-similar P''' with $d' \xrightarrow{\text{rf}'''} e$ such that $P''' \in gen[\![S]\!]$.*

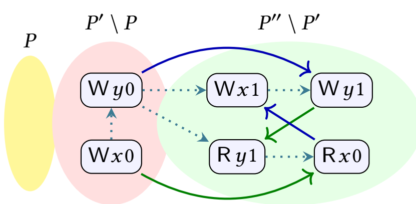
The proof of the lemma follows an inductive construction of gen$[\![S]\!]$, starting from a large set with little order, and pruning the set as order is added: We begin with all pomsets generated by the semantics without imposing the requirements of fulfillment (including only ppo). We then prune reads which cannot be fulfilled, starting with those that are minimally ordered.

We can prove a similar result for (po ∪ rfe)-maximal read and write accesses.

Turning to the proof of the theorem, if P'' is L-sequential after P, then the result follows from (1). Otherwise, there must be a $\lessdot_L$ cycle in P'' involving all of the actions in $(E'' \setminus E')$: If there were no such cycle, then P'' would be L-sequential; if there were elements outside the cycle, then there would be a subset of E'' that satisfies these criteria.

If there is a (po ∪ rfe)-maximal access, we select one of these as e. If e is a write, we reverse the outgoing order in cae; the ability to reverse this order witnesses the race. If e is a read, we switch its fulfilling write to a "newer" one, updating cae; the ability to switch witnesses the race. For example, for P'' on the left below, we choose the P''' on the right; e is the read of x, which races with $(\mathsf{W}x1)$.

$$x := 0;\ y := 0;\ (x := 1;\ y := 1 \parallel \mathtt{if}(y)\{r := x\})$$

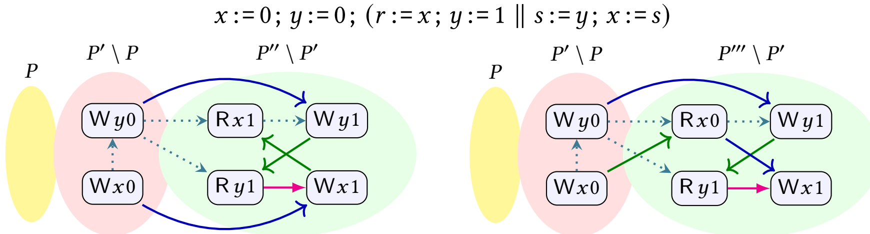


It is important that e be (po ∪ rfe)-maximal, not just (ppo ∪ rfe)-maximal. The latter criterion would allow us to choose e to be the read of y, but then there would be no e-similar pomset: if an execution reads 0 for y then there is no read of x, due to the conditional.

In the above argument, it is unimportant whether e reads-from an internal or an external write; thus the argument applies to PwT-MCA$_2$ and PwT-MCA$_1$ as it does for PwT-MCA$_1$.

If there is no (po∪rfe)-maximal access, then all cross-thread order must be from rfe. In this case, we select a (ppo ∪ rfe)-maximal read, switching its fulfilling write to an "older" one. If there are several of these, we choose one that is po-minimal. As an example, consider the following; once again, e is the read of x, which races with $(\mathsf{W}x1)$.

$$x := 0;\ y := 0;\ (r := x;\ y := 1 \parallel s := y;\ x := s)$$



This example requires $(\mathsf{W}x0)$. Proper initialization ensures the existence of such "older" writes. □

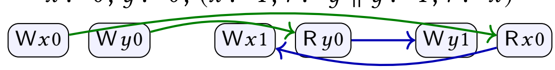
D PwT-MCA: ADDITIONAL EXAMPLES

This appendix includes additional examples. They all apply equally to PwT-MCA$_1$ and PwT-MCA$_2$. Many of these are taken directly from [Jagadeesan et al. 2020]; see there for further discussion.

D.1 Buffering

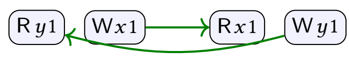
Store buffering is allowed.

$$x := 0;\ y := 0;\ (x := 1;\ r := y \parallel y := 1;\ r := x) \tag{SB}$$



Load buffering is allowed.

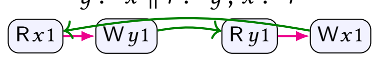
$$r := y;\ x := 1 \parallel r := x;\ y := 1 \tag{LB}$$



D.2 Thin-Air

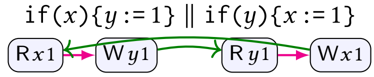
Thin air is disallowed. [Pugh 2004, TC4]:

$$y := x \parallel r := y;\ x := r \tag{OOTA1}$$



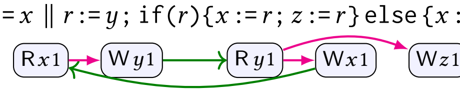
Control variant:

$$\texttt{if}(x)\{y := 1\} \parallel \texttt{if}(y)\{x := 1\} \tag{OOTA2}$$



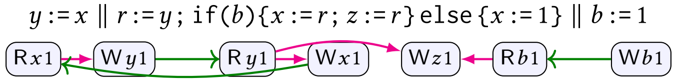
[Jagadeesan et al. 2020, §2]

$$y := x \parallel r := y;\ \texttt{if}(r)\{x := r;\ z := r\}\,\texttt{else}\,\{x := 2\} \tag{OOTA3}$$



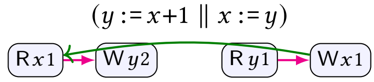
[Jeffrey and Riely 2019, §8] and [Jagadeesan et al. 2020, §6]:

$$y := x \parallel r := y;\ \texttt{if}(b)\{x := r;\ z := r\}\,\texttt{else}\,\{x := 1\} \parallel b := 1 \tag{OOTA4}$$



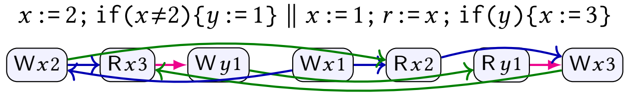
[Svendsen et al. 2018] is disallowed since there is no write to fulfill (Ry1).

$$(y := x{+}1 \parallel x := y) \tag{OOTA6}$$



[Chakraborty and Vafeiadis 2019, Fig. 3]:

$$x := 2;\ \texttt{if}(x{\neq}2)\{y := 1\} \parallel x := 1;\ r := x;\ \texttt{if}(y)\{x := 3\} \tag{OOTA7}$$



[Jagadeesan et al. 2020, §6]:

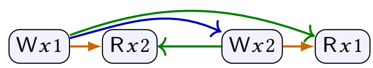
> Boehm's [2018] RFUB example presents another potential form of OOTA behavior. Our analysis shows that there is no OOTA behavior in RFUB, only a false dependency:
>
> $$[\![r := y;\ x := r]\!] \not\supseteq [\![r := y;\ \texttt{if}(r{\neq}1)\{z := 1;\ r := 1\};\ x := r]\!] \tag{RFUB}$$
>
> The left command is half of OOTA3 (). The right command is dubbed RFUB, for *Register assignment From an Unexecuted Branch*. Boehm observes that in the context $x := y \parallel [-]$, these programs have different behaviors. Yet the OOTA example on the left never writes 1. Why should the unexecuted branch change that? Because of the conditional, the write to x in RFUB is independent of the read from y. It useful to considering the Hoare logic formulas satisfied by the two threads above: we have $\{\mathrm{tt}\}$ RFUB $\{x = 1\}$ for the right thread of RFUB, but not $\{\mathrm{tt}\}$ OOTA3 $\{x = 1\}$ for the

right thread of OOTA3. The change in the thread from OOTA3 to RFUB is not a valid refinement under Hoare logic; thus, it is expected that RFUB may have additional behaviors.

D.3 Coherence

The following execution is disallowed by fulfillment (M7a and M7b).

$$x := 1;\ r := x \parallel x := 2;\ s := x$$

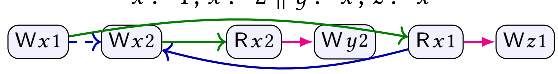


(COH)

M7b requires that we order one write with respect to the other, either before the write or after the read (and therefore after the write). Suppose we pick 1 before 2, as shown. This satisfies M7b for (Rx2). But to satisfy the requirement for (Rx1) we must have either (Wx2) $<$ (Wx1) or (Rx1) $<$ (Wx2). Either way, we have a cycle.

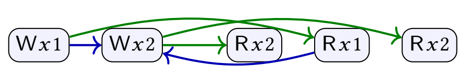
We allow the following execution, which is disallowed by C11:

$$x := 1;\ x := 2 \parallel y := x;\ z := x$$



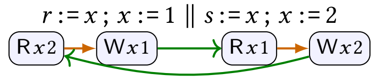
As another example in this vein:

$$x := 1;\ x := 2 \parallel r_1 := x;\ r_2 := x;\ r_3 := x;$$



Our model is more coherent than Java, which permits the following:

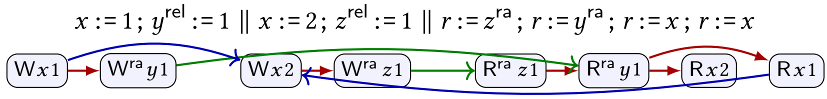
$$r := x;\ x := 1 \parallel s := x;\ x := 2$$



(TC16)

We also forbid the following, which Java allows:

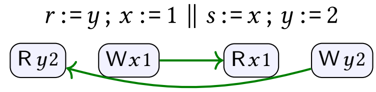
$$x := 1;\ y^{\mathsf{rel}} := 1 \parallel x := 2;\ z^{\mathsf{rel}} := 1 \parallel r := z^{\mathsf{ra}};\ r := y^{\mathsf{ra}};\ r := x;\ r := x$$



(CO3)

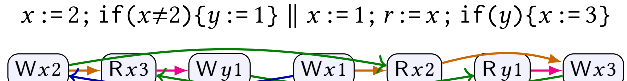
[Dolan et al. 2018] disallows TC16, as well as the one below (due to read-to-write ordering). We allow this execution:

$$r := y;\ x := 1 \parallel s := x;\ y := 2$$



The following outcome is allowed by the promising semantics [Kang et al. 2017], but not in WEAKESTMO [Chakraborty and Vafeiadis 2019, Fig. 3] nor in our semantics, due to the cycle:

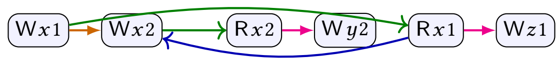
$$x := 2;\ \mathtt{if}(x{\neq}2)\{y := 1\} \parallel x := 1;\ r := x;\ \mathtt{if}(y)\{x := 3\}$$



(COH-CYC)

Since reads are not ordered by intra-thread coherence, we allow the following unintuitive behavior. C11 includes read-read coherence between relaxed atomics in order to forbid this:

$$x := 1;\ x := 2 \parallel y := x;\ z := x$$



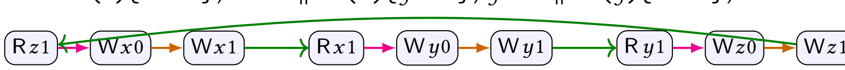
(co2)

Here, the reader sees 2 then 1, although they are written in the reverse order. This behavior is allowed by Java in order to validate CSE without requiring aliasing analysis.

D.4 MCA

Here are a few litmus tests that distinguish MCA architectures from non-MCA architectures. MCA1 is an example of *write subsumption* [Pulte et al. 2018, §3]:

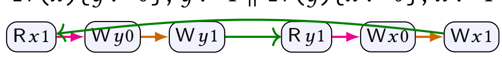
$$\texttt{if}(z)\{x := 0\};\ x := 1 \parallel \texttt{if}(x)\{y := 0\};\ y := 1 \parallel \texttt{if}(y)\{z := 0\};\ z := 1$$



(MCA1)

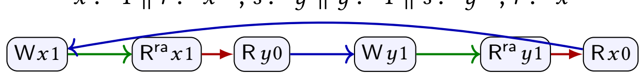
Two thread variant:

$$\texttt{if}(x)\{y := 0\};\ y := 1 \parallel \texttt{if}(y)\{x := 0\};\ x := 1$$



IRIW is allowed if all accesses are relaxed, but not if the initial reads are acquiring:

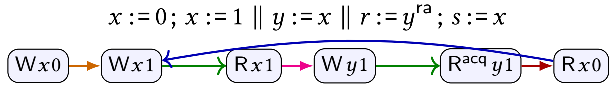
$$x := 1 \parallel r := x^{\mathsf{ra}};\ s := y \parallel y := 1 \parallel s := y^{\mathsf{ra}};\ r := x$$



(IRIW)

MCA2 is a simplified version of IRIW

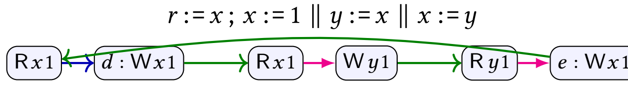
$$x := 0;\ x := 1 \parallel y := x \parallel r := y^{\mathsf{ra}};\ s := x$$



(MCA2)

[Flur et al. 2016] and [Lahav and Vafeiadis 2016, Fig. 4]:

$$r := x;\ x := 1 \parallel y := x \parallel x := y$$



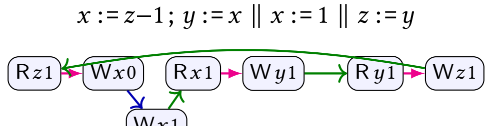
(MCA3)

These candidate executions are invalid, due to cycles.

D.5 Detour

The following example [Podkopaev et al. 2019, Ex. 3.7] is disallowed by IMM by including a detour relation. It is also disallowed by PS.

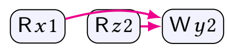
$$x := z{-}1;\ y := x \parallel x := 1 \parallel z := y$$



D.6 Read-Read Coherence Versus CSE

Pugh [1999, §2.3] presented the following example to show that Java's original memory model required alias analysis to validate common subexpression elimination (CSE).

$$r_1 := x\,;\ r_2 := z\,;\ r_3 := x\,;\ \mathtt{if}(r_3{\leqslant}1)\{y = r_2\}$$



Coalescing the two read of x is obviously allowed if $z{\neq}x$. But if $z{=}x$, coalescing is only permitted because we do not include read-read pairs in $\bowtie_{\mathsf{co}}$ (§4.2):

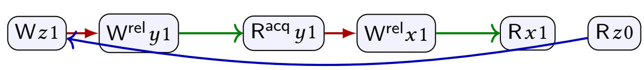
$$\bowtie_{\mathsf{co}} = \{(\mathsf{W}x, \mathsf{W}x),\ (\mathsf{R}x, \mathsf{W}x),\ (\mathsf{W}x, \mathsf{R}x)\}$$

C11 has read-read coherence, and therefore CSE is only valid up to alias analysis in C11.

D.7 Read-Read Dependencies and Java Final Field Semantics Versus If-Closure

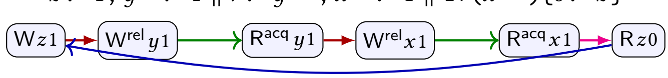
One might worry that the lack of read-read dependencies could cause DRF-SC to fail. For example, the following execution has a control dependency between the reads of the last thread, but this order is not enforced, neither by our model, nor Arm8.

$$z := 1\,;\ y^{\mathsf{rel}} := 1 \parallel r := y^{\mathsf{acq}}\,;\ x^{\mathsf{rel}} := 1 \parallel \mathtt{if}(x)\{s := z\}$$



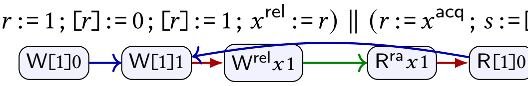
If the first read of the last thread is acquiring, then the execution is disallowed, since acquiring reads are ordered with respect to the reads that follow.

$$z := 1\,;\ y^{\mathsf{rel}} := 1 \parallel r := y^{\mathsf{acq}}\,;\ x^{\mathsf{rel}} := 1 \parallel \mathtt{if}(x^{\mathsf{acq}})\{s := z\}$$



Arm8 enforces address dependencies between reads, but not control dependencies. To support case-analysis (AKA if-closure), we drop all dependencies between reads. This, in turn, invalidates Java's final field semantics.

$$(r := 1\,;\ [r] := 0\,;\ [r] := 1\,;\ x^{\mathsf{rel}} := r) \parallel (r := x^{\mathsf{acq}}\,;\ s := [r]) \tag{ADDR2}$$



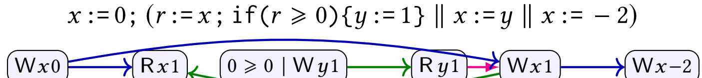
The acquire annotation is required to ensure publication. If address dependencies were enforced between reads then the acquire annotation could be dropped. However, the compiler would need to track address dependencies in order to ensure that case analysis did not convert them to control dependencies.

D.8 Local Invariant Reasoning and Value Range Analysis

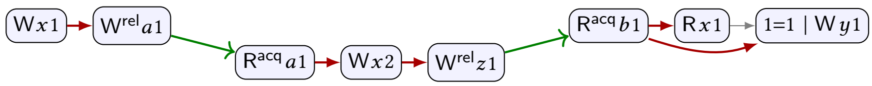
[Todo: Discuss.]

We have already seen TC1 in §4.8 and TC2 in §9.1. Here are some additional examples.

$$x := 0\,;\ (r := x\,;\ \mathtt{if}(r \geqslant 0)\{y := 1\} \parallel x := y \parallel x := -2) \tag{TC9}$$

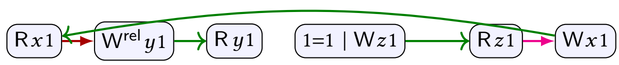


$$x := 1;\ a^{\mathsf{ra}} := 1;\ \mathtt{if}(z^{\mathsf{ra}})\{y := x\} \parallel \mathtt{if}(a^{\mathsf{ra}})\{x := 2;\ z^{\mathsf{ra}} := 1\}$$



(INTERNAL1)

$$r := x;\ y^{\mathsf{ra}} := 1;\ s := y;\ z := s \parallel x := z$$

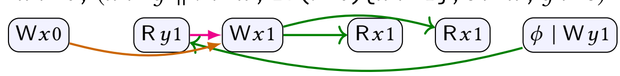


(INTERNAL2)

D.9 TC17-20

Java Causality Test Case 18 asks that we justify the following execution:

$$x := 0;\ (x := y \parallel r := x;\ \mathtt{if}(r{=}0)\{x := 1\};\ s := x;\ y := s)$$



Before we prefix $x := 0$, the precondition of $\mathsf{W}y1$ is:

$$\phi \equiv (1{=}r \vee x{=}r) \Rightarrow ([r{=}0 \wedge ((1{=}s \vee 1{=}s) \Rightarrow s{=}1)] \vee [r{\neq}0 \wedge ((1{=}s \vee x{=}s) \Rightarrow s{=}1)])$$

Simplifying:

$$\phi \equiv (1{=}r \vee x{=}r) \Rightarrow (r{=}0 \vee [r{\neq}0 \wedge ((1{=}s \vee x{=}s) \Rightarrow s{=}1)])$$

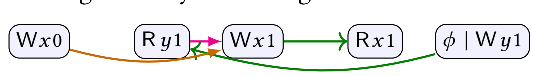
Prefixing $x := 0$:

$$\phi \equiv (1{=}r \vee 0{=}r) \Rightarrow (r{=}0 \vee [r{\neq}0 \wedge ((1{=}s \vee 0{=}s) \Rightarrow s{=}1)])$$

Drilling into the interesting part:

$$\phi \equiv 1{=}r \Rightarrow ((1{=}s \vee 0{=}s) \Rightarrow s{=}1)$$

This is not a tautology. But we get one by coalescing s and r:



$$\phi \equiv 1{=}r \Rightarrow ((1{=}r \vee 0{=}r) \Rightarrow r{=}1)$$

Test case 17 is similar by replaces the condition $r{=}0$ by $r{\neq}1$:

$$\phi \equiv (1{=}r \vee x{=}r) \Rightarrow ([r{\neq}1 \wedge ((1{=}s \vee 1{=}s) \Rightarrow s{=}1)] \vee [r{=}1 \wedge ((1{=}s \vee x{=}s) \Rightarrow s{=}1)])$$

Simplifying and prefixing $x := 0$:

$$\phi \equiv (1{=}r \vee 0{=}r) \Rightarrow (r{\neq}1 \vee [r{=}1 \wedge ((1{=}s \vee 0{=}s) \Rightarrow s{=}1)])$$

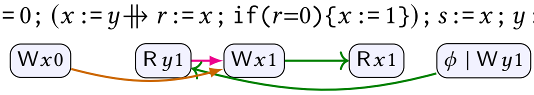
Again, we have:

$$\phi \equiv 1{=}r \Rightarrow ((1{=}s \vee 0{=}s) \Rightarrow s{=}1)$$

which is not a tautology. But we get one by coalescing s and r.

TC20 splits the first thread of TC18:

$$x := 0;\ (x := y \nparallel r := x;\ \mathtt{if}(r{=}0)\{x := 1\});\ s := x;\ y := s$$



Because we take register state from the right, the example is the same as for TC18 above.

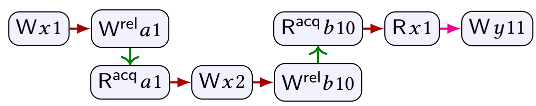
TC19 does the same split for TC17, and follows for the same reason.

D.10 Commuting release and acquire

[Todo: Discuss.]

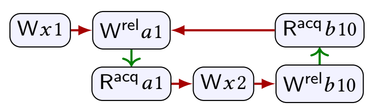
RA example. This is impossible, since $\mathsf{R}x1$ unfulfilled.

$$x := 1;\ a^{\mathsf{rel}} := 1;\ r := b^{\mathsf{acq}};\ s := x;\ y := r{+}s \parallel r := a^{\mathsf{acq}};\ x := 2;\ b^{\mathsf{rel}} := 10$$



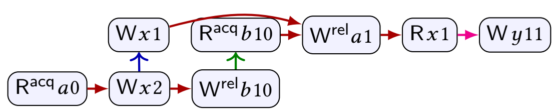
If you swap the release and acquire, then it is impossible for the second thread to get in the middle.

$$x := 1;\ r := b^{\mathsf{acq}};\ a^{\mathsf{rel}} := 1;\ \parallel r := a^{\mathsf{acq}};\ x := 2;\ b^{\mathsf{rel}} := 10$$



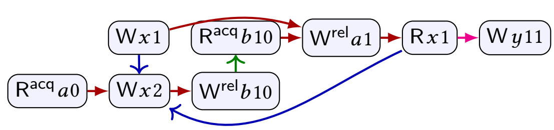
In this case, the following execution is possible:

$$x := 1;\ r := b^{\mathsf{acq}};\ a^{\mathsf{rel}} := 1;\ s := x;\ y := r{+}s \parallel r := a^{\mathsf{acq}};\ x := 2;\ b^{\mathsf{rel}} := 10$$



But not:

$$x := 1;\ r := b^{\mathsf{acq}};\ a^{\mathsf{rel}} := 1;\ s := x;\ y := r{+}s \parallel r := a^{\mathsf{acq}};\ x := 2;\ b^{\mathsf{rel}} := 10$$

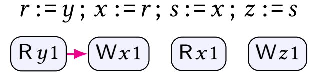


D.11 Write rule

[Todo: Discuss.]

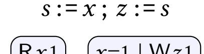
Alan example of why substitute M/x rather than v/x in the write rule:

$$r := y;\ x := r;\ s := x;\ z := s$$

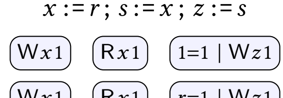


We lost the order from $\mathsf{R}y1$ to $\mathsf{W}z1$.

$$s := x;\ z := s$$



$$x := r;\ s := x;\ z := s$$



D.12 Sevcik examples

[Todo: Discuss.]

Cenciarelli et al. [2007, §7] example. (I incorrectly credit Sevčík and Aspinall [2008].)

$$\texttt{if}(x \land y)\{z := 1\} \parallel \texttt{if}(z)\{x := 1;\ y := 1\}\,\texttt{else}\,\{y := 1;\ x := 1\}$$

$\mathsf{R}\,x\,1$ $\mathsf{R}\,y\,1$ $\mathsf{W}\,z\,1$ $\mathsf{R}\,z\,1$ $\mathsf{W}\,y\,1$ $\mathsf{W}\,x\,1$

Examples from [Sevčík and Aspinall 2008, §4.1] are interesting: Redundant write after read elimination:

```
|| lock m2; x=1; unlock m2
|| lock m1; x=2; unlock m1
|| lock m1; lock m2; r1=x; [x=r1;] r2=x; unlock m2; unlock m1 // [bracketed line removed]
```

Even without the write, r1 and r2 must see the same values, whereas JMM allows different values for the reads when the write is missing.

Redundant read after read elimination:

```
|| y=x
|| r2=y; if (r2==1){[r3=y]; x=r3}else{x=1} // [r3=r2]
```

Interesting case is left $\mathsf{W}\,x\,1$. Initially has predicate $r_3 = 1$. With read rule, we have $y = 1$. In read prefixing, we don't weaken. Instead we weaken with the read into r2.

$\texttt{if}(r_2{=}1)\{r_3 := y;\ x := r_3\}$ $\qquad$ $\texttt{if}(r_2{\neq}1)\{x := 1\}$

$r_2{=}1 \mid \mathsf{R}\,y\,1$ $\quad$ $r_2{=}1 \land y{=}1 \mid \mathsf{W}\,x\,1$ $\quad$ $r_2{\neq}1 \mid \mathsf{W}\,x\,1$

$\texttt{if}(r_2{=}1)\{r_3 := y;\ x := r_3\}\,\texttt{else}\,\{x := 1\}$

$r_2{=}1 \mid \mathsf{R}\,y\,1$ $\quad$ $(r_2{=}1 \land y{=}1) \lor (r_2{\neq}1) \mid \mathsf{W}\,x\,1$

$r_2 := y;\ \texttt{if}(r_2{=}1)\{r_3 := y;\ x := r_3\}\,\texttt{else}\,\{x := 1\}$

$\mathsf{R}\,y\,1$ $\quad$ $\mathsf{R}\,y\,1$ $\quad$ $(y{=}1 \land y{=}1) \lor (y{\neq}1) \mid \mathsf{W}\,x\,1$

To ignore the second read, we use the "delay" trick that we used for JMM TC1, but this is fulfilled by a read rather than a write. In any case, the execution with $x = y = 1$ is allowed.

Roach Motel—all reads 1 impossible, but passible after swapping `r1=x` and `lock m`

```
|| lock m; x=1; unlock m
|| lock m; x=2; unlock m
|| r1=x; lock m; r2=z; if(r1==2){y=1}else{y=r2}; unlock m
|| z=y
```

So Question is whether you can read all 1 in

```
|| lock m; x=1; unlock m
|| lock m; x=2; unlock m
|| lock m; r1=x; r2=z; if(r1==2){y=1}else{y=r2}; unlock m
|| z=y
```

In any execution, we must have 1 before 2, or 2 before 1.

- If thread sees 2, then read x is 2.

- If thread sees 1, then read x is 1.

$$\texttt{if}(r_1{=}2)\{y := 1\}\,\texttt{else}\,\{y := r_2\}$$

$$\boxed{r_1{=}2 \vee (r_1{\neq}2 \wedge r_2{=}1) \mid \mathsf{W}\,y\,1}$$

$$r_1 := x\,;\ r_2 := z\,;\ \texttt{if}(r_1{=}2)\{y := 1\}\,\texttt{else}\,\{y := r_2\}$$

$$\boxed{\mathsf{R}\,x\,1} \quad \boxed{\mathsf{R}\,z\,1} \rightarrow \boxed{\mathsf{W}\,y\,1}$$

So impossible for y and z to be 1.

Irrelevant Read Introduction (can I read 1 for both y and z?)

```
|| r=z; if(!r){if(x){y=1}}else{[s=x;]y=r}
|| x=1; z=y
```

$$\texttt{if}(!r)\{\texttt{if}(x)\{y := 1\}\} \qquad \texttt{if}(r)\{s := x\,;\ y := r\}$$

$$\boxed{r{=}0 \mid \mathsf{R}\,x\,1} \rightarrow \boxed{r{=}0 \mid \mathsf{W}\,y\,1} \qquad \boxed{r{\neq}0 \mid \mathsf{R}\,x\,1} \quad \boxed{r{=}1 \mid \mathsf{W}\,y\,1}$$

$$\texttt{if}(!r)\{\texttt{if}(x)\{y := 1\}\}\,\texttt{else}\,\{y := r\}$$

$$\boxed{\mathsf{R}\,x\,1} \rightarrow \boxed{r{=}0 \vee r{=}1 \mid \mathsf{W}\,y\,1}$$

$$z := 0\,;\ r := z\,;\ \texttt{if}(!r)\{\texttt{if}(x)\{y := 1\}\}\,\texttt{else}\,\{y := r\}$$

$$\boxed{\mathsf{W}\,z\,0} \quad \boxed{\mathsf{R}\,z\,1} \quad \boxed{\mathsf{R}\,x\,1} \rightarrow \boxed{0{=}0 \vee 0{=}1 \mid \mathsf{W}\,y\,1}$$

$$\texttt{if}(!r)\{\texttt{if}(x)\{y := 1\}\} \qquad \texttt{if}(r)\{y := r\}$$

$$\boxed{r{=}0 \mid \mathsf{R}\,x\,1} \rightarrow \boxed{r{=}0 \mid \mathsf{W}\,y\,1} \qquad \boxed{r{=}1 \mid \mathsf{W}\,y\,1}$$

$$\texttt{if}(!r)\{\texttt{if}(x)\{y := 1\}\}\,\texttt{else}\,\{y := r\}$$

$$\boxed{r{=}0 \mid \mathsf{R}\,x\,1} \rightarrow \boxed{r{=}0 \vee r{=}1 \mid \mathsf{W}\,y\,1}$$

$$z := 0\,;\ r := z\,;\ \texttt{if}(!r)\{\texttt{if}(x)\{y := 1\}\}\,\texttt{else}\,\{y := r\}$$

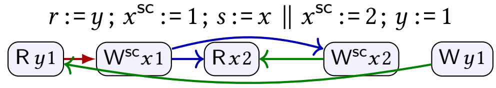
$$\boxed{\mathsf{W}\,z\,0} \quad \boxed{\mathsf{R}\,z\,1} \quad \boxed{\mathsf{R}\,x\,1} \rightarrow \boxed{0{=}0 \vee 0{=}1 \mid \mathsf{W}\,y\,1}$$

If z is initialized to 2, rather than 0, then the dependencies remain and both are disallowed. This relies crucially on the fact that par takes order from both sides.

D.13 SC Access

[Todo: Discuss.]

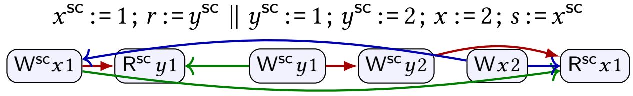
$$r := y\,;\ x^{\mathsf{sc}} := 1\,;\ s := x \parallel x^{\mathsf{sc}} := 2\,;\ y := 1$$



(sc1)

Watt et al. [2020, §3.1]:

$$x^{\mathsf{sc}} := 1\,;\ r := y^{\mathsf{sc}} \parallel y^{\mathsf{sc}} := 1\,;\ y^{\mathsf{sc}} := 2\,;\ x := 2\,;\ s := x^{\mathsf{sc}}$$

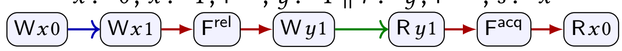


(sc2)

D.14 Fences

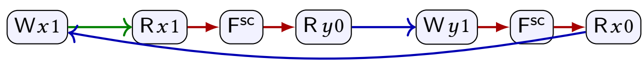
[Todo: Discuss.]

$$x := 0;\ x := 1;\ \mathsf{F}^{\mathsf{rel}};\ y := 1 \parallel r := y;\ \mathsf{F}^{\mathsf{acq}};\ s := x \tag{PUB2}$$



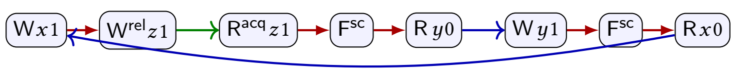
[Lahav et al. 2017, Fig. 5]

$$x := 1 \parallel r := x;\ \mathsf{F}^{\mathsf{sc}};\ r := y \parallel y := 1;\ \mathsf{F}^{\mathsf{sc}};\ r := x \tag{SC3}$$



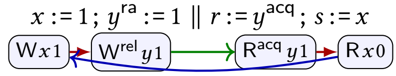
[Lahav et al. 2017, Fig. 6]

$$x := 1;\ z^{\mathsf{ra}} := 1;\ \parallel r := z^{\mathsf{acq}};\ \mathsf{F}^{\mathsf{sc}};\ r := y \parallel y := 1;\ \mathsf{F}^{\mathsf{sc}};\ r := x \tag{SC4}$$

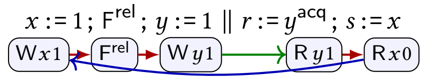


Here are several examples mixing fencing with release/acquire:

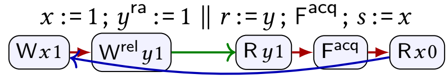
$$x := 1;\ y^{\mathsf{ra}} := 1 \parallel r := y^{\mathsf{acq}};\ s := x$$



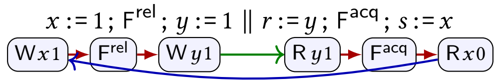
$$x := 1;\ \mathsf{F}^{\mathsf{rel}};\ y := 1 \parallel r := y^{\mathsf{acq}};\ s := x$$



$$x := 1;\ y^{\mathsf{ra}} := 1 \parallel r := y;\ \mathsf{F}^{\mathsf{acq}};\ s := x$$

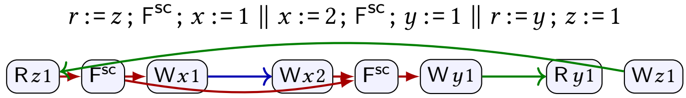


$$x := 1;\ \mathsf{F}^{\mathsf{rel}};\ y := 1 \parallel r := y;\ \mathsf{F}^{\mathsf{acq}};\ s := x$$



[Podkopaev et al. 2019, §D]: The following execution graph is not consistent in the promise-free declarative model of [Kang et al. 2017]. Nevertheless, its mapping to POWER (obtained by simply replacing Fsc with Fsync) is POWER-consistent and $\mathsf{po} \cup \mathsf{rf}$ is acyclic (so it is Strong-POWER-consistent). Note that, using promises, the promising semantics allows this behavior.

$$r := z;\ \mathsf{F}^{\mathsf{sc}};\ x := 1 \parallel x := 2;\ \mathsf{F}^{\mathsf{sc}};\ y := 1 \parallel r := y;\ z := 1$$



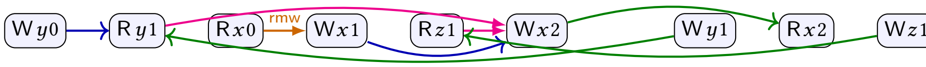
Allowed behavior on POWER... Is there a dependency in the last thread? If so, this is a problem.

[Podkopaev et al. 2019, §8]: To establish the correctness of compilation of the promising semantics to POWER, Kang et al. [2017] followed the approach of Lahav and Vafeiadis [2016]. This approach reduces compilation correctness to POWER to (i) the correctness of compilation to the POWER model strengthened with $\mathsf{po} \cup \mathsf{rf}$ acyclicity; and (ii) the soundness of local reorderings of memory accesses. To establish (i), Kang et al. [2017] wrongly argued that the strengthened POWER-consistency of mapped promise-free execution graphs imply the promise-free consistency of the source execution graphs. This is not the case due to SC fences, which have relatively strong semantics in the promise-free declarative model (see [Podkopaev et al. 2018, Appendix D] for a counter example). Nevertheless, our proof shows that the compilation claim of Kang et al. [2017] is correct.

D.15 RMWs

If RMWs simply use the same semantics as read and write, then we allow LDRF-PF-FAIL, which is used to show failure of LDRF-SC for the promising semantics in [Cho et al. 2021].

$$y := 0;\ \texttt{if}(y)\{\texttt{if}(!\texttt{CAS}(x,0,1))\{\texttt{if}(z)\{x := 2\}\}\} \parallel y := 1;\ \texttt{if}(1{\neq}\texttt{CAS}(x,0,3))\{z := 1\}$$

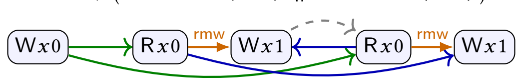


(LDRF-PF-FAIL)

To disallow this, we need to retain the dependency $(\mathsf{R}x2) \rightarrow (\mathsf{W}z1)$. For this, we need to avoid the substitution for x. This is why we use *READ′* instead of *READ* in the independent case for RMWs.

It is not possible for two RMWs to see the same write.

$$x := 0;\ \left(\texttt{FADD}^{\mathsf{rlx},\mathsf{rlx}}(x,1) \parallel \texttt{FADD}^{\mathsf{rlx},\mathsf{rlx}}(x,1)\right)$$

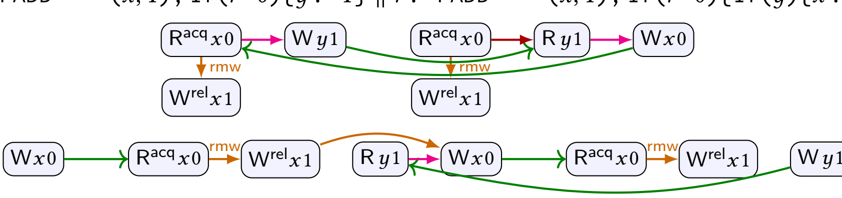


(RMW0)

The gray arrow is required the RMW atomicity axioms.

Lee et al. [2020] introduce PS2.0 to refine the treatment of RMWs in the promising semantics (PS). Their examples have the expected results here, with far less work. First they recall that PS requires quantification over multiple futures in order to disallow executions such as CDRF. (We showed the relaxed variant (CDRF-RLX) in §9.4.)

$$r := \texttt{FADD}^{\mathsf{acq},\mathsf{rel}}(x,1);\ \texttt{if}(r{=}0)\{y := 1\} \parallel r := \texttt{FADD}^{\mathsf{acq},\mathsf{rel}}(x,1);\ \texttt{if}(r{=}0)\{\texttt{if}(y)\{x := 0\}\}$$

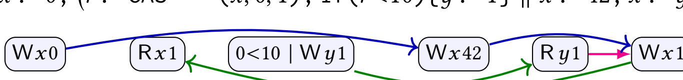


(CDRF)

This execution is clearly impossible, due to the cycle above. In this diagram, we have not drawn order adjacent to the writes of the RMWs, since this is not necessary to produce the cycle. If CDRF is allowed then DRF-RA fails.

PS does not support global value range analysis, as modeled by GA+E below. Our semantics permits GA+E:

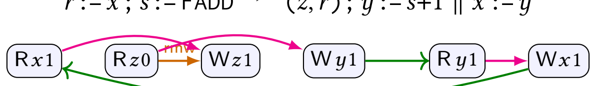
$$x := 0;\ \left(r := \texttt{CAS}^{\mathsf{rlx},\mathsf{rlx}}(x,0,1);\ \texttt{if}(r{<}10)\{y := 1\} \parallel x := 42;\ x := y\right)$$



(GA+E)

PS also does not support register promotion, as modeled by RP below. Our semantics permits RP:

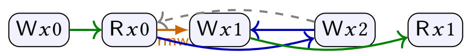
$$r := x;\ s := \texttt{FADD}^{\mathsf{rlx},\mathsf{rlx}}(z,r);\ y := s{+}1 \parallel x := y$$



(RP)

Example D.1. This definition ensures atomicity, disallowing executions such as [Podkopaev et al. 2019, Ex. 3.2]:

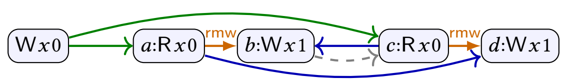
$$x := 0;\ \mathtt{INC}^{\mathsf{rlx},\mathsf{rlx}}(x) \parallel x := 2;\ r := x$$



By **??**, since (Wx2) $\longrightarrow$ (Wx1), it must be that (Wx2) $\longrightarrow$ (Rx0), creating a cycle.

Example D.2. Two successful RMWs cannot see the same write:

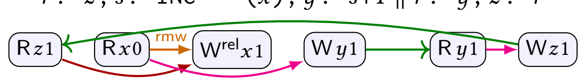
$$x := 0;\ (\mathtt{INC}^{\mathsf{rlx},\mathsf{rlx}}(x) \parallel \mathtt{INC}^{\mathsf{rlx},\mathsf{rlx}}(x))$$



The order from read-to-write is required by fulfillment. Apply **??** of the second RMW to $a \longrightarrow d$, we have that $a \longrightarrow c$. Subsequently applying **??** of the first RMW, we have $b \longrightarrow c$, creating a cycle.

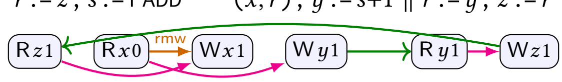
Example D.3. By using two actions rather than one, the definition allows examples such as the following, which is allowed by Arm8 [Podkopaev et al. 2019, Ex. 3.10]:

$$r := z;\ s := \mathtt{INC}^{\mathsf{rlx},\mathsf{rel}}(x);\ y := s{+}1 \parallel r := y;\ z := r$$



A similar example, also allowed by Arm8 [Chakraborty and Vafeiadis 2019, Fig. 6]:

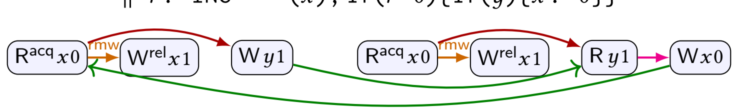
$$r := z;\ s := \mathtt{FADD}^{\mathsf{rlx},\mathsf{rlx}}(x, r);\ y := s{+}1 \parallel r := y;\ z := r$$



This is allowed by WEAKESTMO, but not PS.

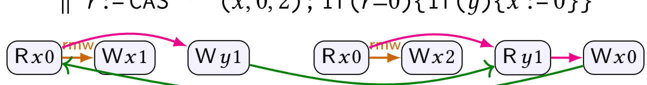
Example D.4. Consider the CDRF example from [Lee et al. 2020]:

$$r := \mathtt{INC}^{\mathsf{acq},\mathsf{rel}}(x);\ \mathtt{if}(r{=}0)\{y := 1\}$$
$$\parallel\ \ r := \mathtt{INC}^{\mathsf{acq},\mathsf{rel}}(x);\ \mathtt{if}(r{=}0)\{\mathtt{if}(y)\{x := 0\}\}$$



Example D.5. Consider this example from [Lee et al. 2020, §C]:

$$r := \mathtt{CAS}^{\mathsf{rlx},\mathsf{rlx}}(x, 0, 1);\ \mathtt{if}(r{\leqslant}1)\{y := 1\}$$
$$\parallel\ \ r := \mathtt{CAS}^{\mathsf{rlx},\mathsf{rlx}}(x, 0, 2);\ \mathtt{if}(r{=}0)\{\mathtt{if}(y)\{x := 0\}\}$$

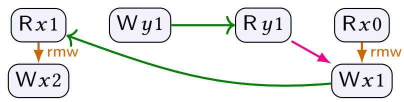


D.16 More RMW

These following examples are from [Cho et al. 2021].

CDRF shows that PwT semantics is not too permissive for ra-RMWs. But what about rlx-RMWs. The following execution is allowed by Arm8, and PS2.0, but disallowed by PS2.1.

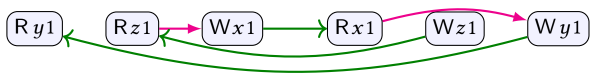
$$r := \mathsf{FADD}^{\mathsf{rlx,rlx}}(x, 1)\,;\ y := 1 \parallel r := y\,;\ s := \mathsf{FADD}^{\mathsf{rlx,rlx}}(x, r)$$



(RMW-W)

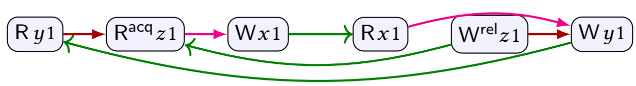
If this $\{z\}$-DRF-RA?

$$\mathtt{if}(y)\{x := z\}\,\mathtt{else}\,\{x := 1\} \parallel r := x\,;\ z := 1\,;\ y := r$$



(NAIVE-LDRF-RA-FAIL)

Interpreting $\{z\}$ as ra:

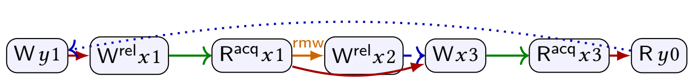


D.17 Fences and RMW

[Todo: Discuss.]

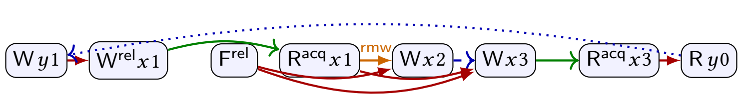
[Podkopaev et al. 2019, Remark 2, After example 3.1]: Aim: allow the splitting of release writes and RMWs into release fences followed by relaxed operations. In RC11 [Lahav et al. 2017], as well as in C/C++11 [Batty et al. 2011], this rather intuitive transformation, as we found out, is actually unsound.

$$y := 1\,;\ x^{\mathsf{ra}} := 1 \parallel \mathsf{INC}^{\mathsf{ra,ra}}(x)\,;\ x := 3 \parallel r := x^{\mathsf{acq}}\,;\ s := y$$



(R)C11 disallows the annotated behavior, due in particular to the release sequence formed from the release exclusive write to x in the second thread to its subsequent relaxed write. However, if we split the increment to fencerel; a := FADDacq,rlx(x, 1) (which intuitively may seem stronger), the release sequence will no longer exist, and the annotated behavior will be allowed. IMM overcomes this problem by strengthening sw in a way that ensures a synchronization edge for the transformed program as well

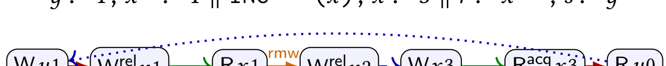
$$y := 1\,;\ x^{\mathsf{ra}} := 1 \parallel \mathsf{F}^{\mathsf{rel}}\,;\ \mathsf{INC}^{\mathsf{ra,rlx}}(x)\,;\ x := 3 \parallel r := x^{\mathsf{acq}}\,;\ s := y$$



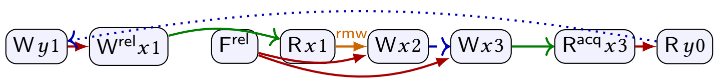
We seem to disallow both of these out of the box.

In the case of a relaxed read in the RMW, the outcome is allowed in both cases:

$$y := 1\,;\ x^{\mathsf{ra}} := 1 \parallel \mathsf{INC}^{\mathsf{rlx,ra}}(x)\,;\ x := 3 \parallel r := x^{\mathsf{acq}}\,;\ s := y$$



$$y := 1\,;\ x^{\mathsf{ra}} := 1 \parallel \mathsf{F}^{\mathsf{rel}}\,;\ \mathtt{INC}^{\mathsf{rlx,rlx}}(x)\,;\ x := 3 \parallel r := x^{\mathsf{acq}}\,;\ s := y$$

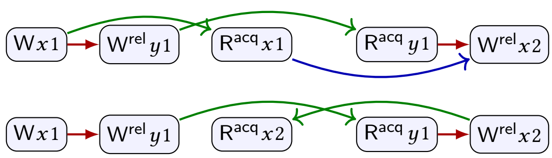


E NOT FOR PUBLICATION

E.1 A Note on Mixed-Mode Data Races

In preparing this paper, we came across the following example, which appears to invalidate Theorem 4.1 of [Dongol et al. 2019].

$$x := 1\,;\ y^{\mathsf{rel}} := 1\,;\ r := x^{\mathsf{acq}} \parallel \mathtt{if}(y^{\mathsf{acq}})\{x^{\mathsf{rel}} := 2\}$$

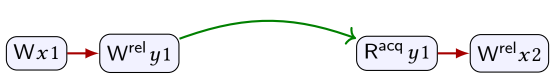


(¶)

The program is data-race free. The two executions shown are the only top-level executions that include $(\mathsf{W}^{\mathsf{rel}}x2)$.

Theorem 4.1 of [Dongol et al. 2019] is stated by extending execution sequences. In the terminology of [Dongol et al. 2019], a read is *L-weak* if it is sequentially stale. Let $\rho = (\mathsf{W}x1)(\mathsf{W}^{\mathsf{rel}}y1)(\mathsf{R}^{\mathsf{acq}}y1)(\mathsf{W}^{\mathsf{rel}}x2)$ be a sequence and $\alpha = (\mathsf{R}^{\mathsf{acq}}x1)$. ρ is L-sequential and α is L-weak in $\rho\alpha$. But there is no execution of this program that includes a data race, contradicting the theorem. The error seems to be in Lemma A.4 of [Dongol et al. 2019], which states that if α is L-weak after an L-sequential ρ, then α must be in a data race. That is clearly false here, since $(\mathsf{R}^{\mathsf{acq}}x1)$ is stale, but the program is data race free.

In proving the SC-LDRF result in [Jagadeesan et al. 2020, §8], we noted that our proof technique is more robust than that of [Dongol et al. 2019], because it limits the prefixes that must be considered. In (¶), the induction hypothesis requires that we add $(\mathsf{R}^{\mathsf{acq}}x1)$ before $(\mathsf{W}^{\mathsf{rel}}x2)$ since $(\mathsf{R}^{\mathsf{acq}}x1) \longrightarrow (\mathsf{W}^{\mathsf{rel}}x2)$. In particular,



is not a downset of (¶), because $(\mathsf{R}^{\mathsf{acq}}x1) \longrightarrow (\mathsf{W}^{\mathsf{rel}}x2)$. As noted in [Jagadeesan et al. 2020, §8], this affects the inductive order in which we move across pomsets, but does not affect the set of pomsets that are considered. In particular,

is a downset of (¶).

F OLD NOTES

F.1 More optimizations

- Sound to strengthen the annotation on an action from rlx to ra, and from ra to sc.

From [Manson et al. 2005]:

- synchronization on thread local objects can be ignored or removed altogether (the caveat to this is the fact that invocations of methods like wait and notify have to obey the correct semantics – for example, even if the lock is thread local, it must be acquired when performing a wait),

- volatile fields of thread local objects can be treated as normal fields.
- redundant synchronization (e.g., when a synchronized method is called from another synchronized method on the same object) can be ignored or removed,

Counterexample for first two:

```
y=1; x^AR=1; r=X^AR; z=1
```

If you see $z = 1$ you must see $y = 1$

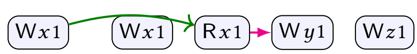
It would be nice if we could get at these with a strength reducing result: synchronization actions can be replaced by relaxed actions in some cases. Then the rules for relaxed read elimination and relaxed write elimination can be used to get rid of them.

F.2 Examples for semicolon semantics

- Parallel asymmetric: state result for *joint free* programs.
- Subsumption can be allowed on registers only
- We build substitutions
- Ignore substitutions when considering semantic equality.

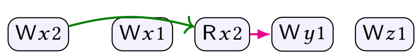
Value for r in (r=1 | Wz1) from (Wx1):

$$x := 1 \parallel x := 1;\ r := x;\ y := r;\ z := r$$



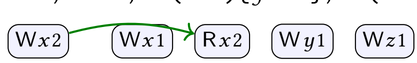
Value for r in (r=1 | Wz1) from (Wx1):

$$x := 2 \parallel x := 1;\ r := x;\ \mathtt{if}(r{>}0)\{y := 1\};\ \mathtt{if}(r{>}0)\{z := 1\}$$

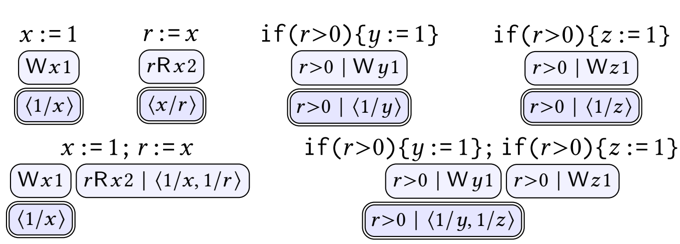


Note that this also contains pomset where value for r in (r=1 | Wy1) also comes from (Wx1):

$$x := 2 \parallel x := 1;\ r := x;\ \mathtt{if}(r{>}0)\{y := 1\};\ \mathtt{if}(r{>}0)\{z := 1\}$$

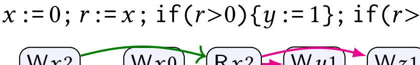


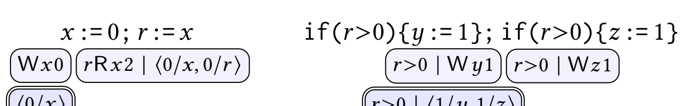
So our semantics will calculate the least ordered version. Then rely on augmentation to get the others.



It is also possible that the read is necessary to give a value for r:

$$x := 2 \parallel x := 0;\ r := x;\ \mathtt{if}(r{>}0)\{y := 1\};\ \mathtt{if}(r{>}0)\{z := 1\}$$





Dependency on two reads:

$$r := x;\ s := y;\ \mathtt{if}(r{<}s)\{z := 1\}$$

$$\boxed{r\mathsf{R}x1}\ \ \boxed{s\mathsf{R}y2} \rightarrow \boxed{\mathsf{W}z1}$$

$$r := x;\ s := y \qquad\qquad \mathtt{if}(r{<}s)\{z := 1\}$$

$$\boxed{r\mathsf{R}x1}\boxed{s\mathsf{R}y2} \qquad\qquad \boxed{r{<}s \mid \mathsf{W}z1}$$

$$\boxed{\langle x/r, y/s\rangle} \qquad\qquad \boxed{r{<}s \mid \langle 1/z\rangle}$$

$$r := x;\ s := y;\ \mathtt{if}(r{<}s)\{z := 1\}$$

$$\boxed{r\mathsf{R}x1}\boxed{s\mathsf{R}y2} \rightarrow \boxed{x{<}2 \mid \mathsf{W}z1}$$

$$\boxed{r{<}s \mid \langle x/r, y/s, 1/z\rangle}$$

Don’t need to worry about confusing reads:

$$r := x;\ s := x;\ \mathtt{if}(s{<}0)\{z := 1\}$$

$$\boxed{r\mathsf{R}x1}\ \ \boxed{s\mathsf{R}x2} \rightarrow \boxed{\mathsf{W}z1}$$

$$r := x;\ s := x \qquad\qquad z := s$$

$$\boxed{r\mathsf{R}x1}\boxed{s\mathsf{R}x2} \qquad\qquad \boxed{s{<}0 \mid \mathsf{W}z1}$$

$$\boxed{\langle x/r, x/s\rangle} \qquad\qquad \boxed{s{<}0 \mid \langle 1/z\rangle}$$

But we also have

$$r := x;\ s := x;\ \mathtt{if}(s{<}0)\{z := 1\}$$

$$\boxed{r\mathsf{R}x1}\ \ \boxed{s\mathsf{R}x2}\ \ \boxed{\mathsf{W}z1}$$

$$r := x \qquad\qquad s := x;\ \mathtt{if}(s{<}0)\{z := 1\}$$

$$\boxed{r\mathsf{R}x1} \qquad\qquad \boxed{s\mathsf{R}x2}\boxed{x{<}0 \mid \mathsf{W}z1}$$

$$\boxed{\langle x/r\rangle} \qquad\qquad \boxed{x{<}0 \mid \langle x/s, 1/z\rangle}$$

Dependency on two reads (No dependency here):

$$r := x;\ s := x;\ \mathtt{if}(r{=}s)\{z := 1\}$$

$$\boxed{r\mathsf{R}x1}\ \ \boxed{s\mathsf{R}x2}\ \ \boxed{\mathsf{W}z1}$$

$$r := x \qquad\qquad s := x;\ \mathtt{if}(r{=}s)\{z := 1\}$$

$$\boxed{r\mathsf{R}x1} \qquad\qquad \boxed{s\mathsf{R}x2}\boxed{r{=}x \mid \mathsf{W}z1}$$

$$\boxed{\langle x/r\rangle} \qquad\qquad \boxed{r{=}x \mid \langle x/s, 1/z\rangle}$$

Another example:

$$r := x;\ s := x;\ z := s$$

$$\boxed{r\mathsf{R}x1}\ \ \boxed{s\mathsf{R}x1}\ \ \boxed{\mathsf{W}z1}$$

$$r := x \qquad\qquad s := x;\ z := s$$

$$\boxed{r\mathsf{R}x1} \qquad\qquad \boxed{s\mathsf{R}x1}\boxed{x{=}1 \mid \mathsf{W}z1}$$

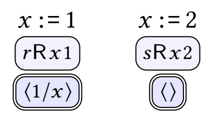
$$\boxed{\langle x/r\rangle} \qquad\qquad \boxed{x{=}1 \mid \langle x/s, 1/z\rangle}$$

Value for r in $(r{<}s \mid \mathsf{W}z1)$ from $(\mathsf{W}x0)$:

$$x := 0;\ r := x;\ s := y;\ \mathtt{if}(r{<}s)\{z := 1\}$$

$$\boxed{\mathsf{W}x0}\ \ \boxed{r\mathsf{R}x1}\ \ \boxed{s\mathsf{R}y2} \rightarrow \boxed{\mathsf{W}z1}$$

Contrary to submission, reverse subsumption not okay.



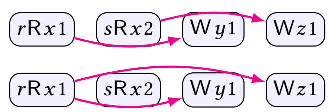
F.3 Playing around with 5a and 4b

If we do this, then swap 4b and 4c, In definition 2.10, take 1-4b of def 2.8, rather than all of it.

Another

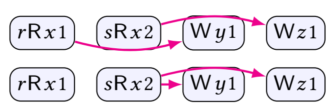
$$r := x\,;\ s := x\,;\ \mathtt{if}(r{>}0)\{y := 1\};\ \mathtt{if}(s{>}0)\{z := 1\}$$

$$r := x\,;\ \mathtt{if}(r{>}0)\{y := 1\};\ s := x\,;\ \mathtt{if}(s{>}0)\{z := 1\}$$

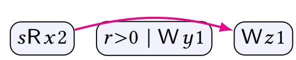


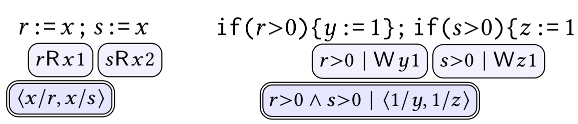
$$s := x\,;\ r := x\,;\ \mathtt{if}(r{>}0)\{y := 1\};\ \mathtt{if}(s{>}0)\{z := 1\}$$

$$s := x\,;\ \mathtt{if}(s{>}0)\{z := 1\};\ r := x\,;\ \mathtt{if}(r{>}0)\{y := 1\}$$



$$s := x\,;\ \mathtt{if}(r{>}0)\{y := 1\};\ \mathtt{if}(s{>}0)\{z := 1\}$$





Idea to get rid of 4b and change 5a to the following:

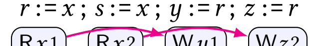
5a. if e writes then either $\kappa'(e)$ implies $\kappa(e)$, or some $c <' e$ reads v from x and $\kappa'(e)$ implies $\kappa(e)[v/x]$,

Need to get rid of 4b because it is sensitive to order of reads.

This change seems sound, because of consistency. But it also fails to validate read reordering on same variable, due to consistency.

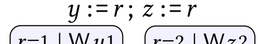
Without 4b, we still do not allow:

$$r := x\,;\ s := x\,;\ y := r\,;\ z := r$$



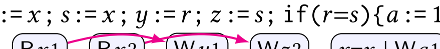
The following is not a pomset (consistency):

$$y := r\,;\ z := r$$



Without 4b, we still do not allow:

$$r := x\,;\ s := x\,;\ y := r\,;\ z := s\,;\ \mathtt{if}(r{=}s)\{a := 1\};$$



The following is not a pomset (consistency):

$$y := r;\ z := s;\ \texttt{if}(r{=}s)\{a := 1\};$$
$$\boxed{r{=}1 \mid \mathsf{W}y1}\quad \boxed{s{=}2 \mid \mathsf{W}z2}\quad \boxed{r{=}s \mid \mathsf{W}a1}$$

We do allow:

$$r := x;\ s := x;\ \texttt{if}(r{=}s)\{a := 1\};$$
$$\boxed{\mathsf{R}x1}\quad \boxed{\mathsf{R}x2}\quad \boxed{x{=}x \mid \mathsf{W}a1}$$

And also

$$r_1 := x;\ r_2 := x;\ r_3 := x;\ \texttt{if}(r_3{\leqslant}1)\{y := 1\};$$
$$\boxed{\mathsf{R}x0}\quad \boxed{\mathsf{R}x2}\quad \boxed{\mathsf{R}x1}\quad \boxed{1{\leqslant}1 \mid \mathsf{W}y1}$$

But we cannot wait forever to satisfy a precondition. This is not a pomset:

$$r := x;\ s := x;\ y := r;\ z := s$$
$$\boxed{\mathsf{R}x3}\quad \boxed{\mathsf{R}x4}\quad \boxed{x{=}1 \mid \mathsf{W}y1}\quad \boxed{x{=}2 \mid \mathsf{W}z2}$$

Note that reads that we delay must all be consistent.

Also note that we cannot have:

$$r := x;\ a := r;\ s := x;\ b := s;\ y := r;\ z := s$$
$$\boxed{\mathsf{R}x3}\quad \boxed{\mathsf{R}x4}\quad \boxed{x{=}1 \mid \mathsf{W}y1}\quad \boxed{x{=}1 \mid \mathsf{W}z2}$$
$$\boxed{\mathsf{W}a3}\quad \boxed{\mathsf{W}b4}$$

Because the following is not a pomset:

$$b := s;\ y := r;\ z := s$$
$$\boxed{r{=}1 \mid \mathsf{W}y1}\quad \boxed{s{=}1 \mid \mathsf{W}z2}$$
$$\boxed{s{=}4 \mid \mathsf{W}b4}$$

But we can have the following, since there is no order the reads:

$$r_1 := x;\ s_1 := x;\ r_2 := x;\ s_2 := x;\ y := r_2;\ z := s_2$$
$$\boxed{\mathsf{R}x1}\quad \boxed{\mathsf{R}x2}\quad \boxed{\mathsf{R}x3}\quad \boxed{\mathsf{R}x4}\quad \boxed{\mathsf{W}y1}\quad \boxed{\mathsf{W}z2}$$

Because this is indistinguishable from:

$$r_1 := x;\ s_1 := x;\ r_2 := x;\ s_2 := x;\ y := r_2;\ z := s_2$$
$$\boxed{\mathsf{R}x3}\quad \boxed{\mathsf{R}x4}\quad \boxed{\mathsf{R}x1}\quad \boxed{\mathsf{R}x2}\quad \boxed{\mathsf{W}y1}\quad \boxed{\mathsf{W}z2}$$

which is the same as:

$$r_1 := x;\ r_2 := x;\ y := r_2;\ s_1 := x;\ s_2 := x;\ z := s_2$$
$$\boxed{\mathsf{R}x1}\quad \boxed{\mathsf{R}x3}\quad \boxed{\mathsf{W}y1}\quad \boxed{\mathsf{R}x2}\quad \boxed{\mathsf{R}x4}\quad \boxed{\mathsf{W}z2}$$

But we can have:

$$p := x;\ r := x;\ s := x;\ y := r;\ z := s$$
$$\boxed{\mathsf{R}x1}\quad \boxed{\mathsf{R}x3}\quad \boxed{\mathsf{R}x4}\quad \boxed{x{=}1 \mid \mathsf{W}y1}\quad \boxed{x{=}1 \mid \mathsf{W}z1}$$

Reads can only swap when their values are interchangeable in the following program.

F.4 Alan comments

```
x=s; y=r; z=3s+2r

x=s; y=r; z1=s; if(r odd){ z2=1} // using 1 and 3 as the reads
```