

Sequential Composition for Relaxed Memory: Pomsets with Predicate Transformers

ANONYMOUS AUTHOR(S)

This paper presents the first compositional definition of sequential composition that applies to a relaxed memory model weak enough to allow efficient implementation on Arm. We extend the denotational model of pomsets with preconditions with predicate transformers. Previous work has shown that pomsets with preconditions are a model of concurrent composition, and that predicate transformers are a model of sequential composition. This paper show how they can be combined.

CCS Concepts: • **Theory of computation** → **Parallel computing models**; *Preconditions*.

Additional Key Words and Phrases: Concurrency, Relaxed Memory Models, Multi-Copy Atomicity, ARMv8, Pomsets, Preconditions, Temporal Safety Properties, Thin-Air Reads, Compiler Optimizations

ACM Reference Format:

Anonymous Author(s). 2021. Sequential Composition for Relaxed Memory: Pomsets with Predicate Transformers. *Proc. ACM Program. Lang.* 0, OOPSLA, Article 0 (October 2021), 8 pages.

1 MODEL

In this section, we present the mathematical preliminaries for the model (which can be skipped on first reading). We then present the model incrementally, starting with a model built using *partially ordered multisets (pomsets)* [Gischer 1988; Plotkin and Pratt 1996], and then adding preconditions and finally predicate transformers.

In later sections, we will discuss extensions to the logic, and to the semantics of load, store and thread initialization, in order to model relaxed memory more faithfully. We stress that these features do *not* change any of the structures of the language: conditionals, parallel composition, and sequential composition are as defined in this section.

1.1 Preliminaries

The syntax is built from

- a set of *values* \mathcal{V} , ranged over by v, w, ℓ, k ,
- a set of *registers* \mathcal{R} , ranged over by r, s ,
- a set of *expressions* \mathcal{M} , ranged over by M, N, L .

Memory references are tagged values, written $[\ell]$. Let \mathcal{X} be the set of memory references, ranged over by x, y, z .

We require that

- values and registers are disjoint,
- values include at least the constants 0 and 1,
- expressions include at least registers and values,
- expressions do *not* include references: $M[N/x] = M$.

Permission to make digital or hard copies of part or all of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. Copyrights for third-party components of this work must be honored. For all other uses, contact the owner/author(s).

© 2021 Copyright held by the owner/author(s).

2475-1421/2021/10-ART0

<https://doi.org/>

We model the following language.

$$\begin{aligned} \mu &::= \text{rlx} \mid \text{ra} \mid \text{sc} & \nu &::= \text{acq} \mid \text{rel} \mid \text{ar} \\ S &::= r := M \mid r := [L]^\mu \mid [L]^\mu := M \mid F^\nu \mid \text{skip} \mid S_1; S_2 \mid \text{if}(M)\{S_1\}\text{else}\{S_2\} \mid S_1 \parallel S_2 \end{aligned}$$

Memory modes, μ , are relaxed (rlx), release-acquire (ra), and sequentially consistent (sc). Relaxed mode is the default; we regularly elide it from examples. ra/sc accesses are collectively known as *synchronized accesses*.

Fence modes, ν , are acquire (acq), release (rel), and acquire-release (ar).

Commands, aka *statements*, S , include memory accesses at a given mode, as well as the usual structural constructs. Following [Ferreira et al. 1996], \parallel denotes parallel composition, preserving thread state on the left after a join. In examples and sublanguages without join, we use the symmetric \parallel operator.

The semantics is built from the following.

- a set of *events* \mathcal{E} , ranged over by e, d, c, b ,
- a set of *logical formulae* Φ , ranged over by ϕ, ψ, θ ,
- a set of *actions* \mathcal{A} , ranged over by a ,

Subsets of \mathcal{E} are ranged over by E, D, C, B .

We require that:

- formulae include tt, ff and the equalities $(M=N)$ and $(x=M)$,
- formulae are closed under $\neg, \wedge, \vee, \Rightarrow$, and substitutions $[M/r], [M/x]$,
- there is a relation \models between formulae, capturing entailment,
- \models has the expected semantics for $=, \neg, \wedge, \vee, \Rightarrow$ and substitutions $[M/r], [M/x]$,
- there are three binary relations over $\mathcal{A} \times \mathcal{A}$: *matches*, *blocks*, and *delays*,
- there are two subsets of \mathcal{A} , distinguishing *read* and *release* actions.

Logical formulae include equations over registers, such as $(r=s+1)$. For use in $\S??$, we also include equations over memory references, such as $(x=1)$. Formulae are subject to substitutions; actions are not. We use expressions as formulae, coercing M to $M \neq 0$. Equations have precedence over logical operators; thus $r=v \Rightarrow s>w$ is read $(r=v) \Rightarrow (s>w)$. As usual, implication associates to the right; thus $\phi \Rightarrow \psi \Rightarrow \theta$ is read $\phi \Rightarrow (\psi \Rightarrow \theta)$.

We say ϕ is a *tautology* if $\text{tt} \models \phi$. We say ϕ is *unsatisfiable* if $\phi \models \text{ff}$.

Throughout $\S 1-??$ we additionally require that

- each register is assigned at most once in a program.

In $\S??$, we drop this restriction, requiring instead that

- there are registers $\mathcal{S}_{\mathcal{E}} = \{s_e \mid e \in \mathcal{E}\}$,
- registers $\mathcal{S}_{\mathcal{E}}$ do not appear in programs: $S[N/s_e] = S$.

1.2 Actions in This Paper

In this paper, we let actions be reads and writes and fences:

$$a, b ::= W^\mu xv \mid R^\mu xv \mid F^\nu$$

We use shorthand when referring to actions. In definitions, we drop elements of actions that are existentially quantified. In examples, we drop elements of actions, using defaults. Let \sqsubseteq be the least order over access and fence modes such that $\text{rlx} \sqsubseteq \text{ra} \sqsubseteq \text{sc}$ and $\text{rel} \sqsubseteq \text{ar}$ and $\text{acq} \sqsubseteq \text{ar}$. We write $(W^{\sqsupset \text{ra}})$ to stand for either (W^{ra}) or (W^{sc}) , and similarly for the other actions and modes.

Definition 1.1. Actions (R) are *read* actions. Actions $(W^{\sqsupset \text{ra}})$ and $(F^{\sqsupset \text{rel}})$ are *release* actions.

We say a *matches* b if $a = (Wxv)$ and $b = (Rxv)$.

We say a *blocks* b if $a = (Wx)$ and $b = (Rx)$, regardless of value.

We say a *delays* b if $a \bowtie_{\text{co}} b$ or $a \bowtie_{\text{sync}} b$ or $a \bowtie_{\text{sc}} b$.

Let \bowtie_{co} capture write-write, read-write coherence: $\bowtie_{\text{co}} = \{(Wx, Wx), (Rx, Wx), (Wx, Rx)\}$.

Let \bowtie_{sync} capture order due to synchronization: $\bowtie_{\text{sync}} = \{(a, W^{\exists ra}), (a, F^{\exists rel}), (R, F^{\exists acq}), (Rx, R^{\exists ra}), (R^{\exists ra}, a), (F^{\exists acq}, a), (F^{\exists rel}, W), (W^{\exists ra}x, Wx)\}$.

Let \bowtie_{sc} capture order due to sc access: $\bowtie_{\text{sc}} = \{(W^{\text{sc}}, W^{\text{sc}}), (R^{\text{sc}}, W^{\text{sc}}), (W^{\text{sc}}, R^{\text{sc}}), (R^{\text{sc}}, R^{\text{sc}})\}$.

1.3 Model

Definition 1.2. A pomset with predicate transformers over \mathcal{A} is a tuple $(E, \lambda, \kappa, \tau, \checkmark, \text{rf}, \leq)$ where

(M1) $E \subseteq \mathcal{E}$ is a set of events,

(M2) $\lambda : E \rightarrow \mathcal{A}$ defines a *label* for each event,

(M3) $\kappa : E \rightarrow \Phi$ defines a *precondition* for each event,

(M4) $\tau : 2^{\mathcal{E}} \rightarrow \Phi \rightarrow \Phi$ is a *family of predicate transformers* over E ,

(M5) $\checkmark : \Phi$ defines a *termination condition*,

(M6) $\text{rf} : E \rightarrow E$ is an injective relation capturing *reads-from* such that

(M6a) if $d \xrightarrow{\text{rf}} e$ then $\lambda(d)$ matches $\lambda(e)$,

(M7) $\leq : E \times E$, is a partial order capturing *causality*, such that

(M7a) if $d \xrightarrow{\text{rf}} e$ and $\lambda(c)$ blocks $\lambda(e)$ then either $c \leq d$ or $e \leq c$.

A pomset is *top-level* if for every $e \in E$,

(M8) $\kappa(e)$ is a tautology,

(M9) if $\lambda(e)$ is a read then there is some $d \xrightarrow{\text{rf}} e$.

We give the semantics of programs in Fig 1.

LEMMA 1.3. For any P in the range of $\llbracket \cdot \rrbracket$, $d \xrightarrow{\text{rf}} e$ implies $d \leq e$.

PROOF. Induction on the definition of $\llbracket \cdot \rrbracket$. \square

The semantics to be closed with respect to *augmentation* Augments include more order and stronger formulae; in examples, we typically consider pomsets that are augment-minimal. One intuitive reading of augment closure is that adding order can only cause preconditions to weaken.

Definition 1.4. P_2 is an *augment* of P_1 if

- | | | | |
|-------------------------------------|---|---|---------------------------------|
| (1) $E_2 = E_1$, | (3) $\kappa_2(e) \models \kappa_1(e)$, | (5) $\checkmark_2 \models \checkmark_1$, | (7) $\leq_2 \supseteq \leq_1$. |
| (2) $\lambda_2(e) = \lambda_1(e)$, | (4) $\tau_2^D(e) \models \tau_1^D(e)$, | (6) $\text{rf}_2 = \text{rf}_1$, | |

LEMMA 1.5. If $P_1 \in \llbracket S \rrbracket$ and P_2 augments P_1 then $P_2 \in \llbracket S \rrbracket$.

PROOF. Induction on the definition of $\llbracket \cdot \rrbracket$. \square

Note that E_1 and E_2 are not necessarily disjoint. In *IF*, the definition of *extends* stops coalescing the *rf* in

$$\text{if}(b)\{r := x \parallel x := 1\} \text{ else } \{r := x; x := 1\}$$

We have given the semantics of *IF* using disjunctive normal form. Dijkstra [1975] used conjunctive normal form. Note that $(\phi \wedge \theta_1) \vee (\neg\phi \wedge \theta_2)$ is logically equivalent to $(\phi \Rightarrow \theta_1) \wedge (\neg\phi \Rightarrow \theta_2)$.

1.4 Full Versions

If $P \in \text{WRITE}(x, M, \mu)$ then $(\exists v : E \rightarrow \mathcal{V}) (\exists \theta : E \rightarrow \Phi)$

(w1) if $\theta_d \wedge \theta_e$ is satisfiable then $d = e$, (w4) $\tau^D(\psi) \models \theta_e \Rightarrow \psi[M/x]$,

(w2) $\lambda(e) = W^\mu x v_e$, (w5a) $\checkmark \models \theta_e \Rightarrow M = v_e$,

(w3) $\kappa(e) \models \theta_e \wedge M = v_e$, (w5b) $\checkmark \models \bigvee_{e \in E} \theta_e$.

Suppose $R_1 : E_1 \times E_1$ and $R_2 : E_2 \times E_2$.

We say R extends R_1 and R_2 if $R \supseteq (R_1 \cup R_2)$ and $R \cap (E_1 \times E_1) = R_1$ and $R \cap (E_2 \times E_2) = R_2$.

If $P \in \text{SKIP}$ then $E = \emptyset$ and $\tau^D(\psi) \models \psi$.

If $P \in \mathcal{P}_1 \parallel \mathcal{P}_2$ then $(\exists P_1 \in \mathcal{P}_1) (\exists P_2 \in \mathcal{P}_2)$

(p1) $E = (E_1 \uplus E_2)$,

(p2) $\lambda = (\lambda_1 \cup \lambda_2)$,

(p3a) if $e \in E_1$ then $\kappa(e) \models \kappa_1(e)$,

(p3b) if $e \in E_2$ then $\kappa(e) \models \kappa_2(e)$,

(p4) $\tau^D(\psi) \models \tau_1^D(\psi)$,

(p5) $\checkmark \models \checkmark_1 \wedge \checkmark_2$,

(p6) rf extends rf_1 and rf_2 ,

(p7a) \leq extends \leq_1 and \leq_2 ,

(p7b) if $d \in E_1$, $e \in E_2$ and $d \xrightarrow{\text{rf}} e$ then $d \leq e$.

If $P \in \text{IF}(\phi, \mathcal{P}_1, \mathcal{P}_2)$ then $(\exists P_1 \in \mathcal{P}_1) (\exists P_2 \in \mathcal{P}_2)$

(c1) $E = (E_1 \cup E_2)$,

(c2) $\lambda = (\lambda_1 \cup \lambda_2)$,

(c3a) if $e \in E_1 \setminus E_2$ then $\kappa(e) \models \phi \wedge \kappa_1(e)$,

(c3b) if $e \in E_2 \setminus E_1$ then $\kappa(e) \models \neg\phi \wedge \kappa_2(e)$,

(c3c) if $e \in E_1 \cap E_2$

then $\kappa(e) \models (\phi \wedge \kappa_1(e)) \vee (\neg\phi \wedge \kappa_2(e))$,

(c4) $\tau^D(\psi) \models (\phi \wedge \tau_1^D(\psi)) \vee (\neg\phi \wedge \tau_2^D(\psi))$,

(c5) $\checkmark \models (\phi \wedge \checkmark_1) \vee (\neg\phi \wedge \checkmark_2)$.

(c6a) rf extends rf_1 and rf_2 ,

(c6b) $\text{rf} \subseteq (\text{rf}_1 \cup \text{rf}_2)$,

(c7a) \leq extends \leq_1 and \leq_2 ,

(c7b) $\leq \subseteq (\leq_1 \cup \leq_2)$.

If $P \in \mathcal{P}_1; \mathcal{P}_2$ then $(\exists P_1 \in \mathcal{P}_1) (\exists P_2 \in \mathcal{P}_2)$

let $\kappa'_2(e) = \tau_1^{\downarrow e}(\kappa_2(e))$, where $\downarrow e = \{c \mid c < e\}$

(s1) $E = (E_1 \cup E_2)$,

(s2) $\lambda = (\lambda_1 \cup \lambda_2)$,

(s3a) if $e \in E_1 \setminus E_2$ then $\kappa(e) \models \kappa_1(e)$,

(s3b) if $e \in E_2 \setminus E_1$ then $\kappa(e) \models \kappa'_2(e)$,

(s3c) if $e \in E_1 \cap E_2$ then $\kappa(e) \models \kappa_1(e) \vee \kappa'_2(e)$,

(s3d) if $\lambda_2(e)$ is a release then $\kappa(e) \models \checkmark_1$,

(s4) $\tau^D(\psi) \models \tau_1^D(\tau_2^D(\psi))$,

(s5) $\checkmark \models \checkmark_1 \wedge \tau_1(\checkmark_2)$,

(s6) rf extends rf_1 and rf_2 ,

(s7a) \leq extends \leq_1 and \leq_2 ,

(s7b) if $d \in E_1$, $e \in E_2$ and $d \xrightarrow{\text{rf}} e$ then $d \leq e$,

(s7c) if $\lambda_1(d)$ delays $\lambda_2(e)$ then $d \leq e$.

If $P \in \text{LET}(r, M)$ then $E = \emptyset$ and $\tau^D(\psi) \models \psi[M/r]$.

If $P \in \text{READ}(r, x, \mu)$ then $(\exists v \in \mathcal{V})$

(r1) if $d, e \in E$ then $d = e$,

(r2) $\lambda(e) = R^\mu x v$,

(r4a) if $(E \cap D) \neq \emptyset$ then $\tau^D(\psi) \models v=r \Rightarrow \psi$,

(r4b) if $E \neq \emptyset$ and $(E \cap D) = \emptyset$ then

$\tau^D(\psi) \models (v=r \vee x=r) \Rightarrow \psi$.

(r4c) if $E = \emptyset$ then $\tau^D(\psi) \models \psi$.

If $P \in \text{WRITE}(x, M, \mu)$ then $(\exists v \in \mathcal{V})$

(w1) if $d, e \in E$ then $d = e$,

(w2) $\lambda(e) = W^\mu x v$,

(w3) $\kappa(e) \models M=v$,

(w4) $\tau^D(\psi) \models \psi[M/x]$,

(w5a) if $E \neq \emptyset$ then $\checkmark \models M=v$,

(w5b) if $E = \emptyset$ then $\checkmark \models \text{ff}$.

If $P \in \text{FENCE}(\mu)$ then

(f1) if $d, e \in E$ then $d = e$,

(f2) $\lambda(e) = F^\mu$,

(f4) $\tau^D(\psi) \models \psi$,

(f5) if $E = \emptyset$ then $\checkmark \models \text{ff}$.

$\llbracket r := M \rrbracket = \text{LET}(r, M)$

$\llbracket \text{skip} \rrbracket = \text{SKIP}$

$\llbracket r := x^\mu \rrbracket = \text{READ}(r, x, \mu)$

$\llbracket S_1 \parallel S_2 \rrbracket = \llbracket S_1 \rrbracket \parallel \llbracket S_2 \rrbracket$

$\llbracket x^\mu := M \rrbracket = \text{WRITE}(x, M, \mu)$

$\llbracket S_1; S_2 \rrbracket = \llbracket S_1 \rrbracket; \llbracket S_2 \rrbracket$

$\llbracket F^\nu \rrbracket = \text{FENCE}(\nu)$

$\llbracket \text{if}(M)\{S_1\} \text{ else } \{S_2\} \rrbracket = \text{IF}(M \neq 0, \llbracket S_1 \rrbracket, \llbracket S_2 \rrbracket)$

Fig. 1. Semantics of programs

If $P \in \text{READ}(r, x, \mu)$ then $(\exists v : E \rightarrow \mathcal{V}) (\exists \theta : E \rightarrow \Phi)$

(R1) if $\theta_d \wedge \theta_e$ is satisfiable then $d = e$,

(R2) $\lambda(e) = R^\mu x v_e$

(R3) $\kappa(e) \models \theta_e$,

(R4a) $(\forall e \in E \cap D) \tau^D(\psi) \models \theta_e \Rightarrow v_e = s_e \Rightarrow \psi[s_e/r]$,

(R4b) $(\forall e \in E \setminus D) \tau^D(\psi) \models \theta_e \Rightarrow (v_e = s_e \vee x = s_e) \Rightarrow \psi[s_e/r]$,

(R4c) $(\forall s) \tau^D(\psi) \models (\bigwedge_{e \in E} \neg \theta_e) \Rightarrow \psi[s/r]$.

2 ARM

For simplicity, we restrict to top level parallel composition and ignore fences¹.

2.1 Arm executions

Definition 2.1. An Arm8 execution graph, G , is tuple $(E, \lambda, \text{poloc}, \text{lob})$ such that

(A1) $E \subseteq \mathcal{E}$ is a set of events,

(A2) $\lambda : E \rightarrow \mathcal{A}$ defines a label for each event,

(A3) $\text{poloc} : E \times E$, is a per-thread, per-location total order, capturing *per-location program order*,

(A4) $\text{lob} : E \times E$, is a per-thread partial order capturing *locally-ordered-before*, such that

(A4a) $\text{poloc} \cup \text{lob}$ is acyclic.

The definition of lob is complex. Comparing with our definition of sequential composition, it is sufficient to note that lob includes

(I1) read-write dependencies, required by $s3$,

(I2) synchronization delay of \preceq_{sync} , required by $s7c$,

(I3) sc access delay of $\triangleright_{\text{sc}}$, required by $s7c$,

(I4) write-write and read-to-write coherence delay of \preceq_{co} , required by $s7c$,

and that lob does *not* include

(I5) read-read control dependencies, required by $s3$,

(I6) write-to-read order of rf , required by $s7b$,

(I7) write-to-read coherence delay of \preceq_{co} , required by $s7c$.

Definition 2.2. Execution G is $(\text{co}, \text{rf}, \text{gcb})$ -valid, under External Global Consistency (EGC) if

(A5) $\text{co} : E \times E$, is a per-location total order on writes, capturing *coherence*,

(A6) $\text{rf} : E \times E$, is a surjective and injective relation on reads, capturing *reads-from*, such that

(A6a) if $d \xrightarrow{\text{rf}} e$ then $\lambda(d)$ matches $\lambda(e)$,

(A6b) $\text{poloc} \cup \text{co} \cup \text{rf} \cup \text{fr}$ is acyclic, where $e \xrightarrow{\text{fr}} c$ if $e \xleftarrow{\text{rf}} d \xrightarrow{\text{co}} c$, for some d ,

(A7) $\text{gcb} \supseteq (\text{co} \cup \text{rf})$ is a linear order such that

(A7a) if $d \xrightarrow{\text{rf}} e$ and $\lambda(c)$ blocks $\lambda(e)$ then either $c \xrightarrow{\text{gcb}} d$ or $e \xrightarrow{\text{gcb}} c$,

(A7b) if $e \xrightarrow{\text{lob}} c$ then either $e \xrightarrow{\text{gcb}} c$ or $(\exists d) d \xrightarrow{\text{rf}} e$ and $d \xrightarrow{\text{poloc}} e$ but not $d \xrightarrow{\text{lob}} c$.

Execution G is $(\text{co}, \text{rf}, \text{cb})$ -valid under External Consistency (EC) if

(A5) and (A6), as for EGC,

(A8) $\text{cb} \supseteq (\text{co} \cup \text{lob})$ is a linear order such that if $d \xrightarrow{\text{rf}} e$ then either

(A8a) $d \xrightarrow{\text{cb}} e$ and if $\lambda(c)$ blocks $\lambda(e)$ then either $c \xrightarrow{\text{cb}} d$ or $e \xrightarrow{\text{cb}} c$, or

(A8b) $d \xleftarrow{\text{cb}} e$ and $d \xrightarrow{\text{poloc}} e$ and $(\nexists c) \lambda(c)$ blocks $\lambda(e)$ and $d \xrightarrow{\text{poloc}} c \xrightarrow{\text{poloc}} e$.

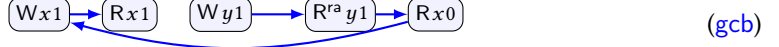
¹Fences are not actions in Arm8, which complicates the theorem statements.

[Alglave et al. 2021] explain EGC and EC using the following example.²

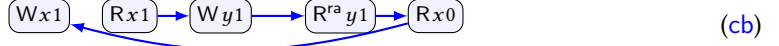
$x := 1; r := x; y := r \parallel 1 := y^{\text{ra}}; s := x$



EGC drops **lob**-order in the first thread using 2.4, since (Wx1) is not **lob**-ordered before (Wy1).



EC drops **rf**-order in the first thread using A8b.



2.2 Arm Compilation 1

Podkopaev et al. [2019] lowers to Arm8 as follows: Relaxed access is implemented using ldr/str, non-relaxed access using ldar/stlr. In this section, we consider a suboptimal strategy, which lowers non-relaxed reads to (dmb.sy; ldar).

We do not distinguish control dependencies from address dependencies, and therefore L5 forces us to drop all dependencies between reads. To achieve this, we modify the definition of κ'_2 in Fig 1.

Definition 2.3. Let $\llbracket \cdot \rrbracket_{\text{RR}}$ be as defined in Fig 1, replacing the definition of κ'_2 with:

$$\kappa'_2(e) = \begin{cases} \tau_1(\kappa_2(e)) & \text{if } \lambda(e) \text{ is a read} \\ \tau_1^{\downarrow e}(\kappa_2(e)) & \text{otherwise, where } \downarrow e = \{c \mid c < e\} \end{cases}$$

THEOREM 2.4. Suppose G_1 is $(\text{co}_1, \text{rf}_1, \text{gcb}_1)$ -valid for S under the suboptimal lowering that maps non-relaxed reads to (dmb.sy; ldar). Then there is a top-level pomset $P_2 \in \llbracket S \rrbracket_{\text{RR}}$ such that $E_2 = E_1$, $\lambda_2 = \lambda_1$, $\text{rf}_2 = \text{rf}_1$, and $\leq_2 = \text{gcb}_1$.

PROOF. First, we establish some lemmas about Arm8.

LEMMA 2.5. Suppose G is $(\text{co}, \text{rf}, \text{gcb})$ -valid. Then $\text{gcb} \supseteq \text{fr}$.

PROOF. Using the definition of **fr** from A6b, we have $e \xrightarrow{\text{rf}} d \xrightarrow{\text{co}} c$, and therefore $\lambda(c)$ blocks $\lambda(e)$. Applying A7a, we have that either $c \xrightarrow{\text{gcb}} d$ or $e \xrightarrow{\text{gcb}} c$. Since **gcb** includes **co**, we have $d \xrightarrow{\text{gcb}} c$, and therefore it must be that $e \xrightarrow{\text{gcb}} c$. \square

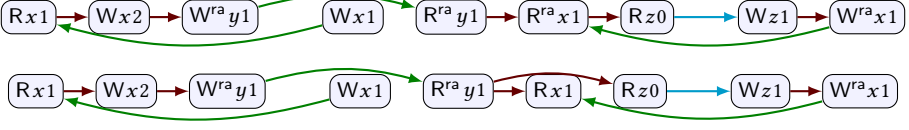
LEMMA 2.6. Suppose G is $(\text{co}, \text{rf}, \text{gcb})$ -valid and $c \xrightarrow{\text{poloc}} e$, where $\lambda(c)$ blocks $\lambda(e)$. Then $c \xrightarrow{\text{gcb}} e$.

PROOF. By way of contradiction, assume $e \xrightarrow{\text{gcb}} c$. If $c \xrightarrow{\text{rf}} e$ then by A7 we must also have $c \xrightarrow{\text{gcb}} e$, contradicting the assumption that **gcb** is a total order. Otherwise that there is some $d \neq c$ such that $d \xrightarrow{\text{rf}} e$, and therefore $d \xrightarrow{\text{gcb}} e$. By transitivity, $d \xrightarrow{\text{gcb}} c$. By the definition of **fr**, we have $e \xrightarrow{\text{fr}} c$. But this contradicts A6b, since $c \xrightarrow{\text{poloc}} e$. \square

We show that all the order required in the pomset is also required by Arm8. m7a holds since **cb**₁ is consistent with **co**₁ and **fr**₁. As noted above **lob** includes the order required by s3 and s7c. We need only show that the order removed from 2.4 can also be removed from the pomset. In order for to remove order from e to c , we must have $d \xrightarrow{\text{rf}} e$ and $d \xrightarrow{\text{poloc}} e$ but not $d \xrightarrow{\text{lob}} c$. Because of our suboptimal lowering, it must be that e is a relaxed read; otherwise the dmb.sy would require $d \xrightarrow{\text{lob}} c$. Thus we know that s7c does not require order from e to c . By chaining r4b and w4, any dependence on the read can be satisfied without introducing order in s3. \square

²We have changed an address dependency in the first thread to a data dependency.

Downgrading messes up publication:

$$x := x + 1; y^{ra} := 1 \parallel x := 1; \text{if } (y^{ra} \ \&\& \ x^{ra}) \{s := z\} \parallel z := 1; x^{ra} := 1$$


2.3 Arm Compilation 2

Definition 2.7. Let $\llbracket \cdot \rrbracket'_{RR}$ be as defined for $\llbracket \cdot \rrbracket_{RR}$ in Def 2.3 and Fig 1, changing s7b and s7c:

(s7b') if $\lambda_1(c)$ blocks $\lambda_2(e)$ then $d \xrightarrow{rf} e$ implies $c \leq d$,

(s7c') if $\lambda_1(d)$ delays' $\lambda_2(e)$ then $d \leq e$,

where *delays'* replaces \bowtie_{co} in Def 1.1 of *delays* by $\bowtie_{lws} = \{(Wx, Wx), (Rx, Wx)\}$.

Note that Lem 1.3 fails for $\llbracket \cdot \rrbracket'_{RR}$, since $d \xrightarrow{rf} e$ may not imply $d \leq e$ when d and e come from different sides of a sequential composition. This means that *rf* must be verified during pomset construction, rather than post-hoc. If one wants a post-hoc verification technique for *rf*, it is possible to include program order (*po*) in the pomset.

LEMMA 2.8. P is top-level iff $d \xrightarrow{rf} e$ implies either

- external fulfillment: $d \leq e$ and if $\lambda(c)$ blocks $\lambda(e)$ then either $c \leq d$ or $e \leq c$, or
- internal fulfillment: $d \xrightarrow{po} e$ and $(\nexists c) \lambda(c)$ blocks $\lambda(e)$ and $d \xrightarrow{po} c \xrightarrow{po} e$.

THEOREM 2.9. Suppose G_1 is EC-valid for S via (co_1, rf_1, cb_1) and that $cb_1 \supseteq fr_1$. Then there is a top-level pomset $P_2 \in \llbracket S \rrbracket$ such that $E_2 = E_1$, $\lambda_2 = \lambda_1$, $rf_2 = rf_1$, and $\leq_2 = cb_1$.

PROOF. We show that all the order required in the pomset is also required by Arm8. m7a holds since cb_1 is consistent with co_1 and fr_1 . s7b follows from A8b. As noted above, lob includes the order required by s3 and s7c. \square

The generality of Thm 2.9 is not limited by the assumption that $cb_1 \supseteq fr_1$:

LEMMA 2.10. Suppose G is EC-valid via (co, rf, cb) . Then there a permutation cb' of cb such that G is EC-valid via (co, rf, cb') and $cb' \supseteq fr$, where fr is defined in A6b.

PROOF. We show that any cb order that contradicts fr is incidental.

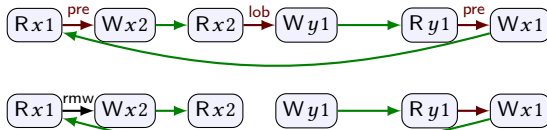
By definition of fr , $e \xleftarrow{rf} d \xrightarrow{co} c$, for some d . Since $cb \supseteq co$, we know that $d \xrightarrow{co} c$.

If A8a applies to $d \xrightarrow{rf} e$, then $e \xrightarrow{cb} c$, since it cannot be that $c \xrightarrow{co} d$.

Suppose A8b applies to $d \xrightarrow{rf} e$ and c is from a different thread. Because it is a different thread, we cannot have $e \xrightarrow{lob} c$, and thus the order in cb is incidental.

Suppose A8b applies to $d \xrightarrow{rf} e$ and c is from the same thread. Since $c \xrightarrow{co} d$, it cannot be that $c \xrightarrow{poloc} d$, using A6b. It also cannot be that $d \xrightarrow{poloc} c \xrightarrow{poloc} e$. It must be that $e \xrightarrow{poloc} c$. By A4a, we cannot have $e \xrightarrow{lob} c$, and thus the order in cb is incidental. \square

Bad example:

$$r := \text{EXCHG}(x, 2); s := x; y := s - 1 \parallel r := y; x := r$$


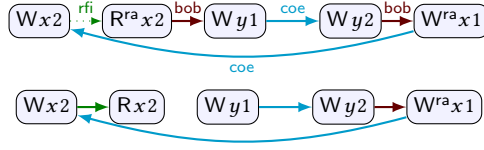
(✓Arm8)

(\leq)

Anton example 1 [rfi-coe-coe]

$$x := 2; r := x^{ra}; y := 1 \parallel y := 2; x^{ra} := 1$$

(RFI-COE-COE)



(✓Arm8)

REFERENCES

- Jade Alglave, Will Deacon, Richard Grisenthwaite, Antoine Hacquard, and Luc Maranget. 2021. Armed Cats: Formal Concurrency Modelling at Arm. *TOPLAS* (2021). To Appear.
- Edsger W. Dijkstra. 1975. Guarded Commands, Nondeterminacy and Formal Derivation of Programs. *Commun. ACM* 18, 8 (1975), 453–457. <https://doi.org/10.1145/360933.360975>
- William Ferreira, Matthew Hennessy, and Alan Jeffrey. 1996. A Theory of Weak Bisimulation for Core CML. In *Proceedings of the 1996 ACM SIGPLAN International Conference on Functional Programming, ICFP 1996, Philadelphia, Pennsylvania, USA, May 24-26, 1996*, Robert Harper and Richard L. Wexelblat (Eds.). ACM, 201–212. <https://doi.org/10.1145/232627.232649>
- Jay L. Gischer. 1988. The equational theory of pomsets. *Theoretical Computer Science* 61, 2 (1988), 199–224. [https://doi.org/10.1016/0304-3975\(88\)90124-7](https://doi.org/10.1016/0304-3975(88)90124-7)
- Gordon D. Plotkin and Vaughan R. Pratt. 1996. Teams can see pomsets. In *Partial Order Methods in Verification, Proceedings of a DIMACS Workshop, Princeton, New Jersey, USA, July 24-26, 1996 (DIMACS Series in Discrete Mathematics and Theoretical Computer Science, Vol. 29)*, Doron A. Peled, Vaughan R. Pratt, and Gerard J. Holzmann (Eds.). DIMACS/AMS, 117–128. <https://doi.org/10.1090/dimacs/029/07>
- Anton Podkopaev, Ori Lahav, and Viktor Vafeiadis. 2019. Bridging the gap between programming languages and hardware weak memory models. *Proc. ACM Program. Lang.* 3, POPL (2019), 69:1–69:31. <https://doi.org/10.1145/3290382>