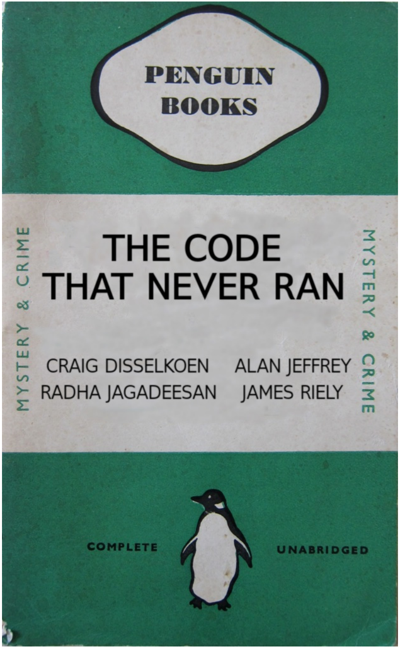
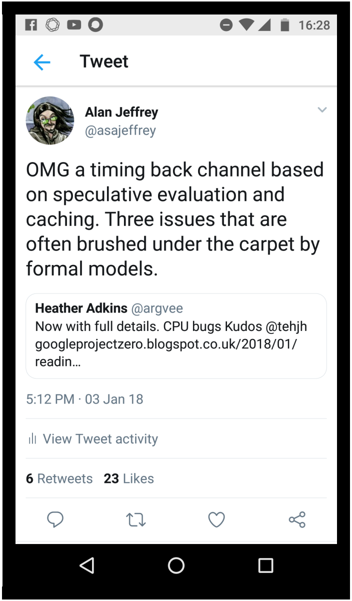


A classic locked-room mystery.
Eve was in the false branch of a
conditional the whole time,
how could she do it?

Mozilla Research | DePaul University | U. California San Diego

Why? Spectre!



Alan Jeffrey @asajeffrey

OMG a timing back channel based on speculative evaluation and caching. Three issues that are often brushed under the carpet by formal models.

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Now with full details. CPU bugs Kudos @tehjh googleprojectzero.blogspot.co.uk/2018/01/readin…

5:12 PM · 03 Jan 18

6 Retweets **23** Likes

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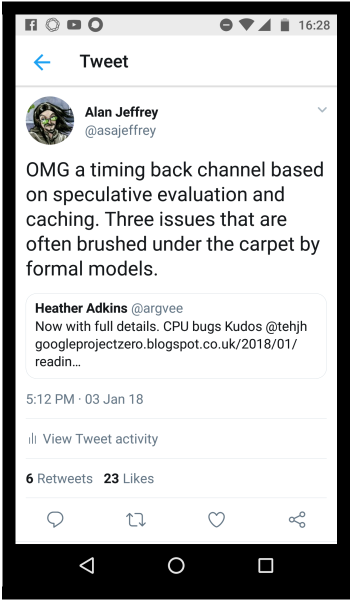

16:28

Tweet

Alan Jeffrey
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View Tweet activity

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Allows reading whole process address space.

Attacks bypass dynamic security checks:

```
if canRead(SECRET) {
  doStuffWith(SECRET);
}
```

Most formal models ignore code in branches that aren't taken.

Models that include speculation?

There are some models that include speculation *relaxed memory models*:

- *The Java Memory Model*
  Manson, Pugh and Adve, 2005.
- *Generative Operational Semantics for Relaxed Memory Models*
  Jagadeesan, Pitcher and Riely, 2010.
- *A promising semantics for relaxed-memory concurrency*
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Question: is there a simple model similar to those of relaxed memory, that can model speculation?

Information flow attacks on speculation

Speculation happens in many places:

- *Speculation in hardware* (branch prediction,. . .)
- *Transactions* (transactional memory,. . .)
- *Relaxed memory* (compiler optimizations,. . .)

Information flow attacks on speculation

Speculation happens in many places:

- *Speculation in hardware* (branch prediction,. . .)
  Attacked by Spectre (Kocher *et al.* 2019).
- *Transactions* (transactional memory,. . .)
  Attacked by Prime+Abort (Disselkoen *et al.* 2017).
- *Relaxed memory* (compiler optimizations,. . .)
  No known attacks.

Question: are there information flow attacks against compiler optimizations?

Contributions

- A simple compositional model.
- Attacks (including a new attack on relaxed memory).
- Experiments (testing practicality of new attacks).

Pomsets

C11-style models are based on *events*
with *labels* (e.g. $(\mathsf{R}\,x\,3)$ or $(\mathsf{W}\,x\,3)$)
and *relations* (e.g. happens-before or reads-from).

Pomsets

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Only one relation, a partial order modeling dependency

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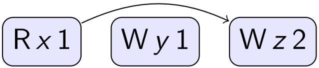

R x 1

W y 1

W z 2

is an execution of ($r := x$; $y := 1$; $z := r + 1$).

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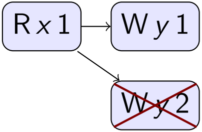

is an execution of ($\texttt{if}\,(x)\,\{\,y := 1\,\}\,\texttt{else}\,\{\,y := 2\,\}$).

Compositional pomset model

First off, straight-line code.

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New idea: put preconditions on events

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$$\boxed{r = 1 \mid \mathrm{W}\, z\, 2}$$

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$$\boxed{\mathsf{W}\,y\,1} \qquad \boxed{r = 1 \mid \mathsf{W}\,z\,2}$$

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Note: no dependency because r does not depend on $y := 1$.

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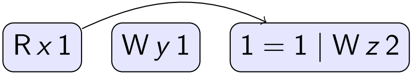

is an execution of $(r := x\,;\ y := 1\,;\ z := r + 1)$.

Note: dependency because r depends on $r := x$.
Also note: performing a substitution $[1/r]$.

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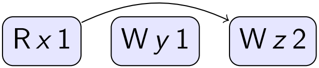

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Visualize: elide tautologies

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when $r \neq 0$

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$$\boxed{r = 0 \mid \mathsf{W}\, y\, 2}$$

is an execution of ($y := 2$)
when $r = 0$

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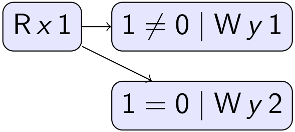
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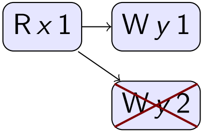

is an execution of $(r := x\,;\,\texttt{if}\,(r)\,\{\,y := 1\,\}\,\texttt{else}\,\{\,y := 2\,\})$

Visualize: elide tautologies and cross out unsatisfiables

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But. . .

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But. . . any execution of C should be an execution of $\texttt{if}\ M\ \{\ C\ \}\ \texttt{else}\ \{\ C\ \}$

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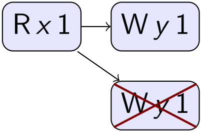

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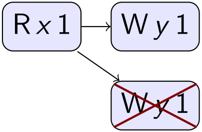

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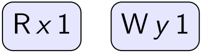

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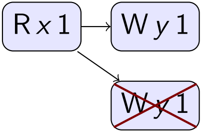

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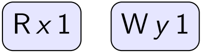

New idea: events from different branches can merge.

Compositional pomset model

Lastly, concurrency.

Compositional pomset model

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Old idea: match reads with matching writes (à la C11)

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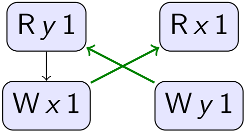

is an execution of $(x := y \parallel r := x ; y := 1)$.

Compositional pomset model

Glossed over some details:

- 3-valued pomsets for negative constraints $d \not< e$,
- sanity conditions on reads-from,
- precise rules for dependency,
- variable declaration,
- . . .

All in the paper!

Information flow example

Imagine a SECRET, protected by a run-time security check:

```
if canRead(SECRET) { ... use SECRET ... } else { ... }
```

For attacker code canRead(SECRET) is always false

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$$\texttt{if}\ \texttt{canRead}(\texttt{SECRET})\ \{\ \ldots \text{use}\ \texttt{SECRET} \ldots\ \}\ \texttt{else}\ \{\ \ldots\ \}$$

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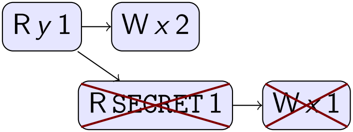

is an execution of
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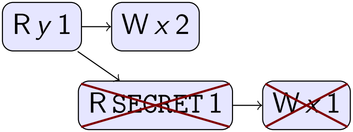

is an execution of
$\mathtt{if}\ y\,\{\,\mathtt{if}\ \mathtt{canRead}(\mathtt{SECRET})\,\{\,x := \mathtt{SECRET}\,\}\,\mathtt{else}\,\{\,x := 2\,\}\,\}$.

Attacker goal: learn if SECRET is 0 or 1.

Modeling Spectre attack

Spectre uses cache timing to discover if a memory location has been touched.

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Glossing over a lot of details, this is

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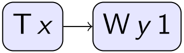

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$$\texttt{if}\,\texttt{touched}\,(x)\,\{\cdots\}\,\texttt{else}\,\{\cdots\}$$

Modeled with a new action $(\mathsf{T}\,x)$, e.g.

$$\begin{tikzcd} \boxed{\mathsf{T}\,x} \arrow[r] & \boxed{\mathsf{W}\,y\,1} \end{tikzcd}$$

is an execution of $\texttt{if}\,\texttt{touched}\,(x)\,\{\,y := 1\,\}$.

Require that if there is an event labeled $(\mathsf{T}\,x)$ then there must be an event labeled $(\mathsf{R}\,x\,v)$ or $(\mathsf{W}\,x\,v)$.

Modeling Spectre attack

A very simplified Spectre attack:

```
if canRead(SECRET) { a[SECRET] := 1 }
else if touched (a[0]) { x := 0 }
else if touched (a[1]) { x := 1 }
```

Modeling Spectre attack

A very simplified Spectre attack:

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if canRead(SECRET) { a[SECRET] := 1 }
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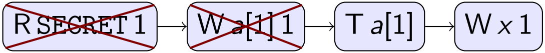
```

e.g. with execution



~~R SECRET 1~~ → ~~W a[1] 1~~ → T $a[1]$ → W x 1

Information flow from SECRET to x.

Modeling Prime+Abort attack

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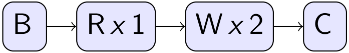

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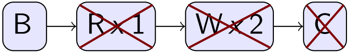

are executions of `begin`; $x := x + 1$; `end`

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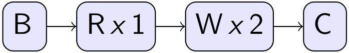
B → R x 1 → W x 2 → C

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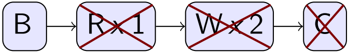
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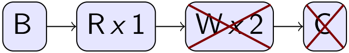
are executions of `begin`; $x := x + 1$; `end`, but *not*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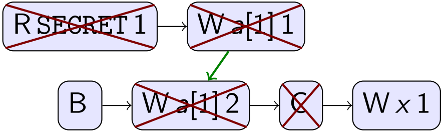
Modeling Prime+Abort attack

Transactions are fine, but not if we add a reason for an abort.

If the attacker knows an aborted transaction does so because of a read/write or write/write conflict, then in

$$\texttt{if canRead(SECRET)}\,\{\, a[\texttt{SECRET}] := 1 \,\} \parallel \\ \texttt{begin};\, a[1] := 2;\, \texttt{loop};\, \texttt{end};\, x := 1$$

the transaction aborts only when SECRET is 1.



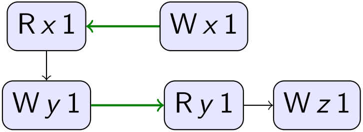
Information flow from SECRET to x.

New store reordering attack

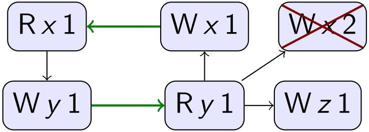
An attack on relaxed memory, *discovered from this model*.

```
y := x || if (y == 0) { x := 1 }
          else if (canRead(SECRET)) { x := SECRET }
          else { x := 1; z := 1 }
```

If SECRET is 1, there is an execution:



If SECRET is 2, there is no execution:

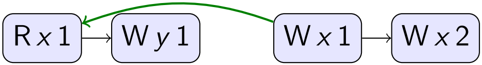


New dead store elimination attack

Another attack *discovered from this model*.

```
y := x || x := 1;
         if (canRead(SECRET)) { if (SECRET) { x := 2 } }
         else { x := 2 }
```

If SECRET is 1, there is an execution:



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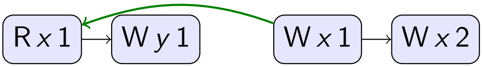
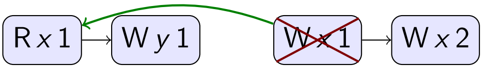


If dead store elimination is performed, there is *no* execution:



Implementing the new attacks

Spectre and Prime+Abort are implemented.
What about the attacks on compiler optimizations?

Implementing the new attacks

Spectre and Prime+Abort are implemented.
What about the attacks on compiler optimizations?

Yes

Implementing the new attacks

Spectre and Prime+Abort are implemented.
What about the attacks on compiler optimizations?

Yes, under unrealistic assumptions:

- `SECRET` is a constant known at compile-time,
- `canRead(SECRET)` is a run-time check.

Implementing load/store reordering

x86 assembly generated by gcc for the main thread of a variant of the load-store reordering attack:

If SECRET is 0:

```
  mov SECRET(%rip), %eax
  mov $1, x(%rip)
  test %eax, %eax
  je label1
  mov $0, x(%rip)
label1:
  mov y(%rip), %eax
  test %eax, %eax
  sete %eax
```

Writes x then reads y, so can read 1

If SECRET is 1:

```
  mov SECRET(%rip), %eax
  mov y(%rip), %eax
  mov $1, x(%rip)
  test %eax, %eax
  sete %eax
```

Reads y then writes x, so cannot read 1

A forwarding thread copies x to y.

Implementing load/store reordering

To make this attack more likely, introduce a small delay between write of x and read of y, increases probability of round trip.

Experimentally gcc will reorder load/store across 30 straight-line instructions.

Repeat attack to leak multiple bits, and increase probability of success.

Attack is 99.9% accurate at 100Kbps.

Implementing dead store elimination attack

DSE attack is similar.

Works against clang as well as gcc.

Attack is 99.9% accurate at 400Kbps (clang), 2Mbps (gcc).

Also in the paper

Details of the model, semantics, etc.

Temporal logic for proving invariants (e.g. no thin-air read).

More examples.

Contributions

A model of program execution that includes speculation.

Examples including existing information flow attacks on branch prediction and transactional memory, and new attacks on optimizing compilers.

Experimental evidence about how practical it is to mount the new class of attacks

A temporal logic which supports compositional proof.

`https://github.com/chicago-relaxed-memory/spec-eval`