

National Institute of Technology
Swarthkal, Karnataka.

Assignment 6-02

Name:- Chikkeri Chinmaya

Roll No:- 211IT017

Branch:- Information Technology

Section:- S13 C B1)

Subject:- Digital System Design
[IT110]

Submitted To:-

Maneetha KM Mam

The Design of Register Transfer Level

Q Synchronous Circuit consists of

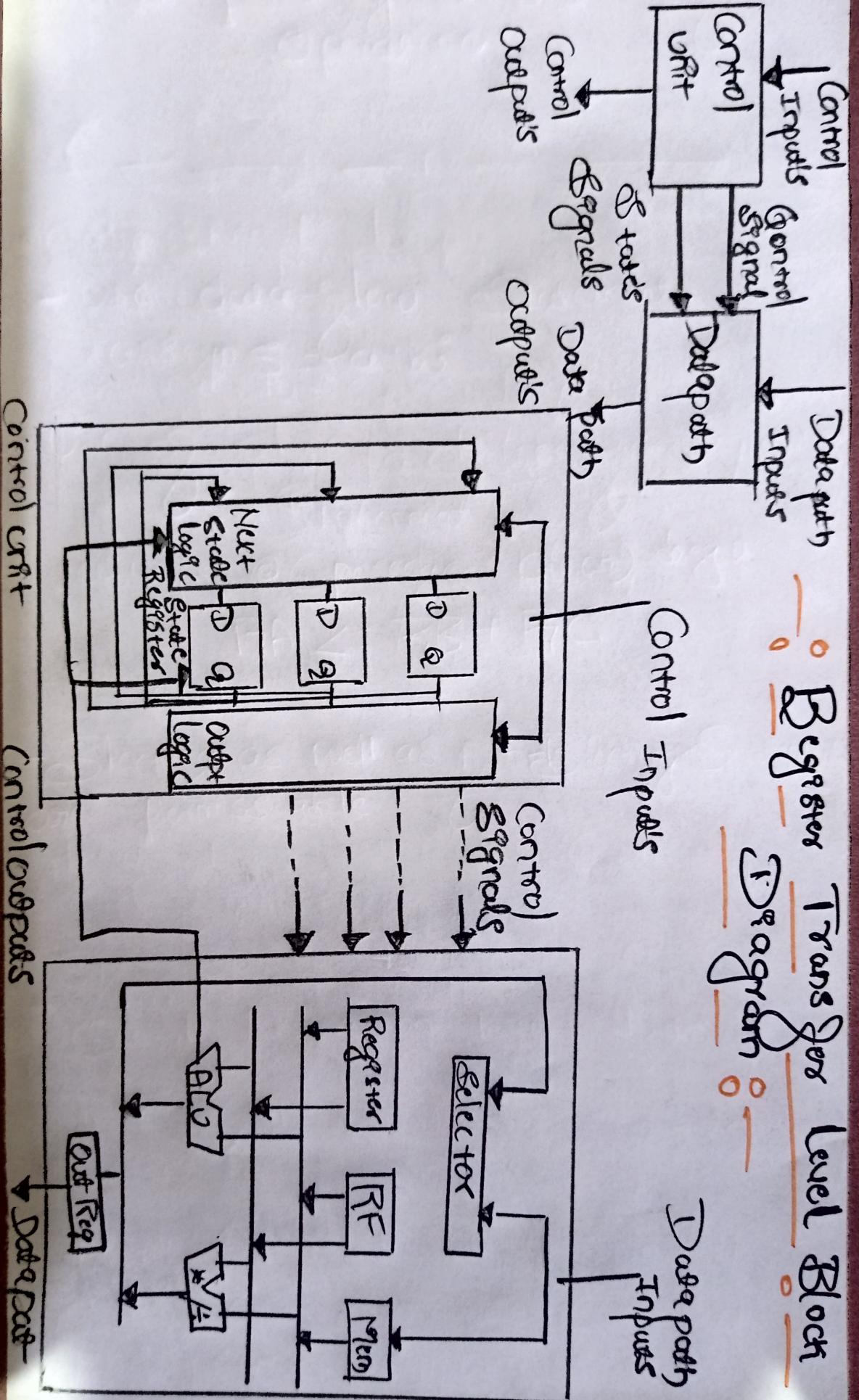
Two kind's of Element's : Register (Sequential) Logic And Combinational Logic.

Registers Usually implemented as D flip-flops

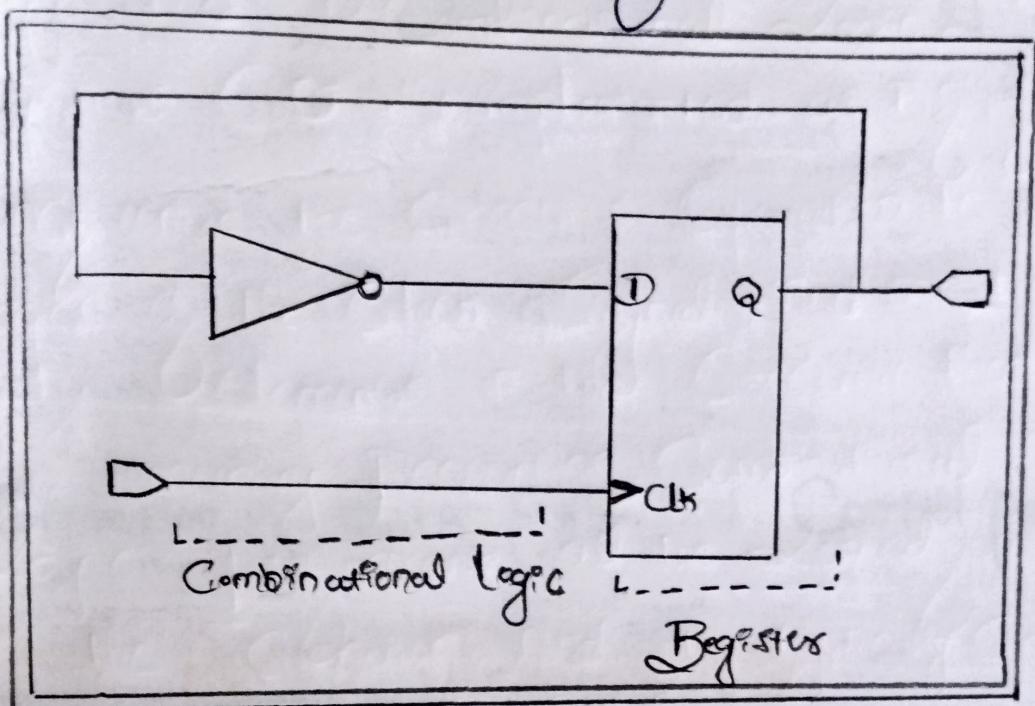
Synchronize the Circuit's Operation to the Edges of the Clock Signal, And are the Only Element's in the Circuits that have memory Properties. Combinational Logic performs all the Logical Functions in the Circuits And it typically consists of Logic gates.

When Designing digital Integrated Circuits with a Hardware description language (HDL), the Designs are Usually Engineered at a higher Level of Abstraction than Transistor level or logic gate level.

In HDL the Designer declares of Register Variable which Roughly Corresponds to Variable in Computer Programming language.



The Combinational logic by using decide that are familiar programming language's such as if - then else And Arithmetic operation. This level is called Register Transfer Level.



- Input is Read from Registers And Output get Written to Registers
 - Directly or Indirectly
 - Chaining of Operation is permissible
- Operations Performed.
 - Arithmetic, Logical, Memory read/write
 - Example
 - $B_1 \leftarrow R_1 + 1$

- Registers are global clock drive.

Implication of RTL Specification

- Operations performed in clock cycle is clear.
 - How many clock cycles required
 - How many hardware resources required
 - What is worst case latency
- Separation of data-path and control path.

Clock Period Discussion:-

- Find the worst case critical path → Decide clock period.
 - One operation may slow entire circuit
 - Overall execution time will be charge
- Decide the clock period → design the data path accordingly
 - put a constraint on design
 - Slow operation are converted into multi cycle operations.

- ① Clock period is decided by fastest operation.

RTL Modelling In Verilog:-

- Combinational Logic
 - Use data-flow Statement
assigns =aths;
- Use of always Block for Sequential Statement
 - always @ (posedge clock) begin
 $RA \leftarrow RB + RC$
end
 - Blocking as well as Non-Blocking Statements are permissible

-:- Programmable Logic Devices :-

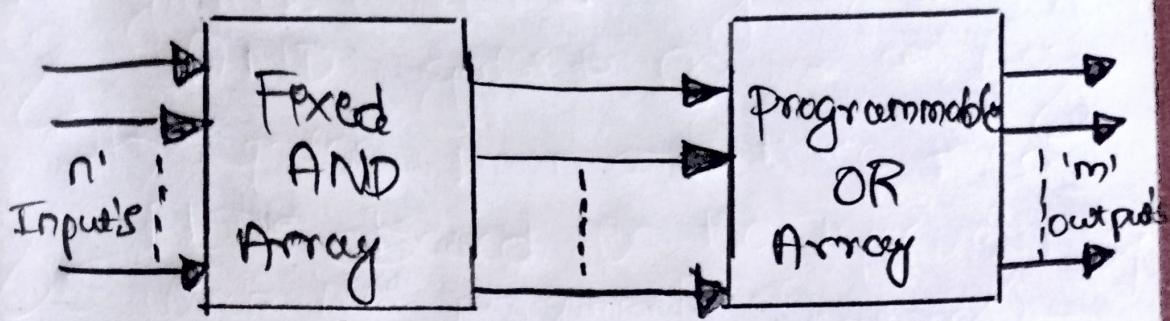
Programmable Logic devices PLDs are Intergrated Circuits. They can an Array of AND gates & Another array of OR Gates. There are three kinds of PLDs Based On the Type of Array which has programmable Features.

- * Programmable Read only Memory
- * Programmable Array Logic
- * Programmable Logic Array

Programmable Read only Memory [PROM]

Read only Memory ROM is memory Device, which stores binary information permanently. that means value can't change that stored information by any means later. if the ROM has programmable feature, then it is called Programmable ROM.

The Block diagram of PROM is shown in following figure.

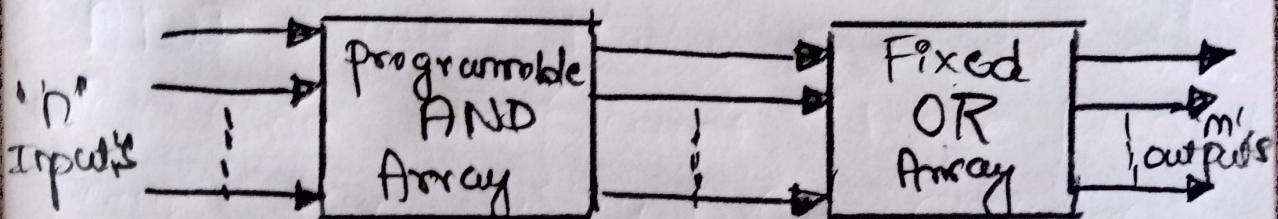


The Inputs of AND gate's are Not of Programmable type. So, we have to generate 2^n Product terms by using n AND gates having n Inputs each. We can Implement these product terms By using $n \times n$ decoder. This Decoder generates ' n ' minterms.

The Inputs of OR Gate's are programmable. That means one can program Any NO. of Required Product terms, Since all outputs of AND gate's are Applied to each OR gate, the output of PROM will be in form of sum of minterms.

Programmable Array Logic [PAL]

PAL is a Programmable logic device that has programmable AND array & fixed OR array. The Advantage of PAL is that we can generate only the required Product terms of Boolean function instead of generating all the Minterm terms by using Programmable AND gate. The Block diagram shown below:-

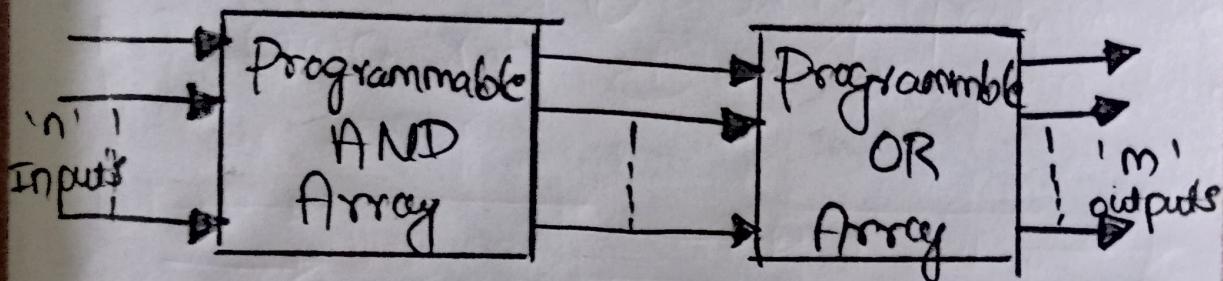


The Inputs of AND gates are programmable. Each AND gate has completed inputs of both normal and variables. Based on those inputs, we can program AND gates. We can generate product terms by using AND gates.

Inputs of OR gates are not programmable. Number of inputs to each OR gate will be fixed type. Apply these required product terms to each OR gate as inputs. The outputs of PAL will be sum of products form.

Programmable Logic Array [PLA] :-

PLA is a programmable logic device that has Both Programmable AND array & Programmable OR array. Hence, it is the most flexible PLD. The Block Diagram of PLA is shown in Figure.



The Inputs of AND gates are programmable. That means each AND gate has Both Normal And Complemented Inputs of Variables. Based on the requirement we can program any of these inputs. We can generate only the Required Product terms By using these AND gates.

The Inputs of OR gates are also programmable. We can program any Number of Required Product terms, since all the Outputs of AND gates are Applied as Inputs to each OR gates. the Outputs of PLA be in form of sum of Product form.