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IT LAB EXAM

DATE:- 21/04/22

① Ans: (b)

The given SR flip-flop And the desired flip-flop is D flip-flop.

D-glop-glop	Present State	Next State
D	$Q_t$	$Q_{t+1}$
0	0	0
0	1	0
1	0	1
1	1	1

SR flip-flop has Two Inputs S & R.  
the Execution Values of SR-flip-flop  
the Combination of Present State  
And Next State.

D - glop-glop Input	Present State	Next State	SR flip-flop Inputs	
D	$Q_t$	$Q_{t+1}$	S	R
0	0	0	0	X
0	1	0	0	1
1	0	1	1	0
1	1	1	X	0

the Boolean function is  $S = d_3 + m_2$   
 $R = m_1 + d_0$

K-Map's :- 2 Variables  K-Map

For  $S$

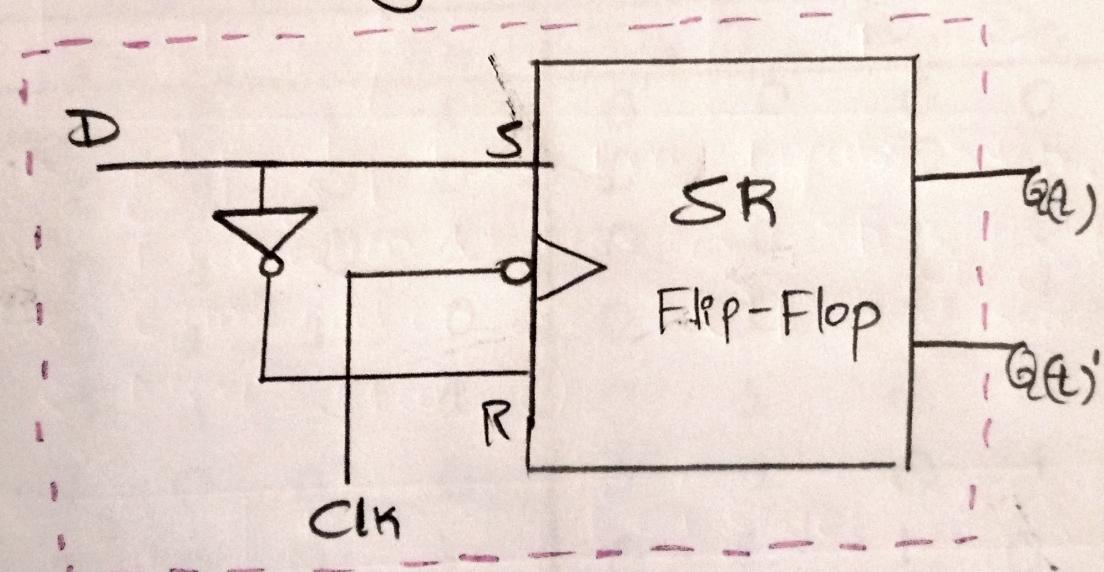
		Q(t)	D
		0	1
		0	
		1	X

For  $R$

		Q(t)	R
		0	1
		0	X
		1	

$$\text{so } S = D \text{ & } R = D'$$

Circuit Diagram :-



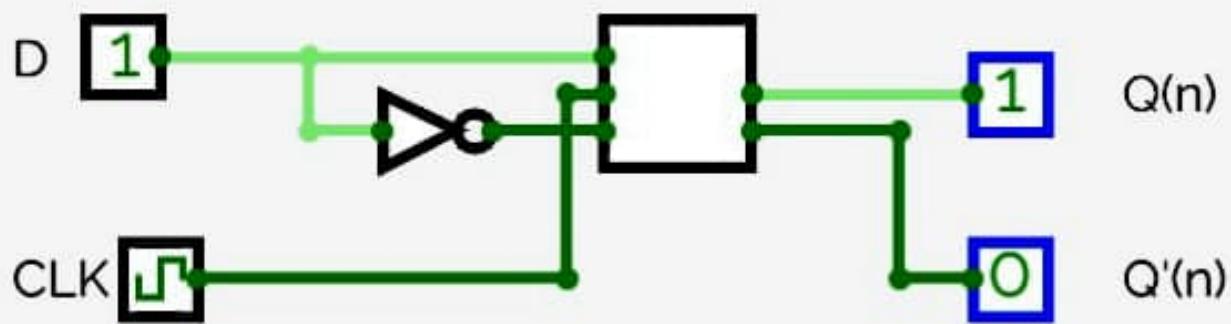
D-Flip-flop

\* SR flip-flop and an inverter

so single  Input, D & Two points

\*  $Q(t)$  &  $Q(t')$ . Hence D flip-flop

SR Flip Flop



Date : 7.4.22

Q) Answer The Excess -3 Binary Code  
as an Example of a Self-Complementary  
BCD Code.

As 4 Bit Excess -3 Code Starts from 3  
And end at 12 C Inputs 0, 1, 2, 3, 14, 15  
Not possible). For impossible Inputs of  
4 bit Excess -3 Code we use don't  
Care Condition.

Truth Table:-

XS - 3

BCD

X <sub>3</sub>	X <sub>2</sub>	X <sub>1</sub>	X <sub>0</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	1
0	1	1	1	0	1	0	0
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1

X3-3

$x_3x_2x_1x_0 = 0000, 0001, 0010 \& 1101, 1110, 1111$ .

are Invalid X3-3 so for that can Insert don't care x, Open K-map.

K<sub>2</sub>-Map's:-

$$D_3 = x_2x_3 + x_3x_1x_0$$

$x_1x_0$	00	01	11	10
$x_3x_2$	00	01	11	10
00	X	0	1	0
01	X	0	X	0
11	0	1	X	1
10	X	0	X	0

$x_1x_0$	00	01	11	10
$x_3x_2$	00	01	11	10
00	X	0	0	1
01	X	0	X	1
11	0	1	X	0
10	X	0	X	1

$$D_2 = \bar{x}_2\bar{x}_1 + x_2x_1x_0 + x_3x_1\bar{x}_0$$

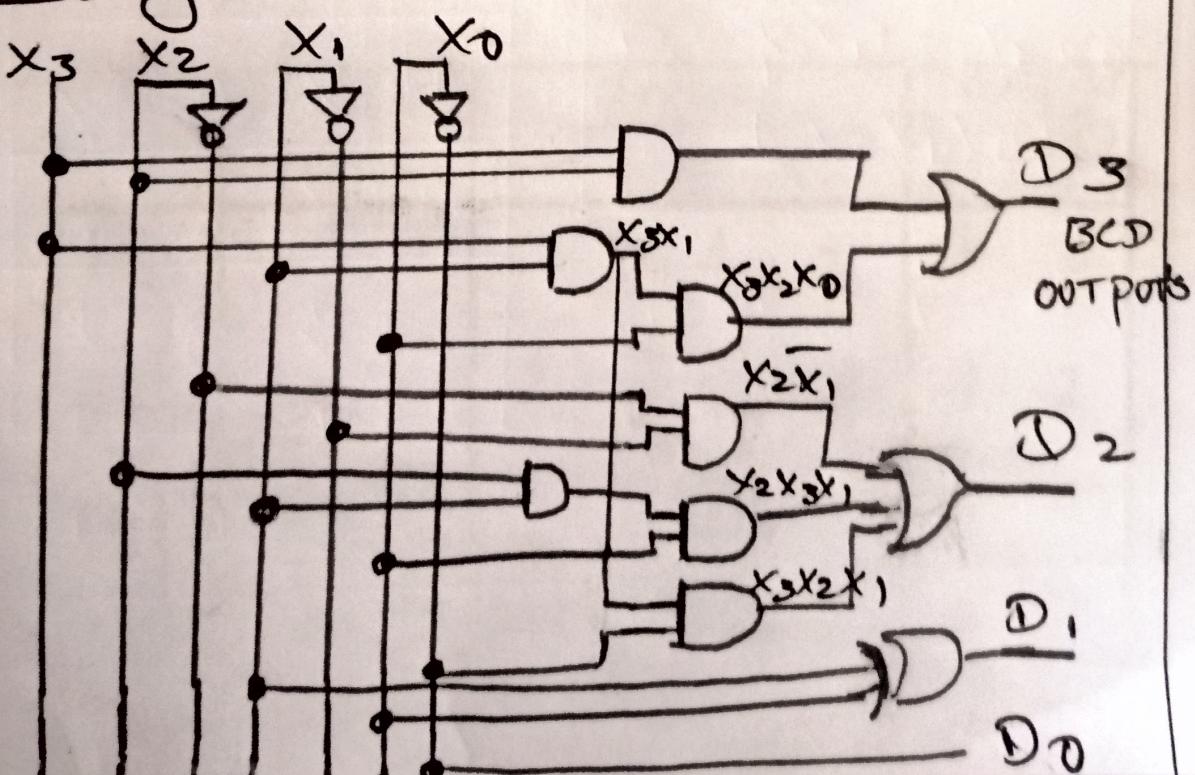
$x_3x_2$	00	01	11	10
$x_1x_0$	00	X 0	0 0	0 0
00	X	0	0	0
01	X 1	X 1		
11	0 0	X 0		
10	X 1	X 1		

$$D_1 = \bar{x}_1x_0 + x_1\bar{x}_0 \\ = x_1 \oplus x_0$$

$x_3x_2$	00	01	11	10
00	X 1 1 1			
01	X 0 X 0			
11	0 0 X 0			
10	X 1 X 1			

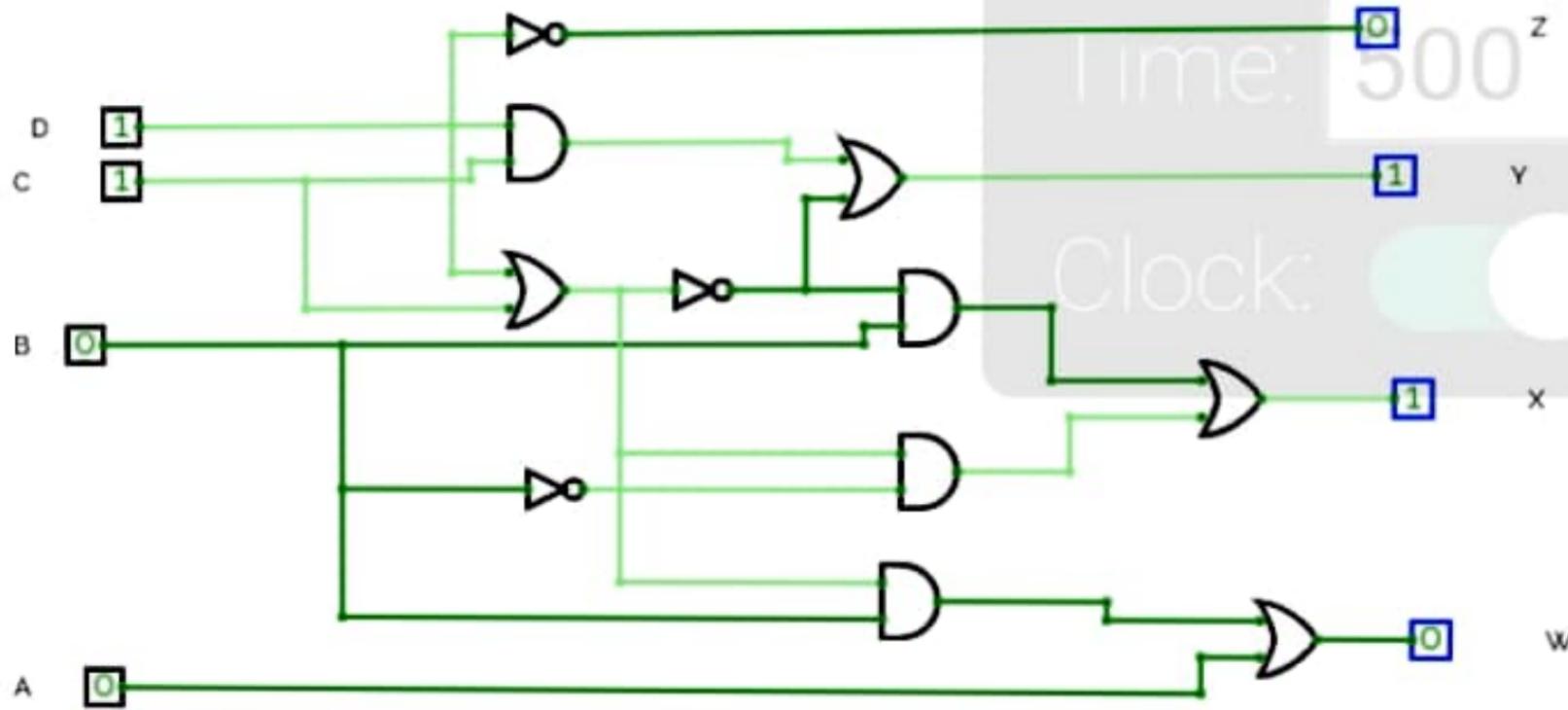
$$D_0 = \bar{x}_0$$

Diagram -



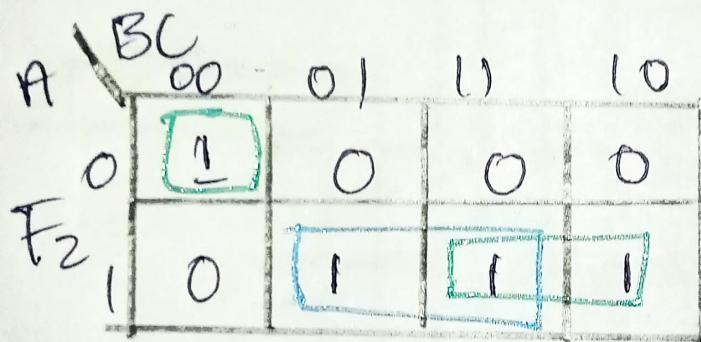
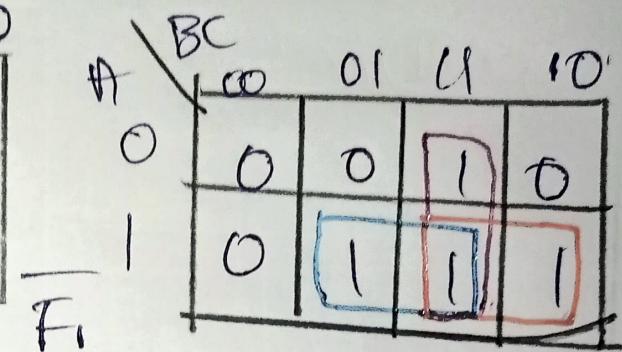
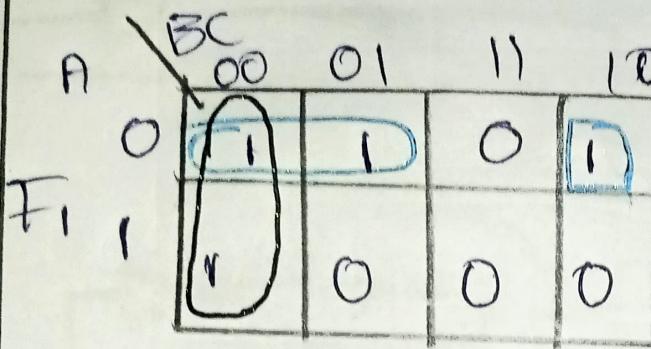
Full Screen

BCD to EXCESS 3 CODE CONVERTER



⊕ Answers :-

K. Map's :-



$$F_1 = AB + AC + BC$$

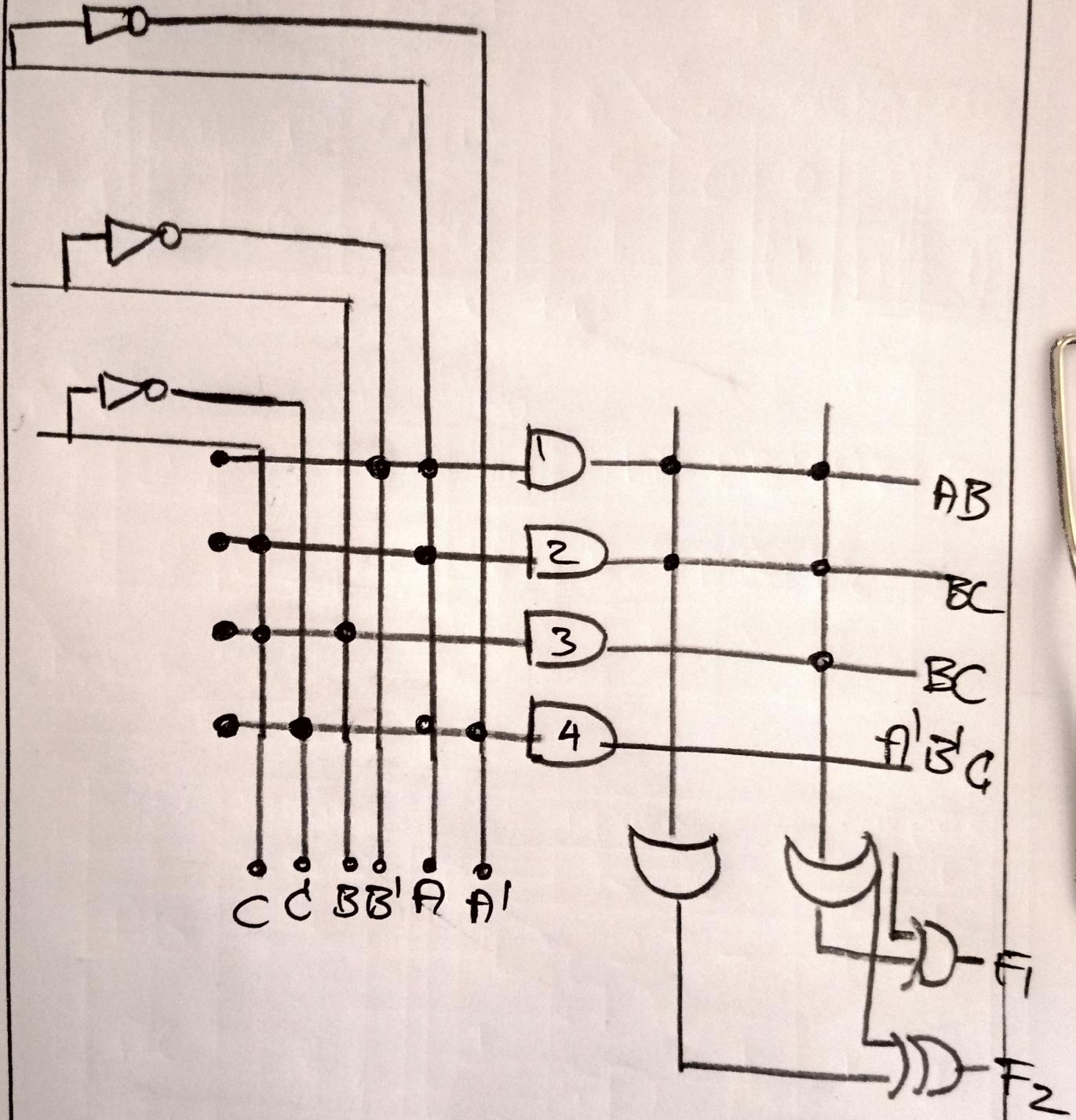
$$F_2 = AB + AC + A'B'C$$

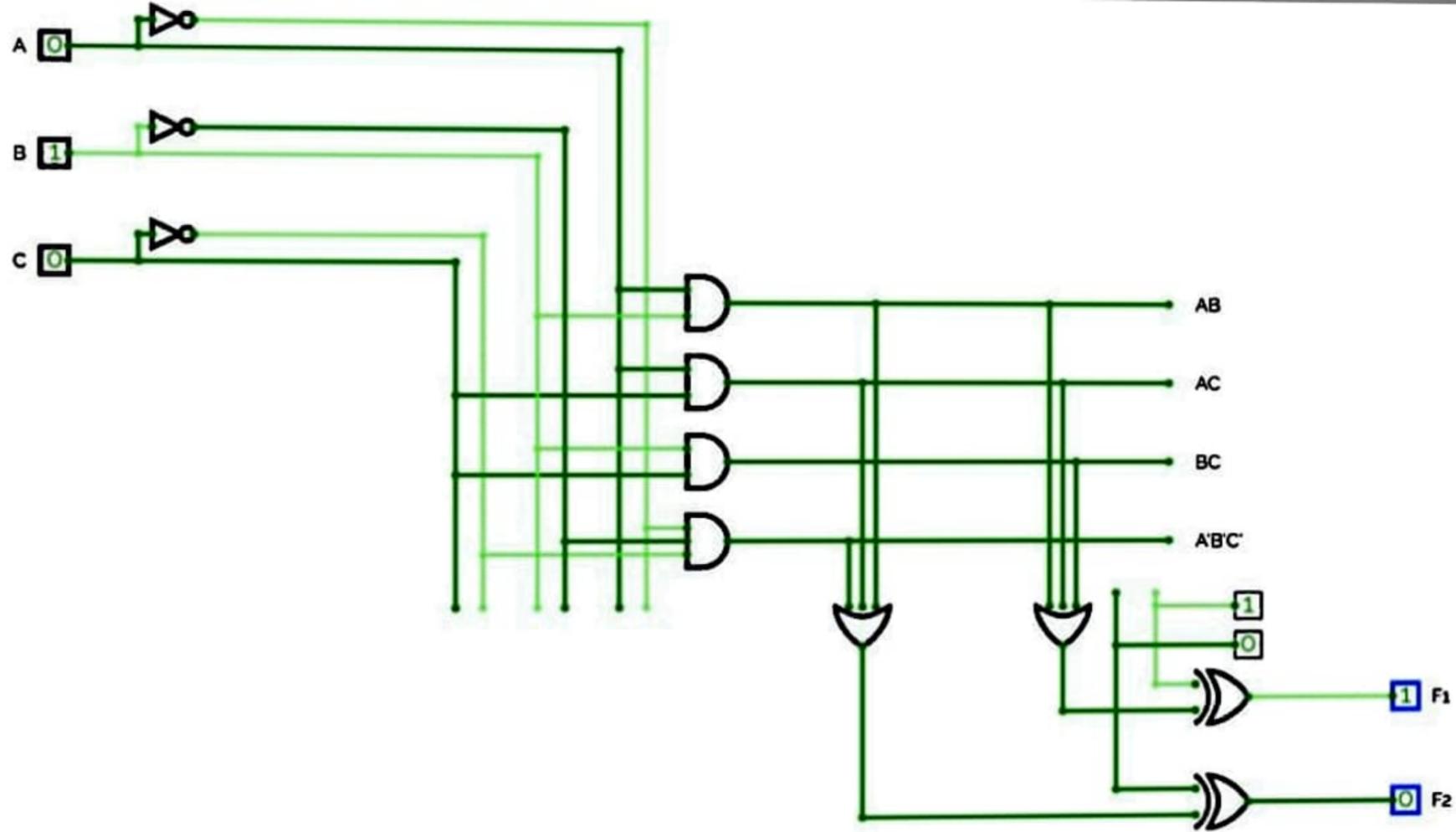
Truth Table :-

	product term	Inputs			Outputs	
		A	B	C	(T)	(C)
					$F_1$	$\bar{F}_1$
AB	1	1	1	-	1	1
AC	2	1	-	1	1	1
BC	3	-	1	1	1	-
$A'B'C$	4	0	0	0	-	1

Date : 7/4/22

# Circuit Diagram -





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## Languages &amp; Libraries

## Testbench + Design

SystemVerilog/Verilog

## UVM / OVM

None

## Other Libraries

None

OVL 2.8.1

SVUnit 2.11

 Enable TL-Verilog Enable Easier UVM Enable VUnit

## Tools &amp; Simulators

Icarus Verilog 0.9.6

## Compile Options

-Wall

## Run Options

Run Options

 Open EPWave after run Download files after run

## Examples

## Community

Collaborate

Forum

## testbench.sv

```
1 // Code your testbench here
2 // or browse Examples
3 //CHIKKERI CHINMAYA 211IT017
4 module jkff_test;
5 reg j,k, clk,reset;
6 wire q;
7
8 jk_ff ob(.j(j)..k(k)..clk(clk)..reset(reset)..q(q));
9
10 initial begin
11   clk= 0;
12   forever #5 clk =~clk;
13 end
14 initial begin
15   $dumpfile("test.vcd");
16   $dumpvars(1);
17
18   reset=1;
19   j= 1; k= 1;
20   #5 reset =0;
21   repeat(10) @ (posedge clk) begin
22     $display("j=%0h,k=%0h,q=%0h",j,k,q);
23     j = $random;
24     k = $random;
25   end
26 end
```

## design.sv

```
1 //CHIKKERI CHINMAYA 211IT017
2 // Code your design here
3
4 module jk_ff ( input j,input k,input clk,input reset ,output q);
5   reg q;
6
7   always @ (posedge clk )
8   begin
9     if(reset == 1)
10       q <= 1'b0;
11     else if (j==0 && k==0)
12       q <= q;
13     else if (j==1 && k==0)
14       q <= 1'b1;
15     else if (j==0 && k==1)
16       q <= 1'b0;
17     else
18       q <= ~q;
19   end
20 endmodule
```

SV/Verilog Design

 Log  Share

VCD info: dumpfile test.vcd opened for output.

j=1,k=1,q=x

j=0,k=1,q=0

j=1,k=1,q=1

j=1,k=1,q=0

j=1,k=0,q=1

j=1,k=1,q=0

j=0,k=1,q=0

j=1,k=0,q=1

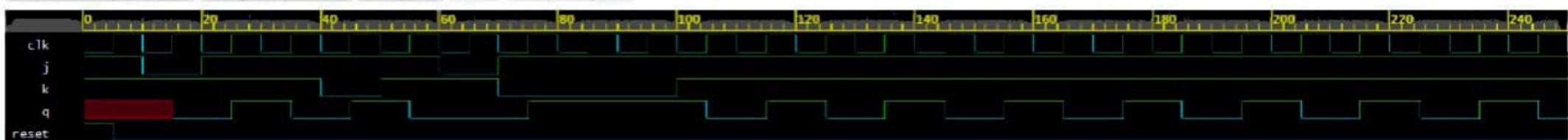
j=1,k=0,q=1

j=1,k=0,q=1

Finding VCD file...

From: 0s To: 250s

Get Signals Radix ▾ 100%



Note: To revert to EPWave opening in a new browser window, set that option on your user page.