Started on	Thursday, 21 April 2022, 2:28 PM
State	Finished
Completed on	Thursday, 21 April 2022, 3:25 PM
Time taken	57 mins 10 secs
Grade	**37.00** out of 50.00 (**74**%)

Question **1**

Complete

Mark 2.00 out of 2.00

In a digital counter circuit feedback loop is introduced to

Select one:

- a. **Asynchronous input and output pulses**
- b. **Reduce the number of input pulse to reset the counter**
- c. **Improve stability**
- d. **Improve distortion**

The correct answer is: **Reduce the number of input pulse to reset the counter**

Question **2**

Complete

Mark 1.00 out of 1.00

S-R type flip-flop can be converted into D type flip-flop if S is connected to R thr

_____

Select one:

- a. **OR Gate**
- b. **Inverter**
- c. **Full Adder**
- d. **AND Gate**

The correct answer is: **Inverter**

Question **3**

Complete

Mark 2.00 out of 2.00

Given a K-map of 4 bit binary (B_4, B_3, B_2, B_1) Minimize and Convert to G_3,G_2, G_1). WHat will be the expression of G_2 ?

B_4B_3 \ B_2B_1	00	01	11	10
00	0	0	1	1
01	1	1	0	0
11	1	1	0	0
10	0	0	1	1

Select one:

- a. **B1 XOR B4**
- b. **B3 XOR B2**
- c. **B4 XOR B2**
- d. **B3 XOR B1**

The correct answer is: **B3 XOR B2**

Question **4**

Complete

Mark 1.00 out of 1.00

Shift registers having 4 bits will enable the shift control Signal for

Select one:

- a. **6 Clock Pulse**
- b. **3 Clock Pulse**
- c. **4 Clock Pulse**
- d. **2 Clock Pulse**

The correct answer is: **4 Clock Pulse**

Question **5**

Complete

Mark 0.00 out of 1.00

Convert (0.7568)10 into an octal number. (Base 10 to Base 8)

Select one:

- a. **(0.60336)8**
- b. **(0.26050)8**
- c. **(0.24040)8**
- d. **(0.19450)8**

The correct answer is: **(0.60336)8**

Question **6**

Complete

Mark 0.00 out of 2.00

Algorithmic state machine , State box in chart represents and which is t

Select one:

- a. **Pulse and next state**
- b. **state and previous state**
- c. **Clock and input**
- d. **Condition and present state**

The correct answer is: **state and previous state**

Question **7**

Complete

Mark 0.00 out of 1.00

The Ability of a register to shift its binary information either to the left or right is

Select one:

- a. **Shift Register**
- b. **Latch Register**
- c. **Binary Register**
- d. **Flip-Flops**

The correct answer is: **Shift Register**

Question **8**

Complete

Mark 0.00 out of 2.00

2' Complement and 1's complement of -18 is ?

Select one:

- a. **00100001 and 11001101**
- b. **10000100 and 11011001**
- c. **00010010 and 11001101**
- d. **10100010 and 11001101**

The correct answer is: **00010010 and 11001101**

Question **9**

Complete

Mark 1.00 out of 1.00

Operator used to trigger an event in HDL is

Select one:

- a. **==**
- b. **$$**
- c. **&**
- d. **@**

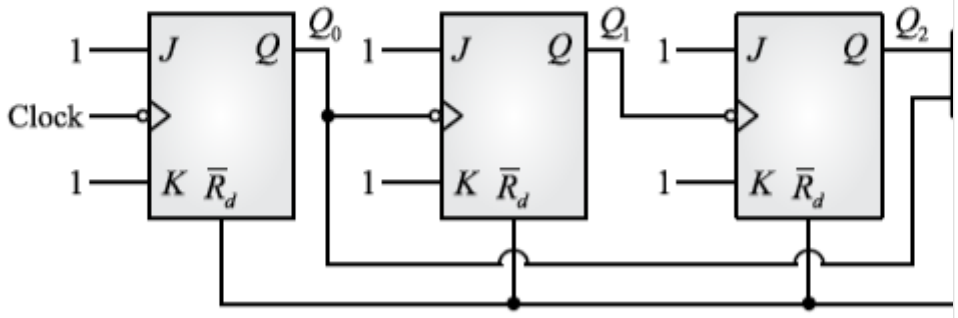
The correct answer is: **@**

Question **10**

Complete

Mark 2.00 out of 2.00

For an JK flip flop shown below each with an active low asynchronou
i.e R_d complement . The counter with relevance to this circuit is



Select one:

- a. **a modulo -6 binary up counter**
- b. **a modulo -6 binary down counter**
- c. **a modulo -5 binary down counter**
- d. **a modulo -5 binary up counter**

The correct answer is: **a modulo -5 binary up counter**

Question **11**

Complete

Mark 1.00 out of 1.00

Carry lookahead logic uses the concepts of _____

Select one:

- a. **Ripple factor**
- b. **Generating and propagating carries**
- c. **Inverting the inputs**
- d. **Complementing the outputs**

The correct answer is: **Generating and propagating carries**

Question **12**

Complete

Mark 2.00 out of 2.00

To add two 17- bit numbers , how many full and half adders are required?

Select one:

- a. **4 half-adders, 13 full-adders**
- b. **1 half-adders, 16 full-adders**
- c. **14 half-adders, 3 full-adders**
- d. **0 half-adders, 17 full-adders**

The correct answer is: **1 half-adders, 16 full-adders**

Question **13**

Complete

Mark 1.00 out of 1.00

.Calculate $(200)_{(10)} - (65)_{(10)}$ using base 5

Select one:

- a. **1065(5)**
- b. **1032(5)**
- c. **1026(5)**
- d. **1024(5)**

The correct answers are: **1065(5)**
, **1024(5)**, **1032(5)**
, **1026(5)**

Question **14**

Complete

Mark 1.00 out of 1.00

Steps involved in the design procedure of Combinational circuits are:

A. Reducing the switching expressions for the outputs
B. Identify the Inputs and outputs from the descriptive question and draw a bloc
C. Framing the switching expressions for the outputs.
D. Implement the simplified expressions using logic gates.
E. Draw the truth table for the expression given.

Select one:

- a. **A, D, E, B, C**
- b. **B, A, E, C, D**
- c. **B, E ,A, C, D**
- d. **A, B, E, C, D**

The correct answer is: **B, E ,A, C, D**

Question **15**

Complete

Mark 1.00 out of 1.00

Convert $6A3B_{16}$ to binary.

Select one:

- a. **0110101010100011**
- b. **101101101010001**
- c. **011010100011101**
- d. **1000101100111111**

The correct answers are:
101101101010001,

0110101010100011,
011010100011101
, **1000101100111111**

Question **16**

Complete

Mark 0.00 out of 1.00

{1'b1, 2'b00,3'b1} will result in

Select one:

- a. **4'b1011**
- b. **4'b1001**
- c. **6'b000001**
- d. **6'b100001**

The correct answer is: **6'b100001**

Question **17**

Complete

Mark 2.00 out of 2.00

A ripple counter of 3 bit constructed using T flip flop of 3 to perform bina
three flip flops have T Inputs fixed at

Select one:

- a. **0 , 0 and 0**
- b. **0, 1 and 1**
- c. **1, 0 and 0**
- d. **1, 1 and 1**

The correct answer is: **1, 1 and 1**

Question **18**

Complete

Mark 2.00 out of 2.00

In the following truth table, V = 1 if and only if the input is valid.

Inputs				Outputs		
D_0	D_1	D_2	D_3	X_0	X_1	V
0	0	0	0	x	x	0
1	0	0	0	0	0	1
x	1	0	0	0	1	1
x	x	1	0	1	0	1
x	x	x	1	1	1	1

Select one:

- a. **Decoder**
- b. **Demultiplexer**
- c. **Priority Encoder**
- d. **Multiplexer**

The correct answer is: **Priority Encoder**

Question **19**

Complete

Mark 2.00 out of 2.00

In PLA, how many programmable fuses are required for 16 inputs and 8 given the 8 OR gates and 32 And Gates.

Select one:

- a. **1270**
- b. **1284**
- c. **1357**
- d. **1348**

The correct answer is: **1284**

Question **20**

Complete

Mark 0.00 out of 2.00

Match List I with List II and select the correct answer form the cod the list A, B, C ???

List I	List II
A. A multiplexer	1. to generate memory can be u
B. A decoder can	2.for parallel to serial conversic
C. A shift register can be	3.converts many signals into o

Select one:

- a. **3 1 2**
- b. **3 2 1**
- c. **2 1 3**
- d. **1 2 3**

The correct answer is: **3 1 2**

Question **21**

Complete

Mark 1.00 out of 1.00

Why is parallel data transmission preferred over serial data transmission for mos applications?

Select one:

- a. **More people use it**
- b. **It is cheaper**
- c. **It is much slower**
- d. **It is much faster**

The correct answer is: **It is much faster**

Question **22**

Complete

Mark 2.00 out of 2.00

The output of which flip flop serves as a source for triggering other flip fl

?

Select one:

- a. **Serial Adder**
- b. **Ripple Counter**
- c. **Parallel Adder**
- d. **Shift Register**

The correct answer is: **Ripple Counter**

Question **23**

Complete

Mark 1.00 out of 1.00

The Keyword @posedge means

Select one:

- a. **Transition from Z to 1**
- b. **Transition from 0 to 1**
- c. **Transition from 0 to 1**
- d. None

The correct answers are:

Transition from 0 to 1, **Transition from 0 to 1**, **Transition from Z to 1**, None

Question **24**

Complete

Mark 2.00 out of 2.00

The simplification in minimal SOP of $Y = F(A,B,C,D) = \Sigma m(0,2,3,6,7) + \Sigma d(8,$ K maps is

Select one:

- a. **Y = Ac'+BD'**
- b. **Y = A'b'+BD**
- c. **Y = Ac+BD'**
- d. **Y = A'c+B'D'**

The correct answer is: **Y = A'c+B'D'**

Question **25**

Complete

Mark 1.00 out of 1.00

The timing signal that is generated using the counter that counts the required num

Select one:

- a. **Reset Signals**
- b. **Pulses**
- c. **Flipflops**
- d. **Latches**

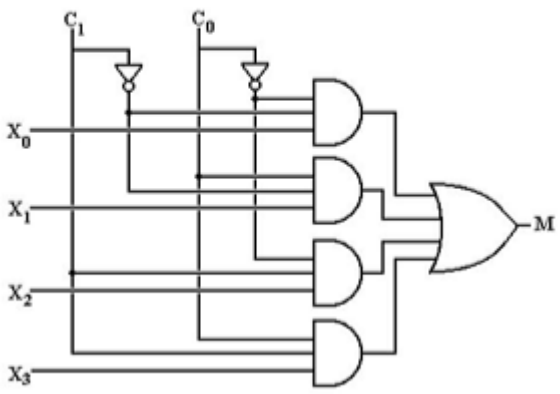
The correct answer is: **Pulses**

Question **26**

Complete

Mark 0.00 out of 1.00

In the given 4-to-1 multiplexer, if c1 = 1 and c0 = 0 then the output M is _____



Select one:

- a. **X1**
- b. **X2**
- c. **X3**
- d. **X0**

The correct answer is: **X2**

Question **27**

Complete

Mark 2.00 out of 2.00

A shift register can be used for

Select one:

- a. **Serial to parallel Conversion**
- b. **Parallel to serial Conversion**
- c. **Digital delay**
- d. **All of the options**

The correct answer is: **All of the options**

Question **28**

Complete

Mark 1.00 out of 1.00

Logic circuitry is used to detect _____

Select one:

- a. **MSD**
- b. **Underflow**
- c. **Overflow**
- d. **LSD**

The correct answer is: **Overflow**

Question **29**

Complete

Mark 1.00 out of 1.00

Carry for the inputs A and B using a half adder is given by _____

Select one:

- a. **A EX-NOR B**
- b. **A XOR B**
- c. **A AND B**
- d. **A OR B**

The correct answer is: **A AND B**

Question **30**

Complete

Mark 0.00 out of 1.00

Programmable Logic Array - which is the true Statement?

Select one:

- a. **Fixed AND Array and Fussed Programmable OR Array**
- b. **Fussed Programmable AND Array and Fussed Programmable OR Array**
- c. **Fussed Programmable AND Array and Fixed OR array**
- d. None

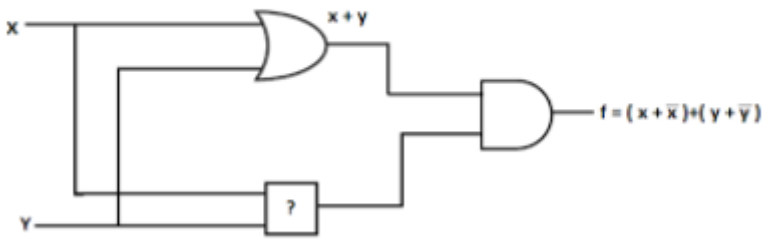
The correct answer is: **Fussed Programmable AND Array and Fussed Programmable OR Array**

Question **31**

Complete

Mark 2.00 out of 2.00

To make the Circuit tautology



(Assume x = 1, y = 1)

Select one:

- a. **OR gate**
- b. **Ex-OR gate**
- c. **AND Gate**
- d. **NAND Gate**

The correct answers are: **OR gate** , **AND Gate**, **NAND Gate**, **Ex-OR gate**

Question **32**

Complete

Mark 0.00 out of 2.00

JK Flip FLop can be converted to D flip flop by converting

Select one:

- a. **J = K = 1**
- b. **J = K**
- c. **J = K'**
- d. **J = K = 0**

The correct answer is: **J = K'**

Question **33**

Complete

Mark 1.00 out of 1.00

The output of a logic gate is 1 when all the input are at logic 0 as shown below:

The gate is either _____

Select one:

- a. **An OR or an EX-NOR**
- b. **A NOR or an EX-NOR**
- c. **An AND or an EX-OR**
- d. **A NAND or an EX-OR**

The correct answer is: **A NOR or an EX-NOR**

Question **34**

Complete

Mark 1.00 out of 1.00

In J K flip flop ,If the output oscillates between 0 and 1 at a certain clock puls
Q is uncertain at end of the clock pulse and this condition is known as

Select one:

- a. **Race around condition**
- b. **Lock out state**
- c. **Conversion condition**
- d. **Forbidden State**

The correct answer is: **Race around condition**

Question **35**

Complete

Mark 1.00 out of 1.00

D flip-flop is a circuit having _____

Select one:

- a. **3 NAND gates**
- b. **5 NAND gates**
- c. **2 NAND gates**
- d. **4 NAND gates**

The correct answer is: **4 NAND gates**

◄ Lab Assignment 6

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