-: National Institute of Technology Surathkal, Karnataka....:-

Lab Assignment: 3

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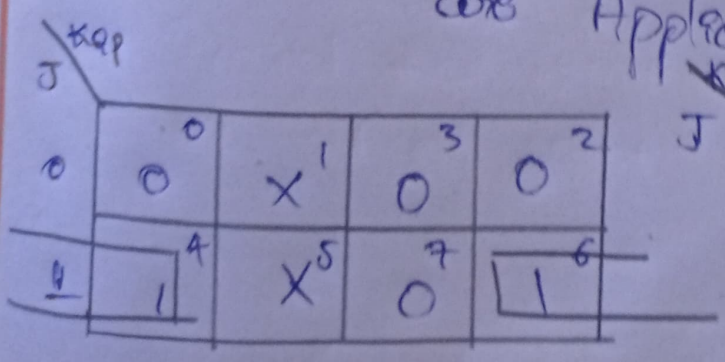
Topic:- IT110 - Digital System Design.

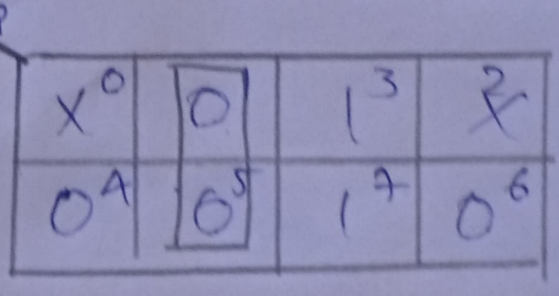
① SR Flip-Flop to JK Flip-flop Conversion.

J and K will be given as External inputs to S And R. A block in logic Diagram below. S And R will be the Outputs of the Combinational Circuit.

J-K Inputs		Out puts		S-R Inputs	
J	K	Q_n	Q_{n+1}	S	R
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	X	0
1	1	0	1	0	1
1	1	1	0	0	1

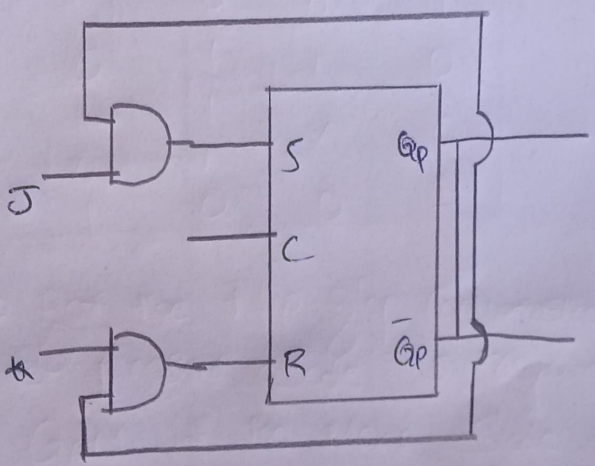
The Truth table for the Flip flop Conversion are given below. The present state is required by Q_n and Q_{n+1} is the Next state to be obtained when the J and K inputs are Applied.

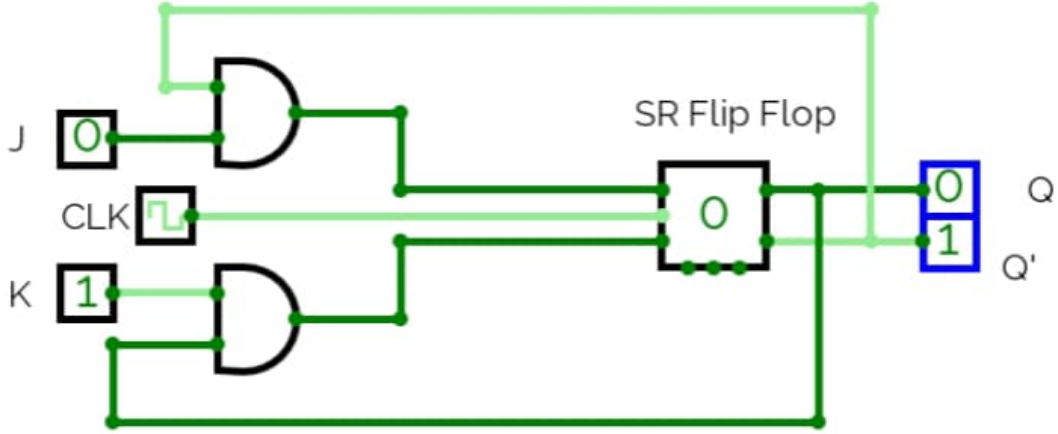




Date :.....

For two Inputs J and K, there will be eight possible Combinations. For each Combination For each Combination of J, K and Qp; the Corresponding Qp+1 States are found. Qp+1 simply suggests the future Values to be obtained by the JK Flip Flop after the Value of Qp. The Table is then Completed by writing the Values of S And R Required to get each Qp+1 from the Corresponding Qp. That is, the Values of SR that Required to Change the State of the Flip flop from Qp to Qp+1 are written.




J
0
CLK
K
1
SR Flip Flop
0
0
1
Q
Q'

② JK Flip-flop to D Flip-flop Conversion.

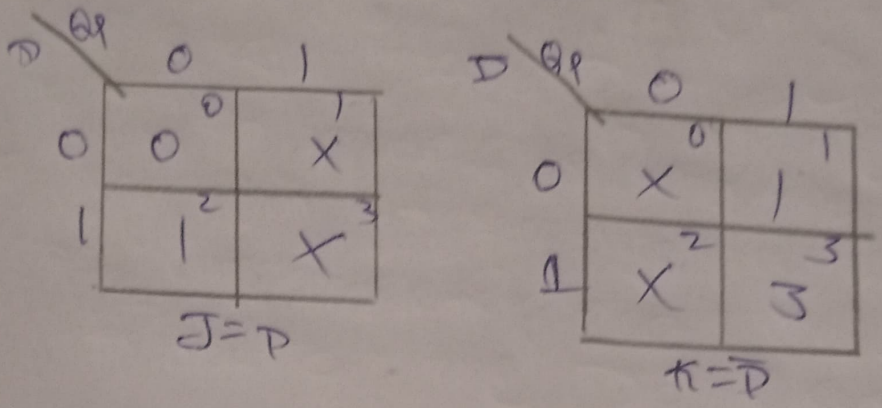
By writing the JK-to D conversion let use a K-map to obtained Logic Expressions for the Inputs for J & K. in terms of D & Q.

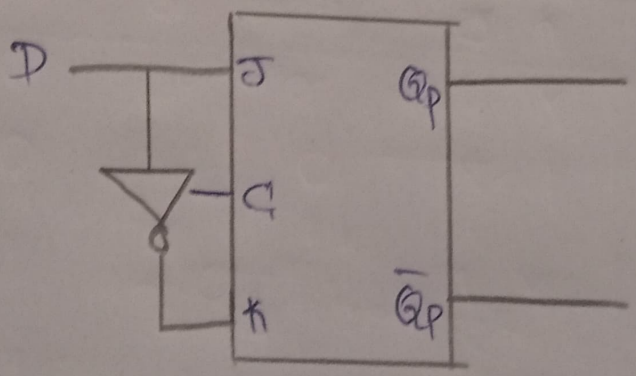
It Can be seen that given JK flip flop can be Converted into a D-type flip flop by Driving J & K inputs pins with the D Inputs & Its Negetation, Respectively. Thus the Additional hardware Components Required would be a NOT gate, Resulting the Digital System.

D Inputs	outputs Qn	Qn+1	J-K Inputs J	K
0	0	0	0	X
0	1	0	X	1
1	0	1	1	X
1	1	0	X	0

We Shall verify our system so as to ensure that it Behaves like we expect.

It can be clearly seen that the entries in the first, second, & sixth columns of the JK-to-D conversion table (shaded in beige) are the same as those in the D flip-flop Truth table. Thus, it can be concluded that the conversion process of JK flip-flop into D-Type.





JK FLIP FLOP USING D FLIP FLOP