Study of a digital PLL in a digital communication chain

SCS Master, 2014-2015

1 – Introduction

The objectives of this workshop is 1) to simulate with MATLAB the behavior of a DPLL 2) to include the DPLL in a baseband digital communication chain

2- Study of the DPLL

2-1 Open Loop

Open the file PLL_QPSK_BO_NDA.m. The DPLL is programmed, except de phase error detector expression.

Plot the detector S_curve for an input phase error range [-180° 180°].

What can you conclude about the phase ambiguity? What solution do you propose to cope with it?

2-1 Closed loop

Loop dimensioning

For a second order loop, the filter coefficients A and B are determined using the file AB.m

Acquisition

Open the file PLL_QPSK_NDA_incomplet.m.

Add the detector in the file.

Plot the PLL response for an input phase error equal to 10°, Eb/No=100 dB and Eb/N0=7 dB. Test several values for the loop noise bandwidth and observe the resulting behaviour.

Plot the PLL response for an input frequency error equal to 1%Rs where Rs is the symbol rate. Take Eb/No=100 dB and Eb/No=7 dB.

Tracking

Plot the phase jitter in function of the loop noise bandwidth for Eb/No=10 dB (use the file PLL_QPSK_jitter_NDA.m).

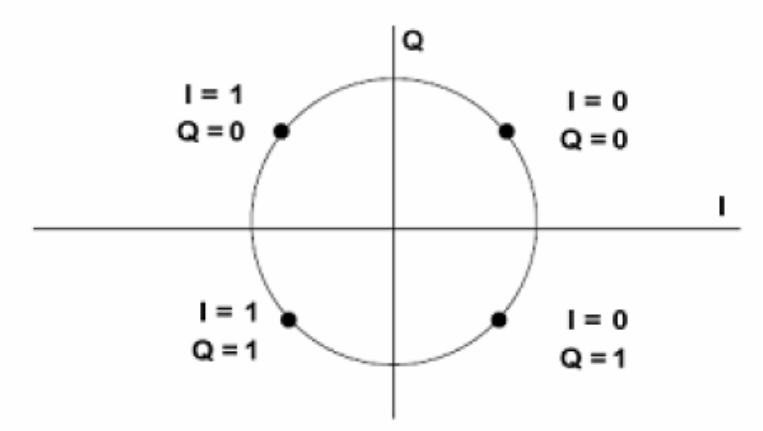
Plot the phase jitter in function of Eb/No for BlT=10-2.5 (use PLL_QPSK_NDA_EbNo.m).

Check if the resulting curves are coherent with the theory which states that

$$\sigma_\varepsilon^2 \quad \propto \quad \frac{B_l T_s}{E_s/N_0}$$

3- Insertion in a digital communication chain

Use the QPSK modulator developed in the SIMCOM workshop.



The emitter filter is a SRRC filter with roll-off equal to 0.35.

Include the DPLL in the reference chain.

Evaluate the loss due to the insertion of the DPLL. What can you conclude?