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CS211 Cache Simulator Report.pdf

For my cache simulator, I used a double array of Lines to simulate my cache. Each Line consists of a tag (a long representation of the tag), a valid bit (integer with value 1 or 0), an order (the long representation of the position in the Line), and a timestamp (long representation of the "time" it was accessed);

When comparing the cache with a prefetcher to the one without a prefetcher there were some very noticeable differences. The cache that did not prefectch data had less reads, less hits, yet more misses. The cache with the prefecther had more reads, more hits, less misses.

These results make perfect sense. The prefectcher would constantly grab extra data from "memory" resulting in more reads. Due to the extra information being stored in the "cache", it allowed for more hits to take place, which of course results in overall less misses.

The two caches did however have the same number of writes. This makes sense because there is no extra writing going on between the two caches.