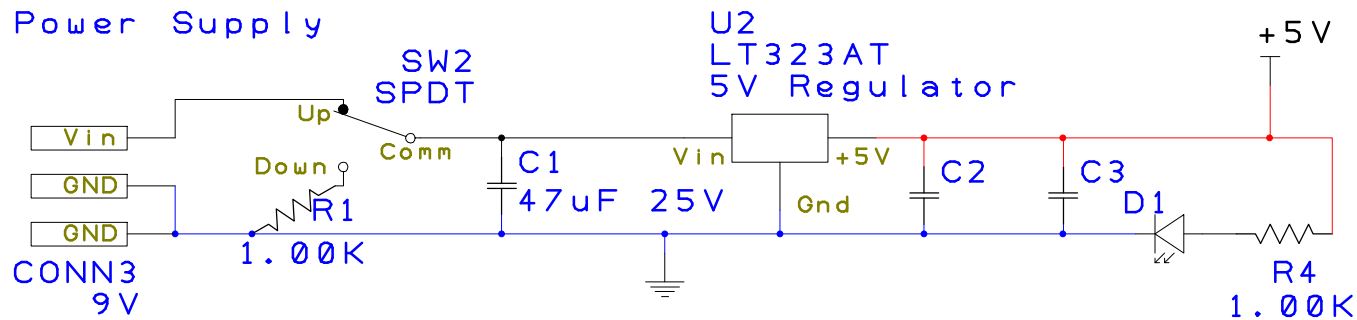
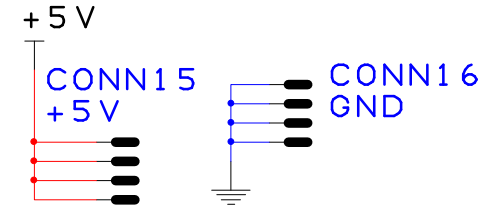


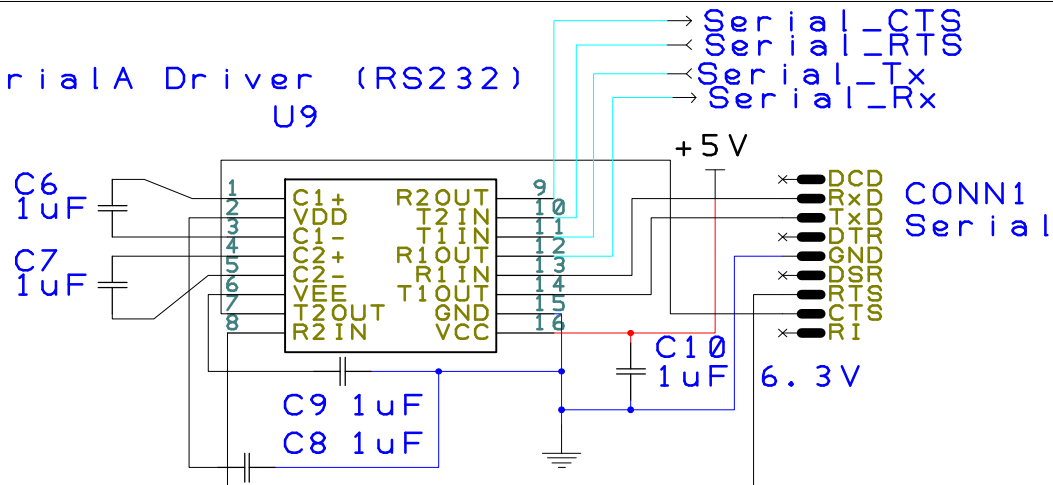
## Power Supply



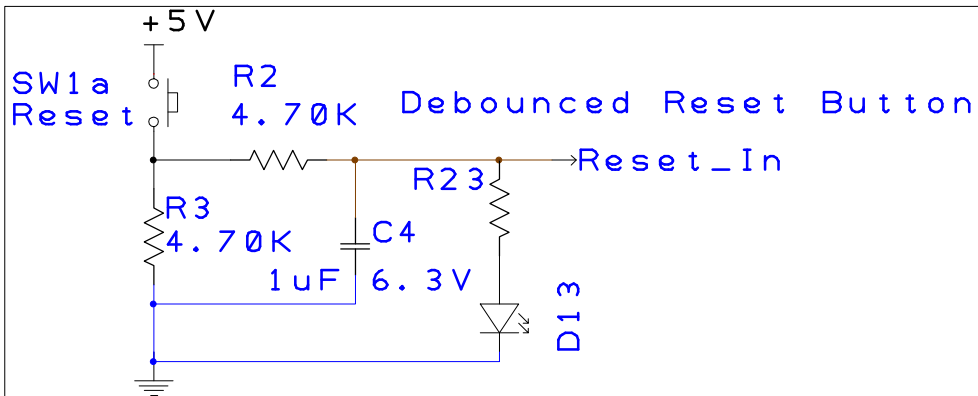
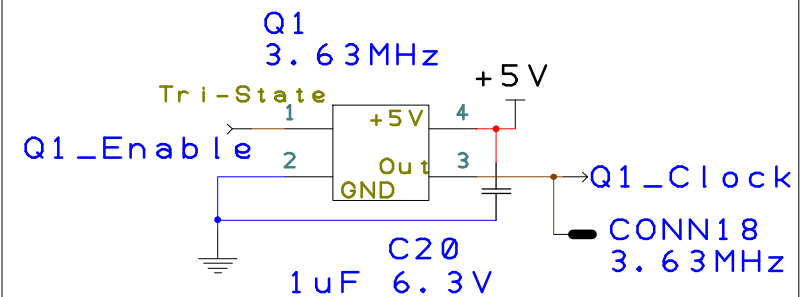
## Extra Power Connectors



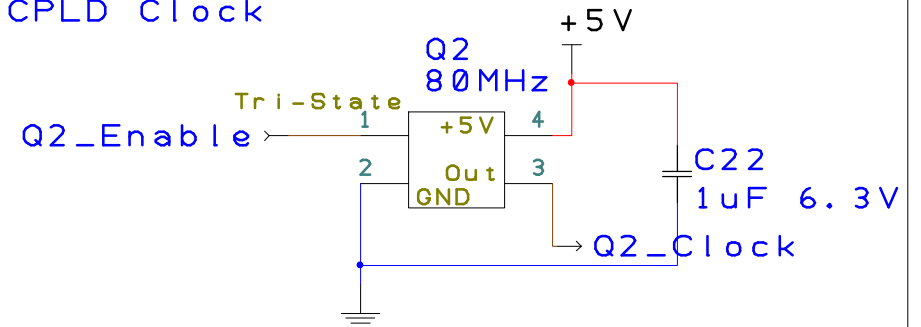
## SerialA Driver (RS232) U9



## DUART Clock



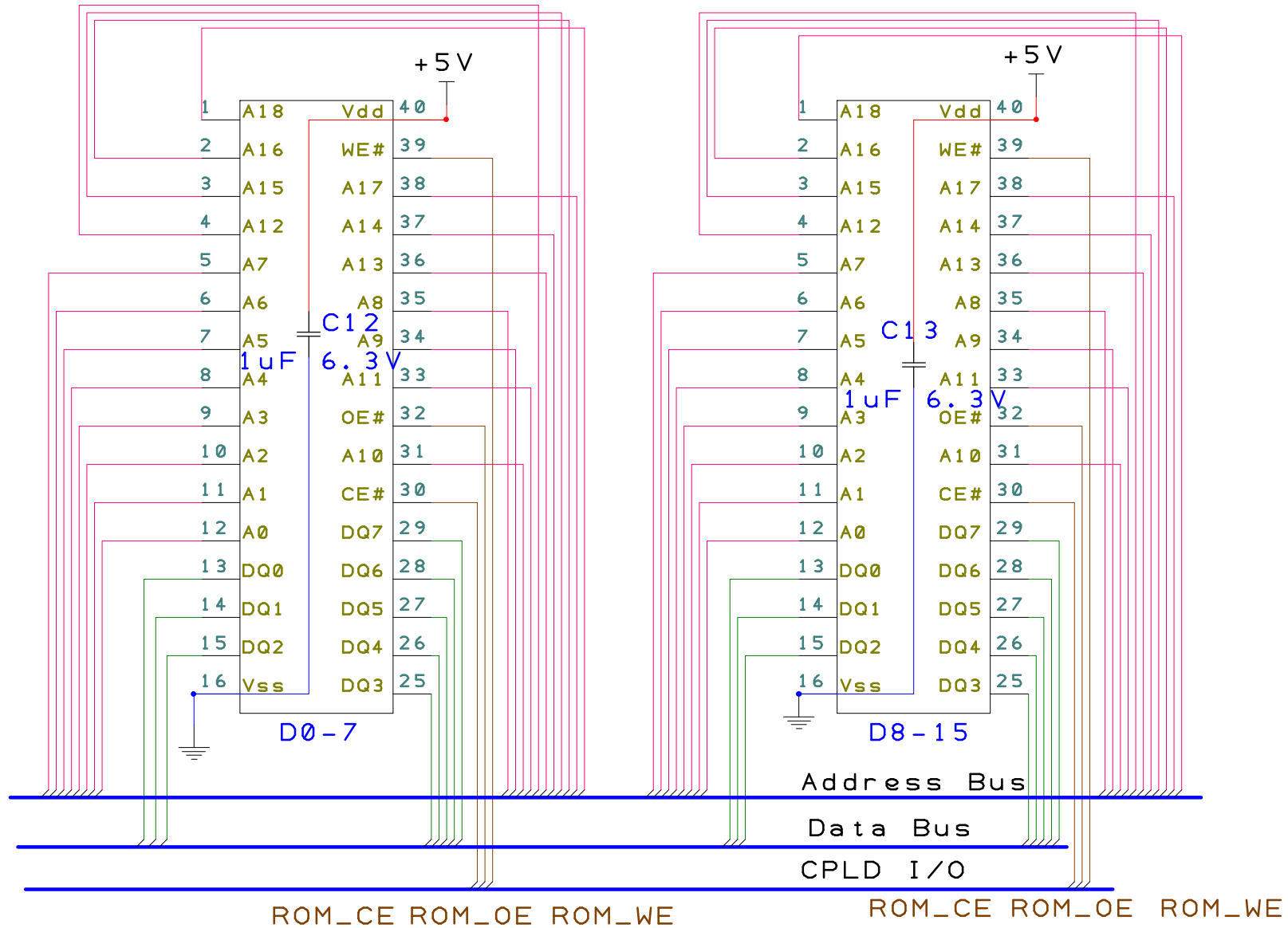
## CPLD Clock





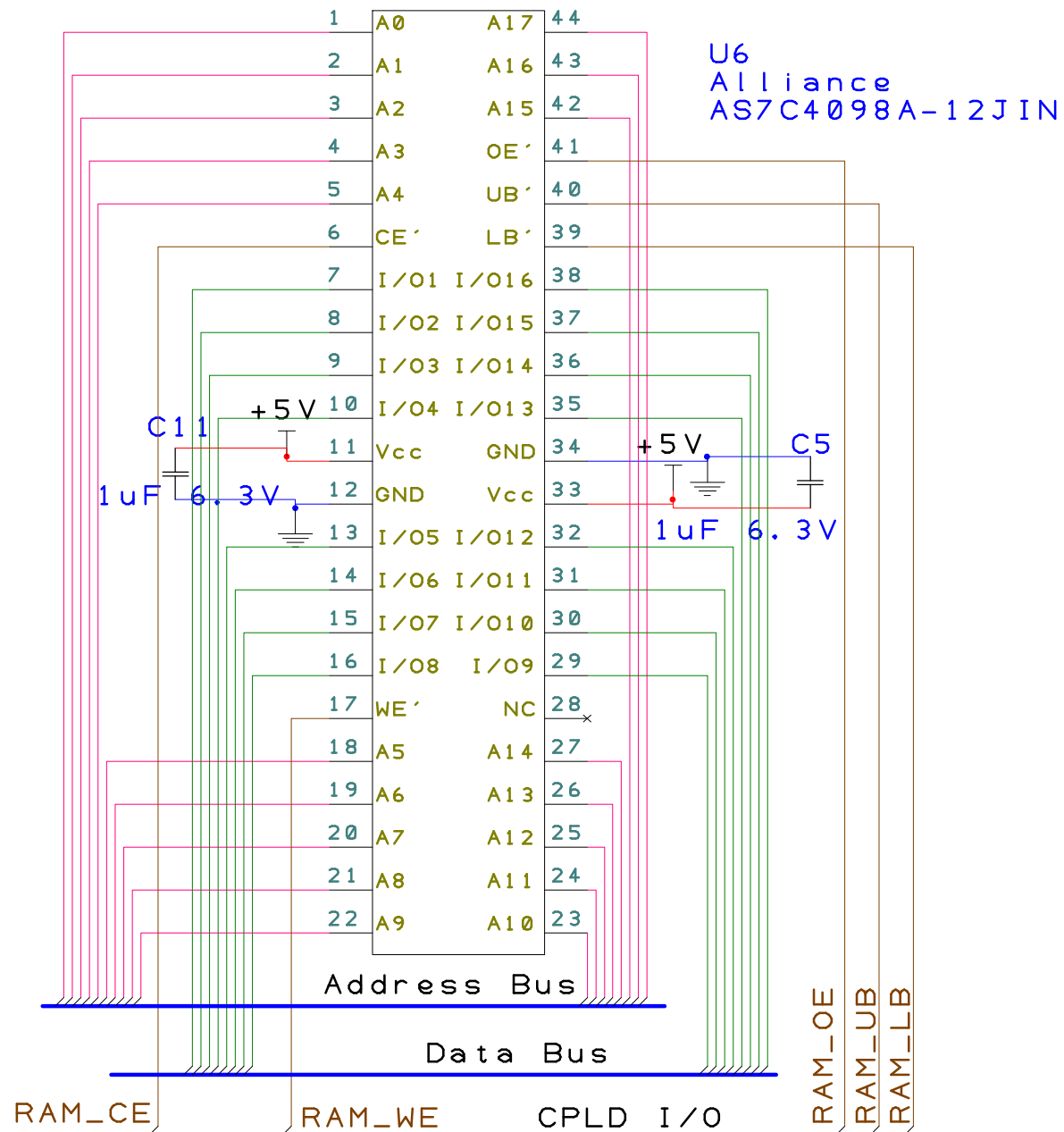
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Drn	Drn	Drn	Drn	Project	Microcomputer Design			Client	LeTourneau University
Chk	Chk	Chk	Chk	Title	Chandler Griscom M68000 Computer Schematic			Filename	CJG_Microcomputer.sch
							Drawing No.	Sheet 1 of 7	1



U4  
Microchip Technology  
SST39SF040-70-4C-PHE

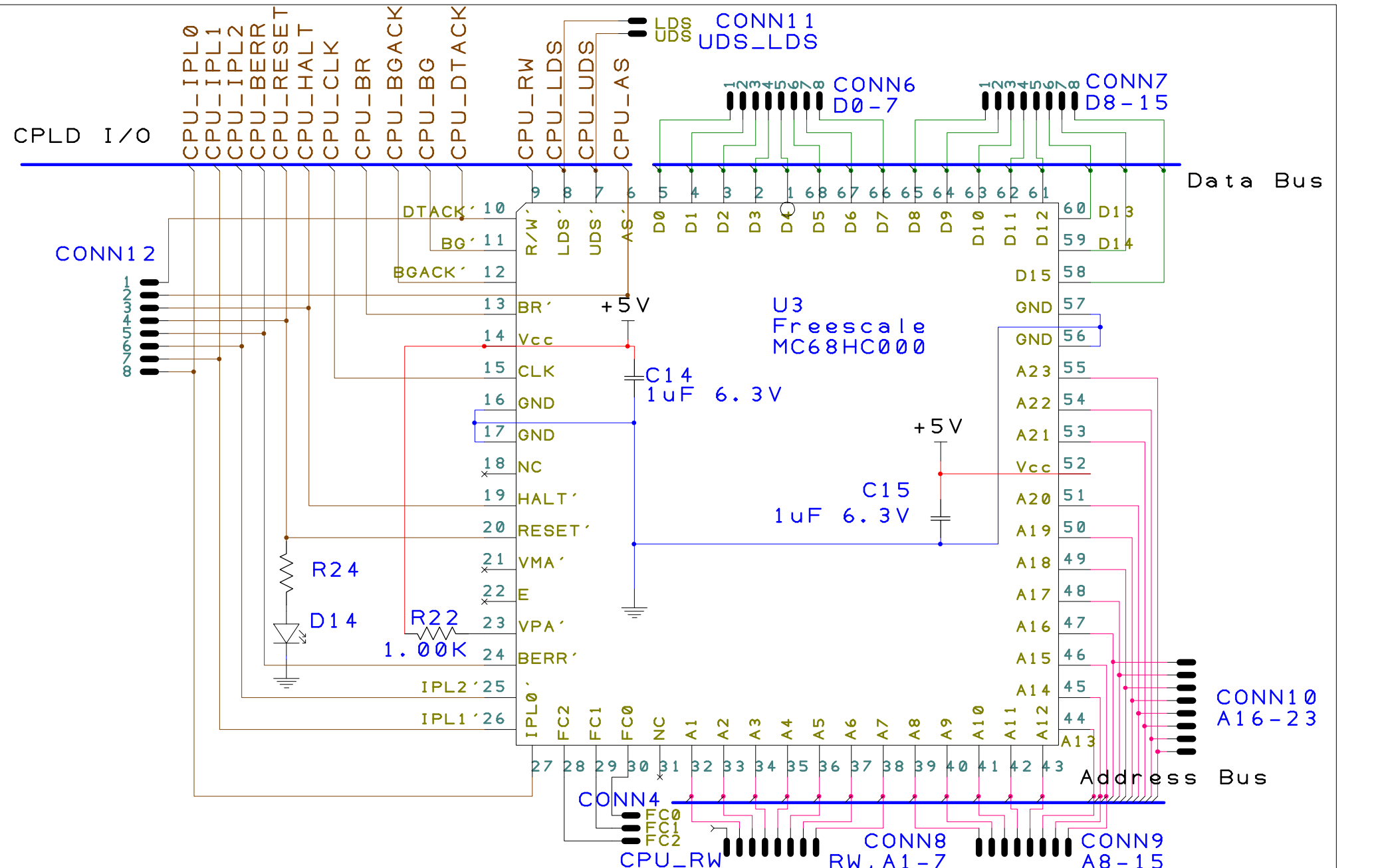
U5  
Microchip Technology  
SST39SF040-70-4C-PHE





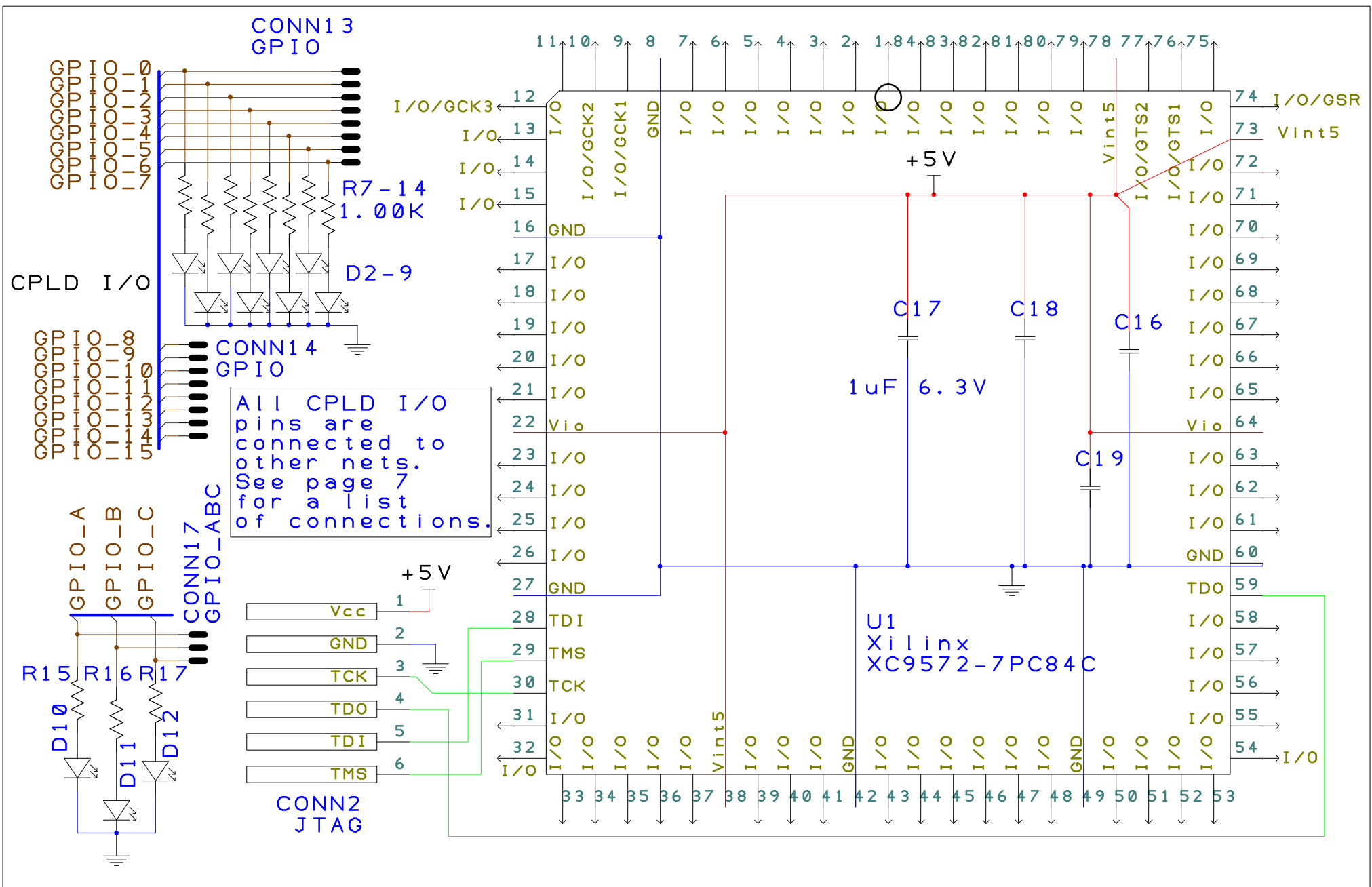
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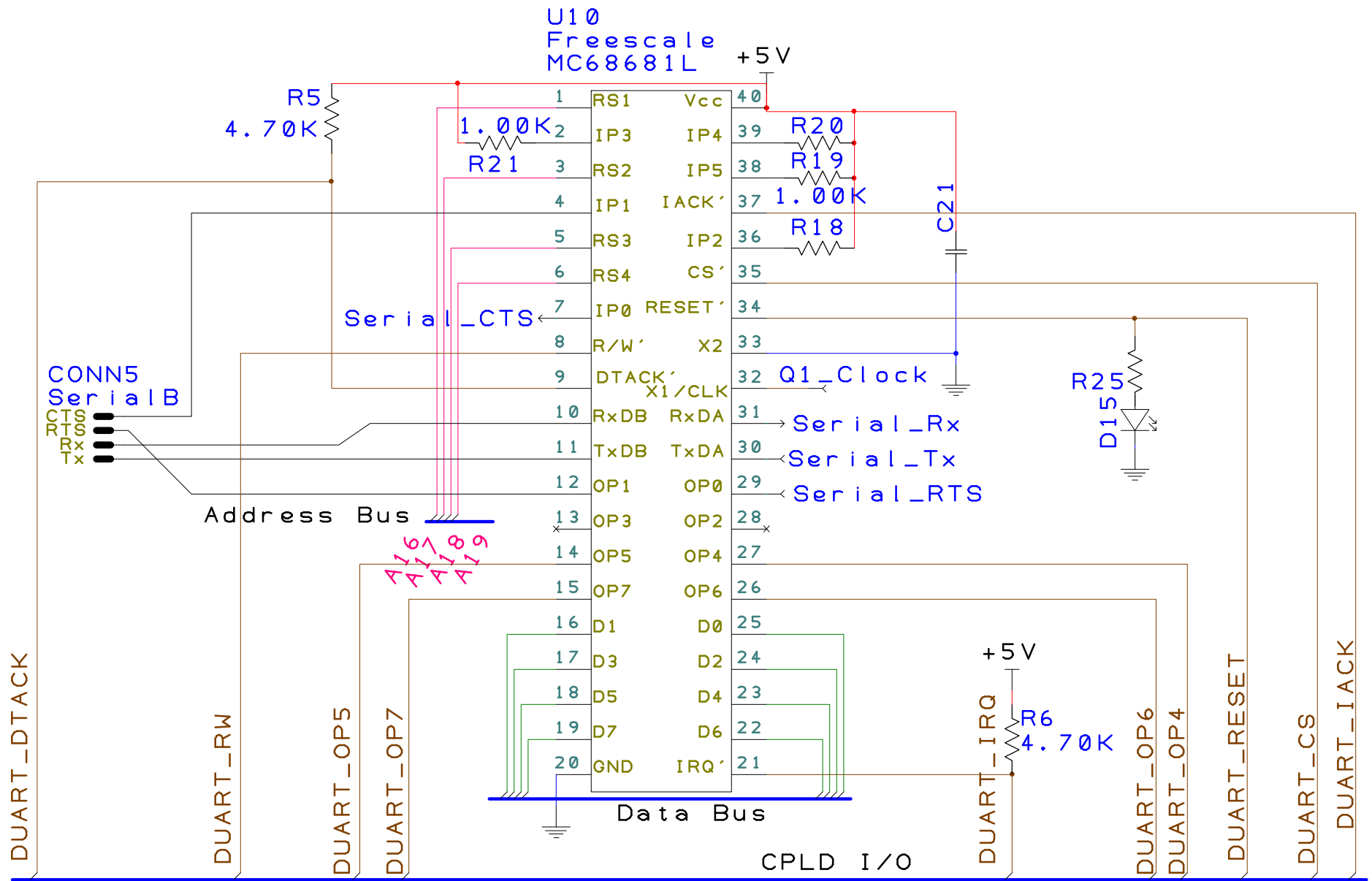
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



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E	D	C	B	A	Drawn <b>CJG</b> 31Jan2017	Check	Projection Do Not Scale		
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E	D	C	B	A	Drawn CJG 31Jan2017	Check	Projection Do Not Scale			
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Chk	Chk	Chk	Chk	Title	Chandler Griscom M68000 Computer Schematic		Filename		CJG_Microcomputer.sch	
							Drawing No.		Sheet 6	
							1		of 7	

## CPLD Netlist

Net Name	Pin		
A20	70	DUART_CLK	3
A21	69	DUART_CS	82
A22	72	DUART_DTACK	80
A23	71	DUART_IACK	77
CPU_AS	47	DUART_IRQ	74
CPU_BERR	52	DUART_OP4	76
CPU_BG	45	DUART_OP5	81
CPU_BGACK	43	DUART_OP6	79
CPU_BR	48	DUART_OP7	84
CPU_CLK	46	DUART_RESET	75
CPU_DTACK	44	DUART_RW	68
CPU_HALT	51	GPIO_0	10
CPU_IPL0	6	GPIO_1	13
CPU_IPL1	53	GPIO_2	15
CPU_IPL2	5	GPIO_3	18
CPU_LDS	40	GPIO_4	20
CPU_RESET	50	GPIO_5	23
CPU_RW	41	GPIO_6	25
CPU_UDS	39	GPIO_7	31
D0	58	GPIO_8	12
D1	83	GPIO_9	14
D2	61	GPIO_10	17
D3	4	GPIO_11	19
D4	63	GPIO_12	21
D5	1	GPIO_13	24
D6	62	GPIO_14	26
D7	2	GPIO_15	34
		GPIO_A	32
		GPIO_B	36
		GPIO_C	33
		Q1_Enable	7
		Q2_Clock	9
		Q2_Enable	11
		RAM_CE	56
		RAM_LB	54
		RAM_OE	57
		RAM_UB	55
		RAM_WE	65
		Reset_In	35
		ROM_CE	66
		ROM_OE	67
		ROM_WE	56

E	D	C	B	A	Drawn CJG 31Jan2017	Check	Projection Do Not Scale			
Drn	Drn	Drn	Drn	Project	Microcomputer Design			Client	LeTourneau University	
Chk	Chk	Chk	Chk	Title	Chandler Griscom M68000 Computer Schematic			Filename	CJG_Microcomputer.sch	
								Drawing No.	1	Sheet 7 of 7