

Silicides for integrated circuits: TiSi₂ and CoSi₂

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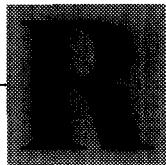
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Contents

1. Introduction	53
2. Fundamentals and materials aspects	54
2.1. Fundamentals of thin film diffusion.	54
2.1.1. Thermodynamics and equilibrium phases	54
2.1.2. Nucleation of crystalline phases	54
2.1.3. Growth kinetics	56
2.2. Silicide formation in thin film diffusion couples	59
2.2.1. Bulk phases of Ti-Si and Co-Si	60
2.2.2. Metal deposition and initial reaction	61
2.2.3. Phase sequence and moving species	64
2.2.4. Effects of the crystallinity of the substrate	72
2.2.5. Influence of the annealing ambient	72
2.2.6. Ion mixing	76
2.2.7. Formation of epitaxial CoSi ₂	77
2.2.8. Reaction of Ti and Co on SiGe alloys	78
2.3. Silicidation of doped Si	78
2.3.1. Metal-dopant interactions	78
2.3.2. Kinetics of silicidation	81
2.3.3. Redistribution of dopants during silicide formation	82
2.3.4. Diffusion of dopants in the silicide	84
2.3.5. Dopant outdiffusion from the silicide	86
2.3.6. Heat treatment of a silicide film on doped Si	89
2.4. Defect generation/recombination	90
2.4.1. Effect of silicidation on extended defects	90
2.4.2. Diffusion of dopants in buried layers during silicidation	91
2.5. Interaction of Ti and Co with SiO ₂	92
2.5.1. Thermodynamics of M-Si-O systems	92
2.5.2. Interactions between Ti and Co on SiO ₂	94
2.5.3. Diffusion on Ti and Co in SiO ₂	98
2.5.4. Oxidation of silicides	98
2.6. Interaction with contacting metals	100
2.6.1. Interaction with Al	100
2.6.2. Interaction with W	102
2.7. Thermal behaviour of thin film silicides	102
2.7.1. Stress build-up and thermal expansion	102
2.7.2. Thermal stability	103

3.	Technological aspects and implementation	105
3.1.	Implementation of self-aligned silicides in MOS technologies	105
3.1.1.	Use of silicides in MOS devices	105
3.1.2.	Self-aligned silicidation	108
3.2.	Formation of thin silicides	108
3.2.1.	Minimization of Si consumption and controllability	108
3.2.2.	Scaling of silicide thickness and controllability	113
3.2.3.	Interfacial cleaning	117
3.3.	Silicidation of laterally confined areas	118
3.4.	Silicided shallow junctions	122
3.4.1.	Characterization of shallow junctions	122
3.4.2.	Preformed junctions	124
3.4.3.	Outdiffused junctions	130
3.4.4.	Contacting technologies	135
3.5.	Silicided gates and runners	136
3.5.1.	Thermal stability of narrow runners	136
3.5.2.	Effect on gate quality	139
3.5.3.	Lateral diffusion of dopants using n ⁺ and p ⁺ poly	140
3.6.	Lateral silicide growth	141
3.7.	Rapid thermal processing	144
3.7.1.	Pattern-induced temperature non-uniformity	144
3.7.2.	Temperature control	145
4.	Conclusions	146
Acknowledgements		147
References		147

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Abstract

Silicides have been a topic of intensive research for more than a decade. The driving force for these investigations has certainly been the interesting materials aspects of the silicides and their applications in integrated circuits. The advantages of easy formability and low resistivity for both CoSi₂ and TiSi₂ have led to an intensive use of these silicides in self-aligned processes for simultaneous silicidation of source, drain and gate.

The fundamental investigations of these silicides include thermodynamic and kinetic aspects of phase formation, interactions with doped Si and related defect generation, and the interaction with oxide and metals. Specific issues related to the technological implementation of silicides in a full process will be discussed in view of the trend to scale the silicided area both in the vertical and in the lateral dimensions.

1. Introduction

Silicides have been a subject of research for many years. Their attractiveness has certainly been triggered by the characteristics of the metal/Si reaction, which have made the metal/Si diffusion couple a standard research subject for thin film reactions. The potential microelectronics applications have widened the scope of research and have brought new characterization methods, which have contributed to the full understanding of the silicide in a device environment. Silicides are highly valued for their material properties. However, no material would ever be considered for device implementation if its compatibility with current device processing were not optimal and if the process were not suitable for integration in a full technology.

Almost all metals in the periodic table form silicides when they react with Si. In general, the silicides are divided into three categories: the refractory metal silicides, the near-noble metal silicides and the rare earth metal silicides. The majority of the silicides are metallic and have a low resistivity. The refractory metal silicides, in general, have a high thermal stability, whereas the main asset of the near-noble metal silicides lies in their low chemical reactivity. The rare earth silicides are mainly investigated for their optical properties. Extensive overviews of materials properties of silicides are available in the literature [1,2].

Silicides have been implemented in devices to lower the sheet resistance of highly doped Si. They have been preferred to pure metals because of the stability of their contacts with Si and because of their self-passivating nature in an oxygen-rich environment. The implementation of silicides is currently considered for many applications. They have been incorporated in CMOS processing as source/drain and gate shunt materials. In bipolar technologies, silicides have been investigated for contacting of the extrinsic base as well as the emitter. Silicides have also been used for infrared detectors and optical applications.

For many technological applications, the reaction of the metal with Si but not with SiO₂ is a crucial factor. It allows an alignment of the silicide with SiO₂-defined window edges, which cannot be achieved by any other means. The most important silicides with good self-aligning properties are PtSi, NiSi, CoSi₂ and TiSi₂. PtSi has been used extensively in bipolar and detector applications. It has not been the first choice for CMOS applications because of its low thermal stability. NiSi has been investigated in detail, but is unstable in contact with Si as the NiSi/Si system evolves to the more resistive NiSi₂. The two main silicides of interest are TiSi₂ and CoSi₂. TiSi₂ is widely accepted, but recent studies have shown that CoSi₂ should be considered as a serious candidate as well, with even better material characteristics.

In this review, the CMOS technology will be used as a guideline for the selection and discussion of topics. This choice is in line with the fact that CMOS is indeed the driving technology, both for current and future research in microelectronics. The goal of this work is to provide a fundamental understanding of the phenomena that occur when silicides are applied in a technology. The reviews on silicides by Nicolet [1] and Murarka [2] have served as a basis for this paper. There will be no attempt to reproduce data that are available in these references. The first part of this paper will deal with the fundamentals of the metal/Si reaction and with the interaction with other materials that are used in device processing. In the second part, an overview of specific characteristics of the silicides when implemented in a transistor will be given. There will, however, be a constant link between the two parts of the paper. This reflects how closely materials properties are influencing technology and device behaviour and, on the other hand, how a successful technology development should be based on insight into material properties. In particular, as the scaling of MOS technologies progresses, the scalability and controllability of the silicidation process become very important properties which are strongly interrelated with the fundamental characteristics of the silicide material.

2. Fundamentals and materials aspects

2.1. Fundamentals of thin film diffusion

2.1.1. Thermodynamics and equilibrium phases

In this section we shall consider a diffusion couple, consisting of a thin film metal layer on a Si substrate. From a thermodynamic point of view, a system consisting of a thin film on a substrate is far from equilibrium. When kinetic constraints are removed, e.g. by heating the system and allowing elements to diffuse, the system will evolve in order to lower its free energy by the formation of intermetallic compounds. This can be seen from a schematic free energy diagram as depicted in Fig. 1, showing that the presence of stable compounds is more favourable than a combination of the two elements, as it is in the diffusion couple itself. Therefore these phases will nucleate and grow if favourable conditions are present. In the next sections a short overview will be given of the nucleation of new phases and the kinetics of the growth of compound layers.

2.1.2. Nucleation of crystalline phases

Since the formation of new compounds involves a nucleation process, it is important to summarize some aspects of classical nucleation theory. For a more extensive treatment, the reader is referred to ref. 3.

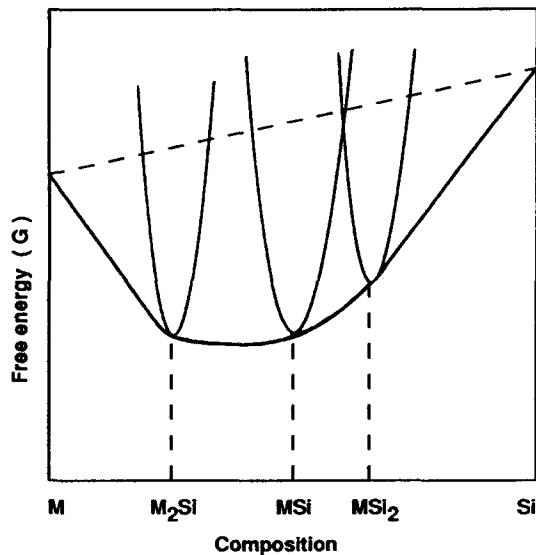


Fig. 1. Free energy vs. composition diagram for an M-Si diffusion couple and its intermetallic compounds.

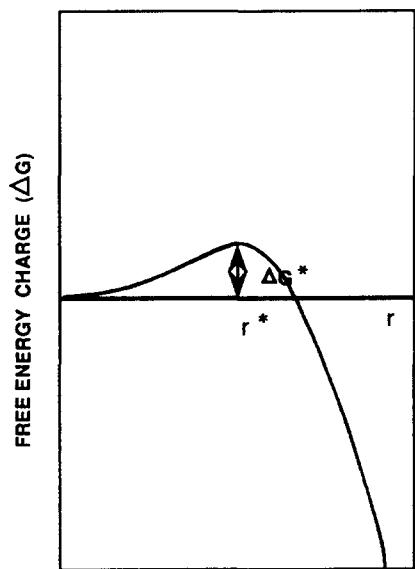


Fig. 2. The free energy of a nucleus as a function of its radius.

The formation of a nucleus, driven by a lowering of the energy of the system ΔG , will be opposed by the increase of interfacial area, with a specific surface energy σ . If ΔG is calculated per unit volume, a nucleus of average radius r will have a free energy given by

$$\Delta G_n = r^2 \sigma - r^3 \Delta G \quad (1)$$

As is seen in Fig. 2, ΔG_n passes through a maximum that corresponds to a critical nucleus size r^* . The population of nuclei with a radius smaller than r^* will exist in equilibrium distribution, whereas bigger nuclei will tend to grow.

The critical radius is given by

$$r^* = 2\sigma/3\Delta G \quad (2)$$

The rate of nucleation ρ^* will be proportional to the concentration of critical nuclei and to the rate at which such nuclei originate and can be described as follows:

$$\rho^* \sim \exp(-\Delta G^*/kT) \exp(-Q/kT) \quad (3)$$

with ΔG^* the free energy of the critical nuclei and $\exp(-Q/kT)$ the diffusion of matter necessary for growth. Since ΔG^* is inversely proportional to T^2 , the rate of nucleation will vary as $\exp(-1/T^3)$.

The classical theory of nucleation predicts accurately that nucleation usually occurs within narrow temperature limits, below which nothing occurs and above which the reaction is extremely fast. In the case of silicides, as with most intermetallic compounds, the free energy is not known with sufficient precision to allow meaningful calculations. However, since ΔG^* is proportional to $\sigma^3/\Delta G^2$, one may anticipate large values of ΔG^* for small ΔG and therefore a nucleation-dominated reaction whenever the evolution of the system is driven by a small change of free energy and a large increase in surface energy.

Although models have been proposed to predict the first phase nucleating in a diffusion couple based on information from the phase diagram [4,5], they do not agree very well with experimental observations [6]. Nevertheless, it will be shown below that nucleation phenomena play an important role in both $TiSi_2$ and $CoSi_2$ formation.

2.1.3. Growth kinetics

Considering the fact that the metal-Si phase diagrams include several intermediate compounds, the sequence of phase formation is an intriguing issue. Purely from energetic considerations, a compound is more stable than a solid solution of metal and silicon, and in principle all equilibrium phases are expected during the reaction, with the metal-rich phases next to the metal and the Si-rich phases close to the Si.

The kinetics of thin film growth has been described in detail by Gösele and Tu [7]. In their model, the diffusion of matter across the compound layers is taken into account as well as the rearrangement of the atoms required for the growth of the compounds at the interfaces. This rearrangement may involve a reaction barrier.

The kinetics of a solid state reaction can either be diffusion-controlled or reaction-controlled. Interface-controlled growth will always change over time to diffusion-controlled growth if the layer has grown to a sufficiently large thickness.

In order to visualize the evolution of the metal-Si diffusion couple during a reaction, let us consider a system consisting of a metal (M), Si and two intermediate compounds i.e. MSi_α and MSi_β with $\alpha < \beta$ (Fig. 3). (Note that the symbols α and β are used differently from ref. 7.) The change in thickness of the two layers can be described by

$$dx_\alpha/dt = G_\alpha j_\alpha^{Si} - G_{\alpha\beta} j_\beta^{Si} \quad (4)$$

$$dx_\beta/dt = G_\beta j_\beta^{Si} - G_{\beta\alpha} j_\alpha^{Si} \quad (5)$$

G_α , G_β , $G_{\alpha\beta}$ and $G_{\beta\alpha}$ are weight coefficients and account for the change in composition at the interface.

The diffusion fluxes of Si atoms in the MSi_α and the MSi_β layer are given by

$$j_\alpha^{Si} = \Delta C_\alpha^{eq} \kappa_\alpha^{eff} / (1 + x_\alpha \kappa_\alpha^{eff} / D_\alpha) \quad (6)$$

$$j_\beta^{Si} = \Delta C_\beta^{eq} \kappa_\beta^{eff} / (1 + x_\beta \kappa_\beta^{eff} / D_\beta) \quad (7)$$

with ΔC^{eq} the difference between equilibrium and actual concentration at the various interfaces.

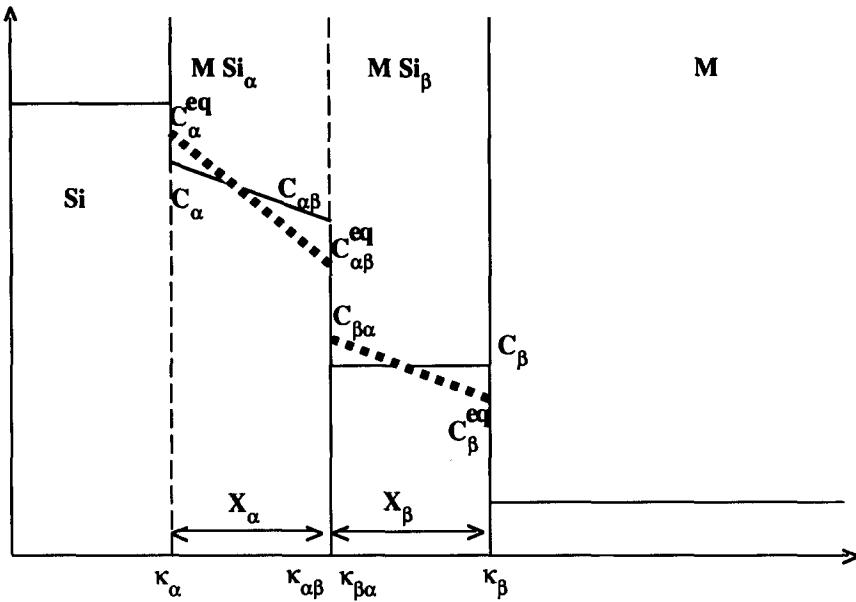


Fig. 3. Schematic of concentration profile of Si atoms across a $Si/MSi_\alpha/MSi_\beta/M$ diffusion couple with or without interface reaction barriers.

The reaction rates at the interface are characterized by coefficients κ_α , $\kappa_{\alpha\beta}$, $\kappa_{\beta\alpha}$ and κ_β . For instance, the quantity $\kappa_{\alpha\beta}$ characterizes the barrier against the growth of the MSi_α layer at the expense of the MSi_β layer, and $\kappa_{\beta\alpha}$ characterizes the barrier against the growth of the MSi_β layer at the expense of the MSi_α layer. κ^{eff} is an effective interfacial barrier and is given by

$$1/\kappa_\alpha^{eff} = 1/\kappa_\alpha + 1/\kappa_{\alpha\beta} \quad (8)$$

$$1/\kappa_\beta^{eff} = 1/\kappa_{\beta\alpha} + 1/\kappa_\beta \quad (9)$$

D_α and D_β are the chemical interdiffusion coefficients and are expressed in terms of elemental diffusion coefficients as follows:

$$D_\alpha = D_\alpha^{\text{Si}}/(\alpha + 1) + \alpha D_\alpha^M/(\alpha + 1) \quad (10)$$

$$D_\beta = D_\beta^{\text{Si}}/(\beta + 1) + \beta D_\beta^M/(\beta + 1) \quad (11)$$

It is important to note that in this model the fluxes j_α^{Si} and j_β^{Si} are independent of each other. At the interface between MSi_α and MSi_β , for example, the flux can be described as

$$j_\alpha^{\text{Si}} = \kappa_{\alpha\beta} \Delta C_{\alpha\beta}^{eq} \quad (12)$$

$$j_\beta^{\text{Si}} = \kappa_{\beta\alpha} \Delta C_{\beta\alpha}^{eq} \quad (13)$$

The change of x_α and x_β with time depends on the balance of the two fluxes. The basic difference between this formalism of growth and that of normal diffusion-controlled growth shows up in the occurrence of interfacial reaction barriers. For very fast interfacial rearrangements, the κ coefficients go to infinity and the normal formalism for diffusion-controlled growth is recovered.

The model allows us to predict whether the MSi_α layer will grow ($dx_\alpha/dt > 0$) at the expense of the MSi_β layer ($dx_\beta/dt < 0$) or vice versa, or whether both layers will grow. Let r be the ratio of the fluxes $j_\alpha^{\text{Si}}/j_\beta^{\text{Si}}$. r_1 denotes the case for which $dx_\alpha/dt = 0$ and is given by

$G_{\alpha\beta}/G_\alpha$. If $r > r_1$, the MSi_α phase will grow; if $r < r_1$, the MSi_α layer will shrink. r_1 depends only on the composition of the compounds. Similarly, one can define r_2 for the growth of the MSi_β layer. In general, if the flux ratio is not in the range between r_1 and r_2 , one of the layers will shrink while the other grows.

Without going into a detailed discussion of all possible cases, a summary of the most important conclusions will be given.

If the formation of both silicide layers is diffusion-controlled ($\kappa \rightarrow \infty$), the flux ratio r is simplified to

$$r = (\Delta C_\alpha^{eq} D_\alpha / \Delta C_\beta^{eq} D_\beta) x_\beta / x_\alpha \quad (14)$$

r depends on the initial thickness of the layers and will change with time. The system will, however, always evolve to a situation where $r_1 > r > r_2$, and both layers will grow.

If the formation of both silicide layers is reaction rate-controlled, the flux ratio is given by

$$r = \Delta C_\alpha^{eq} \kappa_\alpha^{eff} / \Delta C_\beta^{eq} \kappa_\beta^{eff} \quad (15)$$

The growth or shrinkage of both phases depends on the actual flux of material across both layers. If, however, one of the layers starts to grow, the kinetics will eventually become diffusion-controlled and will change over to the following case.

If there is a different growth mechanism for the two layers, this is the most revealing case for the understanding of the differences between the thin film and the bulk reaction. Let us assume that the transport across the MSi_β layer is diffusion-controlled, whereas that of MSi_α is reaction rate-controlled. Under these circumstances, the flux ratio r may be expressed as

$$r = (\Delta C_\alpha^{eq} \kappa_\alpha^{eff} / \Delta C_\beta^{eq} D_\beta) x_\beta \quad (16)$$

In this case the ratio of fluxes $j_\alpha^{Si} / j_\beta^{Si}$ is proportional to the thickness of the MSi_β layer, x_β . For relatively large values of the flux ratio ($r > r_1$), the MSi_α and MSi_β layers will coexist at all times. For relatively small ratios ($r < r_1$), the MSi_β layer grows and the MSi_α layer shrinks as long as the thickness x_β is sufficiently small and $r < r_1$ still holds. This is a typical case, where for kinetic reasons the MSi_α layer cannot coexist together with the MSi_β layer as long as x_β is below a critical thickness x_β^{crit} defined by

$$x_\beta^{crit} = (r_1 \Delta C_\beta^{eq} D_\beta / \Delta C_\alpha^{eq} \kappa_\alpha^{eff}) \quad (17)$$

When the thickness of the MSi_β phase exceeds this critical thickness, the MSi_α layer can grow simultaneously.

Figure 4 gives a schematic representation of the evolution of such a system. At first, MSi_β (the compound phase with the lowest effective interface barrier) will grow linearly with time and subsequently according to a parabolic growth law. After the thickness x_β of the first compound layer exceeds the critical value x_β^{crit} , the second phase will form and grow.

The compound phase that forms as the second one depends on the material supply conditions in the model. It frequently occurs that in the reaction of an M-Si thin film diffusion couple the films are so thin that the supply of material (usually the metal and in some particular cases the Si) is limited. In the model this can be described by setting one of the fluxes to 0. In that case, the second phase begins to form and grow when the supply stops, even if the critical thickness has not yet been reached. This type of second phase formation is supply limitation induced. In practice this is the case, as will be discussed

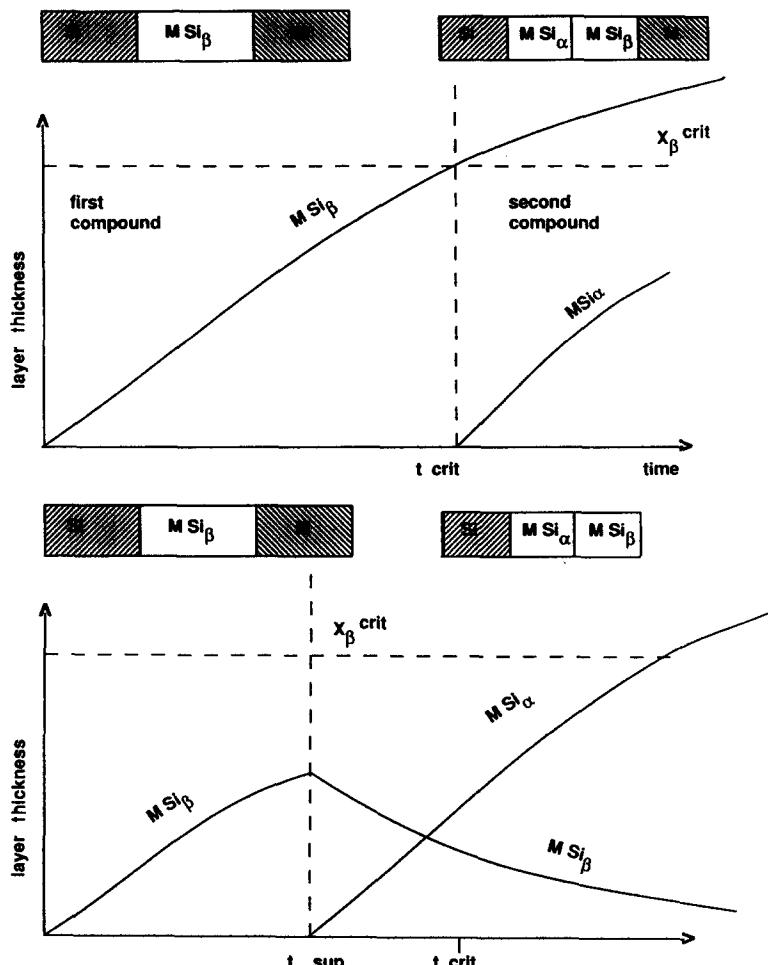


Fig. 4. Schematic of growth/shrinkage behaviour of first forming compound MSi_β and growth of second forming compound MSi_α in an M/Si diffusion couple. In (a) the MSi_β layer reaches its critical thickness, x_β^{crit} , when unreacted M and Si are still available. In (b) M is transformed completely into MSi_β before reaching its critical thickness.

in Section 2.2.3, for the growth of $CoSi_2$. The three possible routes are depicted schematically in Fig. 5.

It is important to note that according to this model the phase sequence in a thin film reaction is determined by kinetic arguments. Even if nucleation of a phase is possible, the growth kinetics can be such that the growth of this phase is unstable and therefore does not occur. According to the model presented here, the first phase formation in a diffusion couple is that with the lowest effective interface reaction barrier. Since information on the interface reaction barriers cannot be extracted from the phase diagram, the model does not allow us to predict the formation of the first phase from the phase diagram.

2.2. Silicide formation in thin film diffusion couples

The aim of the study of the interactions in metal–Si diffusion couples is to obtain an atomistic model of the behaviour of the species involved in the reaction and to predict the intermediate and final phases. The interaction starts during the deposition of the metal on the Si substrate and proceeds as temperature treatments are carried out. After a short discussion of the bulk phases, the next sections will present an overview of the interactions

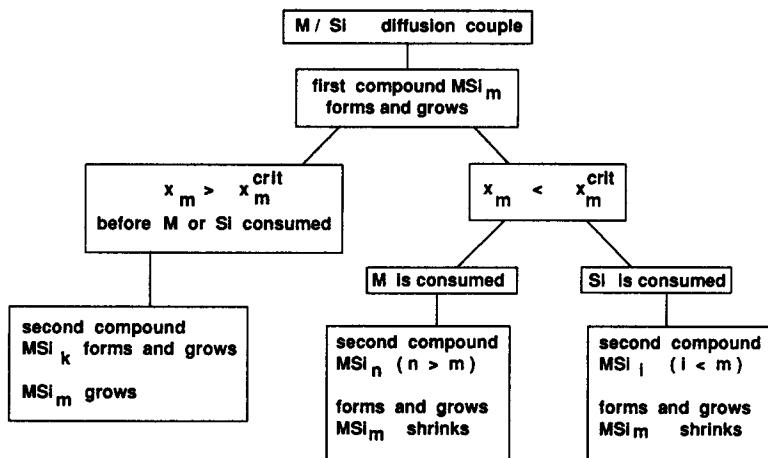


Fig. 5. Block diagram of the three possible routes for second-phase formation under different supply conditions of M and Si in an M/Si diffusion couple.

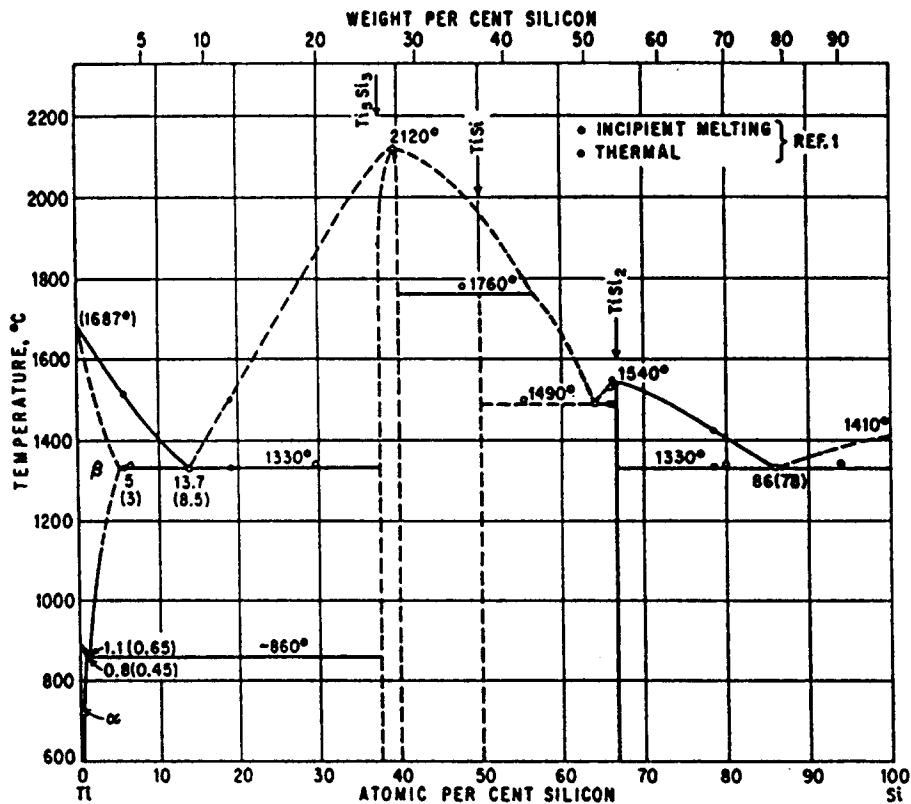


Fig. 6. Binary phase diagram of Ti-Si (after ref. 8).

in Ti-Si and CoSi diffusion couples in the various reaction stages and under various experimental conditions.

2.2.1. Bulk phases of Ti-Si and Co-Si

The constitution of both the Ti-Si and Co-Si systems, based on bulk experiments, is fairly well established. The phase diagrams are depicted in Figs. 6 and 7.

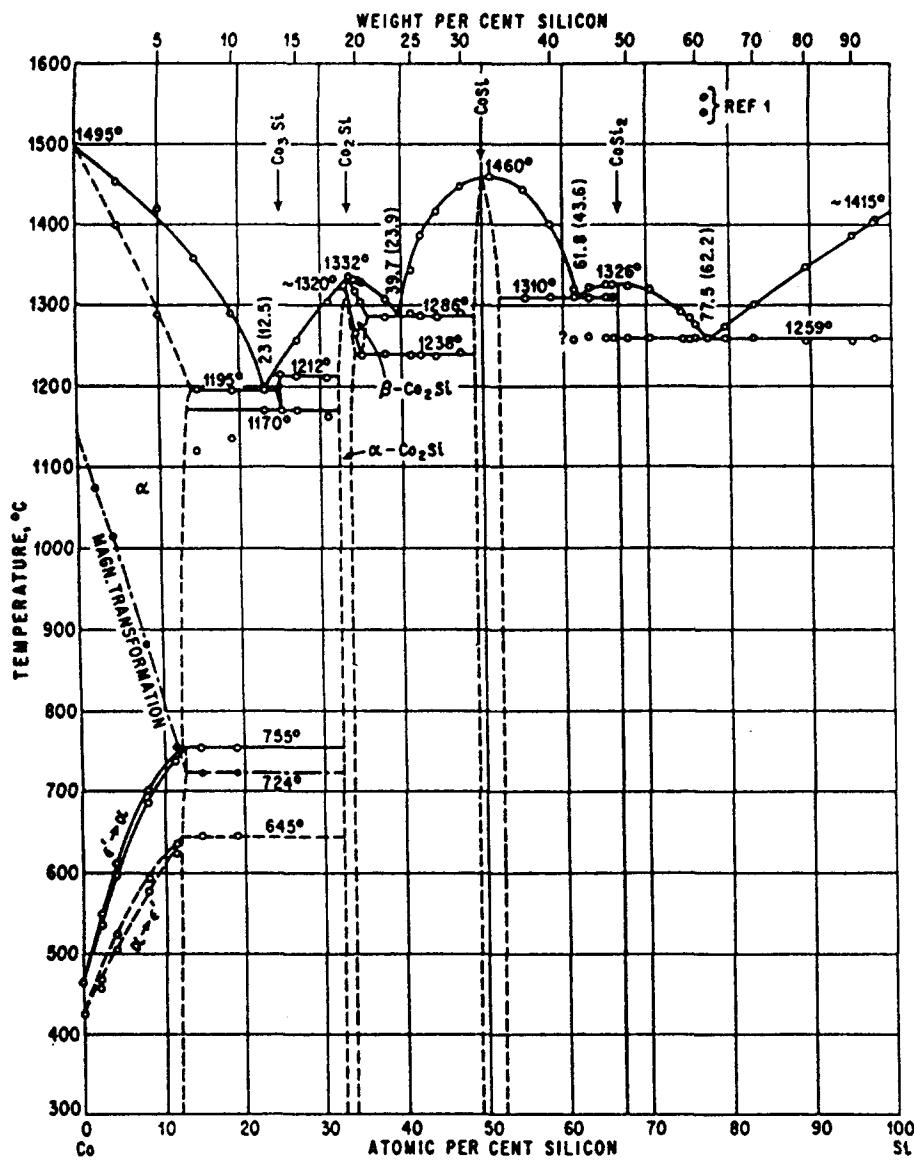


Fig. 7. Binary phase diagram of Co-Si (after ref. 8).

According to Hansen [8] there are three compounds in the Ti-Si system: Ti_5Si_3 , $TiSi$ and $TiSi_2$. The solid solubility of Ti in Si is very low [9-11], e.g. of the order of 10^{14} at. cm^{-3} at 1200 °C.

In the Co-Si phase diagram, the Co_2Si , $CoSi$ and $CoSi_2$ phases [8] are very well established. Evidence for the Co_3Si and $CoSi_3$ phases is lacking. The solid solubility limit of Si in Co, as depicted in the phase diagram is considered to be tentative. The solubility of Co in Si has been reported to be 1×10^{16} Co cm^{-3} at 1200 °C [9,12].

The crystal structures of the various phases are summarized in Table 1.

2.2.2. Metal deposition and initial reaction

The M-Si diffusion couples are fabricated by deposition of the metal on a Si substrate. Sputter deposition is generally preferred over other deposition techniques because of its

TABLE 1
Structural data of the various Ti and Co silicide phases

Phase	Structure	Unit cell
Co_2Si	Orthorhombic	$a = 0.4918$ $b = 0.3737$ $c = 0.7109$
$CoSi$	Cubic	$a = 0.444$
$CoSi_2$	Cubic	$a = 0.543$
Ti_3Si_5	Hexagonal	$a = 0.7465$ $c = 0.5162$
$TiSi$	Orthorhombic	$a = 0.654$ $b = 0.363$ $c = 0.499$
$TiSi_2$	Orthorhombic C49 Orthorhombic CS4	$a = 0.362$ $b = 1.376$ $c = 0.36$ $a = 0.8252$ $b = 0.4783$ $c = 0.8540$

good controllability. The as-deposited state differs, however, from the ideal picture of a diffusion couple. It is important to characterize the samples after sputter deposition, since some initial interactions already occur at this stage.

After sputtering of Ti on Si, an amorphous layer is observed at the interface [13–15]. A detailed study [13] using high-resolution TEM (transmission electron microscopy) and EDS (energy dispersive spectroscopy) analysis reveals that the amorphous layer consists of Ti and Si and extends over most of the interface area. Figure 8(a) shows a high-resolution cross-section micrograph of the Ti–Si interface. The Ti was sputter deposited on an *in situ* sputter-etched Si substrate. In this case two amorphous layers are present. The lower amorphous layer (lighter band) is amorphized Si induced by the back sputtering, whereas the upper layer (darker band) is an amorphous interdiffused Ti–Si layer as confirmed by the EDS data of Fig. 8(b).

The interface between the amorphous Ti–Si layer and the Si is virtually atomically flat. After annealing at temperatures around 400 °C the thickness of the amorphous Ti–Si alloy increases. During growth, a composition gradient builds up in the reacted layer. The composition across the layer varies gradually from 30% Si close to the Ti interface to about 70% Si near the Si substrate.

The growth kinetics of the amorphous layer was studied by carrying out isothermal anneals and subsequently measuring the alloy thickness by cross-sectional TEM. In Fig. 9 the square of the amorphous silicide layer thickness is plotted as a function of the anneal time [14]. Although the initial reaction exhibits a diffusion-like behaviour, the longer anneals result in a slowing down of the growth. This reduced reaction rate is attributed to the formation of Kirkendall void formation at the interface with Si.

Following the discussion of the schematic free energy diagram of Section 2.1.1, one can obtain information from the free energy curves in a phase diagram by considering the competing stable and metastable phases (Fig. 10). The free energy curves of the Ti/Si solution phases at 600 K were constructed according to the method of Kaufman [16–18].

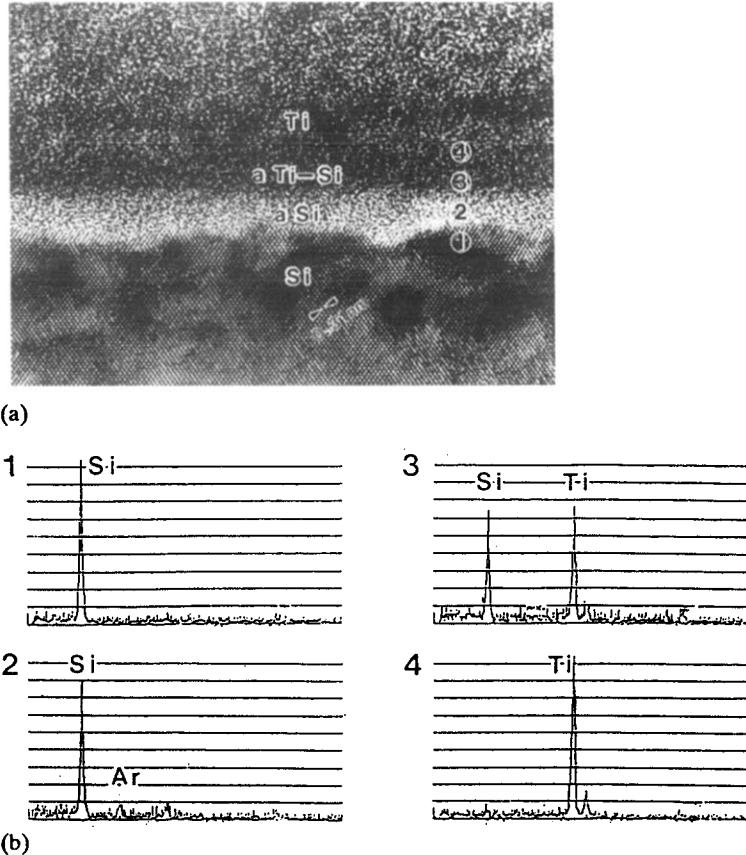


Fig. 8. (a) Cross-section HRTEM micrograph and (b) EDS spectra (using 2 nm probe) from areas 1 to 4 of the Ti-Si interface for which Ti was sputter-deposited on a sputter-etched Si wafer. In the 2 nm thick lighter band (2), Si and Ar signals, and in the 2.5 nm thick darker band (3), Si and Ti signals were observed, while Ar was not detected in the Si crystal (1) adjacent to the lighter band and the Si signal was not detected in the Ti layer (4) adjacent to the darker band (after ref. 13).

It is assumed that (i) metastable thermodynamic equilibrium is established between the metal on the one side and Si on the other side of the reaction region and (ii) neither crystalline solid solutions nor compound phases are formed. Examination of the full set of free energy vs. composition curves from 0 to 1500 K yields the metastable phase diagram. For each temperature, the metastable concentration range of the amorphous layer between Ti and Si can be constructed. Based on this metastable phase diagram, a gradual change in composition range of the intermixed α Ti-Si layer is expected. The composition ranges from 25% Si at the interface with Ti to about 60% Si near the interface with the Si substrate. This is in very good agreement with the experimental results described above.

The formation of an amorphous phase in diffusion couples is well known for metal-metal systems [19]. Such amorphous phase formation and growth is not a unique phenomenon. It is more likely to occur if the heat of mixing of the adjacent metals is high and if one of the elements is a fast diffuser in the other matrix [20]. The heat of mixing in metal-Si systems is indeed very high, and as such an important condition for amorphous phase formation is fulfilled. In the case of Ti-Si, the amorphous phase formation has been attributed to the immobility of Ti in Si at the interdiffusion temperature [18]. The lack of coordination between Si, which is the main moving species, and Ti prohibits the formation of a crystalline

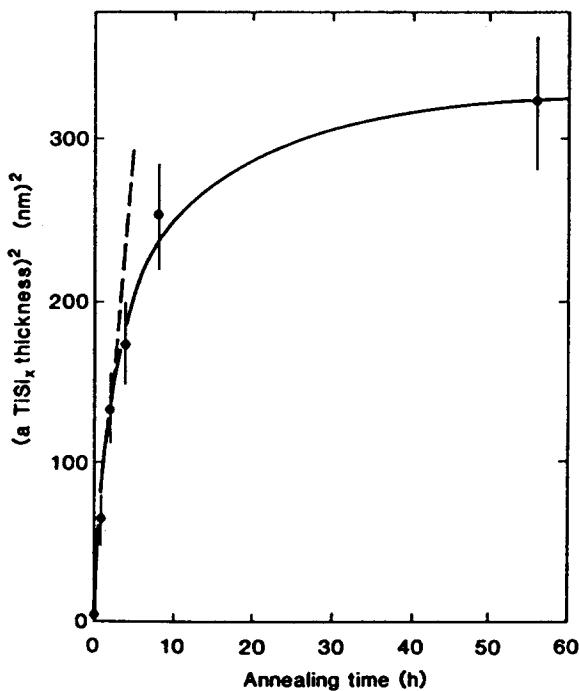


Fig. 9. The squared amorphous silicide thickness as a function of time at 400 °C. It is obvious that the growth of the layer is not controlled by a simple diffusion process (after ref. 14).

unit cell. It should, however, be noted that the initial amorphization during sputtering is at least partly initiated by ion bombardment during the sputtering process.

The formation of an amorphous silicide after metal deposition and in the initial stage of the reaction has also been observed for other metal/Si multilayers [21–25]. There is experimental evidence of amorphous Ni-silicide formation and a complete thermodynamic description of the system based on calorimetric measurements [26,27]. Not much experimental data on Co/Si is available. Nathan [22] reports that the formation of an amorphous Co silicide does not occur under similar conditions as for Ni.

2.2.3. Phase sequence and moving species

The phase formation sequence during the solid state reaction of Ti or Co with Si has been discussed widely in the literature. In both cases, the disilicide is the compound in thermodynamic equilibrium with Si. The disilicide is also the phase with the lowest electrical resistivity.

In the following an overview will be given of experimental observations on phase formation and reaction kinetics, taking into account various experimental conditions such as substrate crystallinity, interfacial impurities, reaction ambient and so on.

2.2.3.1. Co/Si reaction

The reaction of Co with Si has been studied by furnace treatments [28–32] and rapid thermal processing [33]. Figure 11 shows the sheet resistance after deposition of 80 nm of Co on Si and a 30 s anneal at various temperatures. From 300 °C on, the sheet resistance increases until a maximum is reached at 500 °C. At higher temperatures the sheet resistance decreases. The change in sheet resistance can be directly correlated to the phase formation. X-ray diffraction spectra show (Fig. 12) the presence of Co_2Si and $CoSi$ at the lower

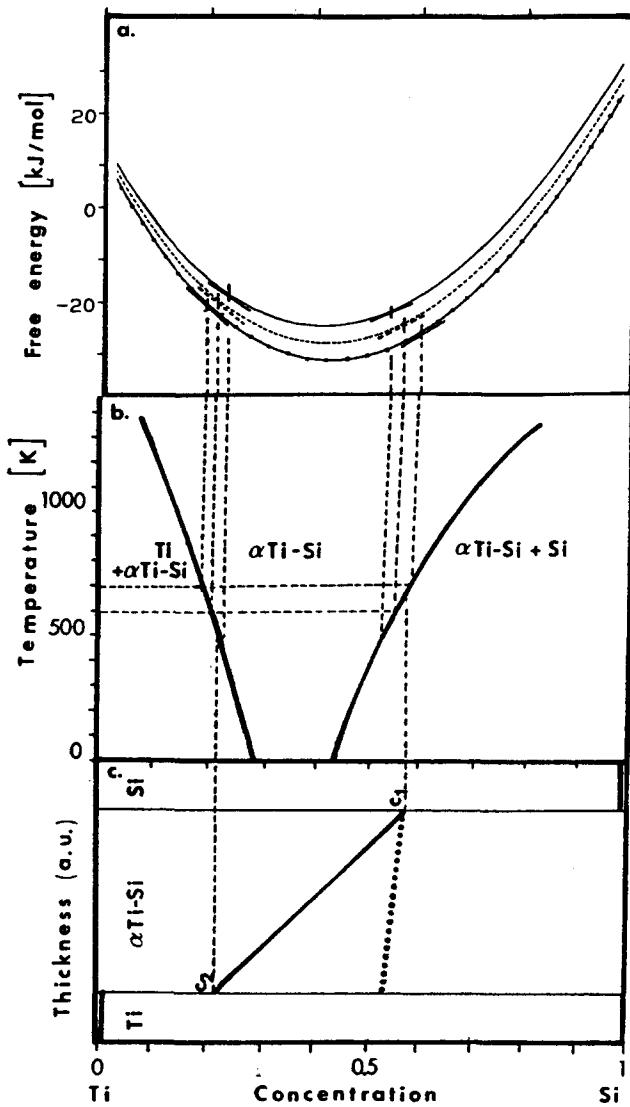


Fig. 10. Quasi-equilibrium phase diagram (b) from a set of free energy curves for the liquid phase (a) for the Ti-Si system and construction of a schematic model of the reaction between Ti and Si (c). The solid line gives the quasi-equilibrium concentration at 400 °C. C_1 and C_2 are the quasi-equilibrium concentrations at both interfaces.

temperatures. The $CoSi$ phase grows, and at 500 °C the Co layer is completely converted to $CoSi$. Treatments at higher temperatures lead to the formation of $CoSi_2$. The phase sequence obtained from X-ray diffraction (XRD) agrees well with the sheet resistance data, taking into account the resistivities of the various phases [1]: $\approx 70 \mu\Omega \text{ cm}$ for Co_2Si , $100-150 \mu\Omega \text{ cm}$ for $CoSi$ and $14-17 \mu\Omega \text{ cm}$ for $CoSi_2$.

The phase sequence $Co \rightarrow Co_2Si \rightarrow CoSi \rightarrow CoSi_2$ described here for rapid thermal processing (RTP) is the same as for furnace treatment. Co_2Si and $CoSi$ form by diffusion-controlled kinetics with respective activation energies of 1.5 eV and 1.9 eV [31,34]. Whereas the simultaneous presence of Co, Co_2Si and $CoSi$ commonly occurs, the coexistence of those phases with $CoSi_2$ has never been observed in thin film reactions. The simultaneous presence of various phases in a diffusion couple has been discussed in Section 2.1.2. Similar to the case of $NiSi$ [7], it is generally accepted that the critical thickness of $CoSi$ is larger

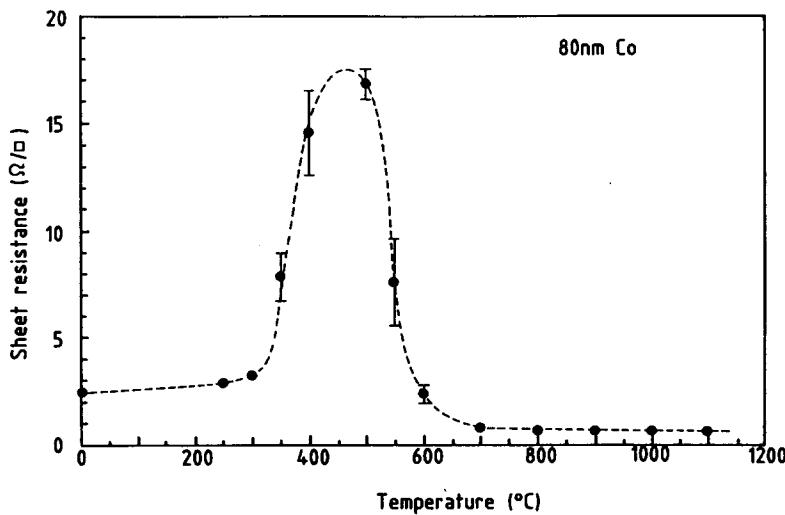


Fig. 11. Sheet resistance as a function of reaction temperature during RTP for 30 s in N_2 . The deposited Co layer was 80 nm.

than the thicknesses that appear in the experimental thin film reactions. As such, the formation of $CoSi_2$ starts after a full conversion of the Co film into $CoSi$. The $CoSi_2$ formation is a case of supply-limited growth. The reaction mechanism of $CoSi$ into $CoSi_2$ is quite complicated. The nucleation of the $CoSi_2$ phase occurs at triple points between two $CoSi$ grains and Si. Then lateral growth takes place until a continuous $CoSi_2$ -Si interface is formed. The reaction then proceeds layer by layer [35–37]. Thus, after an initial fast transformation, the interaction slows down. Van Gurp *et al.* [34] did marker experiments to identify the main moving species during the formation of the various Co-silicide phases. The experiments show that the $Co_2\text{Si}$ layer grows predominantly by Co diffusion and that the $CoSi$ phase grows predominantly by Si diffusion. The mechanism of diffusion has been further clarified by the use of radioactive ^{31}Si tracers in conjunction with metal markers [38]. The conclusion of these experiments is that $CoSi$ grows by silicon vacancy diffusion. The $CoSi_2$ phase again grows predominantly by Co diffusion [34,35]. The diffusion of Co through $CoSi_2$, however, is slow and has a high activation energy [39]. This is reflected in a slow $CoSi_2$ growth at low temperatures following diffusion controlled kinetics.

Recently, the phase sequence during silicide formation has been monitored *in situ* during rapid thermal processing systems [40,41]. A real-time emissivity measurement during the process allows very accurate control of the temperature during RTP and monitoring of changes in the silicide formation process [42,43]. In Fig. 13 the emissivity at a wavelength of $2.4 \mu\text{m}$ is shown as a function of time for the front side of a wafer on which 40 nm of Co was deposited. The temperature profile is plotted in the same figure. At higher temperatures the emissivity of the wafer increases rapidly with temperature. A plateau in the emissivity is observed at about $620 ^{\circ}\text{C}$. Detailed analysis with Rutherford backscattering spectrometry (RBS) and XRD has revealed a correlation between the emissivity changes and the presence of the various Co-silicide intermediate phases, as shown in Fig. 14. The probing wavelength during the measurement determines the sensitivity for the various phases. Whereas at longer wavelength the transitions of the Co-rich phases are more pronounced, the measurement at $2.4 \mu\text{m}$ is sensitive to the $CoSi$ - $CoSi_2$ transition.

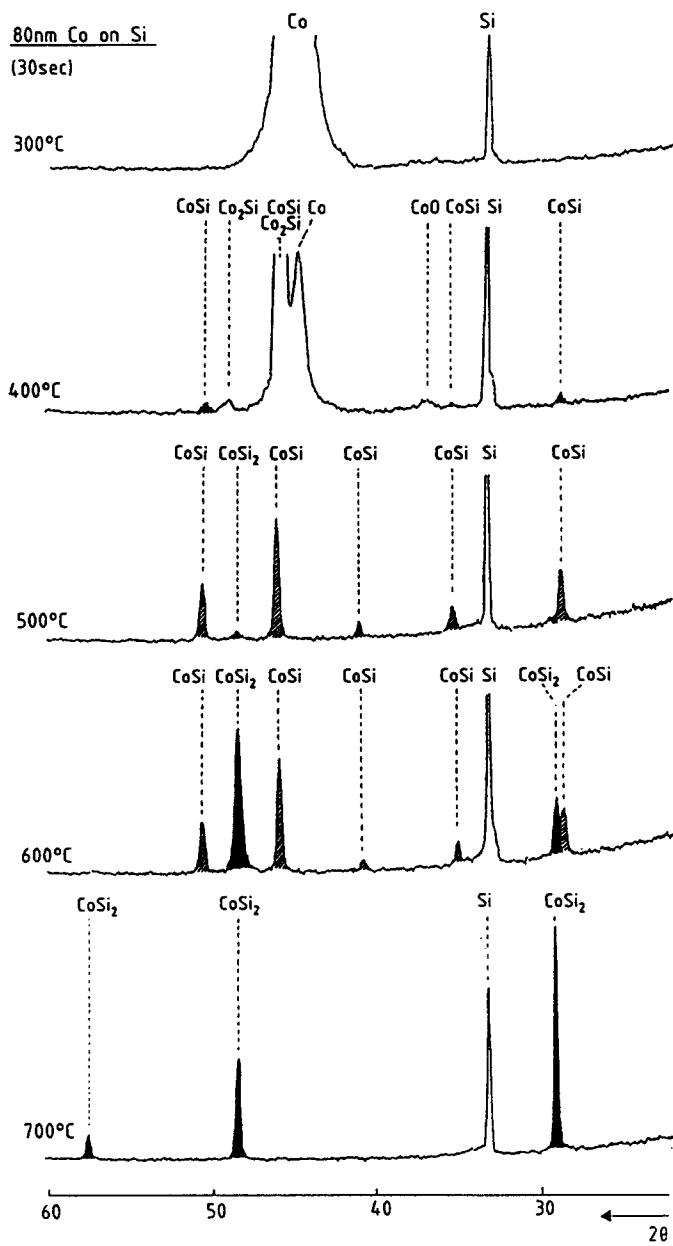


Fig. 12. X-ray diffraction spectra ($Cu K\alpha$) of 80 nm Co on Si after RTP at various temperatures for 30 s.

The *in situ* emissivity measurement has been used to monitor the $CoSi$ - $CoSi_2$ transition during various isothermal anneals. For a silicidation temperature of 520 °C, no $CoSi$ - $CoSi_2$ transition takes place during isothermal annealing for about 40 s. After 50 s some $CoSi_2$ has nucleated. At higher temperatures, around 620 °C, a mixture of $CoSi$ and $CoSi_2$ occurs after 10 s, indicating a much faster nucleation of the $CoSi_2$ phase at this temperature.

The $CoSi_2$ layer grown by the reaction of deposited Co on Si (100) is polycrystalline. The grain size of the layer varies with heat treatment, interfacial cleaning etc. Since the mismatch of $CoSi_2$ and Si is only 1.2% and since the growth of epitaxial $CoSi_2$ on Si by

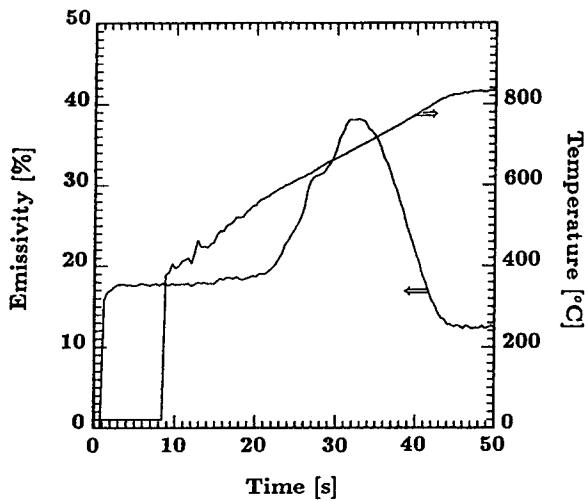


Fig. 13. Emissivity signal originating from the front side of a Si wafer deposited with 40 nm of Co as a function of RTP temperature for a probing wavelength of $2.4 \mu m$. The temperature was measured using the same optical detector and corrected for the emissivity variations.

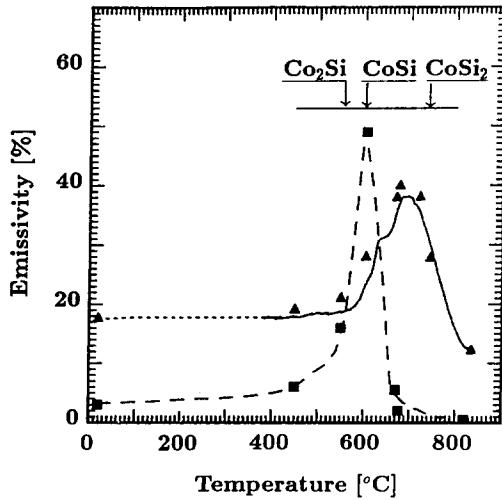


Fig. 14. Emissivity vs. temperature for a Si wafer deposited with 40 nm of Co for a probing wavelength of $2.4 \mu m$ and $10 \mu m$.

MBE has been successful [44–46], the question arises as to why $CoSi_2$ films do not grow epitaxially on Si under these experimental conditions.

A study by Bulle-Lieuwma *et al.* [47] suggests that for (100) Si epitaxial growth of (100) oriented $CoSi_2$ is difficult, owing to the competition between different epitaxial orientations with similar matching. Furthermore, it appears from their study that a good match is obtained only in a small temperature interval. Consequently, various orientations are formed when the temperature is ramped. Therefore, they conclude that considerable attention has to be paid to the temperature program. However, the use of Co/Ti bilayers has resulted in a successful growth of epitaxial (100) $CoSi_2$ on Si (100), using a very similar technique to the conventional silicide growth process (see Section 2.2.7). Ti is mainly used to getter impurities and to reduce the reaction rate. Both mechanisms seem to be relevant to the final epitaxial $CoSi_2$ orientation.

2.2.3.2. Ti/Si reaction

The solid state reaction between Ti thin films and Si has been reported for the first time by Bower and Mayer [48]. Kato and Nakamura [49] investigated the phase formation sequence by XRD and electron diffraction measurements. They concluded that in the initial stage of the reaction Ti_5Si_3 and $TiSi$ are present, converting into $TiSi_2$ at temperatures higher than 650 °C. More recently, the phase formation sequence has been studied under a large number of experimental conditions, leading to different conclusions concerning the exact sequence [50–59]. All treatments lead, however, to the final $TiSi_2$ phase, which is in equilibrium with the Si substrate. In general, one can conclude that the amount of impurities (especially oxygen) [60–62] influences the character of the Ti–Si reaction. In particular, the first phase formed is very dependent on specific experimental conditions. If the processing is very clean (by good control of the native oxide removal [63] or by processing in ultra-high vacuum [64]), no Ti-rich phases are observed.

When special care is taken to minimize the amount of SiO_2 on top of Si [62] the formation of Ti silicide proceeds by diffusion-limited growth, both for furnace silicidation and rapid thermal silicidation [60]. The RBS spectra of Fig. 15 show the evolution of a typical Ti–Si reaction in Ar ambient, using an HF clean prior to Ti deposition [65]. The silicidation starts at 600 °C and saturates at 800 °C. The composition of the silicide at this

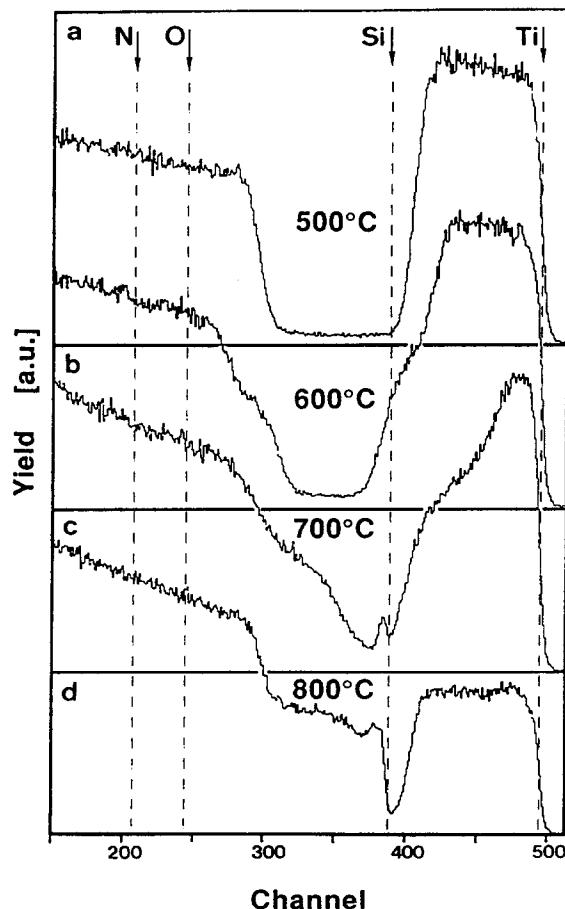


Fig. 15. RBS spectra of a 150 nm initial Ti film on Si and after silicidation in Ar at the indicated temperatures for 10 s. The dotted line corresponds to the surface positions of the elements.

temperature corresponds to $TiSi_2$. Si has been determined as the main moving species during the reaction of Ti with Si for the formation of $TiSi_2$ [66] based on the displacement of implanted Xe markers.

In Fig. 16 the sheet resistance of the layers obtained by reacting Ti on Si is plotted against first silicidation temperature, with (curve b) and without (curve a) chemical removal of the unreacted Ti in an ammonia solution. Curve c represents the sheet resistance of the same samples as curve b after an additional heat treatment at 800 °C. Although shifts in the actual data can occur for slightly different processing conditions, the overall evolution of the sheet resistance is very typical for the Ti-Si reaction. Three distinct regions are observed. In region 1 the Ti film has only reacted partially with Si, resulting in a sheet resistance increase after removal of the unreacted Ti. Between 700 °C and 800 °C (region 2) all the Ti has reacted with Si, but the sheet resistance is further lowered by the second reaction at a higher temperature. $TiSi_2$ can exist in two phases, namely the metastable C49 and the stable C54 phase. In this temperature region C49- $TiSi_2$ is formed, exhibiting a higher sheet resistivity. In region 3 the Ti film has reacted completely to the stable C54- $TiSi_2$, leading to the lowest sheet resistance with a resistivity of about 15 $\mu\Omega$ cm.

The $TiSi_2$ phase formation during reaction of Ti with Si has been confirmed by *in situ* XRD measurements [67]. The results are summarized in Fig. 17. The nucleation of the C49- $TiSi_2$ phase starts around 550 °C, whereas the transition to the C54 phase takes place at about 700 °C. These transition temperatures are in good agreement with results reported in refs. 63 and 68. The transition temperature depends on film thickness, impurities in the Ti and doping elements in the Si [68,69]. C49- $TiSi_2$ has a specific resistivity of more than 60 $\mu\Omega$ cm, which makes it unattractive for applications. Complete conversion to C54- $TiSi_2$ is required.

A detailed high-resolution TEM study of the C49 phase has been carried out by Chou *et al.* [70]. They claim that the metastability of C49- $TiSi_2$ is primarily due to its low density and a large number of stacking faults compared to C54- $TiSi_2$. There are four equivalent stacking schemes of atomic layers along the [010] direction. It is very easy to misplace one atomic layer and to affect the subsequent stacking sequence. A high frequency of misplacements results in a high density of stacking faults and a disordered structure.

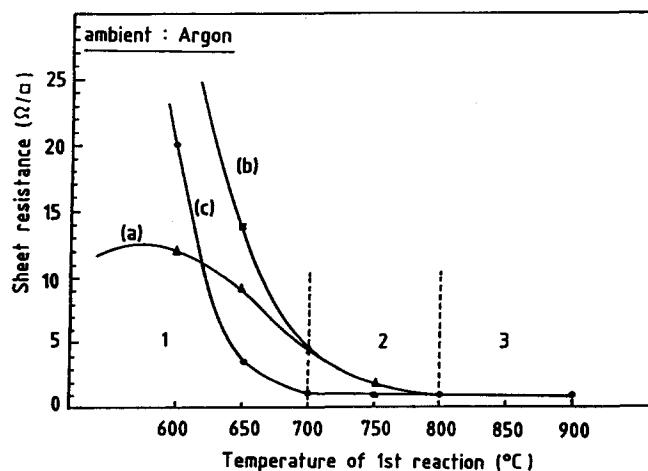


Fig. 16. Sheet resistance as a function of the first reaction temperature during silicidation of 60 nm Ti on Si: (a) after a first heat treatment for 30 s; (b) after subsequent unreacted Ti removal; (c) after an additional treatment at 800 °C for 30 s.

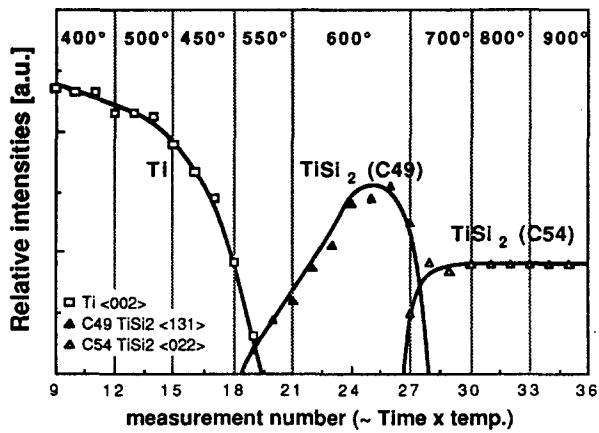


Fig. 17. *In situ* XRD measurement as a function of temperature and time of a 100 nm Ti film during the silicidation reaction. The sample was held for 15 min at the same temperature. In this time interval, three XRD spectra were recorded.

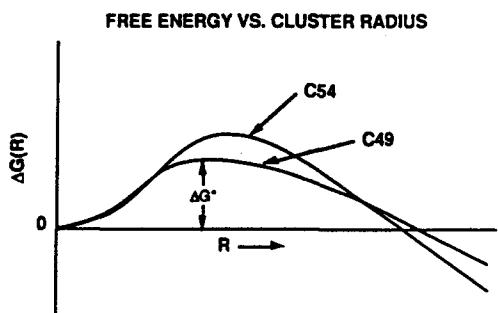


Fig. 18. Free energy vs. nucleus size for C49 and C54- $TiSi_2$ (after ref. 64).

The metastability of C49- $TiSi_2$ has been verified by several authors [63–71]. No reversible transformation was detected after lengthy annealing of C54- $TiSi_2$ below the transition temperature. The formation of C49- $TiSi_2$ by a solid state reaction between Ti and Si indicates that the nucleation and growth are energetically favoured over that of C54- $TiSi_2$. The nucleation process is influenced by surface and interface energies. The relation of free energy versus nucleus size for both $TiSi_2$ phases as proposed by Nemanich *et al.* [64] is illustrated in Fig. 18. Since the C49- $TiSi_2$ is metastable, its bulk free energy must be larger than that for C54- $TiSi_2$ for all nucleus sizes. However, the preferred nucleation of the C49 phase is an indication of a smaller surface energy than that of the C54 phase. The lower bulk energy of the C54 phase will dominate its higher surface energy term for an increasing nucleus size. This has serious consequences for the transition of the C49 phase into the C54 phase. For a fine grained C49- $TiSi_2$ film, the surface to volume ratio will be significantly larger than for a coarse grained layer. The transition of a small grained C49- $TiSi_2$ layer into the C54 form will be difficult, since the free energy difference between the C49 and the C54 nuclei is too large to be overcome by the lower bulk energy of the C54 phase. This agrees with the increase of C49–C54 transition temperature for thinner silicide layers. As will be discussed in Section 3.2.2, the nucleation of the C54 phase becomes problematic for thinner layers, and hampers the scalability of the $TiSi_2$ process.

2.2.4. Effects of the crystallinity of the substrate

The crystallinity of the Si substrate implies important thermodynamic consequences, considering the reaction sequence of a metal with Si [35]. This is especially true for the last stage of the reaction, where the disilicide grows at the expense of the monosilicide. For most silicides the disilicide on Si is barely more stable than the monosilicide. Therefore it is important to consider the following reaction schemes and their associated free energy changes ΔG :



where M stands for the metal, x for crystalline and α for amorphous Si and $\Delta G_{\alpha-x}$ for the Gibbs free energy of crystallization of α -Si. ΔG_x is of the order of kT [1,72]. As already mentioned in Section 2.1.2, for reactions with such small free energy changes, nucleation plays a crucial role in the silicidation process [3]. The heat of crystallization of α -Si is much higher, of the order of 15 kJ mol^{-1} [73,74], which is much more than the free energy change from the monosilicide to the disilicide.

The above explains why a nucleation-controlled process occurs during the growth of the disilicide from the monosilicide on x-Si and a diffusion-controlled growth process on α -Si, for many silicides including $CoSi_2$ [75] and $TiSi_2$ [76].

The formation of cobalt silicide on top of amorphous silicon is faster and provides a better surface morphology [77,78]. If the Si has been pre-amorphized by Ge before metal deposition, the $CoSi_2$ grain size is much smaller. Similar results were obtained for titanium silicide. Moreover, the transition from C49– $TiSi_2$ into C54– $TiSi_2$ takes place at lower temperatures and/or at shorter times [78].

Silicidation of both Co and Ti are similar on mono- and polycrystalline Si [79–81]. Although polycrystalline Si has a preferential (111) orientation, no major differences in reaction kinetics have been reported. This is in agreement with the finding that the reaction kinetics for $CoSi_2$ on (111) Si is the same as for (100) Si [35]. No metal diffusion along grain boundaries towards the underlying gate oxide has been reported during normal silicidation conditions. The silicidation reaction affects, however, the grain size of the underlying polycrystalline Si. Chou *et al.* [82] report on the enhanced grain growth of phosphorous-doped poly-Si during Ti silicidation at 700°C and attributes this to the redistribution of P, analogous to the alloying and dealloying process in diffusion-induced grain boundary migration. On the other hand, Zheng *et al.* [83] observed no enhanced grain growth during silicidation of Ti on As-doped poly-Si at 750°C for 8 h.

2.2.5. Influence of the annealing ambient

Although one is tempted to consider an M–Si diffusion couple as a two-component system, the actual experimental conditions are very often such that more components come into play. A factor that has certainly to be taken into account is the role of elemental impurities coming from the ambient during silicidation.

The effect of the silicidation ambient was recognized early on and is especially important for the case of Ti [84,85]. The formation of $TiSi_2$ in an Ar ambient using RTP has been investigated by Krooshof *et al.* [65] using RBS and elastic recoil detection (ERD). Information about the depth distribution of N and O and the total amount of H in the layer is obtained from ERD spectra. Figure 19 gives an overview of the amount of incorporated impurities in the samples. Apparently, nitrogen is incorporated during the RTP treatment and is

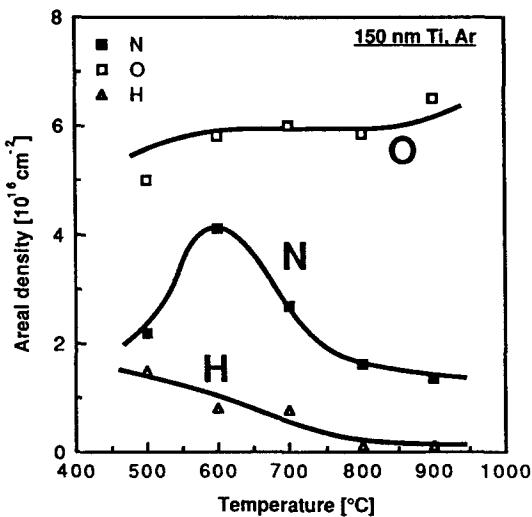


Fig. 19. The number of O, N and H atoms in the layer structures as a function of the RTP temperature in Ar. The initial Ti layer was 150 nm thick.

mainly located in a thin surface layer (10 nm). The N content in this layer depends slightly on the temperature.

The presence of oxygen in Ti is easily detectable after RTP treatment at 500 °C. It extends deeper into the unreacted Ti film. Its concentration is estimated to be below 4 at.-% in the bulk of the Ti film. After RTP at 600 °C the total amount of oxygen does not increase, but it concentrates at the interface between the silicide and the Ti. The O is further snowploughed by the silicide formation front into the unreacted Ti layer at higher temperatures [65,86]. The amount of H in the Ti is about 0.5% after 500 °C treatment and decreases for higher temperatures.

Silicidation of Ti in an N_2 ambient represents a totally different case, since N_2 reacts with Ti at the temperatures used for silicidation and plays as such an active role in the whole process. The reaction sequence between Ti and Si is basically the same as that in Ar, yielding almost the same set of RBS spectra as in Fig. 15. However, except for the fact that for the highest heat treatment almost all Ti atoms are involved with the silicidation reaction in Ar, only 85% of the Ti atoms have reacted with Si in an N_2 ambient for the same experimental conditions (Fig. 20). Again, a full study of incorporated O, N and H impurities was carried out by Krooshof *et al.* [65]. The overview of the measurements is given in Figs. 21 and 22. The behaviour of H is similar to that in the case of Ar annealing. Oxygen is distributed throughout the bulk of the Ti film at 500 °C. At this temperature, nitrogen is incorporated in a thin surface layer of about 10 nm in an amount which is comparable to the Ar case. At higher temperatures the amount of N incorporated is larger than for Ar and reaches a saturation level. The number of O atoms remains constant, but its distribution in the layer changes with temperature. The O moves both from the silicide reaction front to the surface and inwards from the surface. At temperatures above 750 °C a trilayer structure results, with an oxygen-rich layer being squeezed between the silicide and the titanium nitride on the surface. It should be noted that the relative thickness of the layers in the trilayer structure depends on experimental parameters.

The formation of a TiN layer on top of $TiSi_2$ is indeed predicted by the ternary Ti–Si–N phase diagram calculated by Beyers *et al.* [87]. This diagram is represented in Fig. 23. TiN

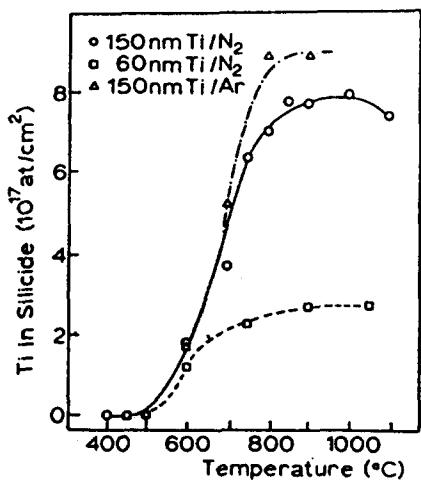


Fig. 20. Number of Ti atoms present in the silicide as a function of the RTP temperature for an initial Ti thickness of 150 nm.

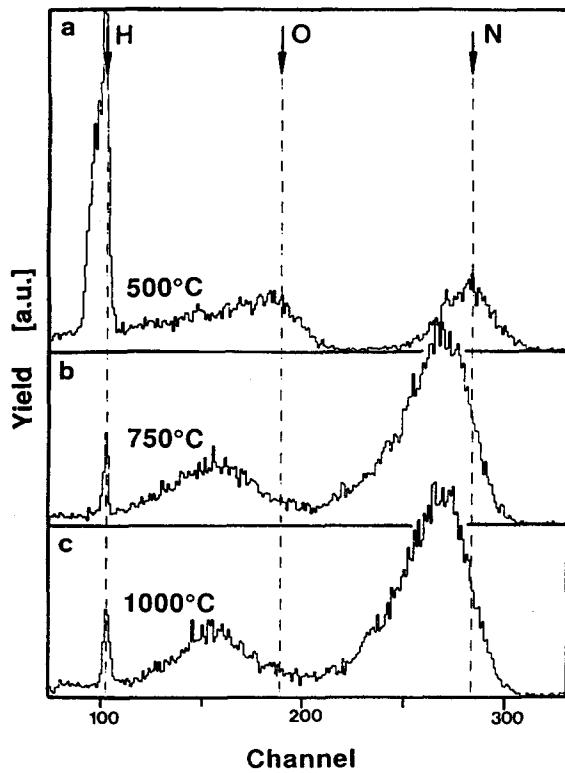


Fig. 21. ERD spectra of N_2 annealed samples at the indicated temperatures. The initial Ti thickness was 150 nm. The dotted line gives the surface positions of the elements.

has a tie line towards $TiSi_2$, indicating the thermodynamical stability of the $TiN/TiSi_2$ structure. However, if more N is supplied to the system and if there are no kinetic constraints, an evolution of the $TiN/TiSi_2$ to TiN/Si is possible, as represented by the tie line between TiN and Si . The growth of TiN at the expense of previously grown $TiSi_2$ has been experimentally observed [88,89]. The nitridation of $TiSi_2$ requires, however, very high temperatures and is

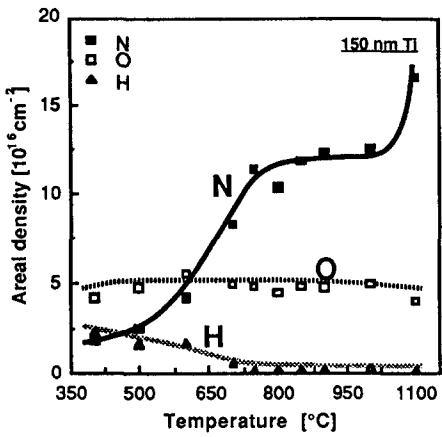


Fig. 22. The integrated number of N, O and H atoms for the same samples versus silicidation temperature.

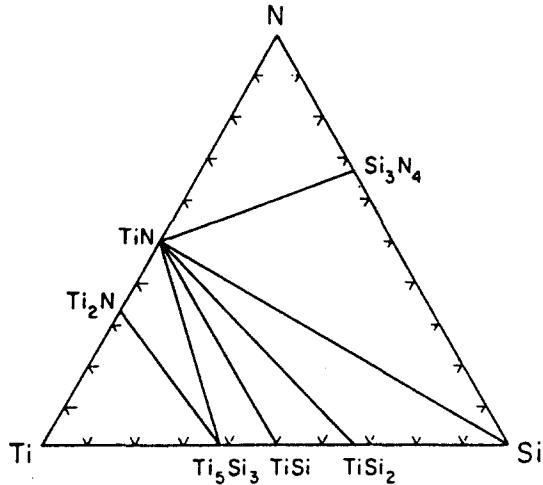


Fig. 23. Ti-Si-N ternary phase diagram for a temperature range of 700 °C to 1000 °C (after ref. 87).

very sensitive to the presence of a native SiO_2 on the silicide [90]. The use of NH_3 as a substitute for N_2 allows for lower nitridation temperature [90,91]. A summary of the evolution of the reaction of Ti with Si in N_2 and Ar ambient is schematically shown in Fig. 24.

The effect of the ambient on Co silicidation is much smaller than for Ti. As seen in the XRD spectrum in Fig. 12, a CoO peak appears at 300–400 °C. This peak disappears again for higher temperature treatments. Since the solubility of N in Co is very low and no compounds of Co and N are likely to form, the effect of N on silicidation is negligible.

It should be noted that impurities in the ambient gas can also play a significant role during silicidation. Since the reaction takes place at atmospheric pressure, contamination of the ambient can occur due to inefficient purging of the furnace, door openings etc. It has been shown that sub-p.p.m. changes in oxygen contamination level of the ambient gas during Ti silicidation can have measurable effects on the sheet resistance of the film [92,93].

Recently, studies have been undertaken to evaluate the influence of the processing furnace itself on ambient purity [94]. Current technology allows process gases to be delivered to the furnace with such high purity that the furnace itself becomes the limiting factor on the quality of the gas, close to the wafer surface during silicidation. Using FAST moisture

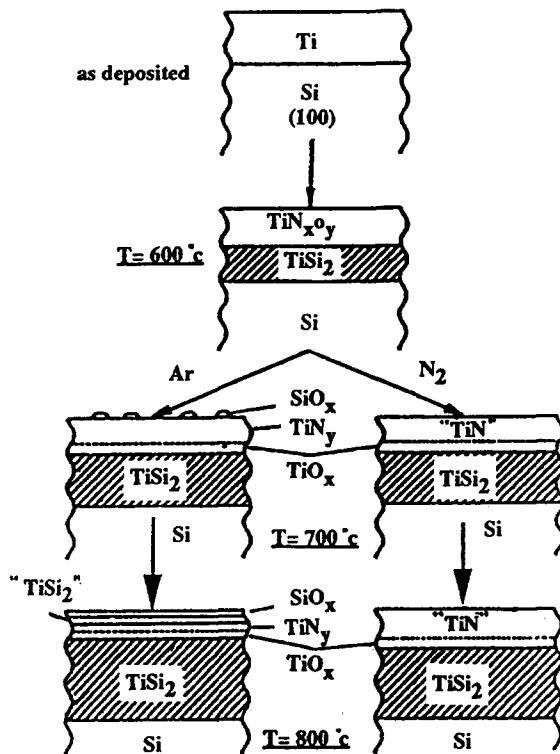


Fig. 24. Schematic presentation of the evolution of the layer structures during silicidation of Ti on Si in Ar and N_2 .

analysis [95], rapidly changing moisture levels can be characterized during RTP. Increased moisture levels have been correlated with specific experimental conditions, such as door opening, purging times and flows etc. Even the wafer itself was found to contribute considerably to the moisture level during processing. An investigation on how this affects silicidation processes is in progress.

2.2.6. Ion mixing

Ion mixing, i.e. silicide formation by implantation through the M-Si interface, is a technique which has received attention over the years. Several detailed investigations have been reported on ion mixing of Ti/Si and Co/Si diffusion couples [96]. Q -curves, representing the onset of radiation-enhanced diffusion have been established. Whereas in general the phase sequence is the same for the ion beam-induced reaction as for the thermally induced reaction, some differences are noticeable. The growth of the amorphous layer (see Section 2.2.2) in the case of Ti/Si mixing is much more important and the three intermediate phases have been observed simultaneously in a layer-by-layer geometry in the case of Co/Si. The full discussion of ion mixing of Ti/Si and Co/Si diffusion couples is beyond the scope of this paper.

Room temperature ion mixing with doses similar to those necessary for making highly doped Si is considered attractive for some applications. The silicide formation is initiated by ion implantation, yielding an amorphous layer at the metal/Si interface, which is thicker than after sputter deposition. In addition, the implanted Si underneath the metal/Si interface is amorphous, and as such the nucleation of the disilicide phases becomes more favourable (Fig. 25), as discussed in Section 2.2.3.

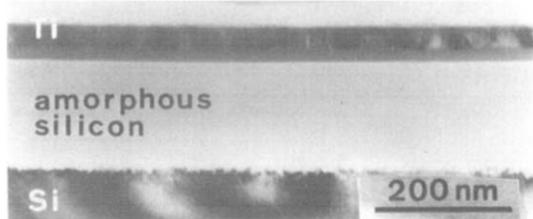


Fig. 25. Cross-sectional TEM micrograph of a 60 nm Ti layer on top of Si after ion mixing with $5 \times 10^{15} \text{ cm}^{-2}$ As at 200 keV.

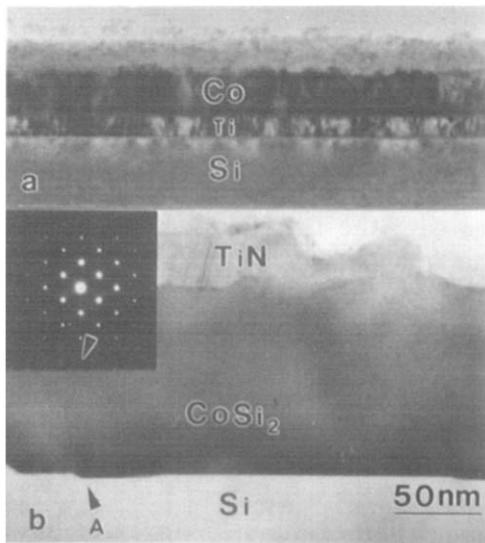


Fig. 26. Cross-sectional TEM image of (a) as-deposited (100) Si with 10 nm Ti/25 nm Co and (b) after annealing at 750 °C and at 900 °C with a wet etching of the unreacted alloy in between the two high-temperature steps. A $\langle 011 \rangle$ zone axis selected area diffraction pattern from the Si/ $CoSi_2$ interface is shown in the inset (after ref. 99).

2.2.7. Formation of epitaxial $CoSi_2$

Whereas the formation of epitaxial $CoSi_2$ layers on (100) Si could only be achieved by MBE and ion beam synthesis by the process called mesotaxy, recently a technique has been developed based on Ti/Co multilayers [97–103]. This technique is very attractive since it allows the growth of epitaxial $CoSi_2$ layers in a way which is completely compatible with the current technology of silicide formation. The process has some similarities with the technique of solid phase epitaxy through a transport medium, which has been observed both for Si and III-V compounds [104,105]. Here, however, a reaction takes place between Co and Si. The mechanism is based on the absorption of interfacial impurities by the thin Ti layer. A complete picture of how the epitaxial growth comes about is not available yet. A Ti-Co layer remains on top of the $CoSi_2$ layer. Figure 26 shows cross-sectional TEM micrographs of an as-deposited and reacted sample [99]. The interface between the silicide and the Si is atomically flat. The epitaxial nature of the silicide has been confirmed by high-resolution TEM. Channelling yields for the $CoSi_2$ are about 17%, which is still high when compared with other techniques for the growth of epitaxial $CoSi_2$. Treatment at higher temperatures reduces the channelling yield to values as low as 4%.

Typical for the epitaxial $CoSi_2$ layers on Si are the facets along the (111) planes. They are energetically more favourable and are determining the roughness of the epitaxial silicide/

Si interface. Interestingly enough these facets have been shown to shrink upon high-temperature treatments [101]. This is contrary to what has been observed for epitaxial $CoSi_2$ layers made by mesotaxy and needs further investigation.

2.2.8. Reaction of Ti and Co on SiGe alloys

With the recent interest in the use of SiGe alloys for device fabrication, silicide and germanide formation have been investigated by a solid state reaction of Ti and Co on SiGe alloys. The reactions between metals and Ge have already been reported some years ago [106], indicating that germanide formation takes place and is often similar to silicide formation. The reaction temperature is, however, in general lower for germanide than for silicide formation. Recently, Ti and Co germanides have been formed using rapid thermal annealing in argon and nitrogen ambients [107]. Similar to silicidation, the formation of titanium germanide is affected by the annealing ambient. A sheet resistivity of $20 \mu\Omega \text{ cm}$ has been achieved for $C54-TiGe_2$. On the contrary, the formation of Co germanide is not affected by the annealing ambient. Resistivities of $35 \mu\Omega \text{ cm}$ have been measured for $CoGe_2$.

Co silicidation of strained $Si_{1-x}Ge_x$ alloys has been reported to yield a mixture of Si-rich $CoSi_{1-x}Ge_x$, Ge-rich $Si_{1-y}Ge_y$ and possibly $CoSi_2$, with the first two exhibiting some degree of epitaxial alignment with the substrate. The influence of silicidation on strain requires further investigation [108].

2.3. Silicidation of doped Si

The silicidation of Ti and Co is often carried out on highly doped Si. Since the dopants play an active role in the silicidation process it is important to consider the silicidation of both n^+ and p^+ Si. In case of silicidation of doped Si, one is concerned about various effects. The dopants have an influence on the kinetics of the silicidation reaction. The distribution of the dopants in the silicide and the Si is of predominant importance. In all cases, however, one aims at minimizing the effect of dopants both on the silicidation reaction itself and on the dopant profile, in particular at the silicide-Si interface.

2.3.1. Metal-dopant interactions

The final aim of the silicidation process, independent of the specific technology used, is to obtain a thin film silicide on top of a highly doped Si-region. In order to check whether it is likely that the silicidation reaction will evolve to that final state, the thermodynamic stability of the silicide with respect to doped Si has to be considered. The stability of doped Si with respect to the contacting silicide can be investigated by calculating the critical portion of the ternary diagram (Fig. 27). Ternary phase diagrams have been demonstrated to be valuable tools for the understanding of thin film metallization processes. In the absence of an experimental ternary diagram, the determination of tie lines between elements and intermediate phases in ternary systems enables the construction of a ternary diagram. Regions of three-phase equilibrium in a ternary phase diagram form triangles in isothermal sections and the phases at the corners of such triangles are thermodynamically stable in contact with each other. The sides of a triangle are tie lines between two phases and are established by free energy calculations. The existence of tie lines between the most stable silicides on Si i.e. MSi_2 and the solid solution of the dopant in Si ($Si(D)$) is evaluated by considering the various decomposition reactions yielding a metal-dopant compound (M_xD_y) and Si i.e.



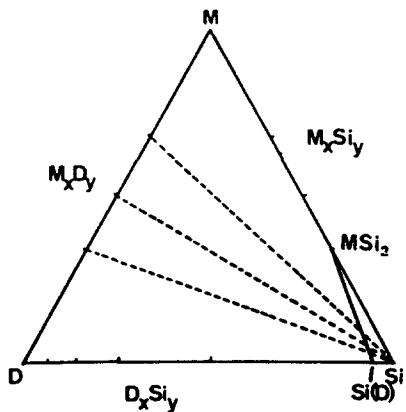


Fig. 27. Ternary phase diagram of an M–Si–D system showing a stable tie line between the silicide (MSi_2) and the solid solution of D in Si ($Si(D)$). The dashed lines indicate the absence of stable tie lines between the metal–dopant compounds (M_xD_y) and Si.

The evaluation of the thermodynamic stability of M–Si–D systems has been carried out for a large variety of metals [109,110].

In the following section the $MSi_2/Si(D)$ decomposition reactions of the M–Si–D systems will be presented for the case of M being Ti or Co and D being As or B.

The Gibbs free energy change ΔG for the above reaction (which is the thermodynamic driving force), has been taken as a measure for comparing thermodynamic stabilities of the various $MSi_2/Si(D)$ couples. The Gibbs free energy of the solid solutions of As and B in Si are expressed in the regular solid solution model:

$$G = (1-x)G^{\circ}_{Si} + xG^{\circ}_D + RT[x \ln x + (1-x) \ln(1-x)] + x(1-x)L_{Si-D} \quad (21)$$

In this equation, G°_{Si} and G°_D are the Gibbs free energies of Si and dopant, respectively, x is the dopant concentration in Si, L_{Si-D} the regular solution interaction parameter, R the gas constant, and T the absolute temperature. We consider Si with a 1 at.% solid solution of B or As. A compilation of thermodynamical data is given in refs. 109 and 110.

The B-doped systems are investigated for temperatures ranging from 600 to 1300 K. For the As-doped systems the highest considered temperature is 900 K, which is slightly higher than the sublimation temperature of As.

For the calculation of the ternary diagrams, the following simplifications were made:

1. In the absence of thermodynamic data, the $SiAs$, $SiAs_2$ and Co_3B phases have been excluded. For the same reason, no ternary phases have been considered. The only known ternary phase among the present systems is BCo_5Si .
2. Only phases recorded in the phase diagrams of Hansen, Elliot and Shunk [8,111,112] have been considered.
3. Ti and Co and the intermediate phases of the binary systems have been treated as stoichiometric.

Based on the thermodynamic data of the binary systems, an isothermal section of the ternary diagrams was calculated. The existence of tie lines among the various elements, compounds and the 1% solution of dopants in Si was critically examined. To check for the existence of a tie line between $TiSi_2$ and $Si(B)$, and between $CoSi_2$ and $Si(B)$, various possible decomposition reactions have been considered, which are listed in Table 2. The Gibbs free energy change ΔG has been calculated for each possible reaction. The results

TABLE 2

Gibbs free energy changes (ΔG) of possible reactions indicating the existence/non-existence of a stable tie line at 1000 K. Here $Si_{0.99}B_{0.01}$ represents a solid solution of B (1 at.%) in Si

Reaction	ΔG
1. $50Si_{0.99}B_{0.01} + 1.5Ti_{0.333}Si_{0.667} = 50.5Si + Ti_{0.5}B_{0.5}$	+ 12923
2. $57.14Si_{0.99}B_{0.01} + 1.2857Ti_{0.333}Si_{0.667} = 57.4257Si + Ti_{0.4286}B_{0.5714}$	- 361
3. $66.667Si_{0.99}B_{0.01} + Ti_{0.333}Si_{0.667} = 66.667Si + Ti_{0.333}B_{0.667}$	- 10192
4. $50Si_{0.99}B_{0.01} + 1.5Co_{0.333}Si_{0.667} = 50.5Si + Co_{0.5}B_{0.5}$	+ 37324
5. $33.333Si_{0.99}B_{0.01} + 2Co_{0.333}Si_{0.667} = 34.333Si + Co_{0.667}B_{0.333}$	+ 46042

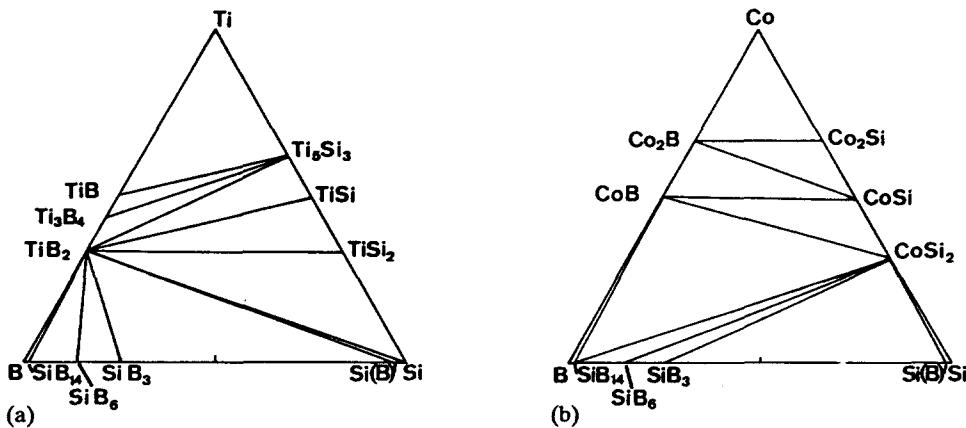


Fig. 28. Isothermal section of the phase diagram of the ternary M-Si-B systems at 1000 K (a) for Ti and (b) for Co. Si(B) stands for the solid solution of B in Si.

show that for the $TiSi_2$ -Si(B) system, reaction (3) is strongly favoured compared with the reactions (1) and (2). In other words, there is no tie line between $TiSi_2$ and Si(B). On the other hand, in the case of $CoSi_2$ -Si(B), neither reaction (4) nor reaction (5) is thermodynamically allowed, indicating the presence of a tie line between $CoSi_2$ and Si(B). Complete isothermal sections of the Ti-Si-B and the Co-Si-B systems (Fig. 28) were calculated in a similar way by checking the various possible reactions at a temperature of 1000 K.

Comparing the diagram of Ti-Si-B with that of Co-Si-B, there are some remarkable differences. In the case of Co-Si-B, tie lines exist between the disilicide and the Si-B compounds, but not between $CoSi_2$ and the solid solution of B in Si. For $TiSi_2$ and the solid solution of B in Si, such a tie line does not exist. This leads to the conclusion that B doped Si is stable with respect to the overlaying $CoSi_2$ film, whereas it is unstable with respect to an overlaying $TiSi_2$ film.

Even though the calculation of these ternary diagrams of B-doped Si is not always based on accurate thermodynamic data, the agreement between the calculated diagrams and some experimental work on the ternary system based on powders is extremely good [113-115].

Similar calculations were carried out for the $TiSi_2$ -Si(As) and $CoSi_2$ -Si(As) systems. The diagrams of the Ti-Si-As and the Co-Si-As systems are shown in Fig. 29 for a temperature of 900 K. In both the Ti-Si-As and the Co-Si-As systems there are no stable tie lines between the disilicide and the As-doped Si. This leads to the conclusion that the

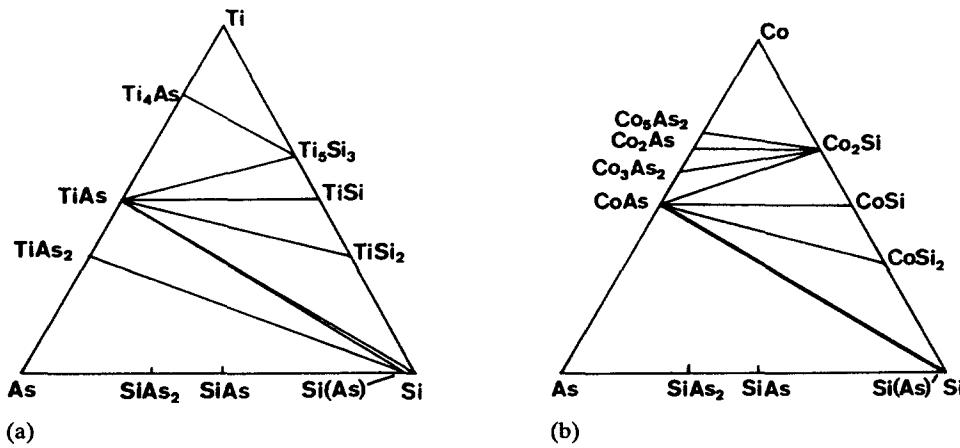


Fig. 29. Isothermal section of the phase diagram of the ternary M-Si-As systems at 900 K (a) for Ti and (b) for Co. Si(As) stands for the solid solution of As in Si.

As-doped Si is unstable with respect to both the overlaying $TiSi_2$ and $CoSi_2$. In the case of $TiSi_2$ -Si(As), the calculation shows that the formation of Ti_4As_3 is not possible, but that the formation of $TiAs$ and $TiAs_2$ is equally likely. However, experimental observations indicate that the formation of $TiAs$ is kinetically favoured over the formation of $TiAs_2$. According to the calculations for the $CoSi_2$ -Si(As) system, the formation of $CoAs$ is possible. The heat of formation is not large.

The presence of As-rich Co-As compounds was not considered in this study, since they were not mentioned in ref. 8. Elliot [111] and Shunk [112] report on some observations of $CoAs_2$ and $CoAs_3$, but remain inconclusive about their structure. Barin and Knacke [116] report, however, thermodynamic data on the heat of formation of $CoAs_2$, Co_2As_3 and $CoAs_3$. When these more As-rich compounds are considered in the Co-As system, the absence of a tie line between $CoSi_2$ and Si(As) becomes questionable [117], since small positive heats of reaction are calculated for the decomposition of the silicide on Si(As) into $CoAs_2$ and $CoAs_3$. Taking into account the inaccuracy of the thermodynamic data used in the calculations, no conclusion can be drawn about the instability of the tie line between $CoSi_2$ and Si(As) for the As-rich compounds. The presence of a tie line between $CoSi_2$ and Si(As) would not be surprising, since no experimental indication has been observed for the formation of Co-As compounds in our experiments.

2.3.2. Kinetics of silicidation

For Ti silicidation of As-doped Si, it has been shown that the $TiSi_2$ formation rate is dependent on the As concentration in the Si. This is attributed to $TiAs$ particles stuffing the $TiSi_2$ grain boundaries, and resulting in a kinetic barrier for Si diffusion and $TiSi_2$ formation [69,118]. In addition, the transformation of the C49 into the C54- $TiSi_2$ phase is retarded by the presence of As.

Fewer data are available on the effect of dopants during the formation of $CoSi_2$. As mentioned in the previous section, compound formation between Co and dopants has never been reported, in agreement with the predictions of thermodynamics.

Very recently, the effect of As on the nucleation of $CoSi_2$ was investigated by *in situ* monitoring of the emissivity during the Co/Si(As) reaction [43]. Figure 30 gives the emissivity vs. time plot for the silicidation of 40 nm Co on highly As-doped Si. As discussed in Section

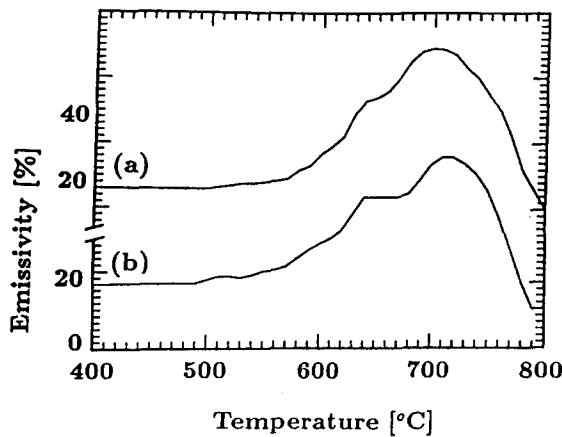


Fig. 30. Emissivity curves measured at $2.4 \mu m$ during RTP of 40 nm of Co on Si. Curve (a) represents the emissivity on undoped Si, curve (b) on As- ($1.5 \times 10^{15} \text{ cm}^{-2}$, 80 keV) doped Si.

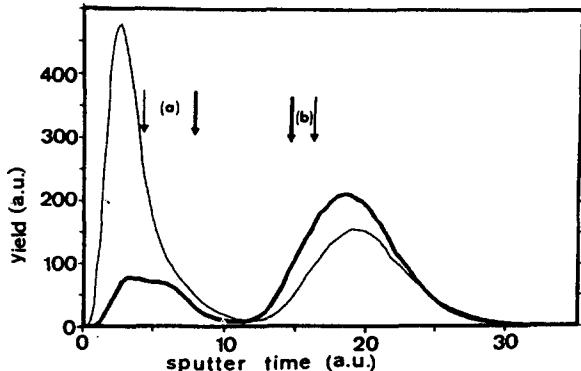


Fig. 31. SIMS profile of B redistributed in an Si ($B, 5 \times 10^{15} \text{ cm}^{-2}$, 35 keV) Ti (60 nm) sample after silicidation using RTP for 10 s at 700°C (thick line) and 1100°C (thin line). The arrows indicate the location of the (a) Ti/TiSi_2 and (b) TiSi_2/Si interfaces as measured by RBS.

2.2.3, the shoulder in the graph is an indication of the delay of CoSi_2 nucleation. Although the effect on the final CoSi_2 is minimal, retardation of the CoSi_2 nucleation can be noticed.

2.3.3. Redistribution of dopants during silicide formation

When the upper part of the doped Si substrate reacts with the overlying metal, the silicidation reaction will cause a redistribution of the dopants with respect to the forming silicide and the Si underneath. The generation of point defects during the silicidation process can possibly influence the diffusion behaviour of the dopants in the Si substrate.

2.3.3.1. Redistribution of dopants in the Si consumed by the silicide

The study of the dopant redistribution in the Si concentrates mainly on the question of whether the dopant accumulates at the silicide/Si interface or is incorporated in the silicide and eventually piles up at the silicide/metal interface [119–123].

For Ti silicidation [124–126] on both As- and B-doped Si, accumulation of impurities at the Ti/TiSi_2 interface and depletion at the TiSi_2/Si interface have been observed. Figure 31 shows a typical example of the B redistribution in Si after Ti silicidation as measured with secondary ion mass spectroscopy (SIMS). Accumulation of B in the unreacted Ti is

observed, whereas the silicide layer itself remains essentially free of dopants. The B peak accumulating in the unreacted Ti layer is larger for silicidation at higher temperatures. The interpretation of the B and As redistribution during silicidation is not straightforward, since many processes occur simultaneously, such as the partial nitridation of the Ti etc. The accumulation of B in the unreacted Ti is consistent with the idea of Ti-B compound formation, as well as the depletion of B in the underlying Si, associated with the predicted instability of B-doped Si with respect to the overlying silicide. The low B concentration in the silicide is an indication, in the absence of any experimental determination, of a low solid solubility of B in $TiSi_2$. These arguments are in agreement with the findings of Gas *et al.* on B diffusion in $TiSi_2$ [127].

For silicidation of As-doped Si, the accumulation of As at the metal/silicide interface and the depletion of As in the silicide is similar to the case of B-doped Si (Fig. 32). In addition, evaporation of As has been reported. The evaporation can be partly responsible for dopant depletion at the silicide/Si interface. The formation of Ti-As compounds was unambiguously confirmed [69,128] by X-ray dispersive analysis and micro-diffraction.

Although the solid solubility of dopants in silicides is not known, there are strong indications that the solid solubility of As and B in $TiSi_2$ and $CoSi_2$ is significantly lower than in Si. Due to the consumption of a doped Si layer during silicidation and the strong difference in solid solubility, the dopant concentration in Si is expected to increase. Since the silicidation reaction proceeds very quickly, the dopant will be pushed ahead by the progressing silicide/Si interface if the diffusion through the silicide is slow and the solubility within the silicide is low at the reaction temperature. The dopant accumulation at the silicide/Si interface, generally referred to as the "snowplough" effect, is of particular interest for applications in technological processes. In addition, this phenomenon is interesting because of the possible generation of point defects during silicide formation. The snowplough effect was originally associated with the formation mechanism of near-noble metal silicides [119]. It has been reported extensively for Pt [129] and Pd [120,130], and also for Ni [131]. The detailed atomic mechanism enabling the dopant species to accumulate at the silicide/Si interface is still unclear. It remains to be elucidated whether the high stress level at the silicide/Si interface has to be taken into account. Snowplough effects have never been reported for $CoSi_2$ or $TiSi_2$, except during extreme conditions using ion beam mixing [132].

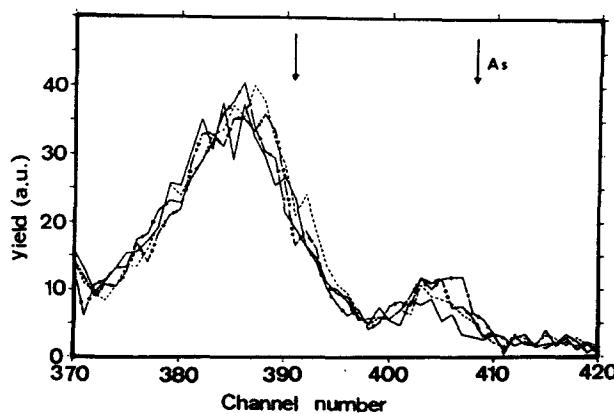


Fig. 32. RBS As signal after silicidation using RTP at 700 °C of Si (As, $5 \times 10^{15} \text{ cm}^{-2}$, 200 keV)/Ti (60 nm) samples for 3 s (solid line), 8 s (dashed line), 15 s (dot-dashed line) and 20 s (double-dot-dashed line). The arrows indicate the position of the As located at the surface and at the $TiSi_2/Si$ interface.

2.3.3.2. Redistribution of dopants in the Si substrate

The Si consumption, inherently connected with the silicidation process, can in some cases affect the behaviour of dopants. The effect of Ti-silicidation on B-doped and unannealed Si was investigated in [133]. A strong impact of Ti-silicidation on B diffusion was observed, since the creation of a dislocation network, characteristic for annealing of B-implanted Si, was inhibited by the Si consumption.

Preliminary results on As, Sb and B profiles in Si after Ti silicidation at temperatures up to 1100 °C show hardly any diffusion [96,133]. It is, however, unlikely that this should be completely attributed to point defect generation. The chemical reaction needed to form TiB_2 and $TiAs$ represents a driving force for the dopants to diffuse towards the silicide film, resulting in an apparently retarded diffusion. More experiments need to be done to determine which phenomena can be attributed to chemical effects and which to a possible generation of point defects.

2.3.4. Diffusion of dopants in the silicide

The diffusion of dopants in the silicide is of interest for the implementation in device technologies. From a crystallographic point of view, the structures of $TiSi_2$ and $CoSi_2$ are very different: the former has a very high atomic density, whereas the latter exhibits a very open structure with as many empty metal lattice sites as there are metal atoms.

Experiments concerning dopant diffusion in silicide films have mainly been based on monitoring of the concentration profiles of implanted species after heat treatment [127,134–137]. Since the silicide films are polycrystalline, both lattice and grain boundary diffusion contribute to the observed dopant mobilities. Lattice diffusion is responsible for the modification of the concentration profile near the implantation peak, whereas grain boundary diffusion and interface diffusion allow long-range dopant transport. In addition, the diffusion at the silicide/silicon interface plays an important role.

Gas *et al.* [135] reported on the diffusion elements B, P, As, Sb, Ga and Ge in $TiSi_2$. For B-implanted $TiSi_2$, hardly any diffusion is observed. The lack of diffusion of B in $TiSi_2$ must be attributed to the formation of TiB_2 (see Section 2.3.1). The diffusion of Sb implanted in $TiSi_2$ is also negligible. However, a tail is observed in the distribution for annealed samples at about 1×10^{17} at. cm⁻³. This behaviour might be due to the very low solid solubility of Sb in $TiSi_2$ and to the possible adsorption of Sb at grain boundaries.

The diffusion of P, As, Ga and Ge in $TiSi_2$ is significant at temperatures in the range of 600–800 °C. Careful interpretation of the SIMS results led to a distinction between the grain boundary and lattice contributions to the diffusion coefficient. Figure 33 shows the coefficient of lattice diffusion as a function of reciprocal temperature. Sb and B are not included in the picture, since their diffusion lengths are not measurable. The activation energy for As and P lattice diffusion in $TiSi_2$, is comparable to the activation energy for Si self-diffusion in $TiSi$ which is 1.8 eV [62]. This similarity suggests that P and As are diffusing in $TiSi_2$ as substitutional impurities do in the Si lattice.

Similar experiments have been carried out by Thomas *et al.* [136] to study the diffusion of dopants in $CoSi_2$. All the profiles of the annealed samples show a rapid increase in dopant concentration at the silicide–silicon interface. This occurs at low temperature (500 °C) without any significant modification of the main distribution of the implanted elements. This is due to grain boundary diffusion and will be dependent on the grain size of the silicide thin film.

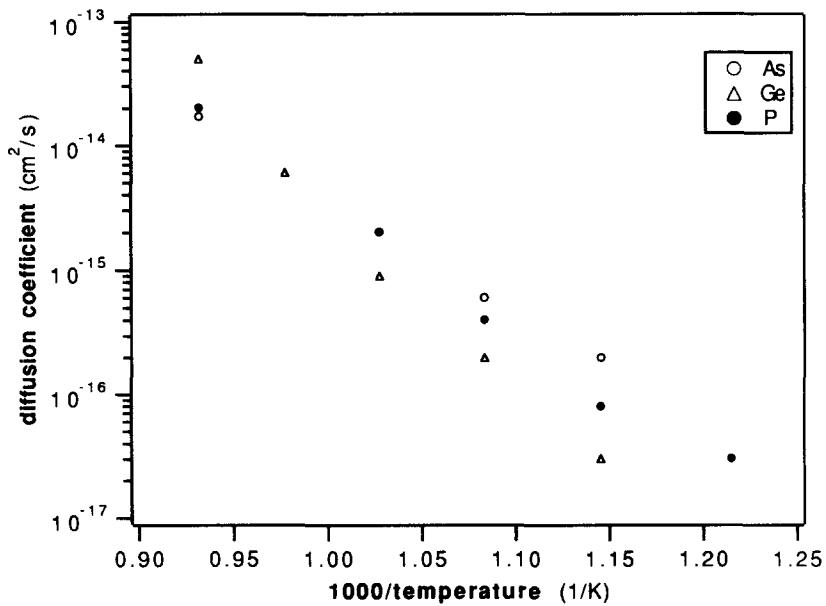


Fig. 33. Coefficients for lattice diffusion of Ge, As and P in $TiSi_2$.

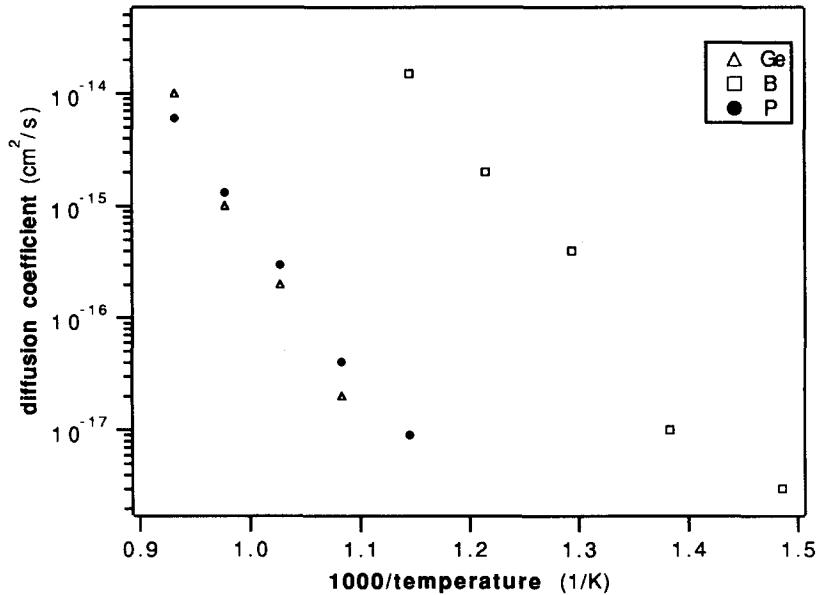


Fig. 34. Coefficients for lattice diffusion of Ge, B and P in $CoSi_2$.

Figure 34 shows the lattice diffusion coefficients of B, P and Ge in $CoSi_2$. Ge was included since it is considered to be representative for Si diffusion. Boron is the fastest diffuser in $CoSi_2$. It is characterized by an activation energy for lattice diffusion of 2.0 eV. In view of its small size, one may anticipate that diffusion occurs via interstitial sites not available to bigger atoms. The very fast lattice diffusion of B in $CoSi_2$ films has been confirmed in bulk $CoSi_2$ by Gas *et al.* [137]. Ga, P and Ge display much lower diffusivities. As and Sb exhibit no detectable lattice diffusion, even after annealing at 800 °C for 0.5 h. In summary, the values obtained for the lattice diffusion of the various dopants in $TiSi_2$

and $CoSi_2$ are of the same order of magnitude as silicon self-diffusion in the silicide, with the exception of B.

The grain boundary diffusion of dopants in the polycrystalline silicide can be much faster than the lattice diffusion described above. Although the diffusion is dependent on small variations in the process, such as grain size, formation temperature and annealing temperature etc., it is interesting to compare $TiSi_2$ and $CoSi_2$ in this aspect for a typical film morphology. Chu *et al.* [138] have measured the lateral diffusion of dopants in silicides using a sensitive Schottky barrier test structure that relies on changes in the $I-V$ characteristics of the silicide/polysilicon interface. In this way they could monitor the dopant mobility over several tens of μm .

Figures 35 and 36 show plots of the diffusion coefficients of B, As and P in $TiSi_2$ and $CoSi_2$. In comparison with the lattice diffusion coefficients of Figures 33 and 34, the lateral diffusion is very fast (except for B in $TiSi_2$), since it is mainly governed by grain boundary diffusion. The average grain sizes of $TiSi_2$ and $CoSi_2$ in this experiment were about 400 nm and 200 nm respectively, which are similar to the layer thickness. A study on how this diffusion depends on technological variations remains to be done.

2.3.5. Dopant outdiffusion from the silicide

The outdiffusion technology aims at the formation of a solid solution of dopants in Si upon thermal treatment of an implanted silicide on "undoped" (or very lightly doped) Si. If the solid solution of dopants in Si is in thermodynamic equilibrium with the silicide, a highly doped region is likely to form when the system is allowed to overcome possible kinetic constraints.

Experiments with $TiSi_2$ indicate that the formation of dopant–metal compounds restricts the supply of dopants at the $TiSi_2$ /Si interface [109,139]. Figure 37 shows diffusion profiles in the underlying Si after heat treatment of a $TiSi_2$ layer, which was implanted with a high dose of B or As. Inspection of the silicide/Si interface by SEM after etching of the silicide has shown precipitate formation at the grain boundaries of $TiSi_2$ (Fig. 38). Indeed, the

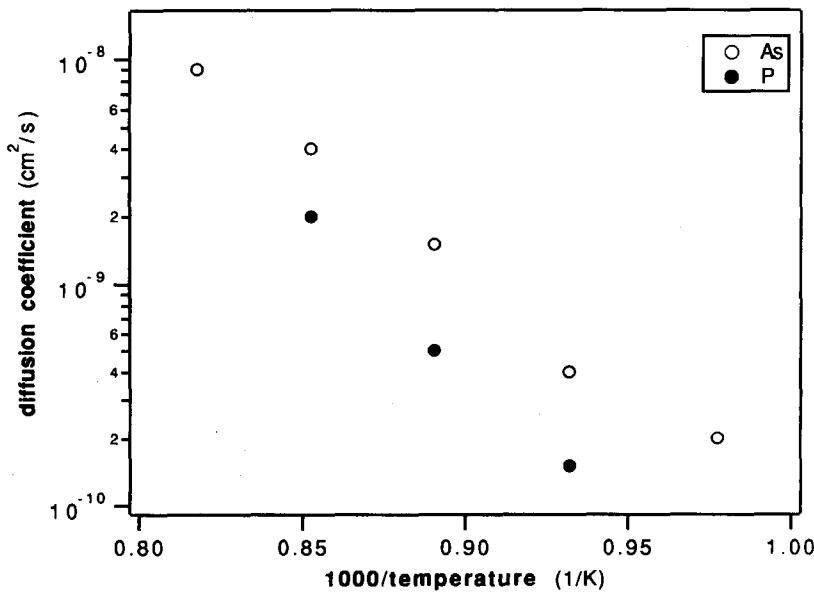


Fig. 35. Diffusion coefficients derived from experiments on lateral diffusion in $TiSi_2$.

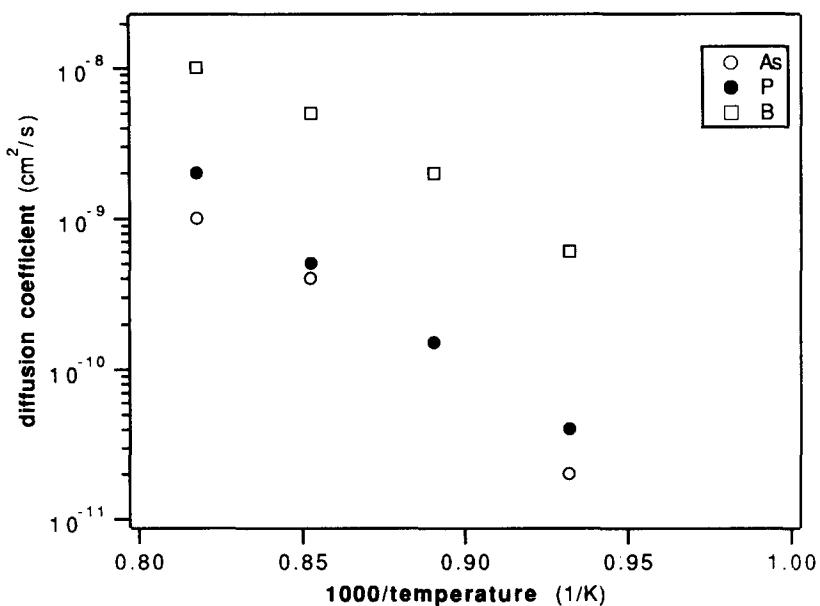


Fig. 36. Diffusion coefficients derived from experiments on lateral diffusion in $CoSi_2$.

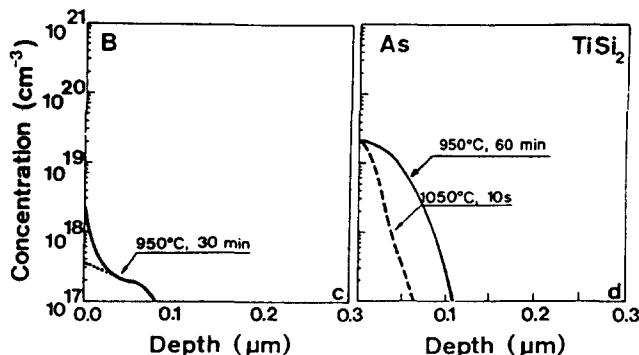


Fig. 37. SIMS measurements of dopant profiles in the Si substrate resulting from diffusion of B and As from $TiSi_2$. The implantation dose was 1×10^{16} at. cm^{-2} . The silicide layer was etched off before measurement.

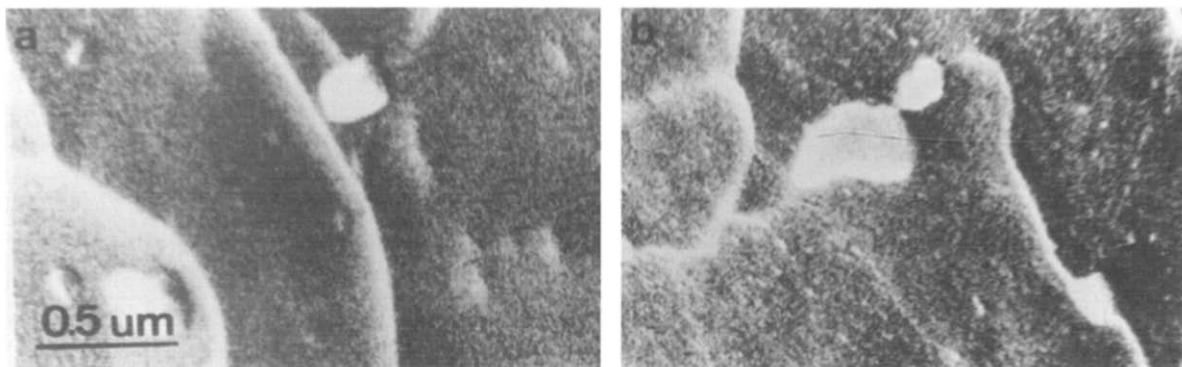


Fig. 38. SEM micrographs of the $TiSi_2$ /Si interface for the case of (a) B-implanted and (b) As-implanted silicide after diffusion at $1100^\circ C$ for 10 s. The samples have been etched to remove the silicide, revealing bright particles along the former silicide grain boundaries.

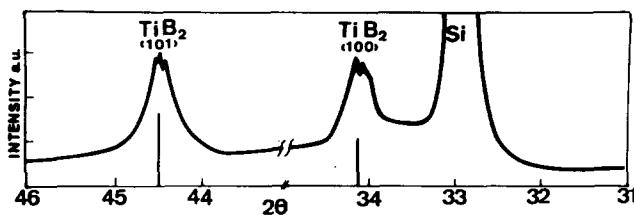


Fig. 39. X-ray diffraction pattern obtained at grazing incidence in comparison with the powder diffraction of TiB_2 . The sample was prepared by implantation of B into $TiSi_2$, annealing at $1100\text{ }^{\circ}\text{C}$ for 2 min and a subsequent selective etch of $TiSi_2$. The remaining particles, analogous to those of Fig. 38(a), consist of TiB_2 .

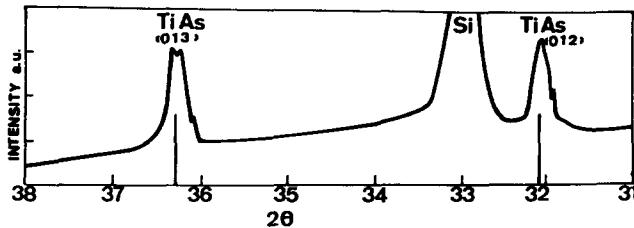


Fig. 40. X-ray diffraction pattern obtained at grazing incidence in comparison with the powder diffraction pattern for $TiAs$. The samples were prepared by implantation of As into $TiSi_2$, diffusion at $1100\text{ }^{\circ}\text{C}$ for 2 min and subsequent selective etch of $TiSi_2$. The remaining particles, analogous to those of Fig. 36(b), consist of $TiAs$.

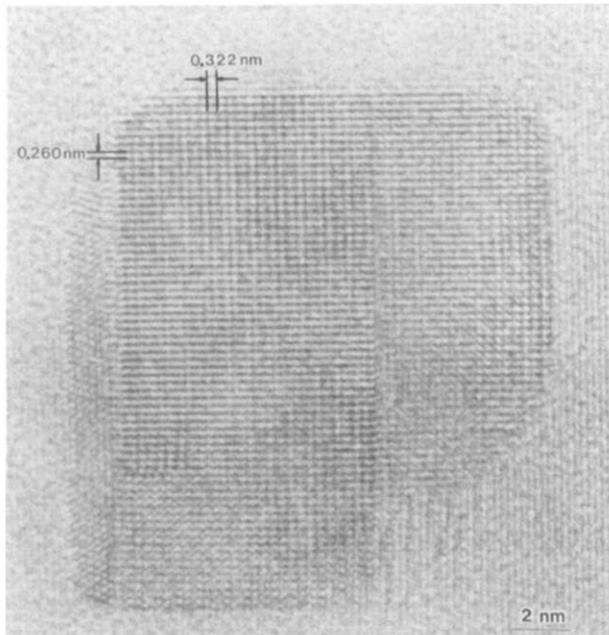


Fig. 41. High-resolution TEM micrograph of a TiB_2 particle in a $TiSi_2$ matrix (after ref. 140).

formation of TiB_2 (Fig. 39) and of $TiAs$ (Fig. 40) was confirmed by XRD [109]. Figure 41 shows a high-resolution TEM micrograph of a TiB_2 precipitate in $TiSi_2$, which was formed upon implantation of B in $TiSi_2$ and similar heat treatment as for outdiffusion [140]. Whereas the formation of TiB_2 was more pronounced than the formation of $TiAs$, the occurrence of both types of precipitates and their influence on the diffusion profile in Si were clearly

revealed. For B it results in a nearly complete inhibition of diffusion in Si. For As, only a limited diffusion was observed.

In the case of $CoSi_2$ as a diffusion source, no similar effects were seen. The diffusion profiles show that the diffusion of B and As are not hindered as in $TiSi_2$ (Fig. 42).

2.3.6. Heat treatment of a silicide film on doped Si

The stability of the doping level at the silicide/Si interface upon additional thermal treatment is extremely important, since it determines the immunity of the device contact resistance with respect to further processing steps at high temperature. This stability has been investigated by growing $CoSi_2$ and $TiSi_2$ layers on As- and B-doped Si regions [109]. After silicidation, the samples were subjected to an additional high-temperature step. The evaporation of the dopants from the sample surface was avoided by a cap layer on top of the silicide. After etching, both the cap layer and the silicide/Si interface was monitored by SEM, revealing precipitation of metal dopant compounds for the case of Ti with B and As as dopant species (Fig. 43). No such compounds were observed for $CoSi_2$ on similar samples.

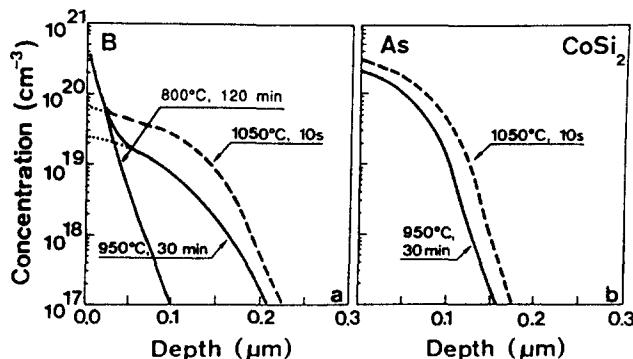


Fig. 42. SIMS measurements of dopant profiles in the Si substrate from the diffusion of (a) B-implanted and (b) As-implanted $CoSi_2$ layer for various times and various temperatures. The implantation dose was 1×10^{16} at. cm^{-2} . The silicide has been etched off before the measurement.

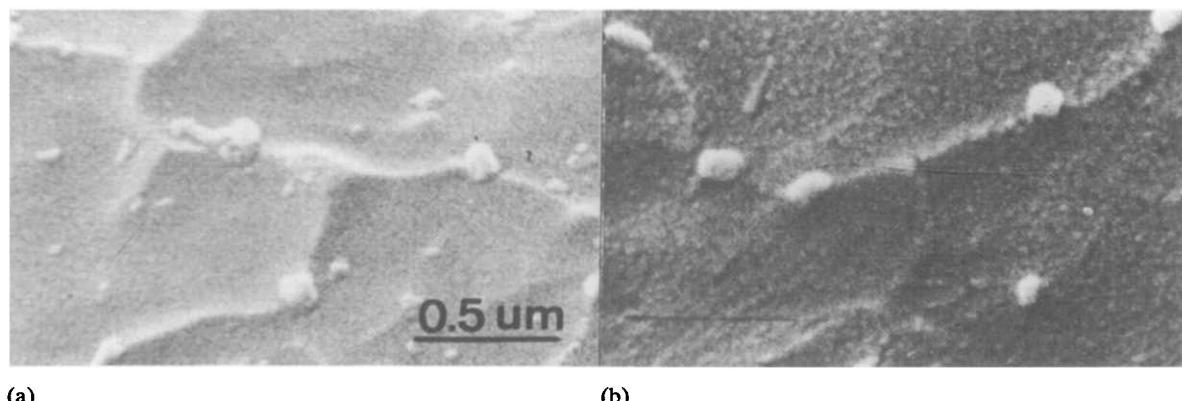


Fig. 43. SEM micrographs of the $TiSi_2$ /Si interface in the case of silicidation of (a) B-implanted Si and (b) As-implanted Si after additional heat treatment at 900°C for 30 min. The samples have been etched to remove the silicide, revealing bright particles, similar to those of Fig. 38.

2.4. Defect generation/recombination

The effect of silicides on the generation/recombination of point defects is important for a better fundamental understanding of silicide formation and dopant diffusion in the Si substrate. As in the case of nitridation and oxidation of Si, experiments have been carried out to determine the identity of the injected point defects, their generation mechanisms, and the kinetics of their motion by monitoring the expansion or shrinkage of extended defects in Si and the diffusion of buried doped layers in Si.

2.4.1. Effect of silicidation on extended defects

It is known from oxidation and nitridation studies that interstitial supersaturation resulting from annealing of extended defects in an O_2 ambient accelerates the growth of interstitial loops, whereas the supersaturation of vacancies from a nitrogen-rich ambient leads to a shrinkage of extended defects [141]. Therefore it was speculated by Wen *et al.* [142] that a silicidation process based on the diffusion of the metal would introduce interstitials (compare to oxidation of Si) and lead to a growth of interstitial-type dislocations, whereas a silicidation process based on the diffusion of silicon (compare with nitridation of Si) leads to a shrinkage of interstitial type dislocation loops.

The expansion and shrinkage of extrinsic dislocation loops was investigated during silicidation reactions. The silicidation of Pd at 250 °C resulted in a limited shrinkage of interstitial-type dislocation loops [143], even though the metal is the main moving species during the reaction of Pd with Si.

Figure 44 shows cross-sectional transmission microscopy (TEM) micrographs of As-implanted Si, annealed at 700 °C for 10 s with and without concurrent silicidation of Ti [133]. At these temperatures, solid phase epitaxial regrowth is complete. In an early stage, the silicidation of titanium results in a reacted layer of a few tens of nm. Where no titanium was deposited, two interstitial-type defect bands remain after regrowth of the amorphous layer. The upper defect layer, located at the peak As concentration, consists of defects

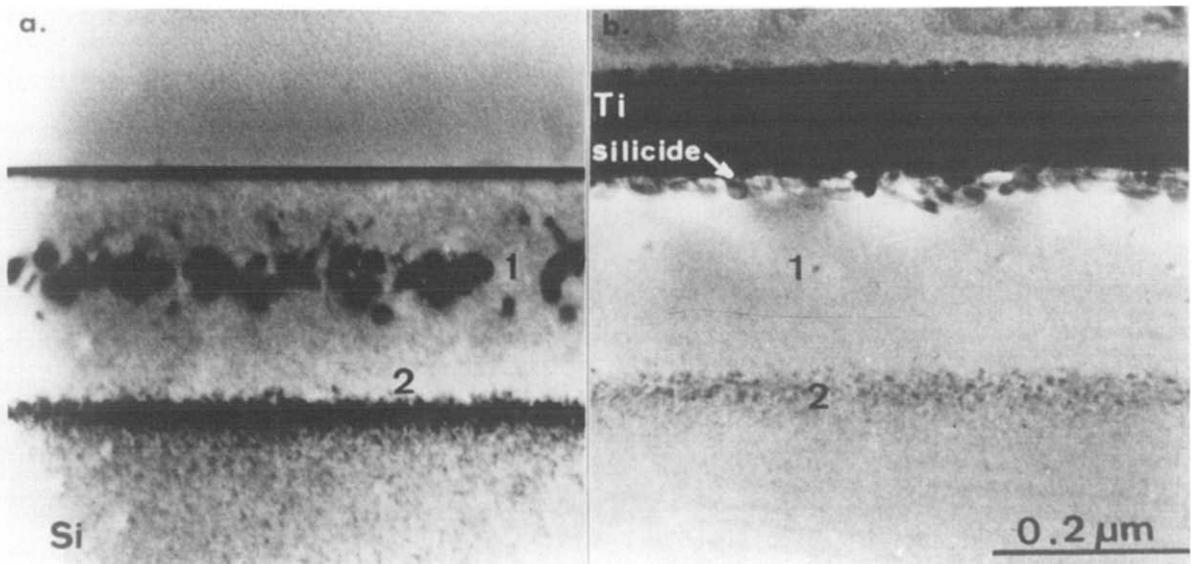


Fig. 44. Cross-sectional TEM micrographs of arsenic ($5 \times 10^{15} \text{ cm}^{-2}$, 200 keV) implanted in silicon, showing two defect bands, labelled 1 and 2: (a) after 700 °C for 10 s; (b) after 700 °C for 10 s with concurrent silicidation of Ti.

with an average length of about 20 nm. The lower defect band is located at the interface between the amorphous and crystalline regions. In the case where the sample was silicided at the same temperature, fewer interstitial type defects are observed. RBS measurements, however, indicate that the concentration of As at the peak of the profile remained the same with and without the partial silicidation. Similar effects are also obtained at higher temperatures. Figure 45 shows a plan view TEM micrograph of As-implanted Si, partly silicided at 1100 °C for 1 s. Where no silicide layer was grown (darker region), dislocation loops appear at the former amorphous crystalline interface. When a Ti silicide layer was grown (lighter region) similar defects were expected about 150 nm below the $TiSi_2/Si$ interface. However, no such defects were observed. Moreover, it is interesting to observe that the region which is free of defects extends laterally into the non-silicided area up to 250 nm from the silicide edge.

Similarly, annihilation of end-of-range extended defects has been reported by Wen *et al.* [142,144]. They have observed total elimination of end-of-range defects in Ge- and B-implanted silicon in the case of silicidation with Ti. Furthermore, the decrease of interstitial defect density was found to correlate with the amount of reacted metal or the amount of silicide formed.

Recently, Honeycutt *et al.* [145] reported on the removal of interstitial-type extended defects during both $TiSi_2$ and $CoSi_2$ formation. An enhanced end-of-range implant damage removal was observed for both silicides, suggesting that the near surface point defect concentrations are modified by the formation and/or by the presence of the silicide (Fig. 46). The mechanisms for this can be attributed to either the silicide/Si interface acting as a sink for interstitials or as a source of vacancies. Since these phenomena occur for both silicides, the assumptions made in the model by Wen, which essentially considered the main moving species during the reaction, are shown to be inaccurate. Honeycutt attributes this ambiguity to a continued Si diffusion after the silicidation reaction, leading to the formation of a Si rich layer on top of the silicide.

2.4.2. Diffusion of dopants in buried layers during silicidation

Another way to look at the dopant behaviour during silicidation is by investigating buried doped layers. In this case, the chemical interactions between dopants and silicide

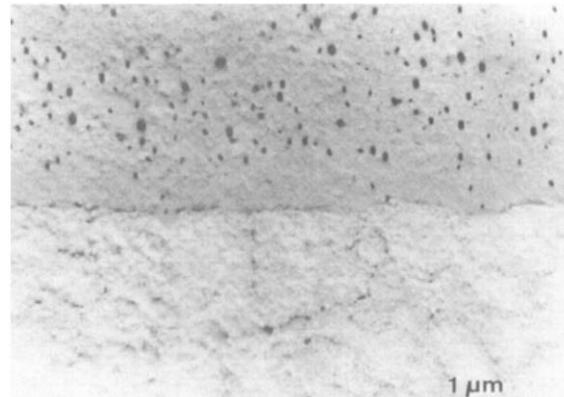


Fig. 45. Plan view TEM micrograph of As-implanted silicon after 1100 °C for 1 s, with (light region) and without (dark region) concurrent $TiSi_2$ formation.

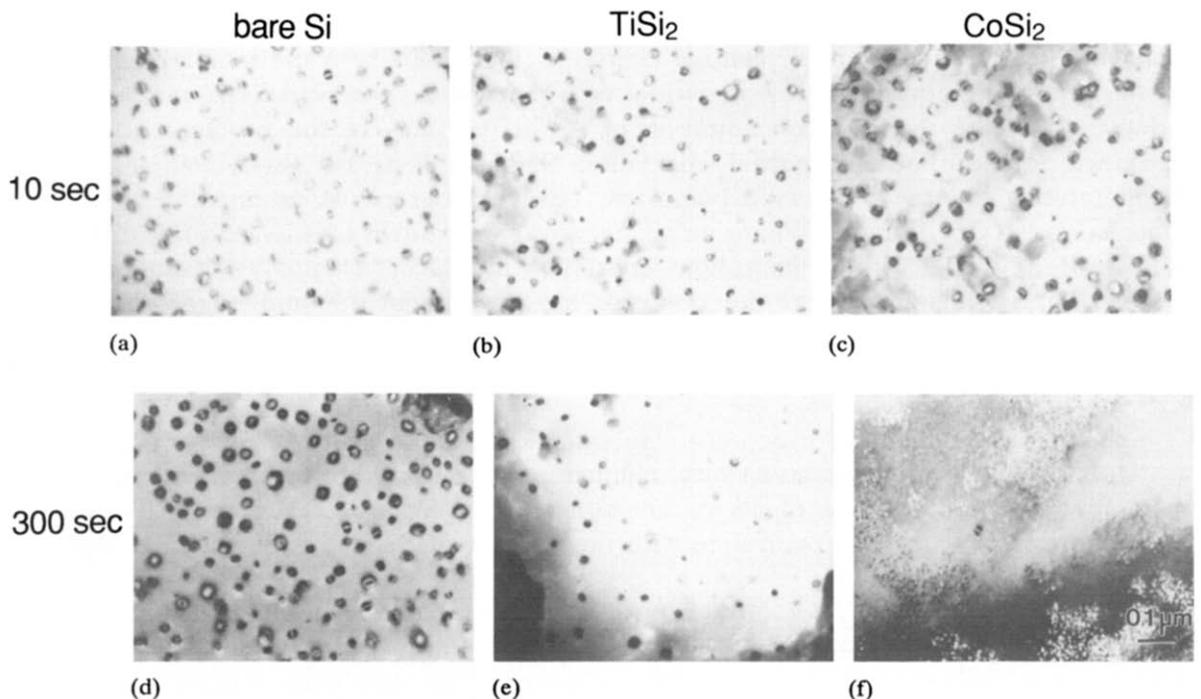


Fig. 46. Plan view TEM micrographs of end-of-range dislocation loops under bare Si ((a), (d)), $TiSi_2$ silicided ((b), (e)), and $CoSi_2$ silicided ((c), (f)) surfaces after 900 °C, 10 s ((a)–(c)) and 300 s ((d)–(f)) (after ref. 145).

are impossible. During Co and Ti silicidation reactions, strongly enhanced diffusion of buried Sb layers has been observed by Honeycutt *et al.* [146,147], with preferential diffusion into the direction of the silicide. In addition, large lateral diffusion effects were reported. Similar results have been claimed during Pd_2Si formation [148,149]. The observed effects are controversial, since the results seem to be difficult to reproduce. In our experiments [150], buried B and Sb layers were studied during Co silicidation, both for extrinsic and intrinsic doping conditions, using a wide range of experimental parameters. The SIMS profiles of the buried dopants in the silicided and non-silicided parts are shown in Fig. 47. No enhanced diffusion is observed.

Recently, Honeycutt [151] has revised his earlier measurements. Taking into account silicide roughness for SIMS measurements and irreducibilities in bevel and staining experiments, no measurable influence on Sb nor on P-doped buried layers was found in spite of a variety of Ti and Co silicidation/annealing conditions.

2.5. Interaction of Ti and Co with SiO_2

In a self-aligned reaction scheme the interaction of the deposited metal with SiO_2 is as important as with Si. The kinetics of the reaction is important in order to estimate the amount of oxide involved, i.e. the oxide loss. On the other hand, the metal atoms can diffuse through the oxide.

2.5.1. Thermodynamics of M-Si-O systems

In order to complete the picture of the possible reactions between Ti or Co and SiO_2 , one should consider the ternary diagrams of the Ti-Si-O and Co-Si-O systems. Figures

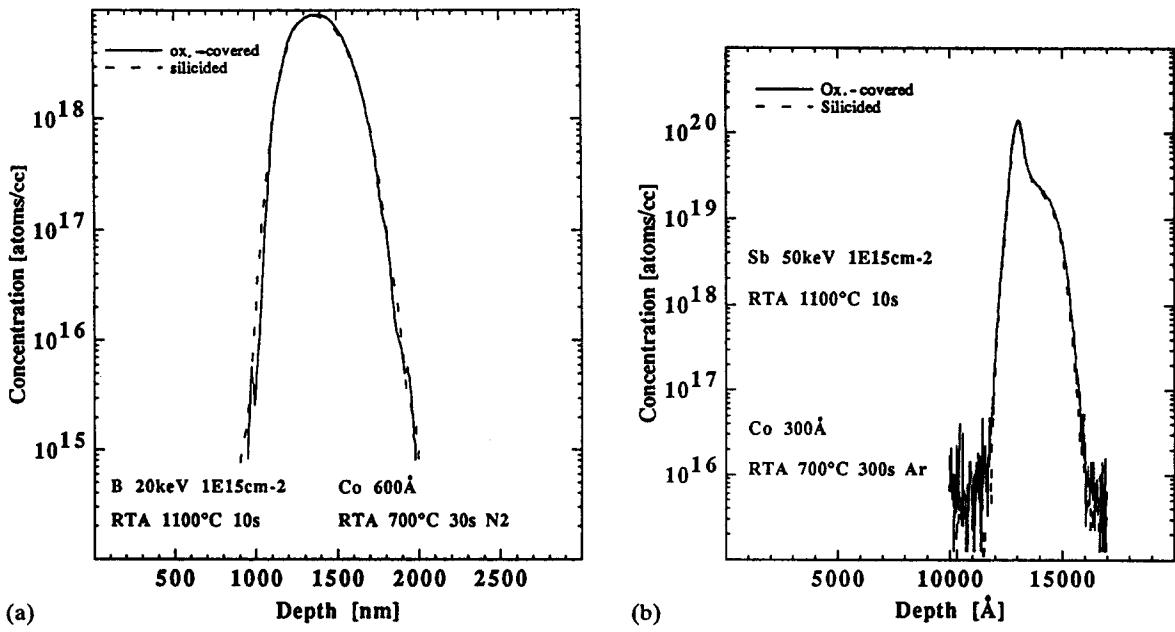


Fig. 47. (a) SIMS profiles of a buried B marker in Si with and without silicidation; (b) SIMS profiles of a buried Sb marker in Si with and without silicidation.

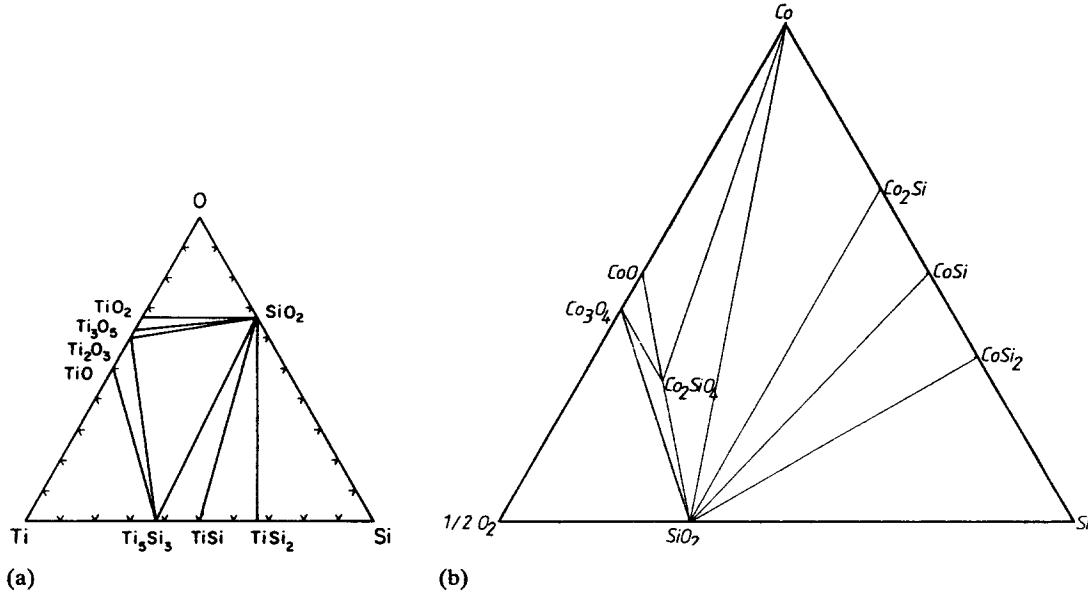


Fig. 48. Calculated phase diagram (a) for Ti-Si-O for the temperature range from 700 °C to 1000 °C (after ref. 152) and (b) for Co-Si-O at 700 °C.

48(a) and (b) show the diagrams of interest for the case at hand. The Ti-Si-O diagram at 700 °C has been taken from Beyers [152]. The Co-Si-O diagram has been calculated at 900 K along similar lines [153]. The Gibbs free energies of the various Co-Si compounds have been taken from Kubachewsky [154] for the Co-O compounds and for SiO_2 from Barin [155]. The ternary compound Co_2SiO_4 , which has been reported by Barin, has been taken into account in the calculations.

It is obvious from these diagrams that Ti and Co are very different in their reaction with SiO_2 . There is no tie line between Ti and SiO_2 , indicating that Ti will reduce SiO_2 and form Ti-O compounds and Ti-Si compounds. On the other hand, Co and SiO_2 are perfectly stable in contact with each other.

2.5.2. Interactions between Ti and Co on SiO_2

Since in a self-aligned process the reaction products of Ti and SiO_2 need to be removed, their identification is important. The reaction of Ti and SiO_2 has been studied in detail, both during treatment in a classical furnace [156] and in a rapid thermal processor [157]. The reaction mechanism consists of a decomposition of SiO_2 by the Ti metal and the formation of Ti-rich silicide, Ti_5Si_3 , at the interface and a Ti-rich oxide on top. A schematic representation of the reaction both in Ar and N_2 ambient is given in Fig. 49.

The amount of SiO_2 loss during the silicidation of Ti on Si areas is a concern. The SiO_2 loss has been summarized in Table 3 for several temperature treatments in Ar using a classical furnace [156]. The data are obtained from $C-V$ measurements, using a Ti film

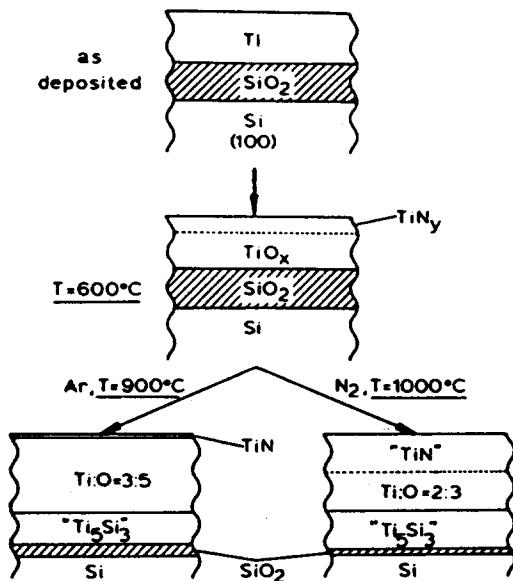


Fig. 49. Schematic representation of the evolution of the reaction of Ti with SiO_2 using RTP in Ar and N_2 .

TABLE 3

Loss of oxide during the reaction between 100 nm Ti and SiO_2 in an argon ambient (from ref. 156)

Heat treatment	Loss of oxide (Å)	
Temperature (°C)	Time (min)	
500	30	55
550	30	90
550	60	105
550	90	110
550	120	115
600	30	150

thickness of 100 nm. In the case of rapid thermal processing, the SiO_2 loss can be seriously reduced for similar reaction temperatures. Fig. 50 shows the SiO_2 loss as measured by ERD for various treatments in Ar and in N_2 ambient. In this experiment, the initial Ti thickness was 150 nm [157].

The reduction of a thin SiO_2 layer during the silicidation of Ti has recently received some attention, since it leads to $TiSi_2$ layers with relatively large grains [158]. The effect of a thin intermediate SiO_2 layer on the $TiSi_2$ growth was reported in detail by Donelly *et al.* [159].

The interaction of Co with SiO_2 has been investigated by XRD and SEM measurements [67] after various heat treatments. XRD spectra are depicted in Fig. 51. As deposited Co layers on SiO_2 are finely grained with the h.c.p. crystal structure (α -Co). Above 400 °C the high-temperature f.c.c. Co phase (β -Co) is formed. This transformation is well documented in the literature [160]. Between 400 °C and 600 °C, CoO is detected by XRD. Similar conclusions were drawn from Auger electron spectroscopy (AES) profiles. After annealing at 500 °C a large amount of O is present in the sample. This amount decreases with increasing temperature, indicating a loss of O. At 700 °C only a small amount of O is present near the surface. The O in the Co layer is thought to originate from the annealing ambient, because Co layers on Si_3N_4 show the same behaviour. Apparently, at higher temperatures CoO is reduced to Co and the O is released, with the total amount of Co remaining constant. This suggests that the O partial pressure in the RTP chamber is changed during the RTP cycle. Initially a large amount of O_2 or H_2O is present in the chamber, probably resulting from the wafer loading process. The CoO may then decompose or be reduced by residual hydrogen in the ambient (see Section 2.2.5).

At high temperatures only Co is detected. Figure 52 shows a series of SEM micrographs of the Co layer to inspect the morphology changes of the Co. The initial thickness of the Co layer was 40 nm and the wafers were treated at 700, 900 and 1100 °C for 30 s. These pictures reveal clearly that the layers agglomerate with increasing temperature. This balling-up effect can be fully described by the tendency of the system to lower its energy. This is accomplished by reducing the surface of the Co/ SiO_2 interface area, which is typical for metals with a low affinity for SiO_2 [161].

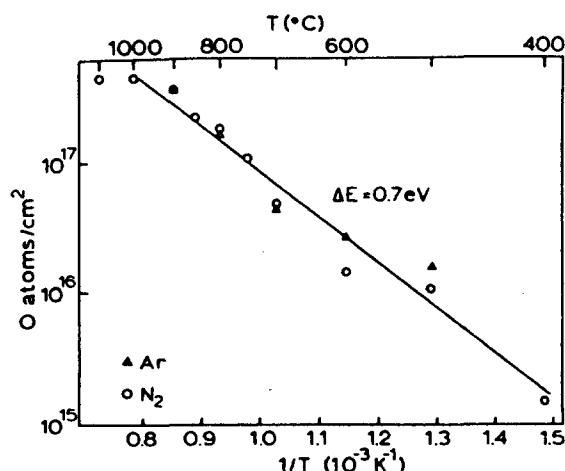


Fig. 50. The amount of O originating from the reduction of SiO_2 , plotted logarithmically vs. the reciprocal temperature for RTP in Ar and N_2 . The initial Ti thickness was 150 nm.

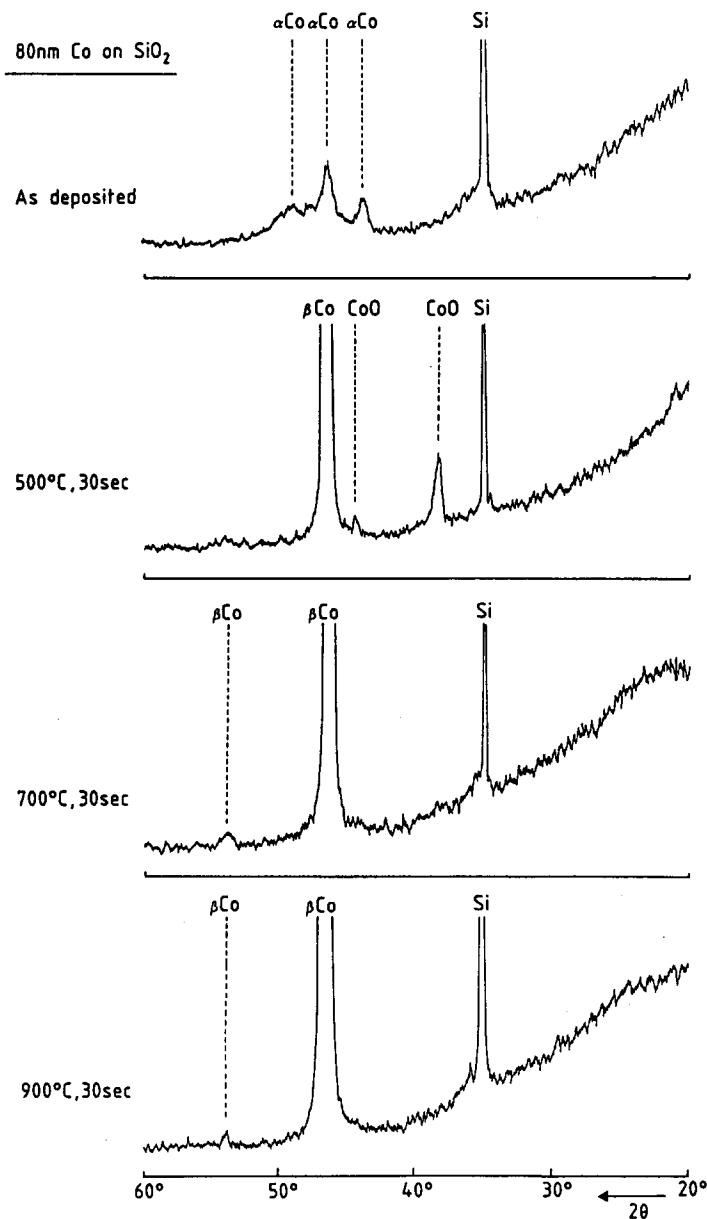
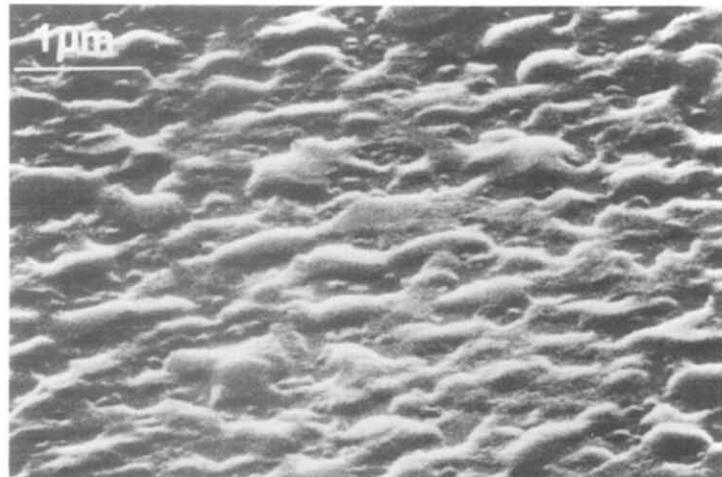
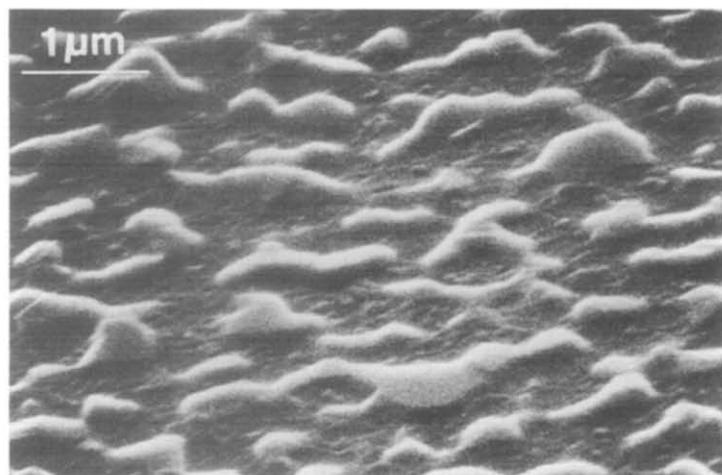


Fig. 51. XRD spectra of 80 nm Co on SiO_2 as deposited and after various heat treatments in N_2 for 30 s.

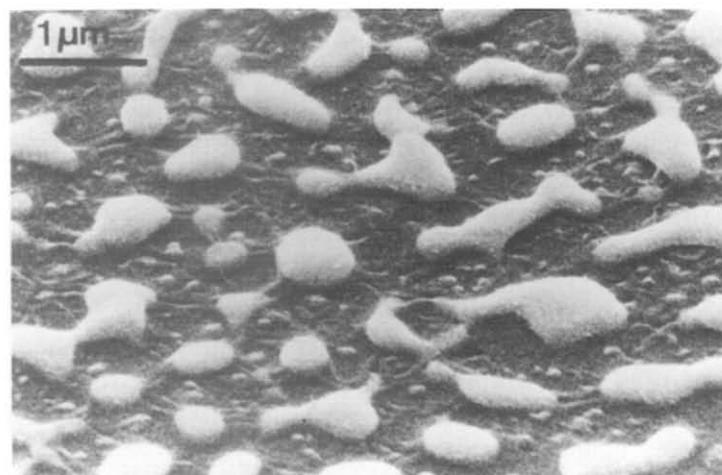
Figure 53 shows a cross-sectional TEM micrograph of agglomerated Co on SiO_2 . It is surprising that the globules have penetrated in the SiO_2 . This may be explained by a reduction of SiO_2 to volatile SiO by residual H_2 present in the RTP ambient. It is known that a Co surface has a catalytic action for the dissociation of molecular H_2 into H. The penetration of the Co globules in the SiO_2 layer explains the often observed grainy footprint in the SiO_2 after chemical etching of unreacted Co in the self-aligned silicidation process. Ho *et al.* [162] have performed similar experiments. They observed the formation of Co_3O_4 together with volatile SiO during the reaction of Co with SiO_2 . They argue that trace amounts of O_2 in the reaction ambient catalyse the reaction between Co and SiO .



(a)



(b)



(c)

Fig. 52. SEM micrographs of the surface of Co layers on SiO_2 after heat treatment at 700 °C, 900 °C and 1100 °C. The initial Co thickness was 40 nm.

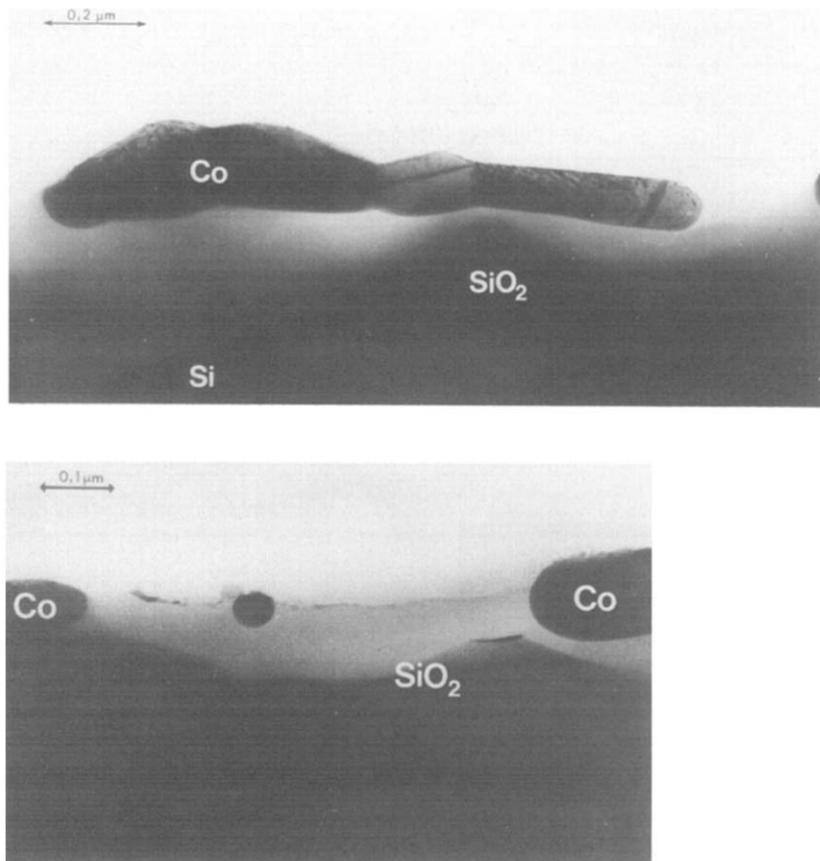


Fig. 53. Cross-sectional TEM micrographs of Co globules on SiO_2 originating from the agglomeration of a 40 nm thick Co layer deposited on SiO_2 and heat treated at 900 °C for 30 s in an N_2 ambient.

Regarding the interaction of Co with O, it should be noted that, despite the fact that the heat treatment is performed in an N_2 ambient, no N is taken up in the layer as measured by AES.

2.5.3. Diffusion of Ti and Co in SiO_2

The diffusion of Co in thermally grown SiO_2 has been reported by Fedorovich [163]. Radioactive profiling of ⁶⁰Co from a deposited $CoCl_2$ film on top of the oxide was used. The bulk diffusion coefficient for Co is represented by the equation

$$D = 10^7 \exp[-(1.70 \pm 0.05)/kT] \quad (22)$$

A study of the diffusion of Ti in SiO_2 has been carried out by McBryer, based on RBS and CV measurements [164]. Since Ti was found to react with the SiO_2 to form Ti oxides, no diffusion of Ti in SiO_2 was observed. Ti is therefore not expected to be an interstitial diffuser in SiO_2 . The same authors [165] report on the diffusion of several metals in SiO_2 at low temperatures in an electric field.

2.5.4. Oxidation of silicides

Thin silicide layers on top of a Si substrate can be thermally oxidized to form SiO_2 . The ternary diagrams, discussed in Section 2.5.2, predict the stability of SiO_2 in contact

with the silicide. Based on thermodynamics, it is not surprising that this oxide growth takes place. Since the presence of oxides, be it native or process-induced, is technologically important, the thermodynamics and kinetics will be considered briefly.

From the Ti–Si–O and Co–Si–O diagrams we can see that the formation of M oxides may be avoided if the system stays in the MSi_2 – SiO_2 –Si triangle. The rapid diffusion of Si through the disilicide towards the reacting interface implies that no metal oxides have been observed [152,166–169].

These arguments clarify the fact that the oxide growth on top of the silicide only takes place when Si atoms are supplied. Without Si supply, e.g. when the temperature for Si diffusion is too low, or when the silicide is not covering Si but instead SiO_2 or sapphire (as in some silicon on insulator (SOI) technologies), either a reduction of the silicide film or the formation of metal oxides occurs.

The formation of SiO_2 on top of silicides is also intriguing from a kinetic point of view [167]. The atomic motion has been studied in detail by marker experiments for the various silicides. The main interest is to learn what happens within the silicide layer, since the latter is not unaffected by the oxidation.

For $TiSi_2$ the oxidation model is depicted in Fig. 54(a). The growth of SiO_2 is dependent upon the diffusion of atoms from the substrate through the silicide layer. The atomic picture is completely different for the oxidation of $CoSi_2$. Detailed observations of atomic motion have led to the conclusion that for two molecules of silicide, three atoms of Si form SiO_2 and two atoms of Co diffuse back together with one Si atom. A schematic representation is given in Fig. 54(b).

The kinetics of the oxide growth on silicides has been analysed based on the same linear parabolic model (Deal and Grove) as used for the oxidation of Si. Figure 55 presents the oxide thickness for various silicides and Si versus oxidation time in a dry O_2 ambient at 800 °C. It can be concluded that SiO_2 forms on all silicides at a rate that is at least ten times larger than on Si. For comparison, an average growth of 70 nm of SiO_2 was reported [169] during oxidation of $TiSi_2$ in dry O_2 at 800 °C for 20 h. The oxidation of $TiSi_2$ was faster for the C49 phase than for the C54 phase.

Although the oxidation of $TiSi_2$ and $CoSi_2$ proceeds in a similar manner, as discussed above, there is an important difference between these silicides if the oxidation occurs at low temperature, e.g. during the silicidation reaction itself. The diffusion of Si for the formation of $TiSi_2$ starts at relatively high temperatures, i.e. above 600 °C. For lower

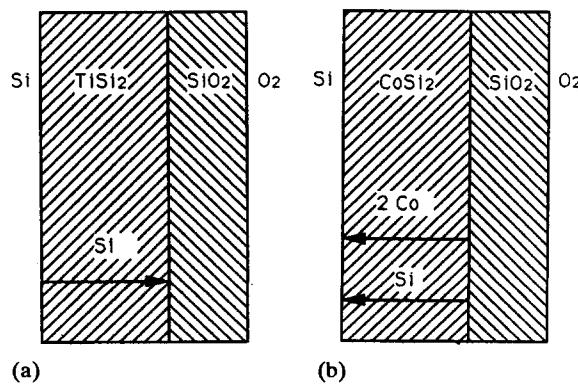


Fig. 54. Schematic representation of various atom motions during thermal oxidation of silicides on Si: (a) $TiSi_2$; (b) $CoSi_2$.

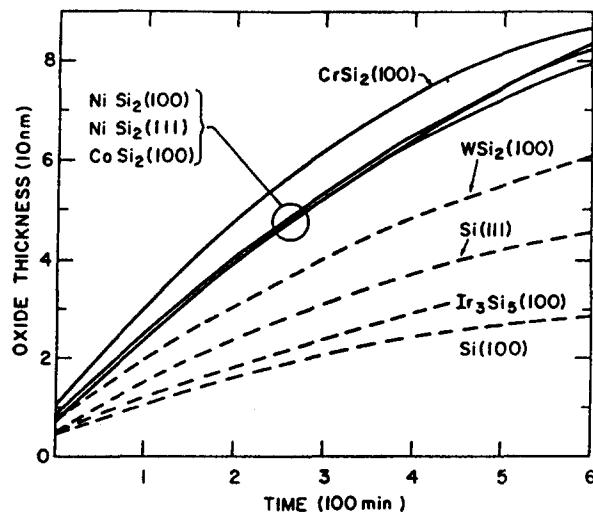


Fig. 55. The kinetics of oxide growth for several silicides at 800 °C in nominally dry O_2 (after ref. 167).

temperatures, for instance during heating up, the Ti is more likely to form Ti oxides instead of SiO_2 . For Co silicidation, however, the Si and Co diffusion starts at much lower temperatures. In experiments where O was added deliberately during Co deposition or annealing, the growth of SiO_2 was already observed during the reaction at the metal/silicide interface [170]. Figure 56 shows cross-sectional TEM micrographs of the SiO_2 growth between the Co and the Co_2Si , $CoSi$ and $CoSi_2$ phases, respectively. For the sample processed at the lowest temperature, the SiO_2 layer is not much thicker than the native oxide. However, an SiO_2 layer as thick as 25 nm can be grown by adding O_2 to the Co layer, without disturbing the silicidation reaction. For the reaction at 700 °C there is inhomogeneous SiO_2 growth and concomitantly inhomogeneous $CoSi_2$ growth.

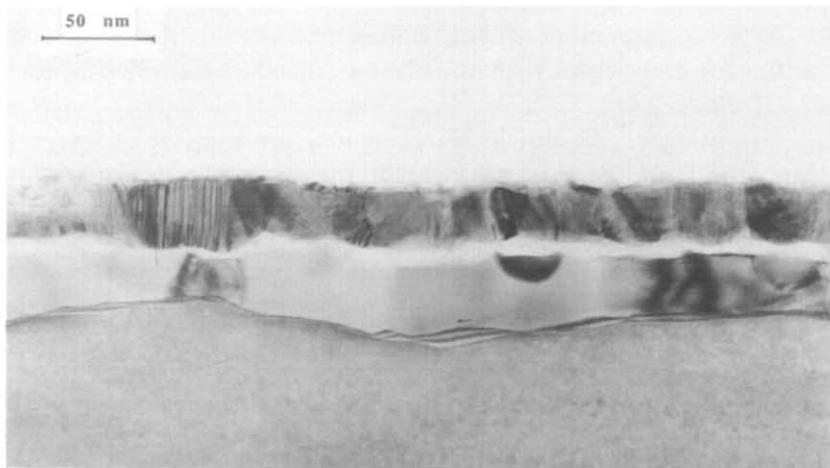
2.6. Interaction with contacting metals

Since both $TiSi_2$ and $CoSi_2$ are metallic materials, the electrical contact with another metal does not pose any problem. Understanding the contact metallurgy requires, however, an investigation of the interactions between the various interconnecting metals or contact fills and the silicide. The contact metallurgy based on Al will be discussed first, followed by the interactions with W, which is used either as an interconnecting metal or as a contact fill.

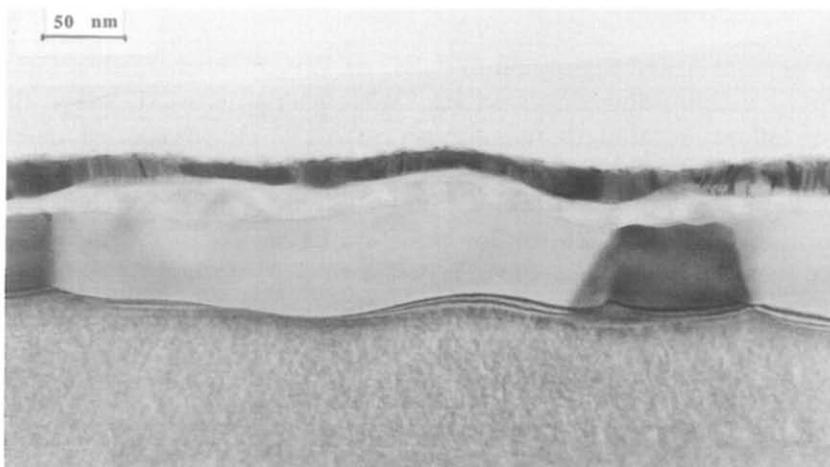
2.6.1. Interaction with Al

The interaction of Al with silicide/Si contacts has been studied in detail by van Gurp *et al.* [171,172] for the case of $CoSi_2$ and by Ting and Wittmer [173] for $TiSi_2$.

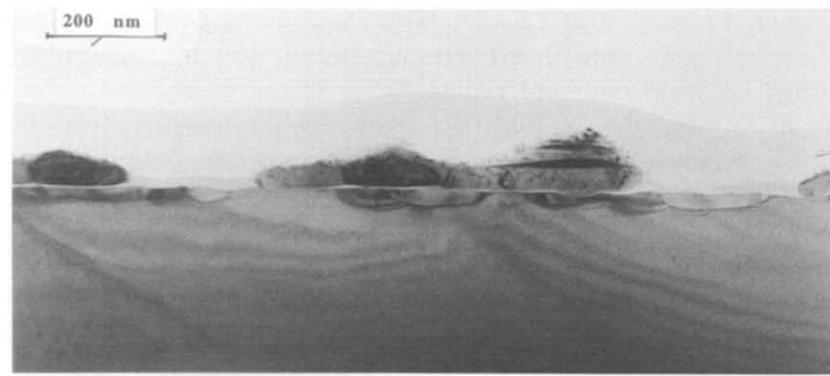
The interaction between $CoSi_2$ contact layers and Al, as investigated by AES, RBS and XRD, starts at 400 °C, yielding large Si precipitates at the sample surface and the formation of the Co_2Al_9 compound. The experimental results suggest that the reaction between the Al and the silicide starts with Si dissolution in Al and accordingly a disintegration of the silicide at the Al/silicide interface. Since the diffusion of Si in the metal takes place at grain boundaries, large amounts can be transported, resulting in the growth of Si precipitates of several microns. The growth of Si precipitates can be retarded by using an Al-Si alloy instead of a pure Al layer. The diffusion of Al through $CoSi_2$ is estimated,



(a)



(b)



(c)

Fig. 56. Cross-sectional TEM micrographs of the silicidation of 40 nm of intentionally O-contaminated Co on Si after (a) 400 °C, (b) 500 °C and (c) 700 °C for 30 s.

based on Schottky barrier height measurements, to be $3 \times 10^{14} \text{ cm}^2 \text{ s}^{-1}$ [172]. The rate of transport of Co through the Al is in agreement with a diffusion constant of $4 \times 10^{13} \text{ cm}^2 \text{ s}^{-1}$ [174]. The kinetics of the Co_2Al_9 compound formation shows a linear time dependence with an activation energy of 2.3 eV.

Similar to $CoSi_2$, a $TiSi_2$ film between Al and Si starts to interact at 400 °C. Large Si precipitates grow first, and accordingly large Al pits form in the underlying Si substrate. At higher temperatures, starting at 550 °C, the ternary compound $Ti_7Al_5Si_{12}$ forms [173].

The high reactivity of the two silicides with Al requires the use of a barrier layer to minimize compound formation and diffusion of Al and Si through the silicide. Commonly used diffusion barriers are TiN and TiW, similar to the contact metallurgy using Al without a silicide layer. By using these barrier layers, contacts on Si can be formed which are stable during heat treatments up to 550 °C [175].

2.6.2. Interaction with W

In the present contact formation schemes, CVD-W has been used quite often to fill the contact hole. The W deposition can be done either selectively or as a blanket layer with a subsequent etch back. There is an extensive literature on CVD-W and its implementation [176].

The blanket deposition of W is based mainly on WF_6/H_2 or WF_6/SiH_4 chemistry. Since W has poor adhesion on SiO_2 , a thin adhesion layer, e.g. TiN or TiW, is used before the deposition. Therefore the problems related to the deposition of W on silicided contacts are to a large extent the same as for non-silicided contacts.

In the case of a direct deposition of CVD-W on $TiSi_2$, the effect of H_2 reduction on $TiSi_2$ results in the consumption of Si from the upper portion of the silicide. Non-volatile insulating TiF_3 is formed at the silicide surface when exposed to WF_6 and H_2 resulting in a high contact resistance. The formation of a thin TiN layer during the second silicidation step in an N_2 ambient has been reported to limit the disintegration of the silicide during the W deposition. Ellwanger *et al.* [177] report on the successful deposition of selective W directly on $TiSi_2$, without removing the *in situ* grown TiN layer. The use of SiH_4 instead of H_2 is very effective in the suppression of fluorine incorporation in the underlying Ti silicide layer. It is believed that SiH_4 can remove fluorine from the surface of the growing layer.

Direct deposition on $CoSi_2$ using WF_6/H_2 chemistry results in Si consumption from the surface of the silicide layer. Formation of Co-rich intrusions in the $CoSi_2$ layer have been reported [178]. It is interesting to note that the reduction of WF_6 by $CoSi_2$ results from WF_6-Si interactions only. Co itself does not reduce WF_6 , as can be concluded from the fact that no deposition of W occurs on a pure Co layer. Higher temperatures yield less Si consumption during the deposition process and result therefore in better junction properties [179]. Void formation at the perimeter of a contact region can take place. Deposition of tungsten on $CoSi_2$ structures is therefore restricted to situations in which the contact perimeter is not exposed to WF_6 .

2.7. Thermal behaviour of thin film silicides

2.7.1. Stress build-up and thermal expansion

The build-up of stress during the silicidation reaction has received much attention [180–182]. In general, intrinsic compressive stress is generated during the silicide formation, followed by relaxation of this compressive stress at high temperatures. During cooling down

of the silicides, tensile stress builds up due to the large difference in the expansion coefficients between silicide and Si. As such, the thermal stress is much more important than the intrinsic stress to determine the final stress level after the silicidation reaction is completed.

In situ stress measurements have been carried out for Co and Ti silicidation. The stress in the silicide layers was determined from wafer curvature measurements performed both at room temperature and *in situ* at high temperature [181]. The room temperature stress of silicides is of purely thermal origin and builds up during cooling from the stress relaxation temperature (this is the temperature above which no stress is observed in the silicide). As shown in Fig. 57, relaxation is observed down to 630 °C for $CoSi_2$ and to 750 °C for $TiSi_2$. The stress level at room temperature is 1.3 GPa for $CoSi_2$ and 2.3 GPa for $TiSi_2$. The larger value for $TiSi_2$ is mainly due to its higher thermal expansion coefficient and to the higher stress relaxation temperature.

Von Allmen *et al.* [183] studied the effect of an applied uniaxial stress on the growth rate of some silicides. It appears, however, that the effect is very small.

The combination of materials with different structure and thermal expansion coefficients may lead to large local stress fields in the Si lattice. For silicides on Si, the thermal expansion of the silicide is always larger than the expansion of the silicon substrate. Engström *et al.* have carried out a detailed study to determine the thermal expansion coefficients of various silicides [184,185]. They evaluated the linear thermal expansion coefficient α with temperature from the variation of the lattice parameter as observed by XRD.

Figure 58 shows the linear expansion coefficient of $TiSi_2$ and $CoSi_2$ in the different crystallographic directions versus temperature. The Si data have been added for comparison. For both silicides the expansion coefficient increases with temperature.

2.7.2. Thermal stability

The thermal stability of the thin silicide film on Si is one of the major concerns at present, since it defines the thermal budget allowed for further processing. Both $CoSi_2$ and $TiSi_2$ are commonly polycrystalline and suffer from thermal grooving and islanding during high-temperature treatments.

Thermal grooving has been characterized in great detail for metals by Mullins *et al.* [186,187]. It is important to note that thermal grooving is influenced by both thermodynamic and kinetic factors. From a thermodynamic point of view, the driving force for the morphological transformation is the reduction of the interface/surface energies. Figure 59 shows a scheme of the morphology changes at various stages. The grooving process takes place owing to

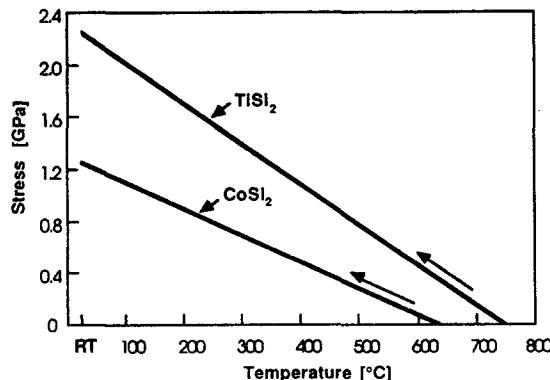


Fig. 57. Stress in the silicide during cooling after $CoSi_2$ and $TiSi_2$ formation (after ref. 182).

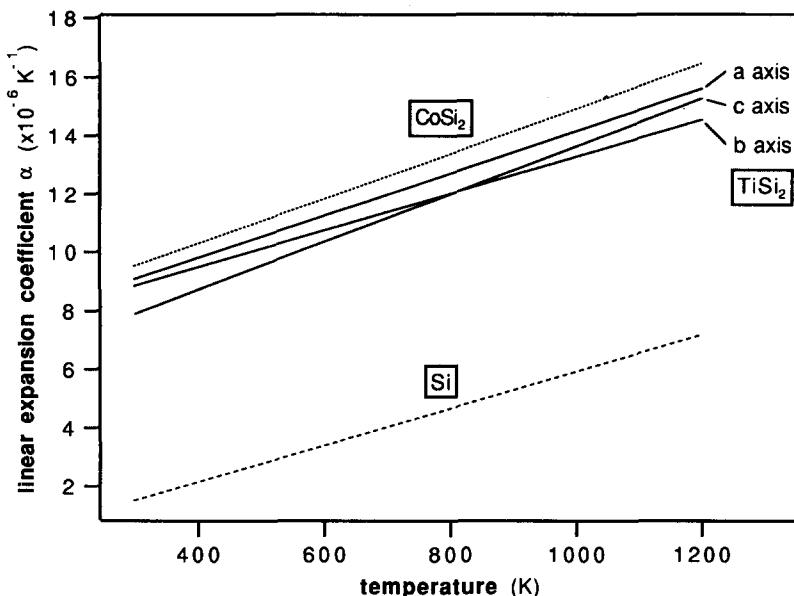


Fig. 58. Thermal expansion coefficient of $TiSi_2$ and $CoSi_2$ in different crystallographic directions vs. temperature (after refs. 184, 185).

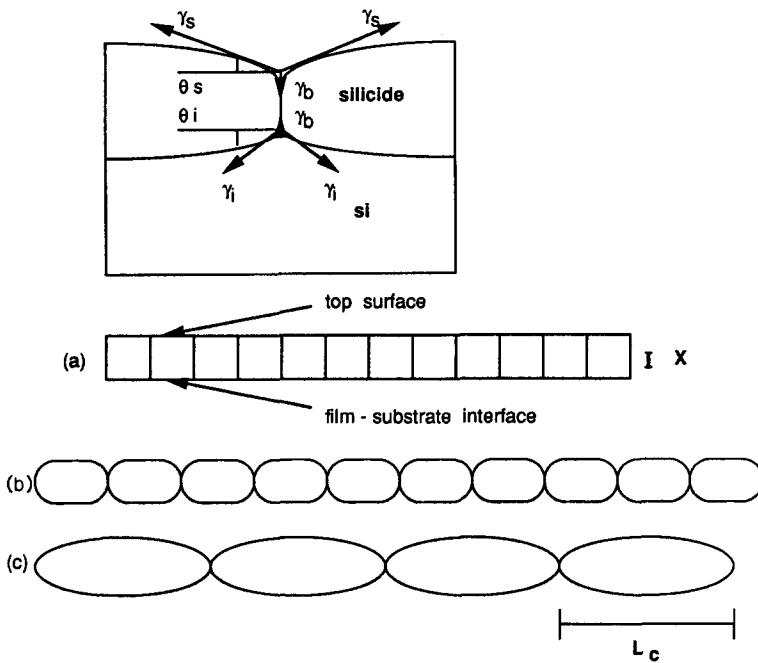


Fig. 59. (a) Energy balances at the grain boundary grooves and (b) schematic cross-sectional view of the evolution thermal grooving of a thin polycrystalline layer.

local energy equilibrium at the intersection of a grain boundary and the film surface or interface and matter diffusion away from the highly curved region which is formed. Groove formation occurs both at the silicide surface and at the silicide/Si interface. Local equilibrium is defined by an energy balance, represented by the well-known relationship between the

surface and interface boundary energies, γ_s and γ_i , the grain boundary energy, γ_b , and the equilibrium groove angles θ_s and θ_i .

$$\gamma_b = 2\gamma_s \sin \theta_s \quad (23)$$

$$\gamma_b = 2\gamma_i \sin \theta_i \quad (24)$$

Since grooving is driven by matter diffusion away from the regions of high curvature, it should continue until a constant curvature is reached.

Based on these assumptions, several models have been proposed [188,189] to determine the critical grain size L_c , below which no islanding occurs. According to these models, L_c increases for thicker films, lower grain boundary energies or higher interfacial and surface energies. The point is to limit grain growth during thermal treatments, such that L_c is not surpassed. Typical L_c values are of the order of 10 times the silicide film thickness, which implies a 500 nm grain size for a 50 nm silicide film.

Diffusion kinetics can also play a significant role. Material transport, for instance, will tend to change the interface and surface contact angles. Such deviation from the equilibrium angle leads to further grooving. Since material transport is a thermally activated process, it can become dominant for the characterization of the grooving and islanding process at the higher temperatures. Mullins *et al.* [186,187] have described the kinetic enhancement of grooving. The depth of the groove was found to be proportional to the diffusion coefficient of the moving atoms.

Widely different data on thermal stability of CoSi₂ and TiSi₂ can be found in the literature [190–194]. Studies of grain size control and related thermal stability have not been performed in a systematic way. In general, impurities at the interface or at the surface improve the thermal stability of TiSi₂. For CoSi₂ smaller grain sizes lead to an increased thermal stability. In general, the use of a capping layer limits thermal degradation. This is due both to the higher silicide/SiO₂ interfacial energy and to the fact that the material transport is hampered by the capping layer. It cannot be emphasized enough that minor changes in the processing conditions during silicidation can have a significant impact on thermal stability [195–197]. The thermal stabilities of both CoSi₂ and TiSi₂ have been reported to be worse on polycrystalline Si than on monocrystalline Si. Systematic studies are under way and will allow the most important parameters for improving the thermal stability to be elucidated. As will be discussed in Section 3.5.1, lateral confinement also has a large impact on thermal stability.

3. Technological aspects and implementation

3.1. Implementation of self-aligned silicides in MOS technologies

3.1.1. Use of silicides in MOS devices

Silicidation of MOS devices is a current subject of investigation [198–205]. Before going into technological details of the integration of silicides in a full process, it is important to discuss briefly some of the requirements for the use of silicides and their effect on the MOS device behaviour. Figures 60(a) and (b) show a cross-section and plan view of a typical MOS transistor with gate length of 0.7 μm. When scaling down the device, critical dimensions become smaller. Figure 60(c) shows the same picture of an MOS device with typical dimensions for a 0.25 μm technology. Table 4 gives typical junction depths for the various generations of memories.

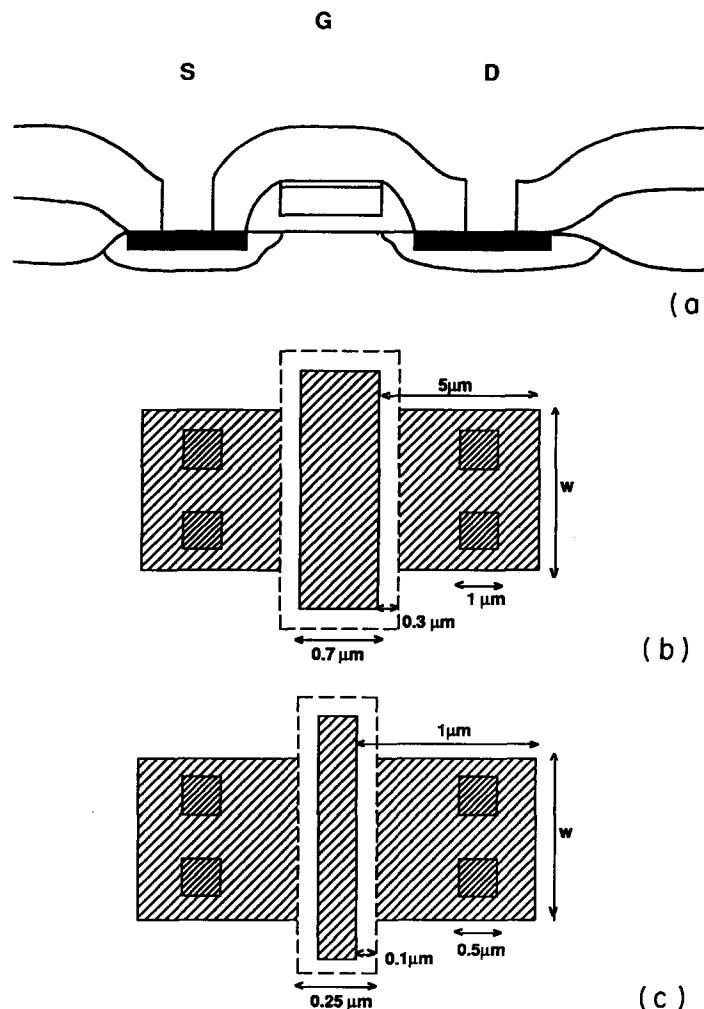


Fig. 60. Schematic in cross-section (a) and plan view of a MOS transistor (b) with typical dimensions for a $0.7 \mu m$ technology and (c) with typical dimensions for a $0.25 \mu m$ technology.

TABLE 4

Typical gate length and junction depth for the various generations of memories

Memory generation	Junction depth	Gate length
4 Mbit	$0.3 \mu m$	$0.8 \mu m$
16 Mbit	$0.2 \mu m$	$0.5 \mu m$
64 Mbit	$0.15 \mu m$	$0.35 \mu m$
256 Mbit	$<0.1 \mu m$	$0.2 \mu m$

The scaling of the junction depth and of the gate length leads to unacceptable levels of the sheet resistance. To overcome this problem, a self-aligned silicidation process is used, in which silicides are formed on the gate and on source/drain areas (see Section 3.1.2). The silicide shunts the sheet resistance of the doped Si and lowers the resistivity of those areas.

The lowering of the sheet resistance of the poly-Si interconnections has an important impact on the RC delay in a device. Scott *et al.* [206] demonstrated the importance of silicides for the device delay time, which can be a factor of 10 lower for p-MOS devices and about a factor of two lower for n-MOS devices. The relative improvement of the device speed using silicides increases with the scaling to smaller dimensions. Hillenius *et al.* reported a multi-gigahertz CMOS technology based on $CoSi_2$ [207].

The silicidation of source and drain regions reduces the total source/drain resistance R_T in a transistor. The total source/drain series resistance consists of two parts: the series resistance R_{DS} and an intrinsic series resistance R_{int} from the channel region. The intrinsic series resistance is dependent on the applied gate voltage.

The source/drain series resistance R_{DS} is determined by:

1. the contact resistance of the silicide to the doped Si;
2. the sheet resistance of the silicided junction;
3. the geometrical layout of the contact.

Both the contact resistance between the silicide and the Si and the sheet resistance of the source/drain area need to be optimized by the junction formation and silicidation process.

The contact using silicided source/drain areas looks very different from the conventional contact technology (Fig. 61). The source/drain series resistance of silicided contacts has been investigated theoretically by Scott *et al.* [208]. A full derivation is given in that reference. Only the main conclusions are discussed here. Considering only the part of the series resistance which is independent of the gate voltage, two limiting cases can be defined.

For $L \ll L_c$, with $L_c = [\rho_c/(\rho_D + \rho_S)]^{1/2}$,

$$R_{SD} = \rho_c/(LW) + (L/W)(\rho_D \rho_S / \rho_D + \rho_S) \quad (25)$$

with ρ_c the specific contact resistance, ρ_s the resistivity of the silicides and ρ_D the resistivity of the doped Si.

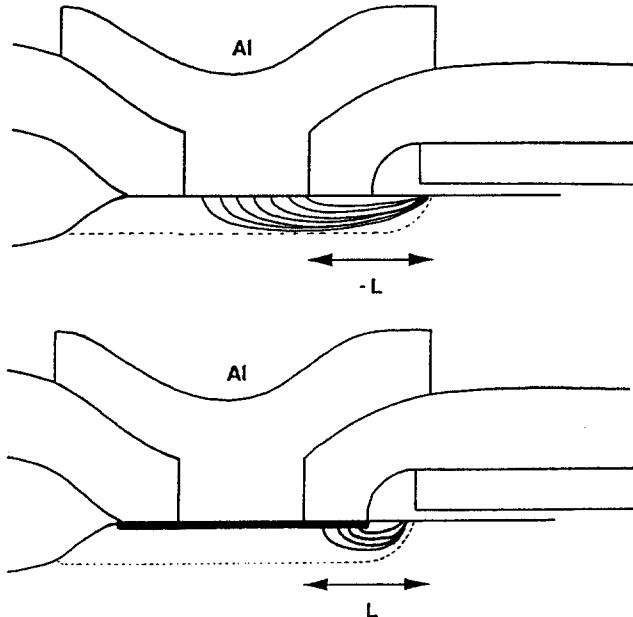


Fig. 61. Cross-sectional schematic of a contact with and without silicidation.

In this case (case 1), the contact resistance is area-dependent and the resistance increases as L decreases.

For $L \gg L_c$,

$$R_{SD} = \frac{1}{W} \frac{(\rho_s^2 + \rho_D^2)}{(\rho_s + \rho_D)^{3/2}} \rho_C^{1/2} + \frac{L}{W} \left(\frac{\rho_D \rho_s}{\rho_D + \rho_s} \right) \quad (26)$$

In this case (case 2) the resistance is given by the sum of a width-dependent contact resistance and a geometrical resistance. The dependence of the series resistance on the junction sheet resistivity is due to current crowding. For small contact resistivities, ρ_c , the current crowds into a relatively small region when flowing across the silicide/doped Si interface. For larger values of the contact resistivity, much current is forced to travel through a considerable distance in the doped Si before reaching the channel region of the device.

The aim of silicidation is to lower L_c such that case 2 holds, in order to suppress the dependence of the total source/drain series resistance on the distance L (see also Section 3.4.4). In addition, this will allow the number of metal contacts per source/drain area to be reduced, which is very important for space reduction.

The effect of silicidation on the transistor behaviour can be observed from experimental data presented in Figs. 62 and 63 [209]. Figure 62 a shows the R_T as a function of gate voltage in the linear region of operation. The source/drain resistance was extracted from the transistor characteristics. It varies between 180Ω at low gate voltages to 60Ω at higher V_{GS} , whereas silicided devices exhibit R_T ranging from 90Ω to 50Ω .

A significant increase in drive current is observed when silicidation is used (Fig. 62(b)). The effect is most pronounced (up to 40%) in the linear region of operation. Besides the drive current, the transconductance increases significantly by silicidation (Fig. 63).

3.1.2. Self-aligned silicidation

Figure 64 shows schematically the process flow for silicidation. Spacers are formed along the poly-Si edges by deposition of SiO_2 and subsequent anisotropic etching. They serve as an electrical insulation between source/drain and gate. Extensions of source and drain regions under the spacer are needed, not only to decrease hot carrier degradation effects but also to provide a conductive path between source/drain and the channel region, since they are spatially separated by the spacer. The optimization of extended source and drain regions is beyond the scope of this review. In order to obtain self-aligned silicide formation on both source/drain and gate areas, metal is then deposited uniformly over the wafer. Self-alignment implies that the control of the lateral silicide growth is such that no silicide paths will form on the spacers, since this would lead to an electrical shorting of the device. Owing to the self-aligned character of the reaction, silicidation will only take place where the metal is in contact with the mono-Si of the source/drain and with the poly-Si of the gate.

3.2. Formation of thin silicides

3.2.1. Minimization of Si consumption and controllability

Whereas in Section 2.2 the thin film growth kinetics and phase formation sequence during silicidation were discussed, this section deals with the controllability of the silicidation process for current and future technologies.

The formation of thin silicides ($< 100 nm$) requires an optimal control of the silicidation process down to very small thicknesses. Even though the silicidation is dependent on several

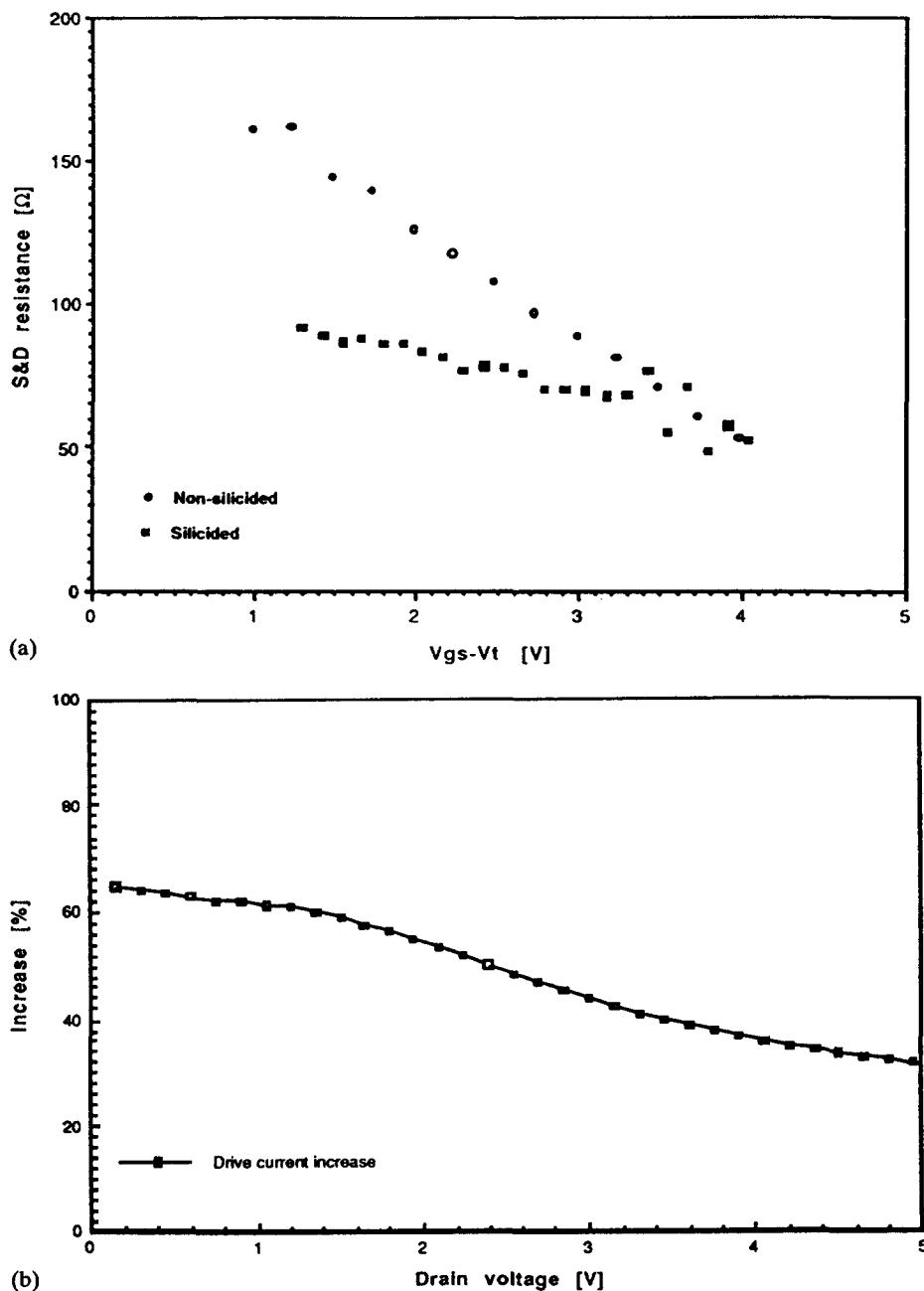


Fig. 62. (a) Total source/drain resistance of a MOS device as a function of the applied gate voltage with and without self-aligned silicidation ($W=20 \mu m$); (b) increase of drive current as a result of self-aligned silicidation of a NMOS transistor ($W=20 \mu m$).

experimental conditions e.g. doping level, crystallinity of the Si, cleaning etc., these different technological situations appear simultaneously on a wafer and as such have a combined influence on the overall process controllability.

A first issue is the minimization of Si consumption. Si consumption is in the first place a consequence of the solid state reaction itself, but depends also on the process, e.g. the selectivity of the chemical removal of the unreacted metals. A comparison between Co and

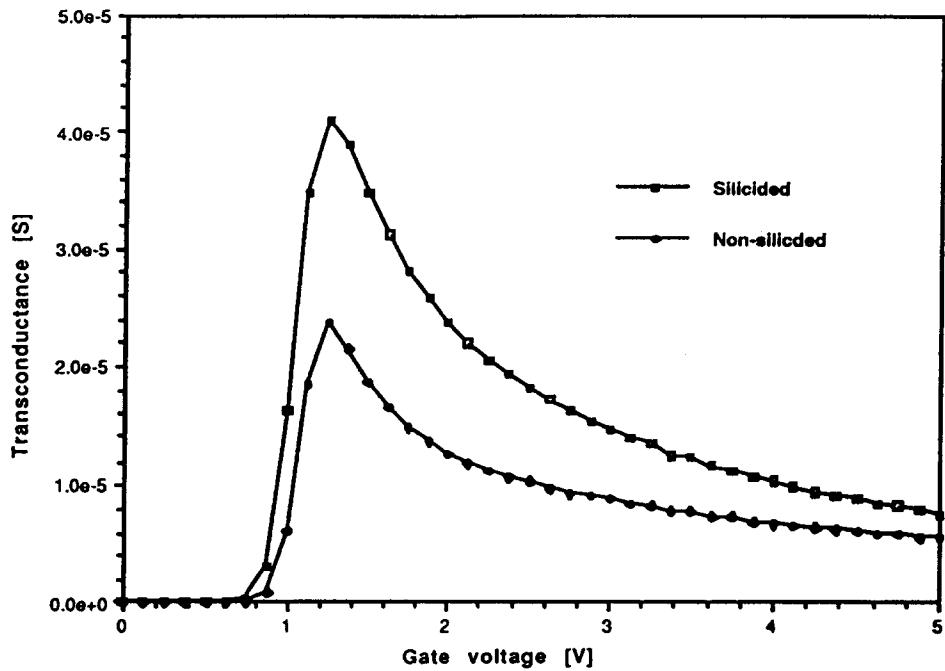


Fig. 63. Transconductance *vs.* gate voltage for an NMOS transistor with and without self-aligned silicidation ($W=20\ \mu m$, $L_{gate}=0.7\ \mu m$).

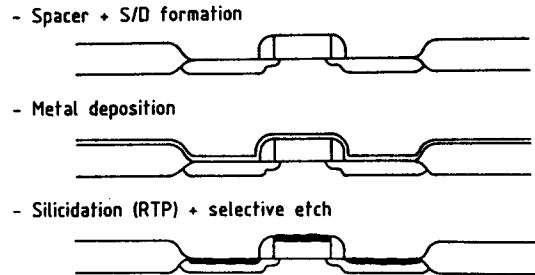


Fig. 64. Schematic process flow for self-aligned silicidation.

Ti silicidation with respect to Si consumption is shown in Fig. 65 [67]. Since the final sheet resistance is the relevant device parameter, the Si consumption is plotted *vs.* sheet resistance. It is clear from these curves that for equal sheet resistance the Si consumption is slightly higher for Co than for Ti. Although this appears as an advantage of $TiSi_2$ over $CoSi_2$, other factors have to be taken into account. Figure 66 shows a silicide implemented in a contact structure. The thickness of the silicide layer is also affected by the selectivity of the etch to remove the unreacted metal. If the selectivity with respect to the silicide is not good, the latter will be thinner, despite the fact that more Si is consumed.

Titanium silicide has a high chemical reactivity, and this certainly becomes clear from the low selectivity with which unreacted Ti can be removed and from the strong dependence on etch parameters [210]. Figure 67(a) shows the sheet resistance value of a $TiSi_2$ layer as a function of the age of the ammonia solution which is used for the selective etch. The $TiSi_2$ layer was formed by sputtering 60 nm Ti followed by two-step RTP using annealing temperatures of 730 and 850 °C. Since the sheet resistance is a measure for the thickness of the resulting silicide, the results illustrate that the final Ti silicide thickness is strongly

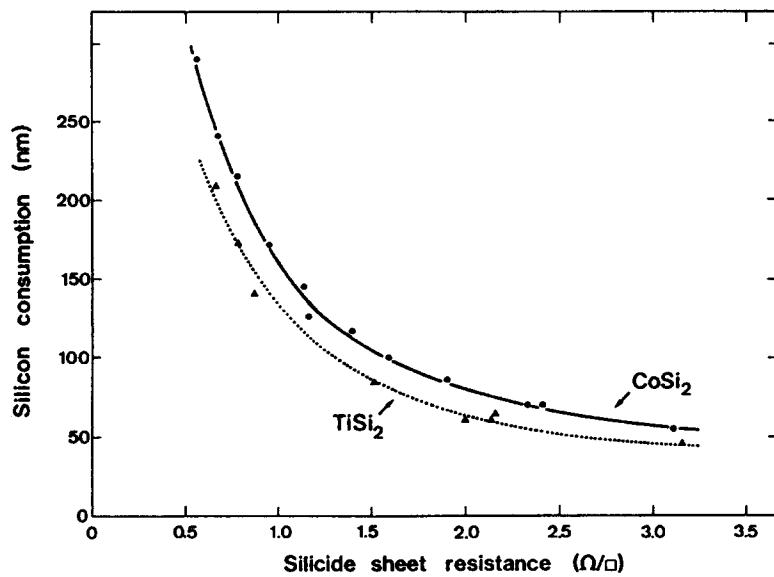


Fig. 65. Silicon consumption during silicidation of Co and Ti vs. silicide sheet resistance.

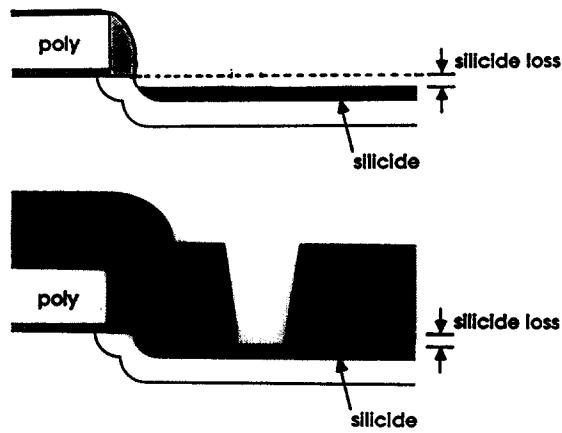


Fig. 66. Schematic of the silicide loss occurring after full implementation of a silicide in a contact hole.

dependent on the age of the selective etch solution. A similar dependence of the silicide etch on the temperature of the ammonia solution was found. No such dependence exists for Co silicidation. Variations of the concentration of the selective Co etch (the H_2SO_4/H_2O_2 ratio was varied from 2:1 to 6:1) and etch time (0–30 min) did not have any effect on the thickness of the intermediate $CoSi$ phase (Fig. 67(b)). Similar differences in etch selectivity of the unreacted metal between $CoSi_2$ and $TiSi_2$ formation were found earlier for dry etching, e.g. during contact hole formation in SiO_2 on top of the silicide layer, and for wet HF etching. Since silicides form a native oxide which is thicker than the equivalent native oxide on Si, the possibility of dipping the oxide away in dilute HF before contact metallization is of technological relevance. Figure 68 shows the etch rate of $TiSi_2$ and $CoSi_2$ in a 2% HF solution, confirming the high resistance of $CoSi_2$ to chemical processing.

Silicides are simultaneously formed on Si regions with different doping levels. The interaction of Ti with doped Si has been described in great detail in Section 2.3. This metal-dopant interaction also determines the control of the final silicide film thickness on

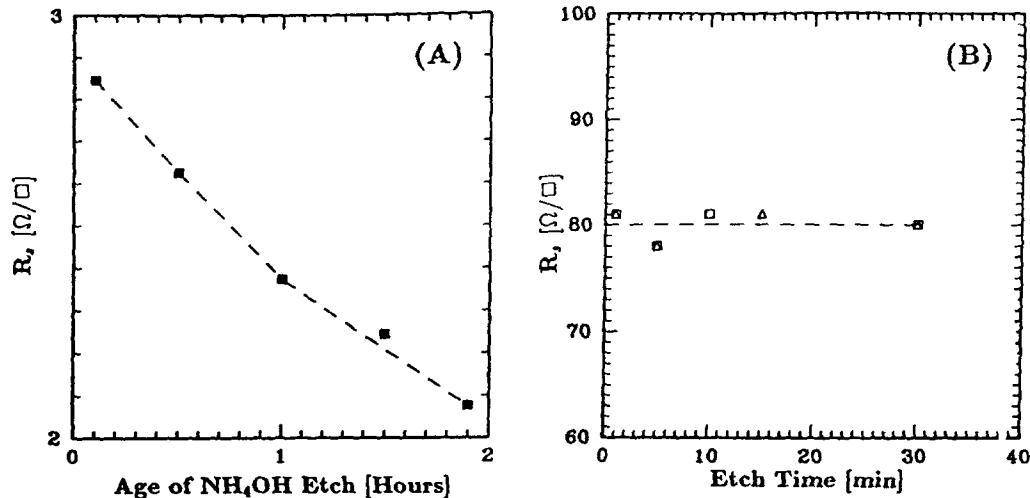


Fig. 67. (a) Sheet resistance value of a $TiSi_2$ layer on Si as a function of the age of the selective NH_4OH etch solution. (b) The influence of the H_2O_2/H_2SO_4 etch time on the sheet resistance of a $CoSi$ film (34 nm) is shown for two different H_2O_2/H_2SO_4 ratios: 1:2 (■) and 1:6 (Δ).

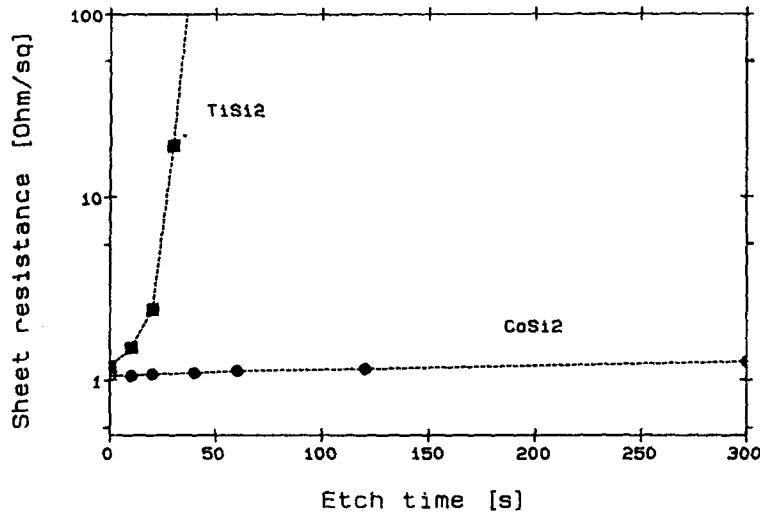


Fig. 68. Increase of sheet resistance of $TiSi_2$ and $CoSi_2$ vs. etch time in a buffered HF (10%) solution.

doped Si. In Fig. 69, the sheet resistance value is plotted vs. the implanted phosphorus dose in poly-Si for silicided wafers using (a) 35 nm Ti and (b) 20 nm Co. The uniformity across the wafer is indicated by the error bar [210]. The absence of any metal-dopant interaction for the Co silicided wafers results in much better thickness control and uniformity, irrespective of the doping level in the silicon. The $TiSi_2$ formation process is clearly dependent on the doping level, which is reflected in the average film thickness and uniformity. Similar results were obtained for silicides on As- and B-doped silicon.

Some work [67,96] has been performed to minimize Si consumption by deposition of Ti-Si or Co-Si alloys. However, this leads to void formation at the interface, loss of self-alignment and silicide precipitation on the SiO_2 areas.

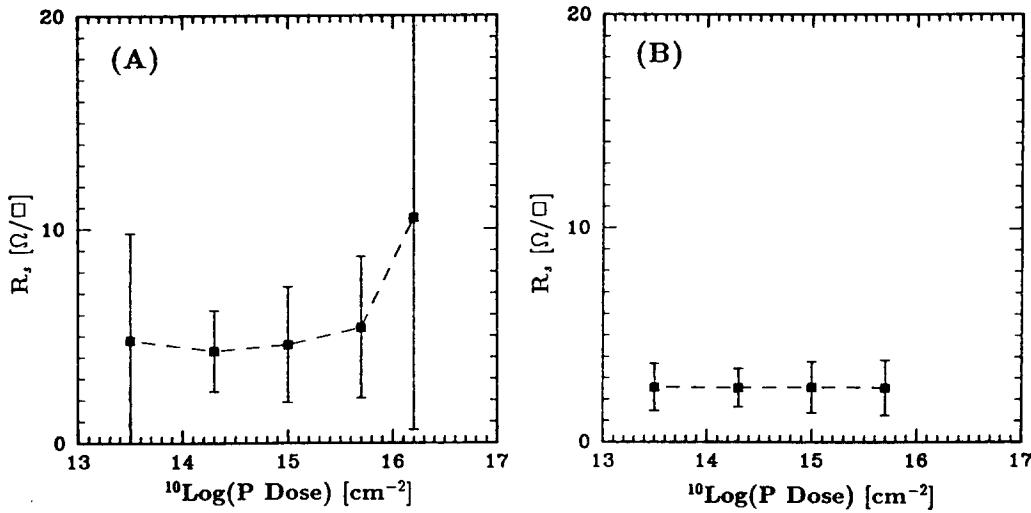


Fig. 69. Influence of P implant dose in polycrystalline Si on the final sheet resistance after silicidation of (a) 35 nm Ti and (b) 20 nm Co.

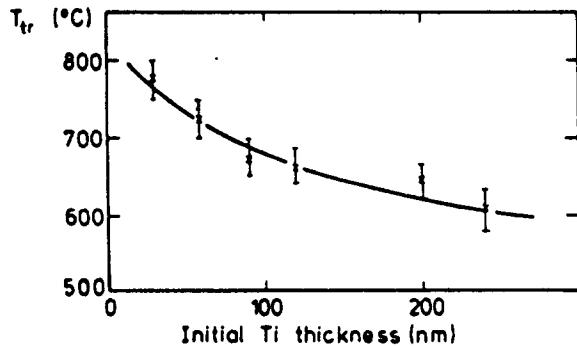


Fig. 70. Transition temperature for the conversion of C49 to C54- $TiSi_2$ as a function of initial Ti thickness (after ref. 211).

3.2.2. Scaling of silicide thickness and controllability

In a self-aligned $TiSi_2$ process only part of the Ti reacts with the silicon, whereas the remainder reacts with the N_2 ambient. The chemical etch following the silicidation step removes the unreacted $Ti(N)$ from the SiO_2 as well as from the silicided areas. The final silicide thickness will therefore depend on deposited Ti film thickness, reaction temperature and reaction time.

The main problem encountered in scaling the $TiSi_2$ thickness is the difficulty of transforming the C49- $TiSi_2$ into the C54 form. An increase in C49-C54 transformation temperature for thin films has been observed by Van Houtum and Raaijmakers [68,211] based on resistance measurements. Figure 70 shows a plot of the transition temperature vs. deposited Ti thickness. Temperatures as high as $800\text{ }^{\circ}\text{C}$ are required for the thinner layers. Recently, Jeon *et al.* [212] have used Raman spectroscopy to extend the experiments to Ti thicknesses down to 5 nm. They confirm that a final silicidation temperature higher than $800\text{ }^{\circ}\text{C}$ is required for the C49-C54 transformation when Ti layers get thinner than 20 nm. The use of RTP has widened the process window for thin $TiSi_2$ formation [213]. Table 5 [214] compares 19 nm and 28 nm deposited Ti thicknesses on n^+ and p^+ areas for furnace and RTP silicidation. The increasing C49/C54 transformation temperature for

TABLE 5

Silicide sheet resistance ($\Omega \text{ sq}^{-1}$) on n^+ and p^+ for two Ti thickness for furnace and RTP silicidation (from ref. 214)

	Ti Thickness	
	19 nm	28 nm
Junction type	n^+/p	p^+/n
Furnace anneal	25.2	4.9
RTA	5.9	4.3
n^+/p		
18.0		5.0
4.2		2.0

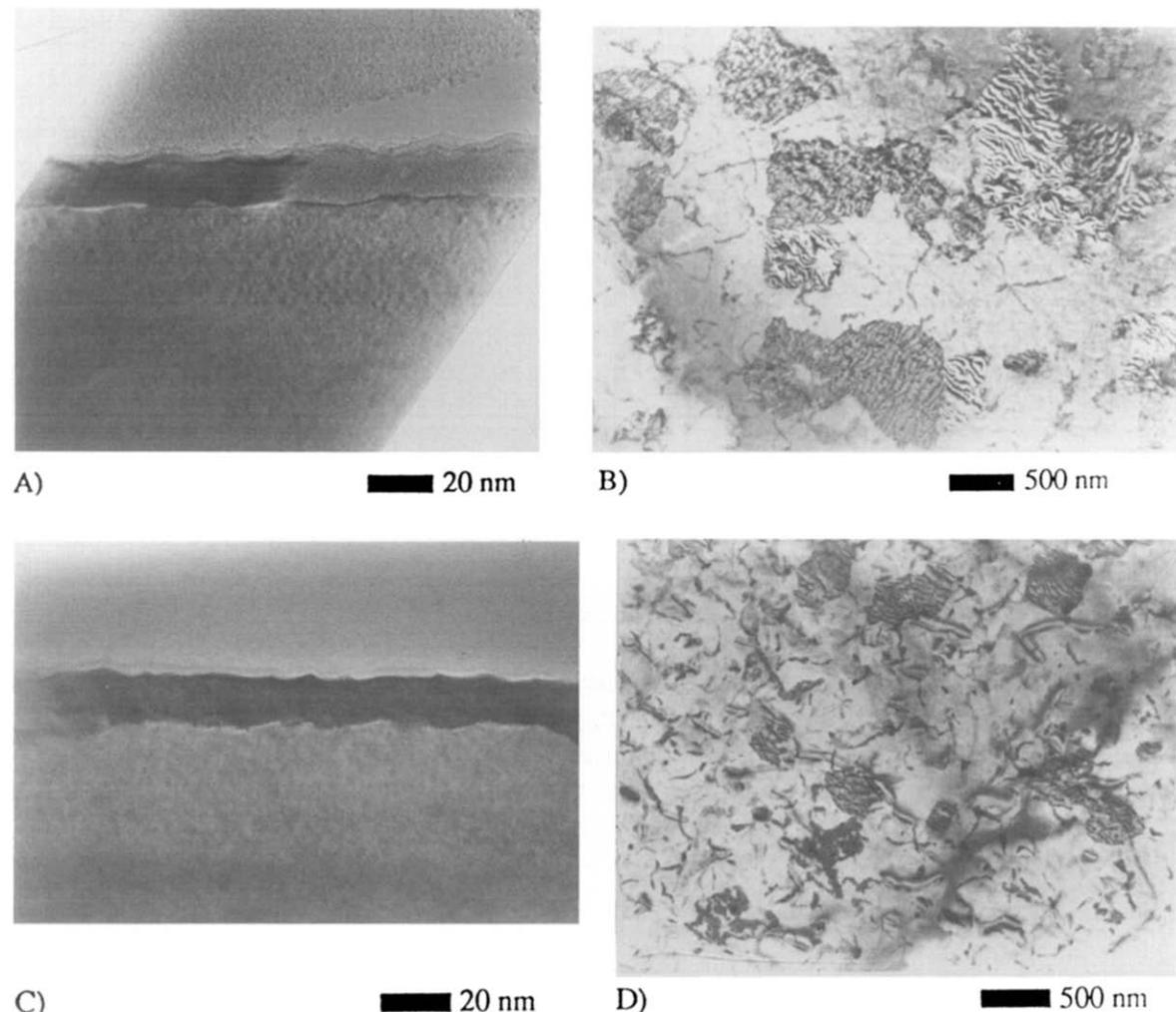


Fig. 71. XTEM and plan view micrographs of $CoSi_2$ layers on ((a), (b)) As-doped ($5 \times 10^{15} \text{ cm}^{-2}$, 50 keV) and ((b), (c)) B-doped ($1 \times 10^{15} \text{ cm}^{-2}$, 20 keV) c-Si substrates annealed at 1100°C , 10 s, and 4 nm deposited Co. No pinholes are observed. The thickness of the $CoSi_2$ is 14 nm.

thinner $TiSi_2$ layers indicates that the formation of homogeneous C54 layers thinner than 40 nm becomes difficult, in particular for silicidation of n^+ doped regions.

In contrast to $TiSi_2$, the growth of thinner $CoSi_2$ films is basically straightforward, since the final thickness depends only on the thickness of the deposited Co layer [210,215]. Figures

71(a)–(d) show cross-sectional and plan view TEM micrographs of ≈ 14 nm $CoSi_2$ films on highly As-doped ((a) and (b)) and B-doped ((c) and (d)) c-Si substrates. The silicide layers were formed by sputtering of ≈ 4 nm Co and a subsequent anneal at 750 °C for 30 s. The sheet resistance of the layers is $12.6 \Omega \text{ sq}^{-1}$.

The reaction kinetics for various deposited Co thicknesses is shown in Fig. 72. The data are taken from *in situ* emissivity measurements in an RTP system [216]. The temperature was ramped gradually from room temperature up to 800 °C with identical temperature profiles for the three wafers. Full conversion to $CoSi_2$ is observed sooner for the thinner Co layer than for the thicker ones. This proves that nucleation problems do not occur for Co as they do for Ti. On the contrary, the thermal budget needed for the formation of thinner $CoSi_2$ is lower than for a thick layer, which is very important for the process window. Ultra-thin silicides can also be formed by using a limited reaction process [210,215]. Here, the Co film is only partially consumed during a first low-temperature step to form an intermediate silicide phase. The amount of cobalt consumed is determined by the reaction temperature and time. The procedure followed in the limited reaction process is shown in Fig. 73(a). A first annealing temperature of 450 – 500 °C leads to a partial reaction of the Co layer into Co_2Si and/or $CoSi$. The reaction is diffusion-controlled and follows a layer-by-layer growth mode. After removal of the unreacted Co, a second thermal treatment follows at a higher temperature (typically 700 °C for 30 s) to form the $CoSi_2$ phase. The final $CoSi_2$ thickness is plotted vs. the anneal time of the first thermal treatment in Fig. 73(b). Figures 74(a) and (b) show XTEM micrographs of $CoSi_2$ layers on (a) B-doped and (b) As-doped c-Si substrates using the limited reaction process. They were formed by an anneal at 450 °C for 5 s, followed by a selective etch, and a second anneal at 700 °C for 30 s. The figures prove that this method results in thin silicide layers with a well-defined $CoSi_2/Si$ interface.

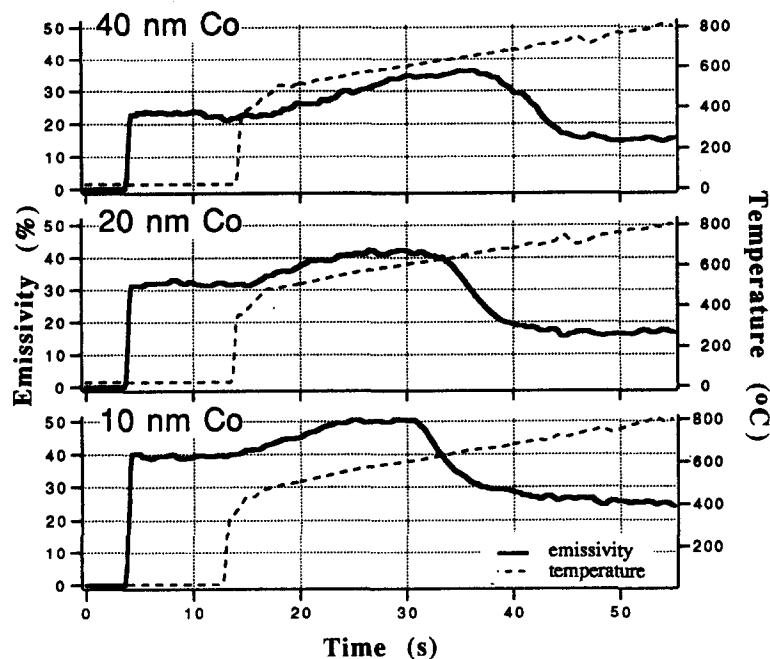


Fig. 72. *In situ* emissivity measurement of (a) 40 nm Co; (b) 20 nm Co; (c) 10 nm Co on Si during silicidation.

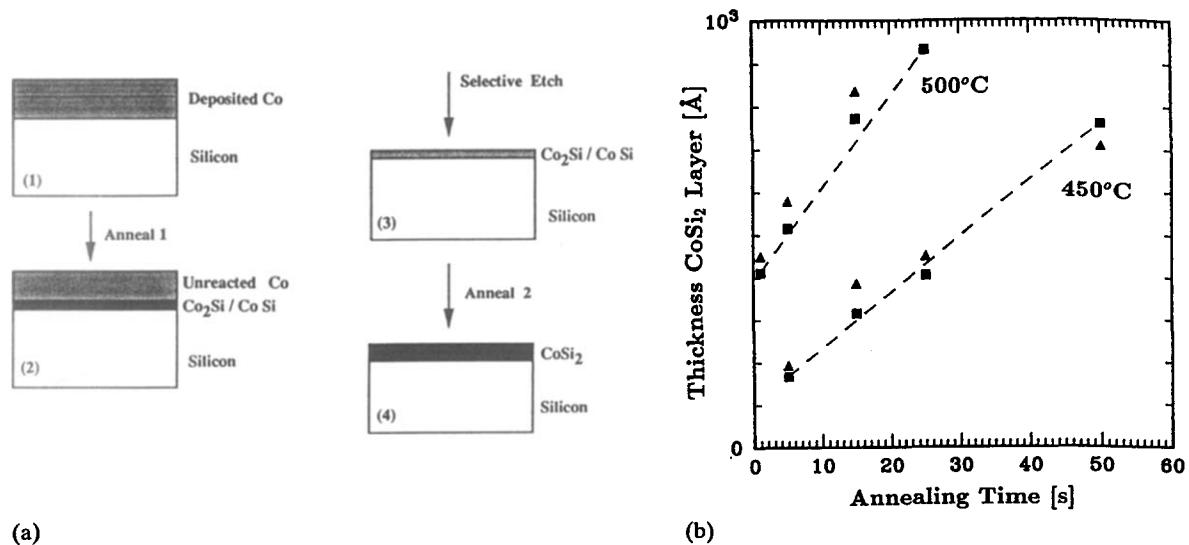


Fig. 73. (a) Schematic overview of the procedure followed during limited reaction processing. (b) Thickness of $CoSi_2$ layers resulting from a limited reaction process versus annealing time. The first temperature step was either 450 °C or 500 °C, and the second temperature step 700 °C for 30 s.

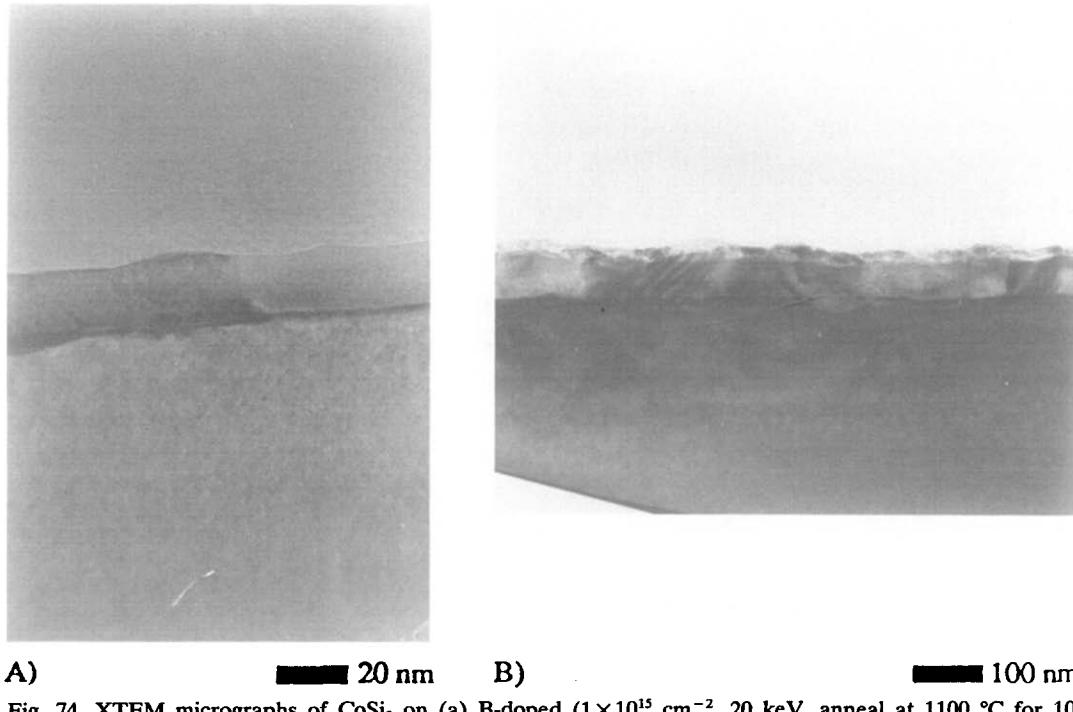


Fig. 74. XTEM micrographs of $CoSi_2$ on (a) B-doped ($1 \times 10^{15} \text{ cm}^{-2}$, 20 keV, anneal at 1100 °C for 10 s) and (b) As-doped ($5 \times 10^{15} \text{ cm}^{-2}$, 50 keV, anneal at 1100 °C for 10 s). The silicides were formed by using a limited reaction process with first temperature at 450 °C for 5 s and second temperature treatment at 700 °C for 30 s.

The application of the limited reaction process to the formation of ultra-thin $CoSi_2$ films puts stringent requirements on the temperature control during rapid thermal processing. This will be discussed in Section 3.7.

3.2.3. Interfacial cleaning

Cleaning of the Si before metal deposition is a key factor in silicide technology. Whereas Ti reduces SiO_2 and therefore reacts with Si despite a thin native oxide, Co is thermodynamically stable on SiO_2 . A thin oxide between Si and Co blocks the reaction or limits it to local spurs of silicidation at weak spots. Besides the native oxide, remnants of dry etching processes (usually C-F polymers), such as the poly-Si and spacer etch, need to be removed carefully.

Cleaning of the Si can be carried out wet before entering the sputter system or by an *in situ* plasma treatment. In addition, sacrificial oxidation steps and/or surface Si etching contribute to the cleaning process. Wet chemical cleaning has attracted a lot of attention during recent years [217,218]. Insight into the surface phenomena during and after cleaning has led to new procedures and to new qualification techniques. HF-last cleans are attractive since they result in a passivated Si surface with low metallic contamination. In particular, Ca, which has a very stable oxide that cannot be reduced by Co or Ti, can be removed in HF-last cleans [219].

In the silicidation process the selectivity of the clean with respect to oxide etching is an important factor, since the design of the spacer is a technological parameter which directly influences the device behaviour. Verhaverbeke *et al.* [219] have studied the removal of native oxide by several HF solutions. They were able to characterize the native oxide removal by contact angle measurements. Figure 75 gives an overview plot of the oxide loss for TEOS and thermal oxide using several native oxide removal processes.

Plasma cleaning in the sputtering system is very efficient in removing a native oxide or C-based contamination layer. However, one has to be careful not to damage the underlying Si or the gate oxide. Antenna effects during sputter etch can be detrimental to the gate capacitor quality, owing to charge build-up on large areas [220,221]. Well-controlled damage created at the Si surface, however, can be beneficial, since it has an impact on grain size and hence on the thermal stability of the silicide [196].

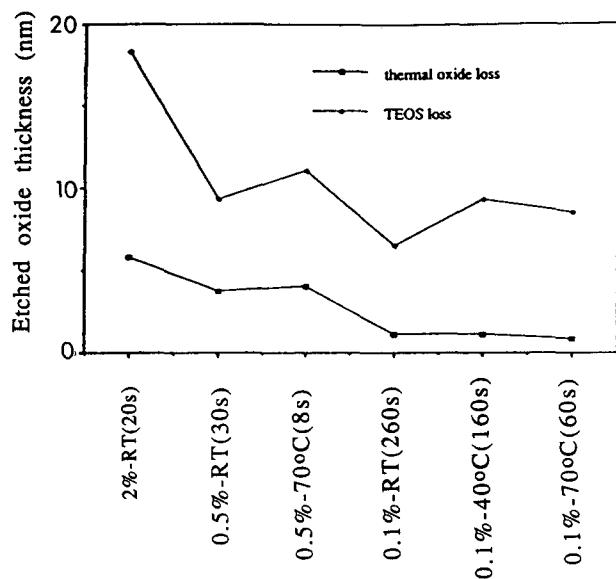


Fig. 75. Loss of thermal oxide and TEOS as a function of the HF process to remove the native oxide.

Recent improvements in sputtering equipment and in sputter etching in particular and the insight into wet chemical cleaning procedures allows further optimization of silicide technology, in view of thinner layers and better reproducibility.

3.3. *Silicidation of laterally confined areas*

The silicidation of confined areas is important for the scaling down of the silicide technology. The kinetics of the reaction between metal and Si has been mainly investigated on unpatterned wafers. The implementation in ULSI technologies requires, however, silicidation of very narrow lines. Although the reaction kinetics does not fundamentally change, new boundary conditions are involved which may influence the way the silicide lines are formed. Process windows need to be defined between a lower temperature limit necessary for silicide formation and a higher temperature limit set by film agglomeration.

Results for $TiSi_2$ and $CoSi_2$ using furnace annealing for silicidation of monocrystalline Si lines with linewidths varying from $40\ \mu m$ to $1\ \mu m$ have been reported [222]. In the case of $TiSi_2$, a strong linewidth dependence is observed for the transformation temperature to the C54 phase, which represents the lower boundary of the process window. After 10 min at $775\ ^\circ C$ all lines are in their low-resistance state. After 6 min at $800\ ^\circ C$, the maximum value of resistance of the $1\ \mu m$ wide resistor has increased. With further annealing this trend continues and an increase is also observed on the wider lines. The increase is due to agglomeration of the $TiSi_2$. The only acceptable process is found in a small temperature range around $775\ ^\circ C$. The narrowing of the process window, due to the retardation of the C49 to C54 transition for $TiSi_2$ on laterally confined areas, can only be avoided by the use of RTP. Higher temperatures yield more nucleation sites for the C54 phase and shorter times postpone the agglomeration of the silicide film to higher temperatures. However, the linewidth dependence of the transformation also remains in this case. As already indicated in Sections 2.2.3 and 3.2.2, the transformation of C49 to C54- $TiSi_2$ is more difficult on n^+ regions than on p^+ regions, resulting in a smaller process window for n^+ . The small number of nucleation sites, combined with a rapid growth of the C54 phase leads to the results described above, especially when the grain size becomes larger than the width of the line. This also explains the observation that thicker $TiSi_2$ films transform at lower temperatures than thinner films (Section 3.2.2). In the case of $CoSi_2$ the opposite is true. Even though the grain size of $CoSi_2$ is usually smaller than that of $TiSi_2$, it is expected that the CoSi-CoSi₂ transformation occurs sooner for thinner films than for thicker ones. No linewidth dependence is observed, indicating that the lower boundary of the process window is not pushed to higher temperatures for narrower lines.

Using an optimized process for $TiSi_2$ and $CoSi_2$, silicidation has been successfully achieved for linewidths as narrow as $0.35\ \mu m$. Figures 76(a) and (b) show the measured and nominal linewidth of silicided submicron lines for both $TiSi_2$ and $CoSi_2$ [223]. The measured linewidth is a result of a comparison of the sheet resistance of a $80\ \mu m \times 80\ \mu m$ van der Pauw structure and the resistance of the narrow line. More details on the measurement technique can be found in refs. 224-226. These results show that for both silicides the formation of narrow silicided lines is possible, even though the variance for $TiSi_2$ remains higher than for $CoSi_2$. It should be noted that the higher process boundary will be pushed downwards for poly-Si lines with respect to monocrystalline Si lines as described above.

Another important issue for the silicidation of narrow lines is related to geometrical effects. Figure 77 shows $CoSi_2$ and $TiSi_2$ on a narrow poly-Si runner. A first observation is that the silicide/poly-Si interface is severely bowed for both $CoSi_2$ and $TiSi_2$. The underlying

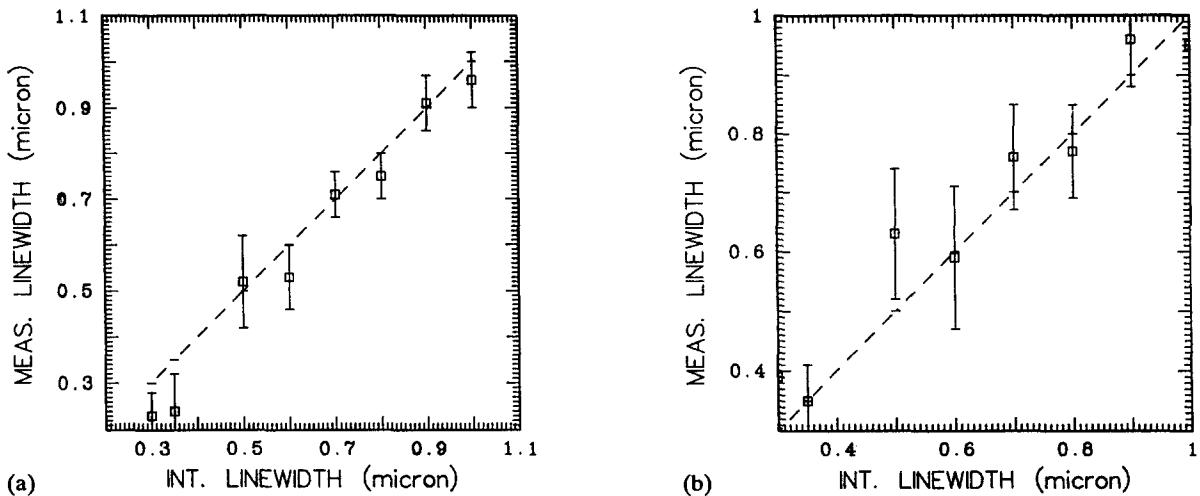


Fig. 76. Measured linewidth for (a) Co- and (b) Ti-silicidized As-doped c-Si lines for linewidths varying from 0.35 to 1 μ m. The sputtered film thickness for Co and Ti was 30 nm and 50 nm, respectively. Co silicidation was done in a one-step annealing at 700 $^{\circ}$ C for 30 s, whereas Ti silicidation was performed by annealing at 730 $^{\circ}$ C and at 850 $^{\circ}$ C for 30 s.

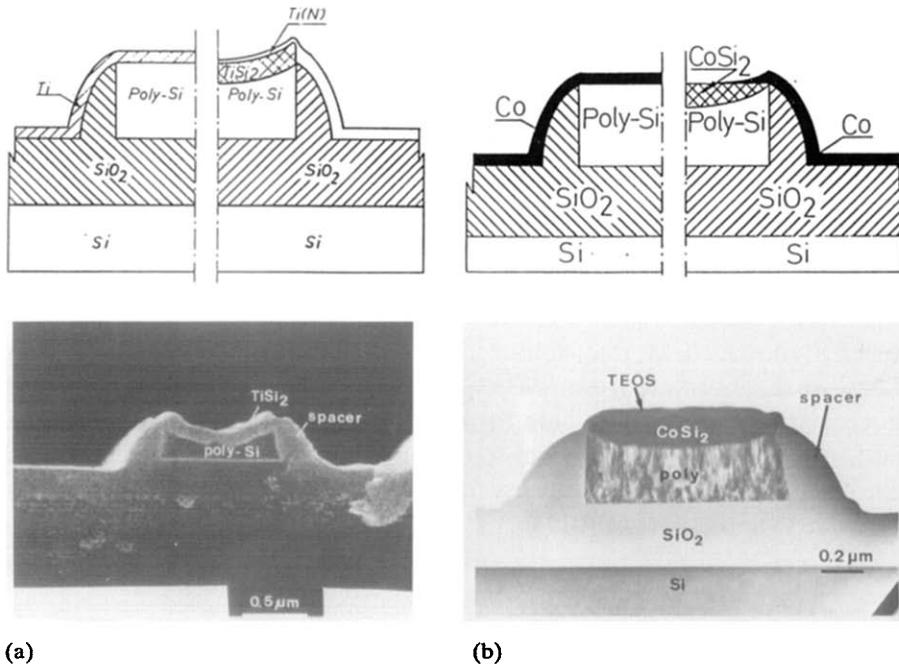


Fig. 77. Cross-sectional TEM and schematic presentation of (a) a TiSi₂/poly and (b) CoSi₂/poly runner.

reason for this phenomenon is mechanical pinning of the metal on top of the spacer [224–226]. This is illustrated for both silicides in Fig. 77. During Ti silicidation, Si is the main moving species. Since the Ti film covers both the Si and the top of the SiO_2 spacer, it cannot move at the spacer edge without a mechanical breakage. Therefore the silicide/poly-Si interface remains fixed at a position determined by the height of the sidewall spacer. Consequently, silicidation close to the spacer will only occur if the necessary Si is supplied from other areas. This leads to an excessive Si consumption from the centre of the line.

On the other hand, Co is the main moving species in the early stage of silicidation when Co_2Si forms. Here again, Co next to the spacer is unable to sink into the poly-Si without a mechanical breakage of the Co layer. The metal film will act as a membrane, resulting in a self-limiting reaction in regions where it is mechanically fixed. The silicide surface will remain relatively flat compared with $TiSi_2$, since no Si diffusion takes place and thus no silicide forms on top of the spacer. The bowing phenomenon is not determined by the crystallinity of the Si. The same observations are obtained for silicidation of narrow lines of amorphous and monocrystalline Si. The solution to this problem lies in careful engineering of the sidewall spacer, to avoid the silicide from reaching the spacer top.

Apart from problems related to silicidation of narrow Si areas, the difference in lateral expansion of silicide and Si creates stress fields in the Si. When the yield strength of Si is exceeded, extended lattice defects may be created. For example, the formation of dislocations at film edges has been studied extensively for stressed Si_3N_4 films used in local isolation processes [227]. The stress levels observed during silicide formation are of similar magnitude. Therefore the defect formation along silicide edges is a potential problem. In practice, silicide films are formed in small stripes, bounded by sharp edges. For the case of a laterally confined silicide, the force ($F = \sigma_f r_f$) is transmitted almost entirely to the Si lattice in the close vicinity of the silicide edge through a small interfacial area. The stress components can be calculated analytically [67,228]. Tensile stress is found in the Si lattice at the silicide edges, whereas compressive stress is found under the silicide.

At temperatures higher than 600 °C, localized stress fields can cause plastic deformation of the Si by generation of dislocations, either heterogeneously by the capture and multiplication of dislocations from other sources or homogeneously by the condensation of Si interstitials [229]. Homogeneous nucleation follows a supersaturation of Si interstitials which align in the stress field and precipitate in a dislocation loop. The localized stress fields at the edges of the silicide films will in this case also be preferential sites for homogeneous defect generation.

Several experiments have been performed to investigate defect formation along $TiSi_2$ and $CoSi_2$ edges. Figure 78 shows SEM micrographs for $TiSi_2$. For 120 nm Ti (yielding 220 nm of $TiSi_2$), defects were observed from 700 °C on. This corresponds to the point where the sheet resistance drops, indicating silicide formation. With increasing temperature, more defects are formed, owing to increasing silicide thickness. When 65 nm Ti was used (yielding 110 nm silicide), small defects were observed as well. The Burgers vectors were determined to be $b_1 = (a/2)[101]$ and $b_2 = (a/2)[011]$. A three-dimensional picture and a cross-

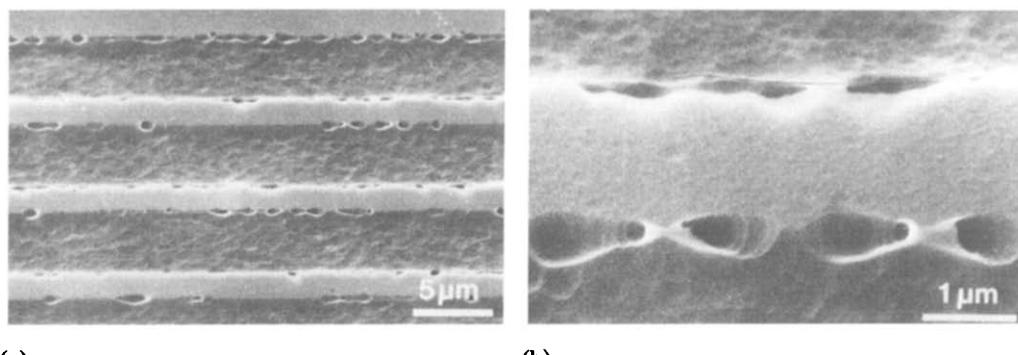


Fig. 78. SEM micrographs of $TiSi_2$ lines after removing the silicide and oxide for 120 nm of Ti reacted at 900 °C for 30 s in N_2 (defects are revealed by Secco etching).

sectional TEM micrograph of a sample reacted at 800 °C are given in Fig. 79. This figure confirms that the loops are located in a {100} glide plane close to the ⟨110⟩ oriented silicide edge.

In similar experiments with $CoSi_2$, no defects were observed for silicide thicknesses up to 300 nm. A low defect density was observed in samples with 540 nm silicide, as illustrated by the SEM micrograph of Fig. 80.

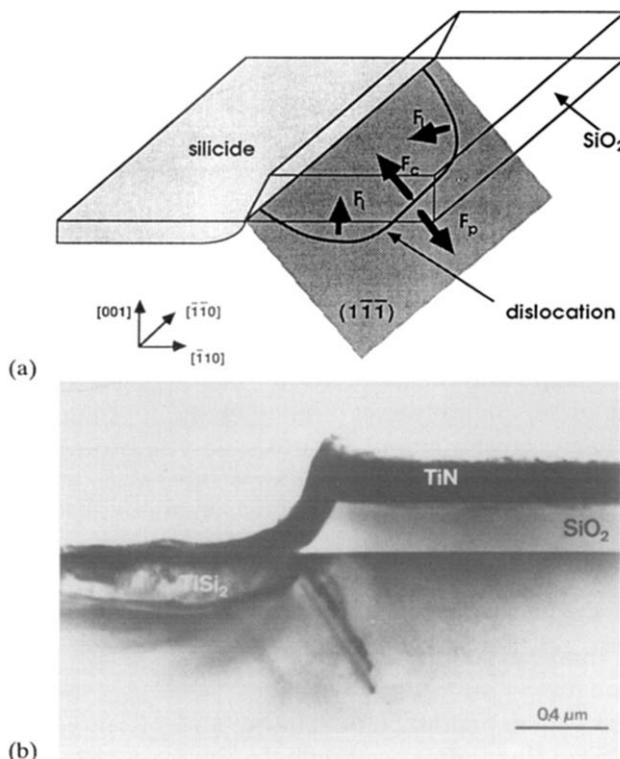


Fig. 79. (a) Schematic diagram and (b) cross-sectional HVTEM micrograph of dislocation half-loops nucleated along a $TiSi_2$ line. The defects are formed in the {111} planes through the silicide edge (silicidation at 800 °C for 30 s in N_2 , starting from 120 nm of Ti).

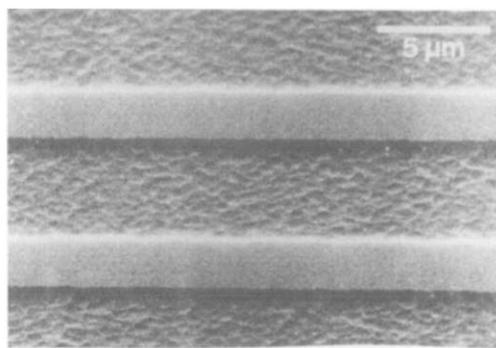


Fig. 80. SEM micrograph of $CoSi_2$ lines after removing the silicide and oxide for 80 nm of Co reacted at 800 °C for 30 s in N_2 (defects revealed by Secco etching).

3.4. Silicided shallow junctions

3.4.1. Characterization of shallow junctions

For the characterization of silicided shallow junctions, one is mainly interested in the doping profile, more particularly the junction depth and the dopant concentration at the silicide interface. Since junction depths become smaller and the determination of the concentration at the silicide/Si interface with SIMS becomes more difficult, it is necessary to discuss dopant profiling. Electrically the diode leakage current at reverse bias is an important issue, as well as the contact resistance. Therefore, the contact resistance structure used in the remainder of this paper will be briefly discussed.

3.4.1.1. Dopant profiling

The profiling of dopants in a silicide/Si structure is quite complicated. Matrix effects during sputtering have to be taken into account when crossing the silicide/Si interface. The metal decay length, which is in the first place affected by ion mixing, is superimposed on the roughness of the silicide/Si interface. In addition, the formation of small precipitates at the interface can affect the profiling.

Figure 81(a) shows a typical SIMS measurement of a $CoSi_2$ layer on a shallow B-doped Si region. The Co signal is plotted in the same figure. The interface between the silicide and the Si is not well defined, owing to the various effects described above. In order to distinguish between the silicide/Si interface roughness and the SIMS decay length, comparative SIMS experiments were carried out by Elst *et al.* on polycrystalline and monocrystalline $CoSi_2$ layers. The latter were formed by ion beam synthesis and exhibit a very flat interface between the silicide and the Si. Figure 81(b) shows the decay length of the Co signal in mono- and polycrystalline $CoSi_2$. The following observations are made [230].

1. The decay length of Co is longer for the polycrystalline sample than for the monocrystalline sample.
2. Within experimental error, no primary beam energy dependence is found for the polycrystalline silicide, in contrast to the monocrystalline sample.
3. O_2^+ profiling provides a smaller decay length.

For the monocrystalline silicide, the observed dependence on energy and primary ions suggests that the depth resolution is limited by sputter-induced defects. In the polycrystalline case, the interface roughness dominates the SIMS profile at the interface and sets a limit to the accuracy of the dopant profiling.

In order to overcome the limitations due to the roughness of the silicide/Si interface, profiling measurements were performed after etching off the capping layer and the silicide itself. Figure 82 presents B profiles formed by diffusion from polycrystalline $CoSi_2$ (see Section 3.4.3 for the outdiffusion process). Three samples were measured: one before etching the TEOS cap layer, one after etching the TEOS cap layer and one after stripping both the TEOS and the $CoSi_2$ layers. The profiles were measured with 5.5 keV oxygen. B peaks are observed at the $SiO_2/CoSi_2$ and $CoSi_2/Si$ interfaces. The shape and height of the interface peaks are sample-specific and cannot be attributed to matrix effects. The variation of the B signal at the interfaces are due to changes in depth resolution. Detailed comparison of the profiles reveals that 15 nm of the B-doped Si has been etched away by the strong HF solution during the $CoSi_2$ strip. The B peak in the latter sample is, therefore, an indication of autoclaving of B during hydrofluoric acid etching.

In the case of dopant profiling below an overlaying $TiSi_2$ layer, additional measurement inaccuracies can occur due to the presence of small precipitates of metal dopant compounds

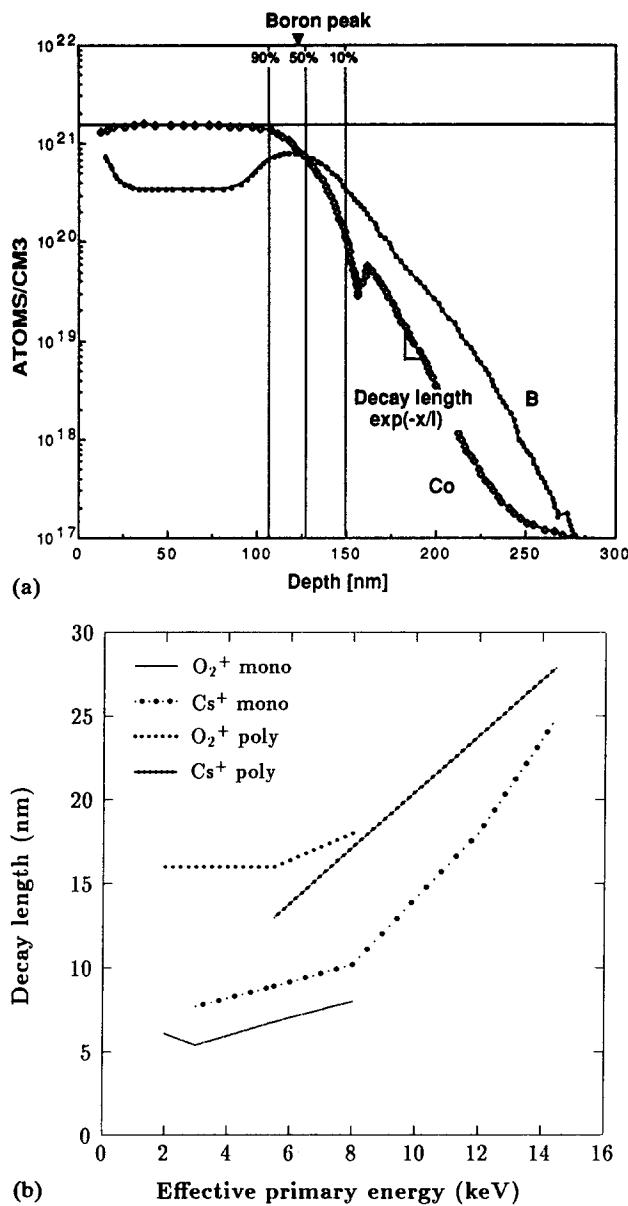


Fig. 81. (a) B and Co SIMS profiles in a $CoSi_2/Si$ structure; (b) decay lengths derived from the decay at the $CoSi_2/Si$ interface for mono- as well as polycrystalline silicide for several experimental conditions.

at the silicide/Si interface. Long tails in the SIMS profiles were observed by Probst *et al.* [139] and attributed to the presence of TiB_2 particles at the interface. It was found that these particles, due to their extremely slow erosion during depth profiling, mask the underlying Si and yield slowly decaying B and Ti signals. It should be noted that etching of the silicide in diluted HF does not solve the problem. A representative profile of the latter is shown in Fig. 83. An SEM micrograph of the SIMS crater reveals the masking effect of the TiB_2 particles leading to the erroneous results. The removal of these particles in an ammonia solution is, therefore, mandatory, in addition to the removal of the silicide. An alternative way to approach the problem is by thinning the back-side of the wafer and by starting the SIMS profiling from the Si substrate up to the interface with the silicide.

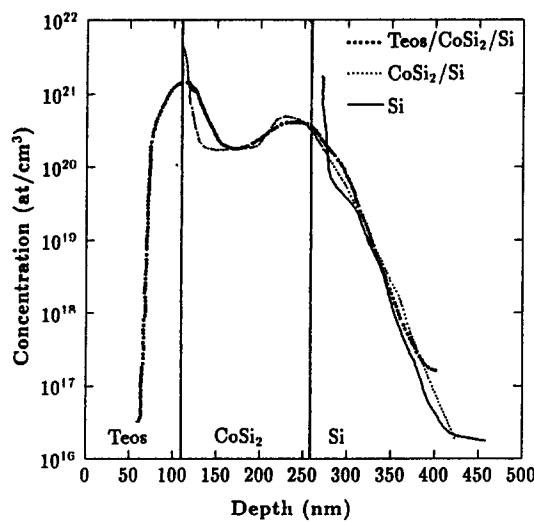


Fig. 82. B-profiles formed by outdiffusion from $CoSi_2$ at $1050\text{ }^{\circ}\text{C}$ for 10 s. Profiling was performed before and after etching off the TEOS layer, and after etching both TEOS and $CoSi_2$.

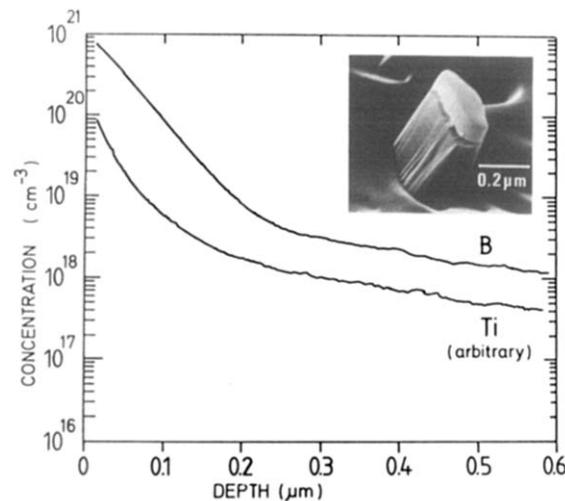


Fig. 83. SIMS depth profiling of B implanted in $TiSi_2$ and diffused at $950\text{ }^{\circ}\text{C}$ for 30 min. The $TiSi_2$ was stripped in HF before the measurement. The insert shows an SEM micrograph of the corresponding SIMS sputter crater at the location of a TiB_2 particle.

3.4.1.2. Contact resistance

For contact resistance measurements, four-terminal Kelvin [231] resistor structures are best suited. Figure 84 shows such a structure in cross-section and top view. To measure the contact resistance between the silicide and the highly doped region, only the contact areas should be silicided. Silicidation of the full diffusion region would provide a measurement of the metal/silicide contact only. The metal/silicide contact resistance is usually an order of magnitude lower than the silicide/Si contact resistance. Therefore the series resistance of both contacts is mainly determined by the silicide/Si contact.

3.4.2. Preformed junctions

As a consequence of the trend to scale silicided shallow junctions, the doping of the Si and the formation of the overlaying silicide become inherently dependent on each other.

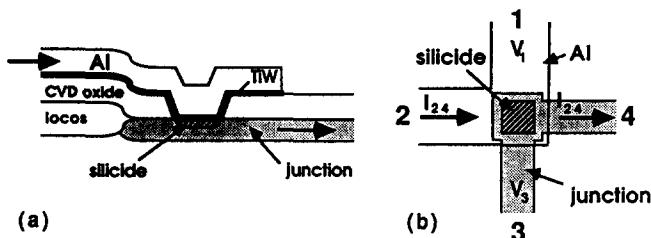


Fig. 84. Four-terminal Kelvin structure for contact resistance measurements between silicide and doped Si: (a) cross-section; (b) top view.

TABLE 6

Mean and standard deviation of leakage current density measured at 5 V reverse bias (100 devices measured) for arsenic diodes with varying silicide thickness. Junction depth before silicidation was $0.25 \mu\text{m}$

Co thickness (μm)	Si cons. (nm)	Silicided devices			Control devices		
		Mean (nA cm^{-2})	St. dev. (nA cm^{-2})	Good devices (%)	Mean (nA cm^{-2})	St. dev. (nA cm^{-2})	Good devices (%)
20	55	1.6	0.3	99	1.3	0.1	98
30	85	1.5	0.1	98	1.2	0.3	100
38	105	3.4	1.2	89	2.9	0.8	96
55	170	2.7	1.8	52	1.2	0.4	100

In the case of preformed junctions, the doped regions are defined prior to silicidation. This means that the junction depth is completely determined by the implant and annealing conditions. The formation of the shallow p^+ junction is the greatest challenge. The use of Ge to pre-amorphize the Si in combination with BF_2 has become a classical method of limiting the junction depth [232]. Alternatively, Sb can be implanted instead of Ge, with the additional effect that it compensates B in the tail region [233,234]. The detailed discussion of shallow junctions is beyond the scope of this paper and can be found in the recent literature [220,235,236].

After the shallow junction formation the silicide is grown on top of the doped region. The silicide formation on highly doped Si is treated in Section 2.3. The thickness of the silicide is limited by the junction depth, owing to the Si consumption. A critical distance between the silicide and the junction region is required to avoid high diode leakage currents. Owing to the silicide/Si interface roughness, this distance has to be large enough to avoid junction spiking.

Table 6 shows leakage currents and yield of Co-silicided n^+ diodes. In this experiment the junction depth was $0.25 \mu\text{m}$ [67]. Various thicknesses of Co were used to vary the amount of Si consumed. When the silicide comes too close to the junction depth, the yield of diodes drops dramatically, owing to local penetration of the junction by the silicide, as depicted schematically in Fig. 85. Similar results were reported for $TiSi_2$ [237].

The critical distance between the silicide/Si interface and the junction has been estimated experimentally by measuring the leakage current of p^+ - n junctions. In Fig. 86, the leakage current is plotted as a function of the silicide sheet resistance as well as a function of the estimated distance between the silicide/Si reaction front and the metallurgical junction. The p^+ junctions were formed by a 20 keV BF_2 implant with a dose of $1 \times 10^{15} \text{ cm}^{-2}$, leading

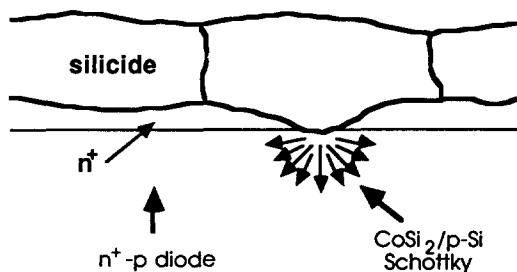


Fig. 85. Junction penetration due to silicide roughness.

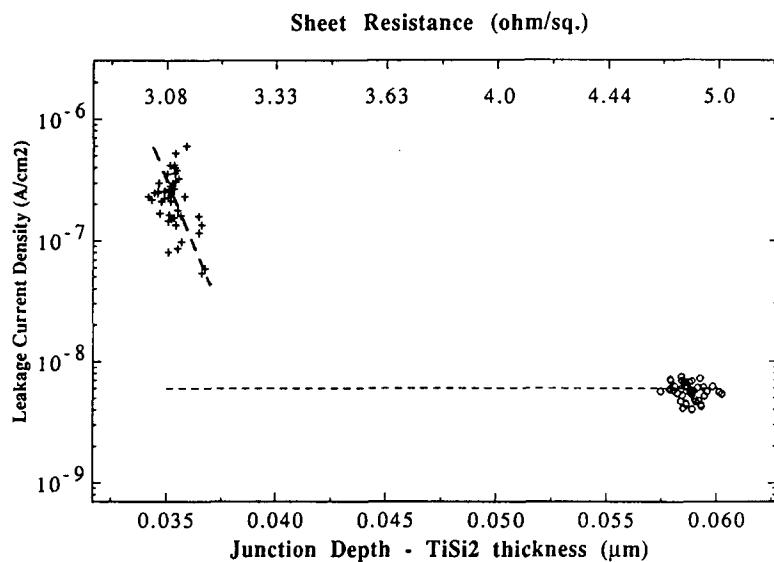


Fig. 86. Leakage current density for samples with a varying distance between the actual junction depth and the silicide/Si interface. The samples were implanted with $1 \times 10^{15} \text{ cm}^{-2} BF_2$ at 20 keV and annealed at 1100 °C for 10 s. The thickness of the deposited Ti was between 30 and 40 nm for silicidation. The dotted line represents the leakage current density for non-silicided samples.

to a junction depth of about 0.09 μm as measured by a spreading resistance probe (SRP). After annealing at 1100 °C for 10 s, either 30 or 40 nm of Ti was deposited to form a silicide. The calculation of the distance between the silicide and the junction depth was based on the sheet resistance of the silicide, assuming a specific sheet resistivity of 15 $\mu\Omega$ cm. The dotted line represents the mean leakage current on a wafer which has not been silicided. The results from this figure suggest that a distance of the order of 50 nm must be maintained between the silicide and the junction. Therefore higher sheet resistances will have to be tolerated on silicided junctions in advanced technologies.

In an attempt to monitor the removal of implantation end of range defects during silicidation (see Section 2.4), test diodes were fabricated [228]. Figures 87(a) and (b) give a schematic of the test diodes. End of range damage was introduced in Si by pre-amorphization with a heavy element, yielding a band of dislocation loops after annealing. Subsequently, a shallow junction was formed in such a way that the space charge region of the reverse biased diode extended beyond the dislocation loops. Diode leakage currents were then compared for diodes without silicide, with $TiSi_2$ and with $CoSi_2$. The magnitude of the leakage current can be considered as a measure of carrier generation in the space charge region, and hence gives an indication of the extent of the end of range defects. In this

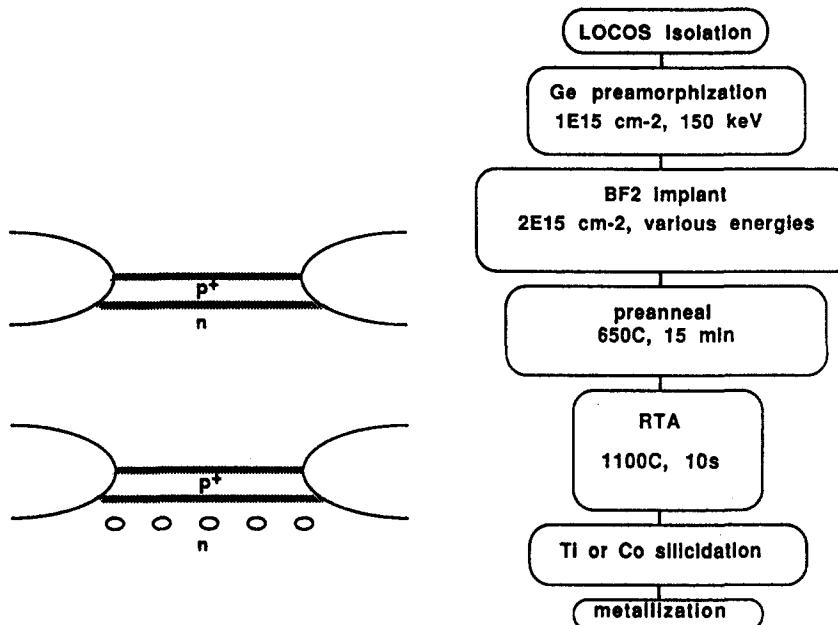


Fig. 87. Schematic of junctions (a) without and (b) with intentional defects and (c) process flow.

way, the distribution of defects can be monitored on a full 125 mm wafer and the homogeneity and reproducibility over large areas can be observed, in contrast to TEM measurements, which cover only a very small surface.

The process flow for the diode fabrication is outlined in Fig. 87(c). After the isolation process, pre-amorphization of Si was performed by Ge implantation in an n-type substrate. Shallow p⁺ implants were then carried out with BF₂ using various energies. The amorphous layer was regrown at 650 °C and the dopants were activated during a rapid thermal cycle at 1100 °C for 10 s. Subsequently, the diodes were silicided with 20 nm of Co at 700 °C for 30 s or with 30 nm of Ti with a two-step process at 730 °C for 30 s and at 850 °C for 30 s with an intermediate wet etch of Ti.

The energy of BF₂ implants was varied between 20 and 45 keV. The sample was pre-amorphized with Ge and implanted with 45 keV BF₂. After annealing, the SIMS F profile shows a small peak at a depth of about 200 nm. This is an indication of the location of the end of range defects at the previous a/c interface which are decorated with F. The B profile has diffused just beyond this defect region, so that the end of range defects are still in close proximity to the space charge region. Hence, for the lower implantation energies (at 20 and 30 keV) the end of range defects are expected to be located beyond the metallurgical junction and a large impact of these defects on diode behaviour is expected.

The leakage currents of diodes fabricated under the various experimental conditions are listed in Table 7 for a reverse bias of 5 V. In the first column, BF₂ was implanted in crystalline Si (no Ge pre-amorphization) at various energies. The diodes were silicided with Co. Leakage currents were all in the range of 5 nA cm^{-2} , which is a typical value for diodes fabricated with this process. The second column represents leakage currents of diodes, in which the end of range damage was introduced. The diodes were also silicided with Co to allow comparison with the diodes of the first column. It is obvious from the high leakage currents that defects in the space charge region are present and have a major influence on carrier generation. For the 45 keV BF₂ implant the junction appears to be

TABLE 7

Leakage current density for diodes implanted with BF_2 with and without Ge pre-amorphization. The diodes are silicided with $CoSi_2$ or $TiSi_2$

Implantation energy of BF_2 (keV)	Leakage current density ($nA\ cm^{-2}$)		
	$BF_2 + CoSi_2$	$Ge + BF_2 + CoSi_2$	$Ge + BF_2 + TiSi_2$
20	6.8	1.5×10^5	40
30	3.0	5.1×10^5	13.4
45	2.4	3.1	6.5

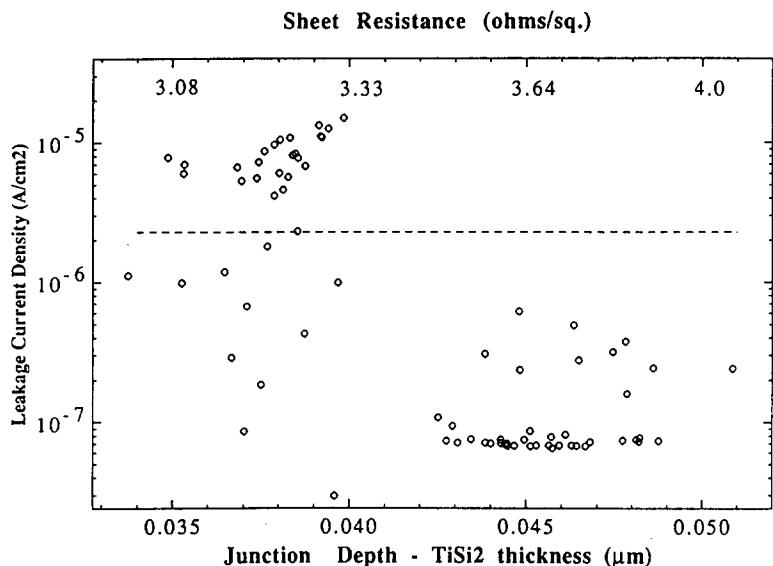


Fig. 88. Leakage current density of samples implanted with $1 \times 10^{15} \text{ cm}^{-2} BF_2$ at 20 keV into Si, pre-amorphized with $1 \times 10^{15} \text{ cm}^{-2} Ge$ at 130 keV. The annealing was performed at 1100 °C for 10 s. The thickness of the deposited Ti was between 30 and 40 nm for silicidation. The dotted line represents the leakage current density for non-silicided samples.

just beyond the defect band and a low leakage current has been measured. In the third column, however, leakage currents are present for diodes silicided with Ti. The leakage currents are surprisingly low and lead to the conclusion that the Ti silicidation has cured the defects. It must be mentioned that the numbers in Table 7 represent average leakage currents from 50 diodes.

The shrinkage of extrinsic defects, i.e. dislocation loops, by the silicidation process could be beneficial for the electrical quality of the junction with a lower temperature budget. However, a more detailed investigation indicates that the annihilation process is difficult to reproduce on large areas. In this case, p^+ junctions were formed with 150 keV Ge pre-amorphization. About 40 nm of Ti was deposited on the wafers for silicidation. In Fig. 88 the leakage current density is plotted similarly to Fig. 86. The dotted line represents the mean leakage current from a wafer which has not been silicided, and where TEM shows defects in the space charge region of the reverse-biased diode. It is observed that the leakage current is greatly improved for the silicided wafer when the silicide sheet resistance is sufficiently high. This would suggest that, if the leakage current density is to be further improved, the silicide front must be moved closer to the defects (i.e. use a thicker silicide).

However, by doing so the leakage current will increase, as mentioned before, owing to the proximity of the silicide front to the junction.

An overview of the state of the art of preformed silicided shallow junctions is given in Table 8. Only junction depths less than $0.15\ \mu m$ were considered. An overview of deeper junctions can be found in ref. 239. Since it is the aim to maximize the silicide thickness for a specific junction depth, and since the silicide roughness (and therefore the chance for junction penetration) increases with increasing silicide thickness, the relative thickness of the silicide with respect to the junction depth is an important technological parameter. It is clear that good diode characteristics can be obtained with both silicides for future shallow junction processes.

In general, the crystalline silicide is chemically stable on Si. Since the solid solubilities of both Ti and Co in Si are very low, no diffusion of metals of the silicide into the Si has ever been observed. Extensive DLTS measurements have been carried out on Co-silicided shallow junctions [243]. The electrically active concentration of deep levels is much lower than the solid solubility of Co at the considered temperature. No effect has been observed on diode leakage current for RTP temperature treatments as high as $1100\ ^\circ C$. An interesting case, however, is when the interfacial layer between the metal and the Si is an amorphous silicide. This occurs for instance when Ti is sputtered on Si, as discussed at length in Section 2.2. It has been shown that the presence of this amorphous interfacial layer is a source of metal atoms, whereas the crystalline silicide is not. Therefore an amorphous silicide layer on doped Si results in low-quality diodes with soft breakdown characteristics [244].

In order to optimize silicidation of shallow junctions, the contact resistance has to be taken into account, in addition to the diode leakage current and the sheet resistance. The contact resistance is very sensitive to the dopant concentration at the metal/semiconductor interface. The contact resistance is a result of defining the silicide thickness appropriately, and by carefully matching the doping profile in order to maintain the maximal doping level in the range of $1 \times 10^{20}\ At.\ cm^{-3}$ at the silicide/Si interface.

Since more high-temperature treatments are needed in the technological process subsequent to the silicidation, it is important to estimate their effect on the contact resistance.

TABLE 8
Summary of characteristics of silicided preformed junctions

Silicide	Silicide thickness (nm)	Junction depth (nm)	Silicide (%)	Leakage ($nA\ cm^{-2}$)	Ref.
$TiSi_2$	60	BF_2 , 130	45	7	238
$TiSi_2$	20	BF_2 , 80	25	5	239
$TiSi_2$	20	As, 80	25	10	239
$TiSi_2$	50	BF_2 , 100	50	6	235
$TiSi_2$	35	As, 110	30	0.63	199
$TiSi_2$	35	B, 113	30	0.9	199
$CoSi_2$	55	As, 150	37	1.3	159
$CoSi_2$	39	BF_2 , 110	35	2.2	240
$CoSi_2$	70	As, 100	70	2	241
$CoSi_2$	20	BF_2 , 80	25	7	239
$CoSi_2$	20	As, 80	25	2	239
$CoSi_2$	70	BF_2 , 100	70	6	242

The latter [245] is recorded for $TiSi_2$ and $CoSi_2$ for various heat treatments after junction silicidation and compared with a reference value without additional heat treatment. A monotonic increase of contact resistance is visible for both dopant species and both silicides. In relation to the reference samples, this increase depends only weakly on the silicide material used. Only B-doped $TiSi_2$ samples yield slightly higher contact resistances than the $CoSi_2$ samples do. The depletion of dopants from the Si region close to the silicide interface is the main reason for the degradation of the contact resistance. The extent of the contact resistance degradation is dependent on (i) the diffusion constants of the dopants in the Si, and is therefore more pronounced for B- than for As-doped Si; (ii) the diffusion of the dopants through the silicide layer; (iii) the metal-dopant compound formation; and (iv) the segregation of dopants at the silicide/capping layer interface.

The diffusion of dopants in polycrystalline silicides has been discussed in Section 2.3 and is in all cases under consideration much faster than the diffusion of B and As in monocrystalline Si. The observed $TiAs$ and TiB_2 formation provides an additional sink for mobile dopants in the case of $TiSi_2$. However, the diffusion of the dopants within Si itself is the most important rate-limiting parameter for contact degradation.

In addition to the optimization of the silicide thickness and the junction profile, the purity of the silicide growth can influence the contact resistivity. In the case of $CoSi_2$, significantly lower contact resistivities have been reported on n^+ and p^+ junctions using UHV growth of the silicide [246].

3.4.3. Outdiffused junctions

The outdiffusion technology consists of the silicidation of undoped Si regions followed by implantation of dopants within the silicide. Subsequently the dopants are diffused out of the silicide into the Si. A suggestive picture of the outdiffusion process is shown in Fig. 89(a). Outdiffusion is an attractive alternative to direct implantation into silicon for the formation of shallow junctions [220,245,247–249]. The main advantage of this process is that the implantation damage and the implantation profile remain confined within the silicide. The latter is easier to obtain than in Si, owing to the higher mass of the metal atoms.

The junction depth is controlled by the implant dose and energy and by the temperature treatment. The spiking of the junction by the silicide is avoided, since the dopant diffusion front is conformal to the silicide/Si interface. Figure 89(b) shows a cross-sectional SEM micrograph of outdiffused doped regions and the overlaying silicide, confirming the ideality of the diffusion source by the conformal diffusion of the dopant with respect to the original silicide/Si interface.

Figure 90(a) shows typical outdiffusion profiles of B and As from $CoSi_2$ for various heat treatments. The figures show both the redistribution of the dopants in the silicide and their profiles in the underlying Si. Whereas the junction depth and interface concentration are controlled by the diffusion temperature and time, there is a significant segregation at the silicide/cap layer interface. Figure 90(b) displays the profiles of B implanted in $CoSi_2$ with different doses followed by an outdiffusion step of 1050 °C for 10 s. From these profiles it becomes clear that for doses higher than 5×10^{15} at. cm^{-2} segregation towards the $CoSi_2$ /Si interface takes place, whereas segregation towards the SiO_2 /Si interface is observed for all doses.

It should be noted that the characteristics of the capping layer have a distinct influence on the outdiffused doping profile. During the deposition of the capping layer on B-implanted

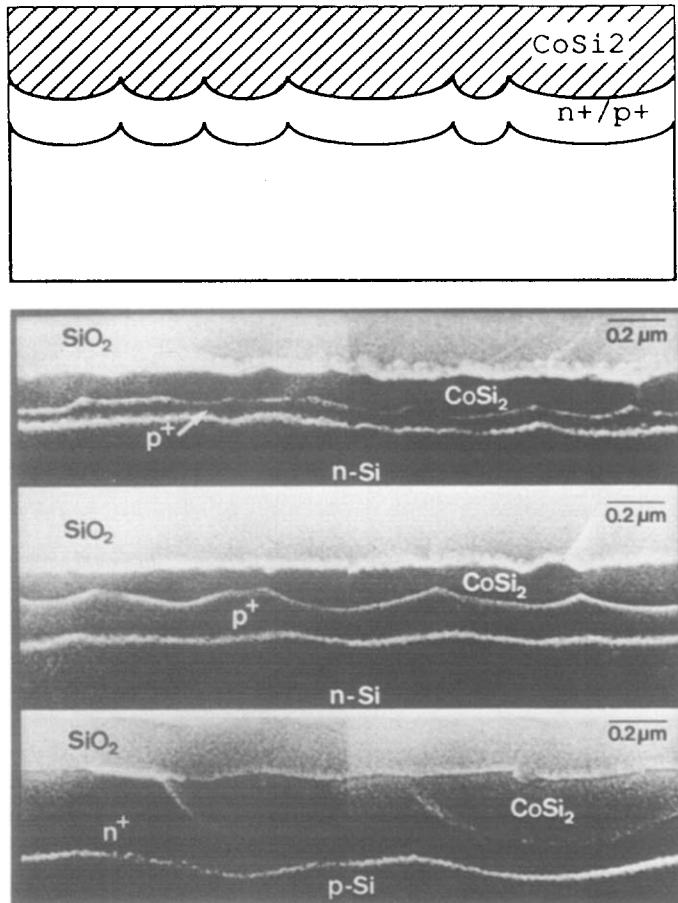


Fig. 89. Schematic (a) and SEM cross-sections ((b)–(d)) of a $CoSi_2$ diffusion source with different doping species and annealing conditions: (b) B, 900 °C, 30 min; (c) B, 1050 °C, 30 s; (d) As, 1100 °C, 60 s. The preparation delineates the diffusion front at a concentration of about $5 \times 10^{18} \text{ cm}^{-3}$.

$CoSi_2$, which takes typically 1 h at 720 °C for TEOS deposition, a redistribution of the as-implanted profile occurs within the silicide [230,250]. The interface with the capping layer also plays an active role during further heat treatments. In Fig. 91, undensified and densified TEOS capping layers are compared. The interface between the capping layer and the silicide is a sink for the dopants. This fact might explain why a different diffusion profile is obtained for different capping layers.

From the discussion in Section 2.3 it is clear that $TiSi_2$ is not a good diffusion source for dopants, owing to the metal-dopant interaction. Although it is not a problem to make low leakage diodes with outdiffusion of dopants from $TiSi_2$ [251–253], the main problem is the contact resistance. Contact resistance measurements are summarized in Figs. 92(a) and (b) for B and As diffusion from $TiSi_2$ and $CoSi_2$. The contact resistance was measured with a Kelvin structure, as discussed in Section 3.4.1, using slight predoping to connect the outer terminals of the bridge structure [245,248,249]. The starting dopant concentration in the reference samples was $3 \times 10^{19} \text{ cm}^{-3}$. Diffusion from $TiSi_2$ yields contact resistances which increase with the outdiffusion temperature and eventually exceed the reference value. The $CoSi_2$ contact resistances display lower values with higher temperatures, confirming the diffusion of dopants and the increase of the interface doping level. The slight increase

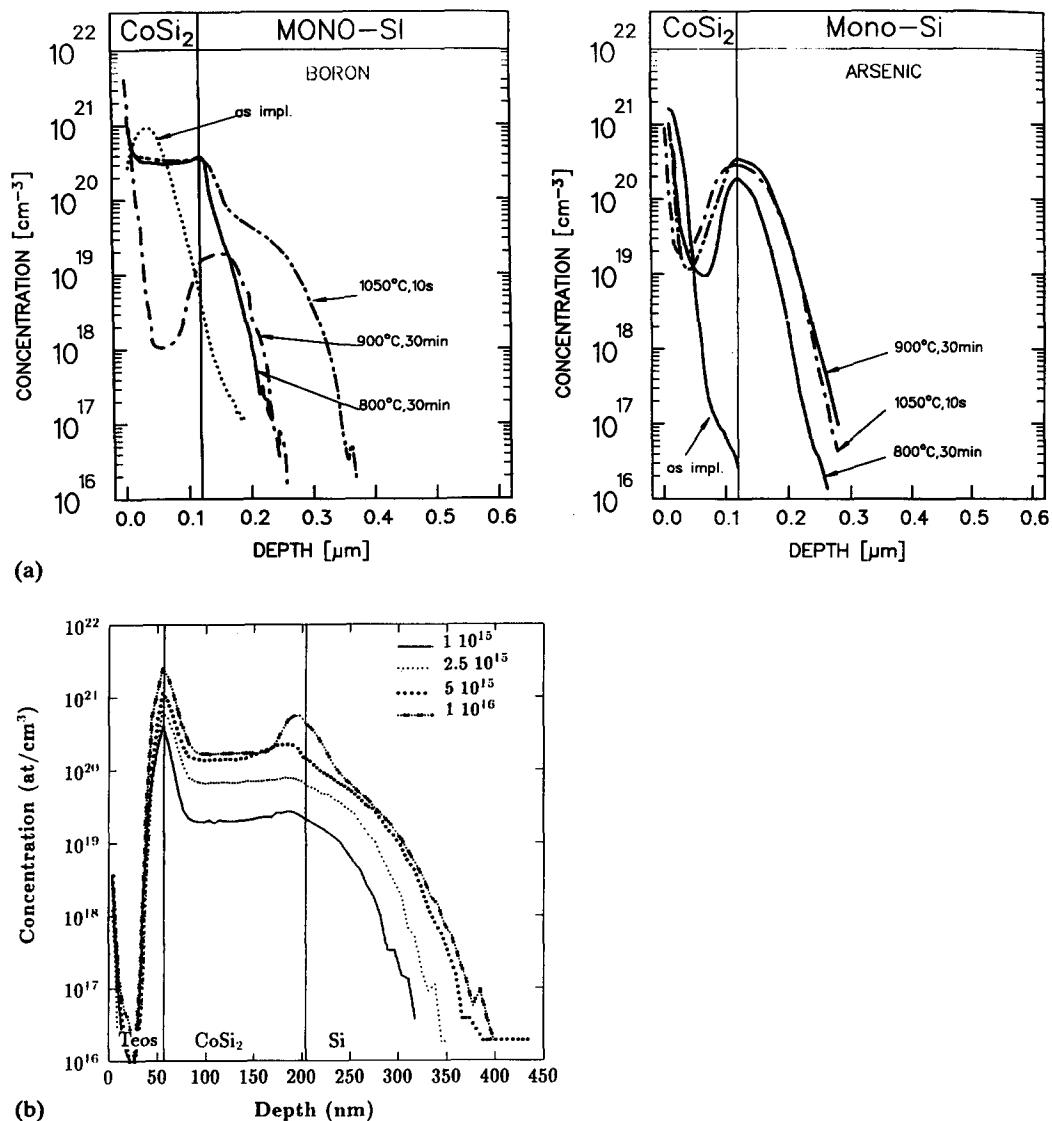


Fig. 90. (a) Profiles of the B and As redistribution in polycrystalline $CoSi_2$ after different diffusion steps; (b) for different B implantation doses.

of the contact resistance in the case of B diffusion with furnace anneal ($900^\circ\text{C}, 30\text{ min}$) from $CoSi_2$ is attributed to the segregation of B at the $CoSi_2/SiO_2$ interface.

In an attempt to limit the diffusion depth from the silicide, the diffusion temperature was varied. Figure 93(a) shows SIMS profiles for B diffused from implanted $CoSi_2$ for 30 s. Temperature treatments as low as 900°C were included in the experiment. For the lower temperatures, no diffusion is observed. The doping profiles are so shallow that the measurement is masked by the $CoSi_2/Si$ interface roughness. This is illustrated by the schematic of Fig. 93(b). However, a detailed investigation, using epitaxial silicides as a diffusion source [250], indicates that even with these low-temperature treatments some diffusion into the Si takes place. The distance between the silicide and the junction was estimated from a detailed comparison of monocrystalline and polycrystalline diffusion profiles, taking into account the roughness of the silicide/Si interface. Figure 94 gives the diffusion depth of B in Si from

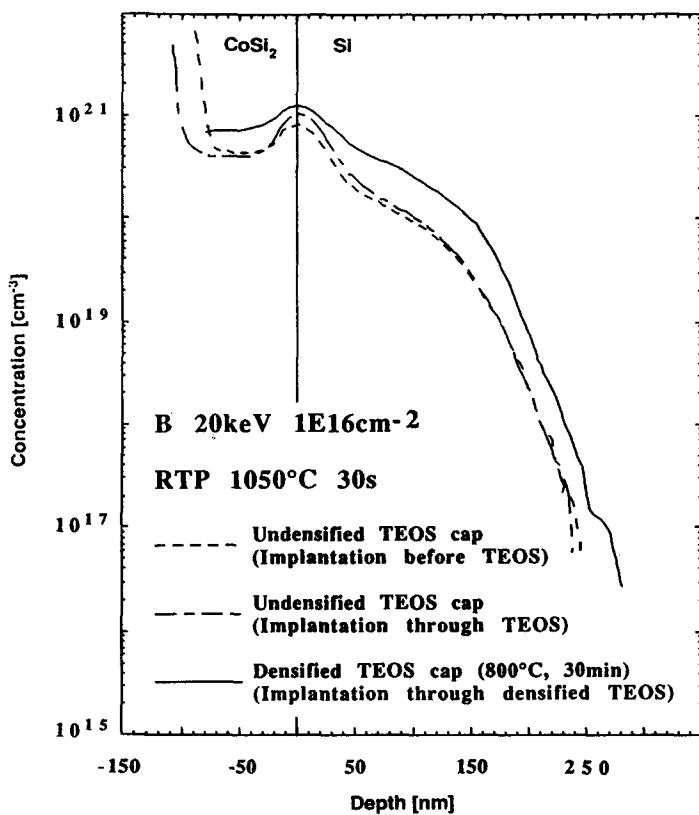


Fig. 91. SIMS profiles after outdiffusion of $1 \times 10^{16} \text{ cm}^{-2}$ B out of a 130 nm thick CoSi_2 layer, using various capping layer conditions.

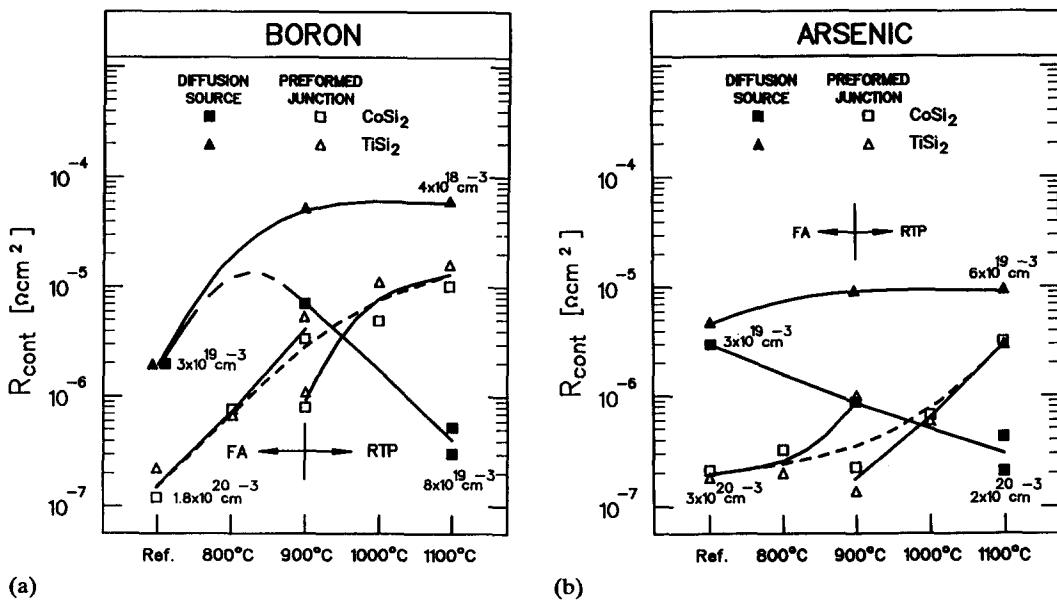


Fig. 92. Specific contact resistances of the silicide/doped Si interface for $TiSi_2$ and $CoSi_2$ as a function of annealing temperature, comparing preformed junctions with outdiffused junctions. The concentration values refer to the dopant concentration within the Si at the silicide/Si interface. (a) B-doped Si; (b) As-doped Si.

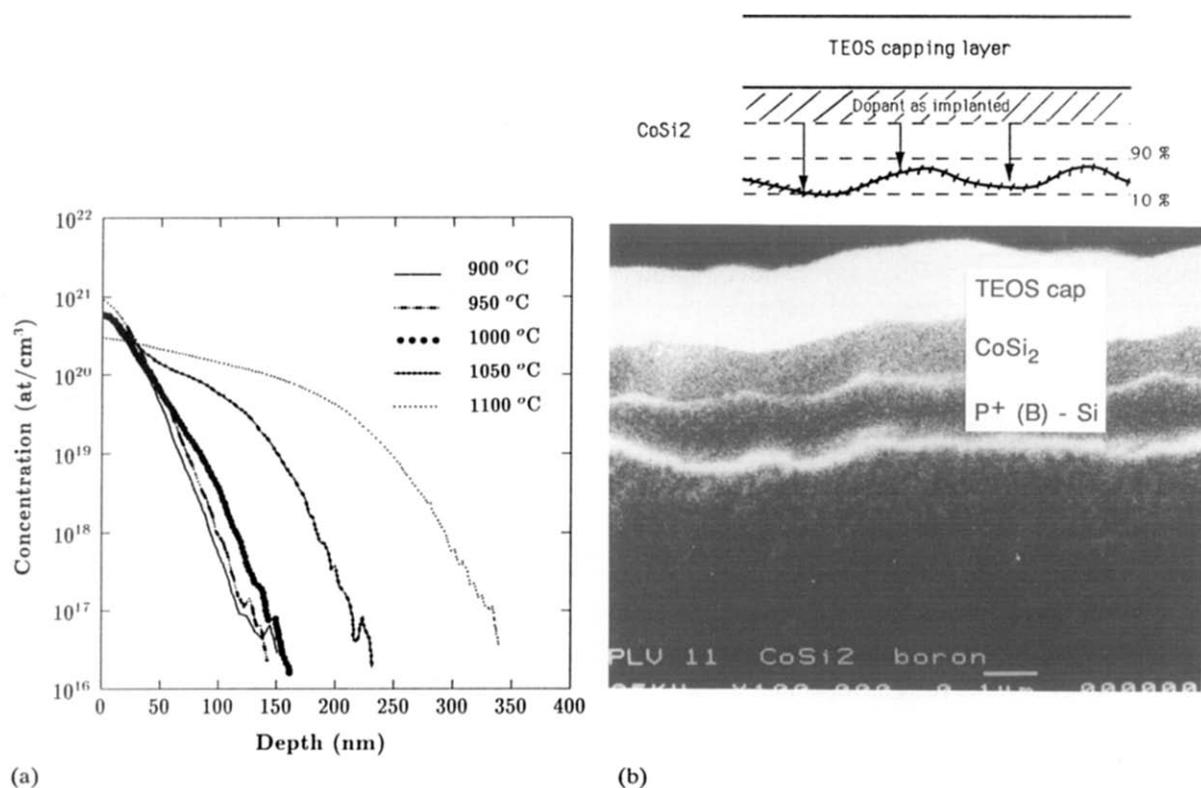


Fig. 93. (a) SIMS profiles after diffusion of $1 \times 10^{16} \text{ cm}^{-2}$ B from a 130 nm thick Co Si_2 layer after various anneals for 30 s. The capping layer during outdiffusion is an undensified TEOS layer. The origin of the depth scale is the silicide/Si interface. (b) Scheme of problem of depth resolution for SIMS because of silicide roughness.

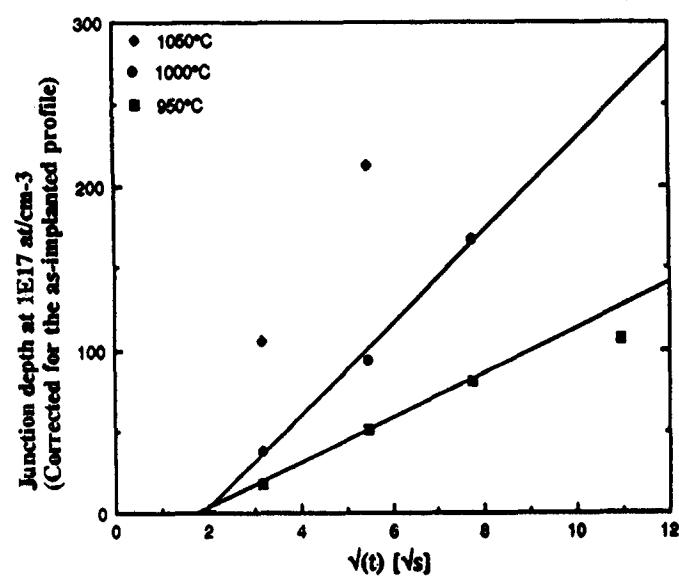


Fig. 94. Diffusion depth of B in Si from an implanted Co Si_2 layer vs. square root of time for various diffusion temperatures.

$CoSi_2$ at various temperatures as a function of the square root of time. Outdiffusion distances of 20 nm were measured for the lowest diffusion temperatures.

Diodes and contact resistance structures were processed using similar outdiffusion conditions as in Fig. 94. The implant was performed through a thin densified TEOS layer. Table 9 gives an overview of the electrical characteristics, namely the diode leakage current density and the specific contact resistance for these junctions. It can be concluded that even for the lowest temperature treatments low diode leakage currents and reasonably low contact resistances are achieved, even though the distance between the silicide/Si interface and the junction can be very small (< 30 nm). This is in contrast to the case of preformed junctions and must be attributed to the conformal diffusion of the dopants with respect to the silicide dopant source. The increase of the contact resistance in the case of B for the higher outdiffusion temperatures might be due to the redistribution of the dopants during the high-temperature treatment.

Technological variations of the two procedures discussed above have been reported [220,239,254,255]. Implantation through the metal can be compared to the process with preformed junctions, and implantation through the silicide has much in common with the outdiffusion process.

3.4.4. Contacting technologies

For a full insight into the role of the contact resistance and for a comparison of various contact schemes, transmission line models have been applied to evaluate the total series resistance of MOS devices. Scott *et al.* [208] have presented calculations to examine the consequences of silicided source/drain regions in scaled MOS technologies. This model has been confirmed by experimental data [206,256] even down to nanoscale dimensions [257].

Figure 95 shows a contact to a silicided junction in a MOS transistor. The parameters L_1 , L_2 and L_3 are indicated on the figure. They are important to optimize the series resistance of the transistor, as will be discussed below. There are two main contacting schemes, i.e. the strap technology, for which $L_2 = L_3 = 0$ (in practice the metal/silicide contact is on top of a field region) and the regular contact, for which L_2 and L_3 do not equal 0. From a design point of view the strap technology is more advantageous than the regular contact, since the contact can be shifted on top of the field region, allowing smaller source and drain areas. There are, however, implications of the contacting scheme for the series resistance of the MOS device.

TABLE 9

Leakage current and specific contact resistance for samples with B and As outdiffusion from $CoSi_2$. The outdiffusion conditions were varied from 900 to 1050 °C

Boron		Arsenic	
Leakage current density (nA cm ⁻²)	Specific contact resistance ($\mu\Omega$ cm ²)	Leakage current density (nA cm ⁻²)	Specific contact resistance ($\mu\Omega$ cm ²)
900 °C 30 s	0.9	0.92	—
950 °C 30 s	1.47	1.16	—
1000 °C 10 s	0.67	4.03	2.8
1050 °C 10 s	0.90	11.8	2.5

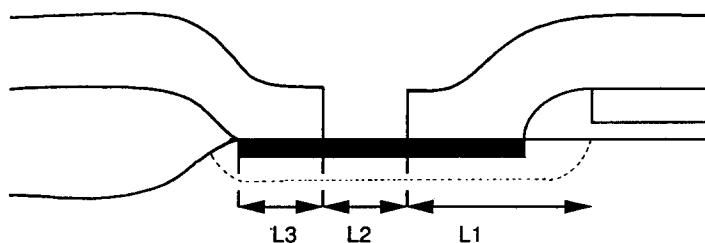


Fig. 95. Scheme of a silicided contact defining the parameters L_1 , L_2 and L_3 .

Figure 96(a) shows the evolution of the gate-independent part of the source/drain series resistance, as calculated with a transmission line model, vs. the length of the silicided region (L_1 in Fig. 95) for a strap technology ($L_2=L_3=0$) [209]. The silicide sheet resistance was $5 \Omega \text{ sq}^{-1}$, whereas the diffusion sheet resistance was $100 \Omega \text{ sq}^{-1}$. The contact resistance between silicide and doped Si was varied as indicated from $5 \Omega \mu\text{m}^2$ to $500 \Omega \mu\text{m}^2$. As the length of the silicided region becomes small, the series resistance increases quite abruptly due to crowding effects, depending on the specific contact resistance. For a realistic case of a specific contact resistance of $50 \Omega \mu\text{m}^2$, the increase in series resistance starts to occur at a silicided length of about $0.5 \mu\text{m}$. For a normal contact technology, with $L_2=L_3=0.5 \mu\text{m}$, and the same values for the silicide and diffusion sheet resistance, the series resistance is about a factor of 2 smaller than in the strap technology. Moreover, a much smaller dependence is observed (Fig. 96(b)) on the spacing between the contact and the spacer edge. Hence this technology will be much less sensitive to lithographic misalignment tolerances.

3.5. Silicided gates and runners

3.5.1. Thermal stability of narrow runners

Many aspects of the silicidation of laterally confined areas have been treated in Section 3.3. The process window for silicidation of laterally confined poly-Si runners is narrower than that of laterally confined mono-Si areas. The higher limit of the process window is shifted downwards, owing to the lower thermal stability of the silicide/poly-Si stack as compared with the silicide/mono-Si stack. In addition to the silicide formation, the thermal stability of narrow silicided lines is an important issue, since after silicidation the process wafers are subjected to several high-temperature treatments. It is, therefore, important to define what thermal budget the silicided line can withstand.

The stability of narrow polycide lines has been studied for the case of $TiSi_2$ /poly-Si using linewidths ranging from 0.5 to $1.0 \mu\text{m}$. The thermal stability was determined electrically by measuring the resistance of the lines and then comparing with sheet resistance measurements of larger areas. For more details about the measurement technique we refer to refs. 224–226. Figure 97 illustrates the effect of additional heat treatments on the distribution of apparent linewidths for undoped poly-Si wafers. The Ti -silicide thickness was about 85 nm for this case. Two effects can be distinguished. Firstly, the average sheet resistance of narrow lines is slightly higher than that of the large areas (resulting in a smaller measured apparent linewidth). Secondly, failures occur and result in extremely high sheet resistances, which points to a fraction of broken lines. The latter increases for narrower lines. Thus, in addition to the smaller process window for Ti -silicide formation on narrower lines, the thermal stability of those lines is worse. The percentage of the lines that failed after heat treatment for 0.5 h for temperatures ranging from 800 to 900°C is given in Fig. 98 for undoped and for B-doped poly-Si. The broken lines refer to a silicide thickness of 85 nm , whereas the

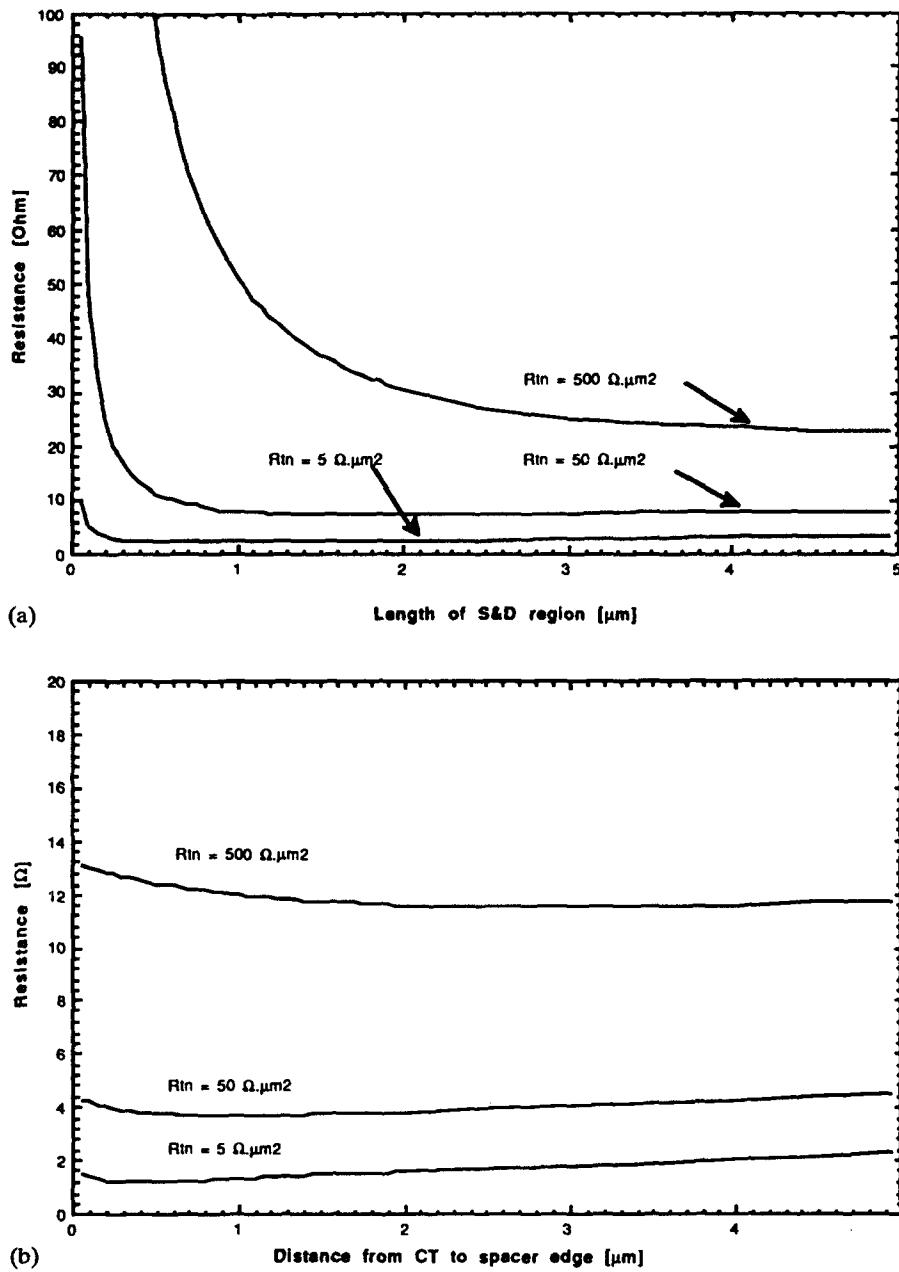


Fig. 96. (a) Resistance of strapped source/drain area as a function of the total source/drain length L_1 ($L_2=L_3=0$); (b) the same with $L_2=L_3=0.5 \mu\text{m}$.

solid line corresponds to a silicide thickness of 95 nm. A comparison of Figs. 98(a) and (b) shows that $TiSi_2$ on B-doped poly-Si exhibits better thermal stability than that on intrinsic poly-Si. The 85 nm thick silicide disintegrates at lower temperatures than the 95 nm thick silicide. The disintegration of $TiSi_2$ on As-doped poly-Si was more severe, since for the same silicidation conditions the silicide on top of As-doped poly-Si is thinner than on undoped or B-doped poly-Si.

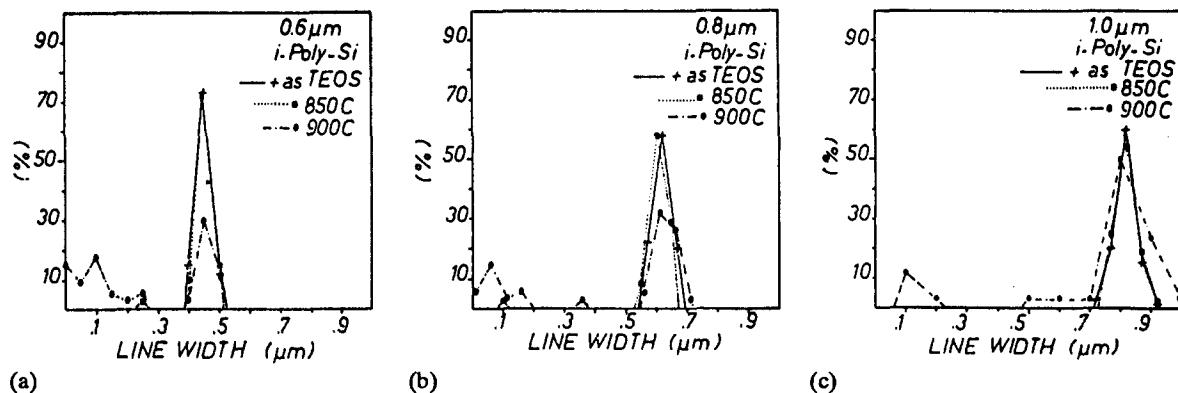


Fig. 97. Linewidth distribution (after TEOS deposition, annealing at 850 °C and 900 °C) for $TiSi_2$ on undoped poly-Si: (a) nominal linewidth of 0.6 μm ; (b) nominal linewidth of 0.8 μm ; (c) nominal linewidth of 1.0 μm .

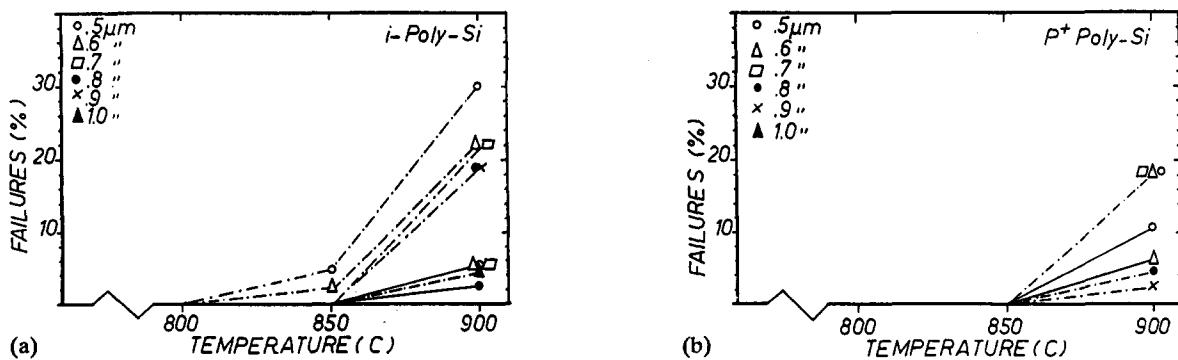


Fig. 98. Number of failure sites of 80 μm long runners with various linewidths as function of annealing temperature: (---) wafers silicided at 680 °C; (—) wafers silicided at 730 °C. The deposited Ti thickness was 60 nm (a) on undoped Si; (b) on Si doped with $2 \times 10^{15} \text{ cm}^{-2}$ B.

Inspection of the silicide/Si interface with SEM reveals the presence of Si precipitates in the narrow lines but not on the larger areas (Fig. 99). It is believed that these Si precipitate chains are responsible for the increase in sheet resistance of the narrow lines. The size of the Si precipitates increases with anneal temperature until they lead locally to a complete electrical isolation of the line.

Similar experiments were carried out with $CoSi_2$ in order to evaluate the thermal stability of the $CoSi_2$ /poly-Si stack [210,258]. Figure 100(a) presents the yield of narrow $CoSi_2$ /poly-Si runners on undoped, B-doped and As-doped poly-Si vs. printed linewidth. The thermal treatment was 800 °C for 30 min and the silicide thickness was 140 nm. The doping dependence of the thermal stability of $CoSi_2$ /poly runners is opposite to that for $TiSi_2$. Even though no linewidth dependence has been found in the formation of $CoSi_2$ on laterally confined areas, the thermal stability of all the lines is worse than that of large areas [259,260]. The electrical results of Van der Pauw structures ($80 \mu m \times 80 \mu m$) showed higher yield values on the same wafers. Interestingly enough, the yield of the silicide runners can be improved by performing an amorphizing implant prior to Co sputtering and silicidation. This is demonstrated in Fig. 100(b). The yield increases from 10–20% to 80%, irrespective of the linewidth considered.

For both Ti silicide and Co silicide, the thermal stability is believed to be determined to a large extent by the grain size of the silicide. Since the grain size of $TiSi_2$ is larger

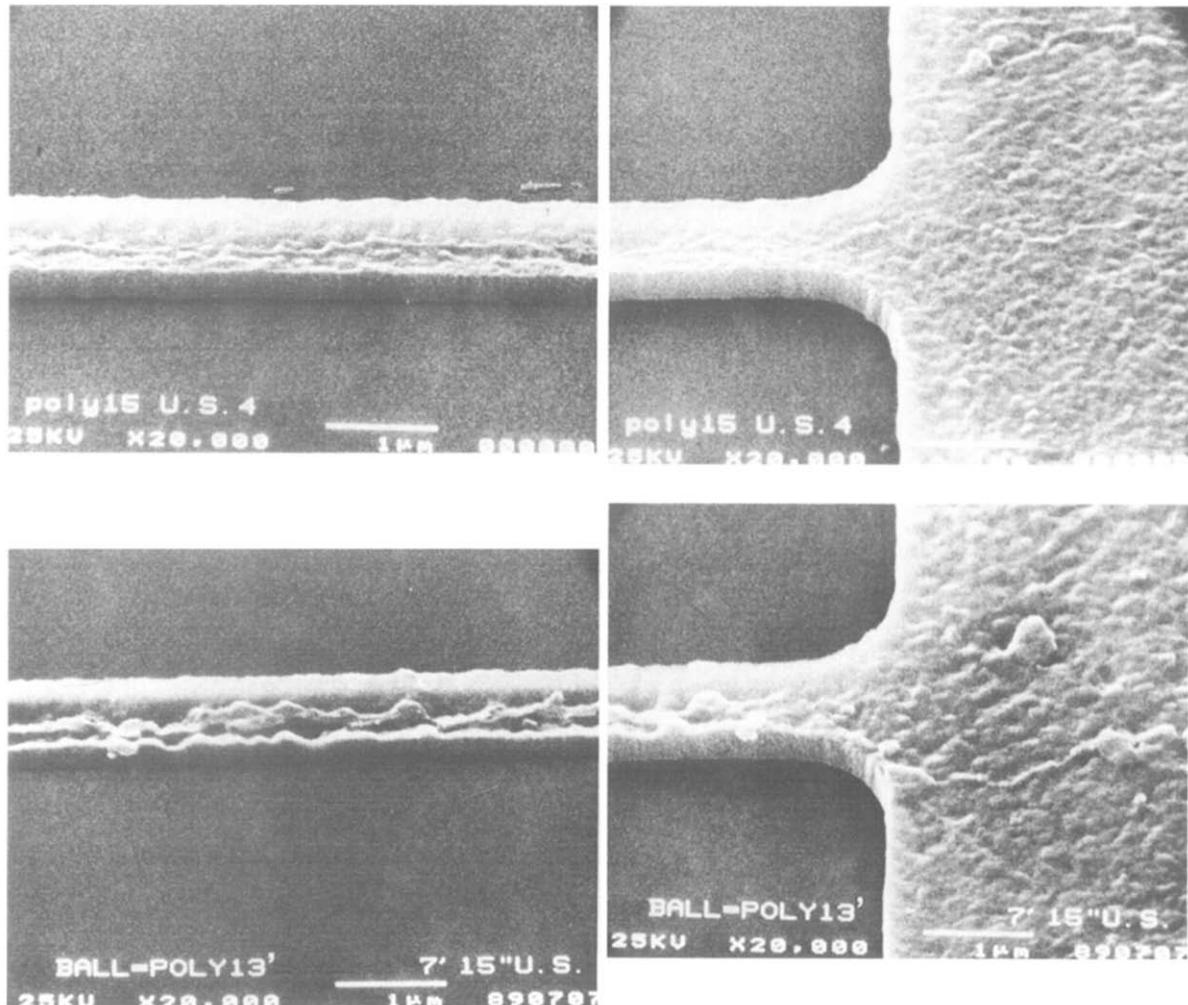


Fig. 99. Plan view SEM micrograph of the lines after removing the $TiSi_2$ and annealed at 850 °C and 950 °C.

than of $CoSi_2$, it is not surprising that a stronger linewidth dependence is found for $TiSi_2$. More experiments are under way to clarify in detail the link between thermal stability and silicide grain size on narrow runners.

3.5.2. Effect on gate quality

To our knowledge, no detailed systematic studies have been published about the effect of silicidation on gate quality. In general, no significant degradation has been observed, provided that the silicidation process is carried out in a reliable way. Recently, Gambino *et al.* [261] studied the extreme case in which the $TiSi_2$ and the $CoSi_2$ reach the gate oxide itself. This might happen at local spots if the thermal treatment after silicidation is too high. In this extreme case, low breakdown voltages have been observed for $TiSi_2$, which has been attributed to thinning of the SiO_2 . In the case of $CoSi_2$ for similar conditions, high interface state densities have been observed. They were attributed to the RTP process rather than to the silicidation itself.

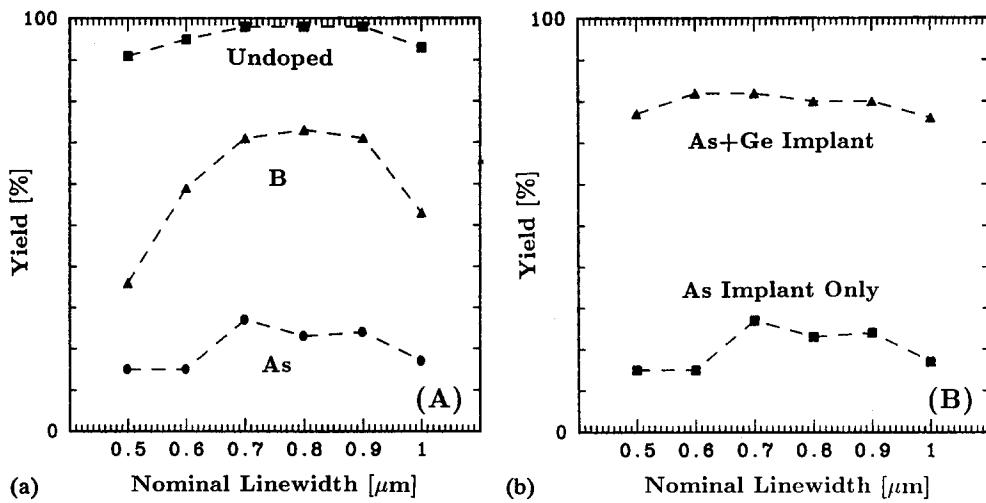


Fig. 100. (a) Yield of $CoSi_2$ on poly-Si lines after an anneal of 30 min at 800 °C for three different poly-Si doping conditions; (b) same as (a) for As-doped poly-Si with an addition Ge amorphizing implant before Co deposition.

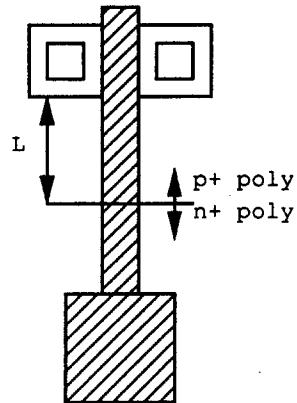


Fig. 101. Layout of test structure.

3.5.3. Lateral diffusion of dopants using n^+ and p^+ poly

In submicron CMOS technologies, the use of dual type poly, i.e. n^+ poly for nMOS and p^+ poly for pMOS is unavoidable in order to maintain good control over the threshold voltage V_T for both types of transistor. In Section 2.3.4 we discussed the diffusion of dopants in polycrystalline silicides, indicating that because of grain boundary diffusion the diffusion lengths are very long. Since both the n^+ -doped and p^+ -doped poly are contacted by the same silicide, the influence of lateral dopant diffusion needs to be considered carefully and can put constraints on the minimum design rule for spacing of two different types of transistor [138,262].

Therefore a special test structure was designed to estimate the effect of an n^+ -doped poly runner on a pMOS transistor for various spacing and similarly for a p^+ doped poly runner on an nMOS transistor (Fig. 101). The spacings were 24, 20, 16, 12, 8 and 4 μm . The poly-Si was doped with 2×10^{15} As cm $^{-2}$ for the n-type and 4×10^{15} B cm $^{-2}$ for the p-type. The silicide thickness was 75 nm for $TiSi_2$ and 50 nm for $CoSi_2$. The thermal

treatment after silicide formation was 800 °C for 30 min. No shift in V_T was observed under the actual conditions for $TiSi_2$ nor for $CoSi_2$ [263].

Similar results have been reported by Chu *et al.* [262]. Figure 102 shows the minimal spacing distance between nMOS and pMOS transistors for several experimental cases. The criterion has been fixed at an allowable shift of the threshold voltage of 100 mV. As expected, the thermal budget after silicidation needs to be kept minimal, with $CoSi_2$ and $TiSi_2$ behaving similarly on this issue. As a comparison the effect of a WSi_2 polycide structure is given in the plot as well. It is clear that WSi_2 has a larger impact on the threshold voltage, due to a higher lateral diffusion, and therefore becomes unacceptable in processes using dual type of poly.

3.6. Lateral silicide growth

The lateral silicidation of a silicide over an oxide window is a result of the large Si diffusion [264]. Since during both Ti and Co silicidation Si is the main moving species, at least at one stage of the reaction, lateral growth of the silicide is a concern. In the case of Ti, the lateral growth of the silicide is suppressed by performing the reaction in an N_2 ambient [51,86]. This is attributed to the blocking of the Ti grain boundaries by nitrogen. The lateral diffusion of Si can also be limited by deposition of a TiN overlayer on the Ti before the reaction [265,266]. In this case it is believed that the diffusion of Si, which mainly takes place through the surface, is blocked. A similar explanation also holds for the silicidation of Co from a Co/TiN stack [267].

In general, ion mixing improves lateral confinement [268,269]. This has been attributed to the removal of interfacial barriers during silicidation and the build-up of impurities at

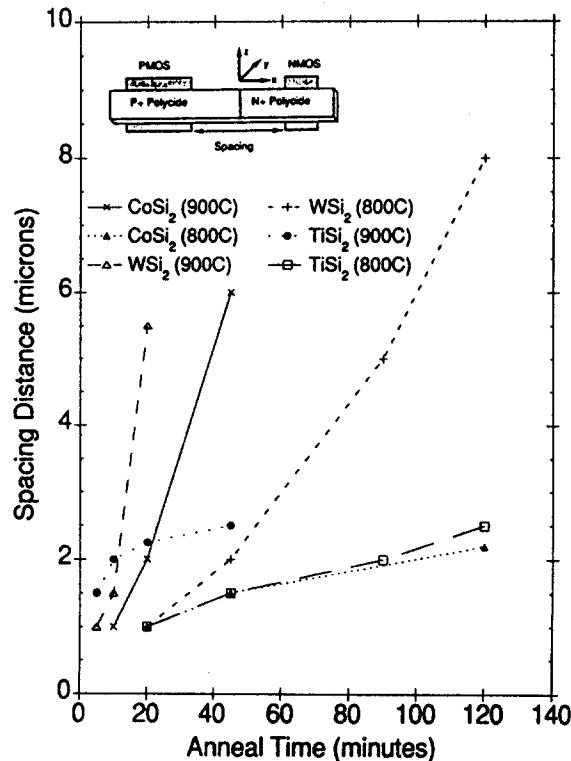


Fig. 102. Minimum spacing required for a maximum ΔV_T of 100 mV for a pMOS:nMOS gate ratio of 2:1 (after ref. 262).

the silicide/metal reaction front to prevent extended lateral diffusion of Si. In more recent experiments, the silicidation on amorphized Si has led to a distinct improvement of the lateral confinement of the silicidation process. This could be due to the reduced nucleation temperature of the silicide. More experiments are needed to clarify the mechanism of reduced lateral growth under the various experimental conditions [258,270].

In a typical MOS device, lateral overgrowth will lead to a short circuit of source/drain and gate, as depicted in Fig. 103. Bridging has been identified as one of the yield killing factors for self-aligned silicidation. Tight control of the lateral silicidation is therefore mandatory. A ULSI circuit consists of many metres of polysilicon/active area perimeter [271]. Therefore, a bridging monitor was designed with a very long gate/source-drain perimeter. The bridging monitor is depicted in Fig. 104. Three structures are included in the design. Structure I consists of an outside corner of polysilicon, structure II of an inside corner of polysilicon and structure III models the configuration for polysilicon in a typical MOS structure. The length of the poly-Si/active area perimeter is defined as the effective length of each structure. The overall effective structure length on each wafer is over 200 m. The yield of structure I and II is systematically lower than for structure II, indicating that the silicidation technology is more critical when inside or outside corners are present in the polysilicon runners. The silicidation process, and as such also the lateral overgrowth,

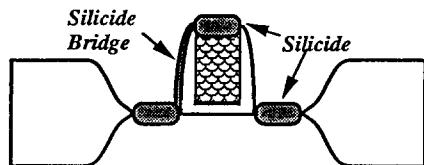


Fig. 103. Schematic of source/gate shortage, called bridging, in a self-aligned silicidation process.

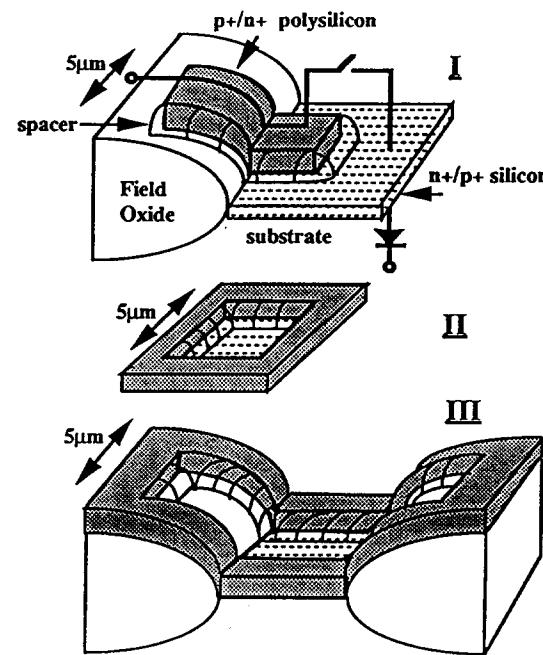


Fig. 104. Test structure for the evaluation of bridging.

is influenced by the silicidation temperature, the efficiency of the chemical etch of unreacted metal, the spacer width etc.

Figure 105 shows the dependence of the bridging on the temperature during the first silicidation step. The second silicidation step was kept constant i.e. 850 °C, 30 s for $TiSi_2$ and 700 °C, 30 s for $CoSi_2$. In the case of Ti silicidation, an increasing yield is obtained for a lower first temperature step. However, the associated increase in sheet resistance is significant. Similar results are obtained for $CoSi_2$, in agreement with previous reports [271,272], but the effect on the sheet resistance is less important. Therefore the processing window for high yield and low sheet resistance might be larger than for $TiSi_2$. By further optimizing the temperature during the first silicidation step, a further increase in yield can be achieved. Schreutelkamp *et al.* [273] demonstrate that accurate temperature control at temperatures below 500 °C completely suppresses the lateral growth over the spacer, maintaining low sheet resistance of the silicided areas.

Another important parameter for the bridging yield is the spacer width. Figure 106 shows the yield as a function of spacer width for $CoSi_2$. A similar dependence of yield versus spacer width has been obtained for $TiSi_2$. It should be noted that the actual spacer width needed for a good process is dependent on the full silicidation process, since the yield is sensitive to the process optimization. The trend, however, remains the same for each process. Sung and Lu [274] reported a good yield with $TiSi_2$ using ion mixing and a spacer as thin as 50 nm.

In addition to the classical silicidation parameters, the characteristics of the Si surface after spacer etch and before metal deposition influence the lateral silicidation. As already discussed in Section 3.2.3, the Si is mainly contaminated with C–F compounds, which are very difficult to remove. The cleaning procedure after spacer etch involves a polymer etch in an O₂ plasma, a short dry etch to remove a few nm of Si, a sacrificial SiO₂ growth and an etch of the sacrificial SiO₂. In our experiments, dramatic yield decreases were observed if the sacrificial oxide was etched away dry. HF removal of the SiO₂ is much more successful, but is more critical since the spacer is attacked by the same treatment.

Optimization of both the spacer etch, the cleaning procedure and the silicidation process has resulted in almost 100% yield both for $TiSi_2$ and for $CoSi_2$ on the three structures.

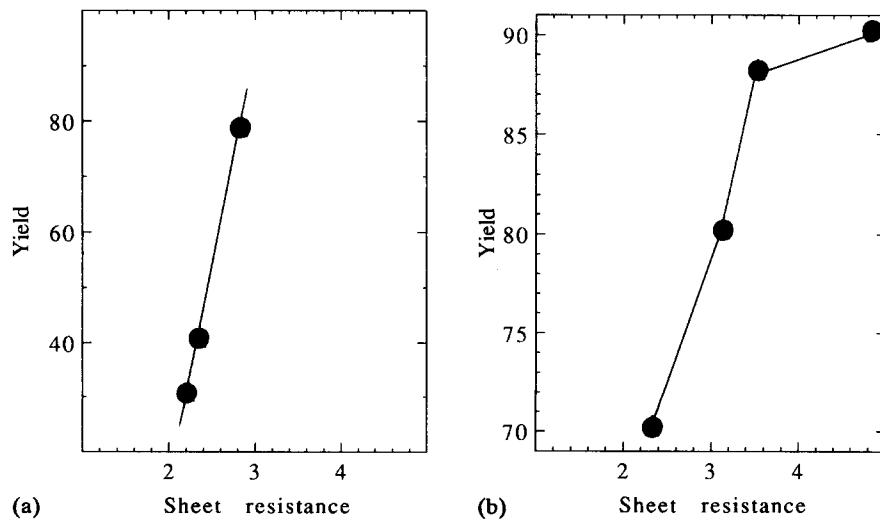


Fig. 105. Yield vs. sheet resistance (a) for $CoSi_2$ starting from 25 nm Co and (b) for $TiSi_2$ starting from 50 nm Ti.

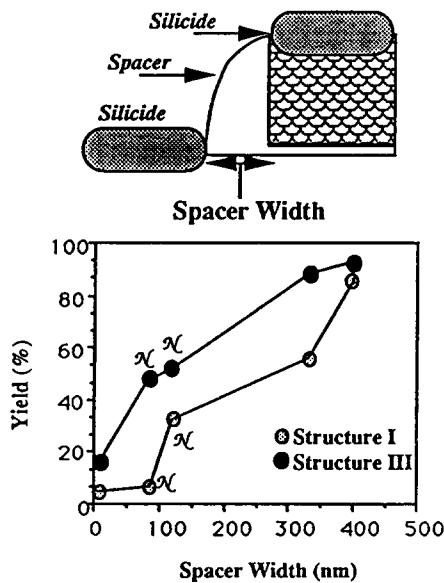


Fig. 106. Yield variation vs. spacer width for a $TiSi_2$ process.

3.7. Rapid thermal processing

The switch from classical furnace processing towards RTP has been advocated in the case of silicidation because RTP offers significant advantages. The reactivity of the metals with the ambient requires good control of the latter. This is more easily achieved in an RTP system, which allows entry of the cold wafer. The wafer is heated after purging the tube with N_2 in order to minimize O contamination. The importance of the silicidation ambient has already been discussed in Section 2.2.5.

The implementation of RTP for submicron device fabrication, however, puts very stringent requirements on temperature control during processing and temperature uniformity over the wafer. This has recently led to systems with multizone heating and guard rings to compensate for radiation non-uniformities within the system [275–280]. Two process-related problems need still to be tackled, i.e. the temperature non-uniformity due to patterns on the wafer and the *in situ* temperature measurement.

3.7.1. Pattern-induced temperature non-uniformity

Since the heat transfer in an RTP system is based on radiation, non-uniform absorption and emission occurs if different parts of the wafer are covered with different layers [280,281]. For large-scale patterns (of the order of 1 cm) thermal conduction in the Si will not be able to smooth non-uniform absorption/emission, resulting in a temperature non-uniformity. This has been investigated for annealing and oxidation [280]. During self-aligned silicidation, optical properties vary during the process [282]. Starting with a uniform metal film which covers the wafer, the situation changes as the properties of the silicide formed vary from those of the unreacted metal on adjacent oxide areas. Since the thermal diffusion length is larger at lower temperatures, perturbations in temperature uniformity extend over much larger distances. The effect of pattern-induced temperature non-uniformities can be evaluated by using a test structure, as depicted in Fig. 107. The front of the test wafer simulates the actual structure used in self-aligned silicidation, whereas the metal on the back will serve as a temperature monitor. The temperature non-uniformity is determined by measuring

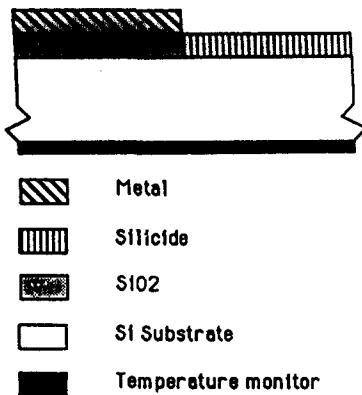


Fig. 107. Test structure for temperature uniformity measurements. Silicidation at the back side of the wafer serves as a temperature monitor.

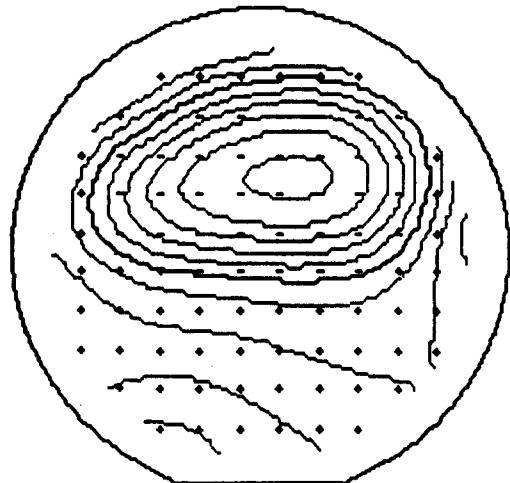


Fig. 108. Sheet resistance variation of the silicided back side of the wafer using $TiSi_2$. The sheet resistance pattern corresponds to the oxide pattern on the front side. The measured non-uniformity is about 25 °C.

sheet resistance variations at the back side. The sheet resistance data for Ti in Fig. 108 clearly show the fingerprint of the pattern on the front side of the wafer. After calibration, the temperature difference was determined to be more than 20 °C, extending laterally over 20 mm. This is in agreement with calculations of the diffusion length of lateral heat diffusion. Similar results are obtained for Co silicidation.

The impact of this temperature non-uniformity during the silicidation reaction is not in the first place important for the thickness of the silicide, but, as discussed in Section 3.6, the influence on bridging can be significant if the process window is tight.

3.7.2. Temperature control

The standard technique for temperature measurement during RTP is pyrometry. However, for the low silicidation temperatures one often relies on thermocouple measurements. The latter can only be used for calibration on a test wafer and do not allow single wafer control.

Hence there is a strong interest to extend the pyrometer measurements to low temperatures. Two problems arise. Firstly, the emissivity of the wafer changes from wafer to wafer [283,284] and secondly, the interference of lamp radiation with the radiation emitted by the wafer is rather large. A quick calculation of the error of the temperature measurement vs. emissivity reveals that the emissivity must be known within 1%. The effective emissivity has been introduced [285,286] to take into account both the emissivity and interference with the lamp radiation. The effective emissivity of the wafer is a complex function of wafer temperature, wafer doping, surface layers, back-side roughness, chamber reflectivity and geometrical setup of the pyrometer. Its *in situ* measurement allows accurate control of the temperature.

The measurement of the effective emissivity has been based on a lamp modulation method [41]. The measurement of reflectivity and transmittance of a wafer becomes possible, since modulation allows a distinction between radiation coming from the lamps and radiation coming from the wafer.

An extended discussion of RTP temperature control and uniformity is beyond the scope of this paper. Nevertheless, it should be noted that a good optical design of RTP systems and emissivity-independent temperature control are necessary for high-yield silicidation processes.

4. Conclusions

Through extensive research on metal/Si reaction, silicides have become a mature material for implementation in device fabrication. Fundamental knowledge of reaction mechanisms and interactions with doped Si, SiO_2 or metals has enabled a successful application of silicides in deep submicron technologies.

In this paper, the characteristics of $TiSi_2$ and $CoSi_2$ have been reviewed. Up to now, $TiSi_2$ has been applied in industrial processes more frequently, although limitations have been encountered for implementation in deep submicron processes. In this area it has been shown that $CoSi_2$ has clear advantages over $TiSi_2$ and becomes a serious candidate to replace $TiSi_2$ for a number of applications.

The silicidation process controllability will benefit a lot from new cleaning technologies, better control of impurities during metal deposition and subsequent thermal processing. The introduction of cluster processes, which allow cleaning, metal deposition and silicidation without exposure of the wafer to air, might introduce distinct improvements in this area.

We have discussed how silicidation influences device characteristics. It is expected that silicided junctions become one of the technology drivers for future processes. The mutual link between junction and silicide formation will become even stronger, the main goals being to keep the total series resistance of the devices as low as possible and to minimize the Si consumption.

A major issue for the further development of silicided junctions will, however, be the evolution of the back-end process. Since the thermal stability of ultra-thin silicides becomes questionable, technological decisions will depend strongly on the thermal budget which the silicide can withstand. Therefore, reducing temperature treatments in the process steps after silicidation will be a major concern.

Even though there are still plenty of challenges from the materials point of view, there is no doubt that silicidation will be a key element in the fabrication of future ICs.

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