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Design Considerations for A Low-Noise CMOS Image Sensor

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ABSTRACT

This paper reports a Low-Noise CMOS Image Sensor. Low-noise operation is achieved owing to the combination of a noise-enhanced pixel, the use of a two-step ADC architecture and the analysis, and the optimization thereof, of the noise contributed by the readout channel. The paper basically gathers the sensor architecture, the ADC converter architecture, the outcome of the noise analysis and some basic characterization data. The general low-noise design framework is discussed in the companion presentation.

1 INTRODUCTION

Among other reasons, the currently witnessed proliferation of solid-state image sensors is driven by the potential of modern CIS technologies to design systems with reduced SWaP (Size, Weight and Power), low cost, large speed and large functional capabilities and flexibility. However, until approximately the mid 90´s, the expansion of CMOS imaging systems was hampered by the lower quality of their compatible photo-sensing devices as compared to CCD counterparts; i.e. images captured by earliest CMOS photo-sensors were not good enough for many industrial applications. In such a scenario CCD was the choice for imaging systems and the potential advantages of CMOS were sort of academic nuances. This drawback was attenuated with the advent of improved CMOS photo-sensors, specifically based on pinned photodiodes, and the subsequent enhancement of the quality of captured images above the feasibility thresholds required for practical applications. Once these thresholds were surpassed CMOS advantages regarding SWaP, production cost, speed and embedded functionality became unbeatable weapons at the CMOS-CCD duel. Actually, CMOS-systems cope todays more than 90% of the market of area imager sensors. CIS assets can be summarized in the following items: i) Cost; ii) Size; iii) Power Consumption; iv) Speed and v) Functional Flexibility [2]-[5].

Major CIS markets call for ever smaller pixel pitch, and ever larger spatial image resolution (number of pixels). Besides the quest of reduced pitch, other prominent CIS challenges include: a) improving the image quality through enhanced readout, signal conditioning and image enhancement circuitry; b) improving the image downloading speed through enhanced communication circuitry and; c) reducing the area, power and cost through on-chip circuit embedding. Besides technology advances, CIS enhancements are in many cases conferred by the on-chip embedded circuitry, starting with the readout channel. This paper presents a readout channel including a non-conventional, two-step analog-to-digital converter and reports a low-noise VGA (640 x 480 pixels) CIS chip based on it – called LoNIS [2] from now on.

2 CHIP ARCHITECTURE

Figure 1 shows the block diagram of LoNIS. It is a complete digital image sensor on a single chip integrating all the necessary elements to acquire images, digitize such images, and to transmit them to an external host via CMOS output ports or low-noise, high-speed LVDS ports. The LoNIS circuitry divides into five sections: Pixel array, Readout and conversion channel, Digital control circuitry, Communication interface, and Auxiliary on-chip blocks. LoNIS is controlled by two internal clocks, which are generated from a single external crystal reference whose frequency is scaled by using a PLL. The nominal reference external frequency is 10MHz.

READOUT CHANNEL FUNCTIONAL DESCRIPTION

Figure 2 shows the functional block diagram of a readout channel. Each readout channel consists of two sample-and-holds (analogue memories) and a two-stage analog-to-digital converter (ADC). The A/D conversion is performed in two steps, which shortens the conversion time with respect to a single stage A/D converter, while keeping the same accuracy

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and almost the same complexity. Following the A/D conversion, data are serialized and finally sent out through the CMOS ports or the LVDS port.

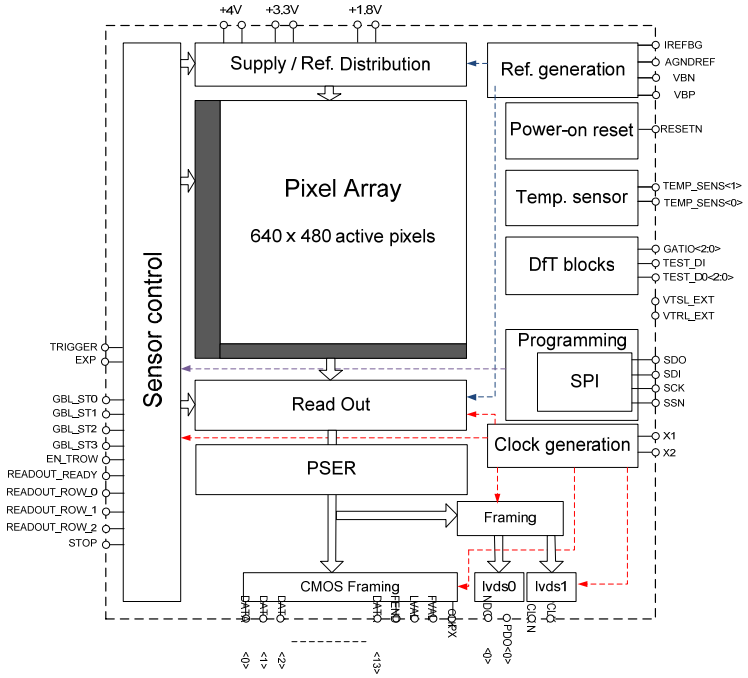

Figure 1. Block diagram of the LoNIS

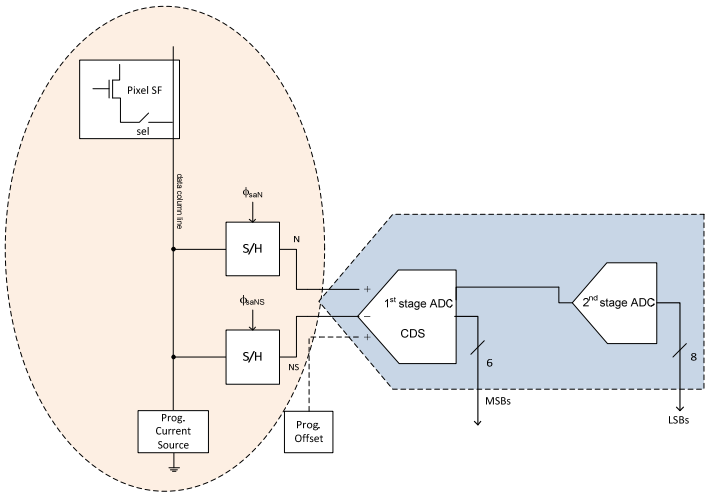

Figure 2. LoNIS readout channel

A the interface between the pixel array and the readout channel data from the array are stored in two analogue memories per pixel: one for the reset value (N) and the other for the signal (S+N). Once the memories are filled, its capacitors are connected to a layer of CDS circuits. The CDS layers cancel all correlated errors between (N) and (S+N). A programmable offset can be added to the first stage of the ADC. The purpose of this "coarse" offset is to avoid loss of codes (due to having negative values at the input of the ADC) and/or significant loss of DR (in case a large dark signal from pixel exhausts a significant portion of the ADC full-scale range). Figure 3 is an exemplary timing diagram showing the exposure and the row-by-row readout sequence. Each time-slot corresponds to a conversion time. Readout and conversion time is the time taken by each readout channel to sample and digitize the pixel signal. Data in line memory stays for one conversion, thus during this conversion time data is read from the pixel and it is fed to the rest of the signal path.

A/D CONVERTER

Analog-to-Digital conversion is performed by two stages following a two-step conversion technique. Figure 4 shows the block diagram of the Analogue-to-Digital (A/D) converter used in LoNIS.

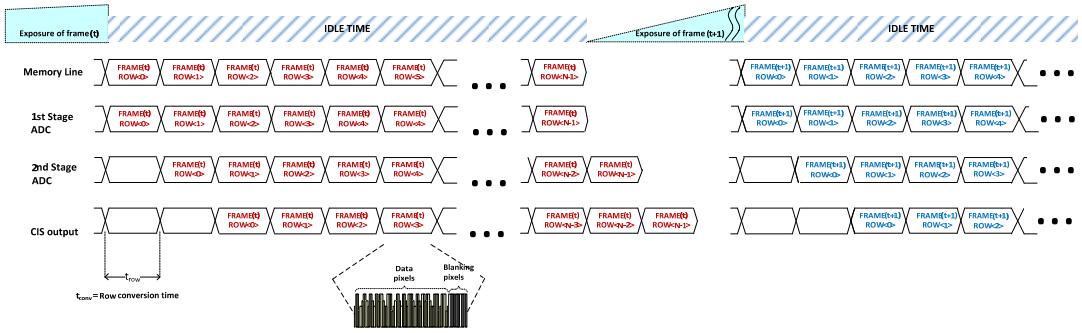

Figure 3. Sensor operation for the exposure and readout of consecutive frames

THE A/D CONVERTER

AD conversion is performed into two-steps. Figure 4 shows a block diagram for the ADC used in LoNIS. The first ADC stage delivers 6 bits, while the second stage delivers 8 bits, resulting in a complete output word of 14 bits.

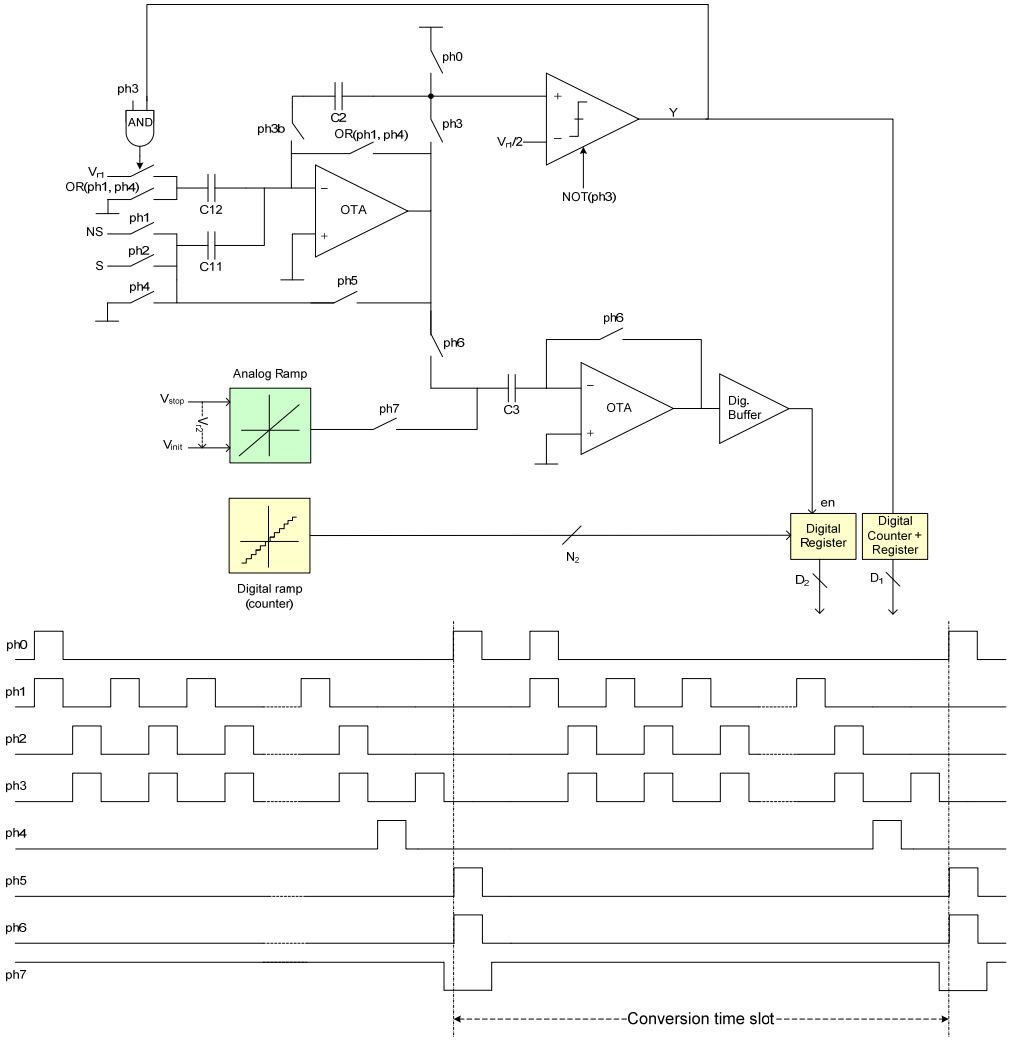

Figure 4. A/D converter block diagram

3 NOISE ANALYSIS: READOUT CHANNEL

Figure 5 shows the main noise contributions of the Readout channel, including three components: i) pixel; ii) line memory circuit; iii) ADC.

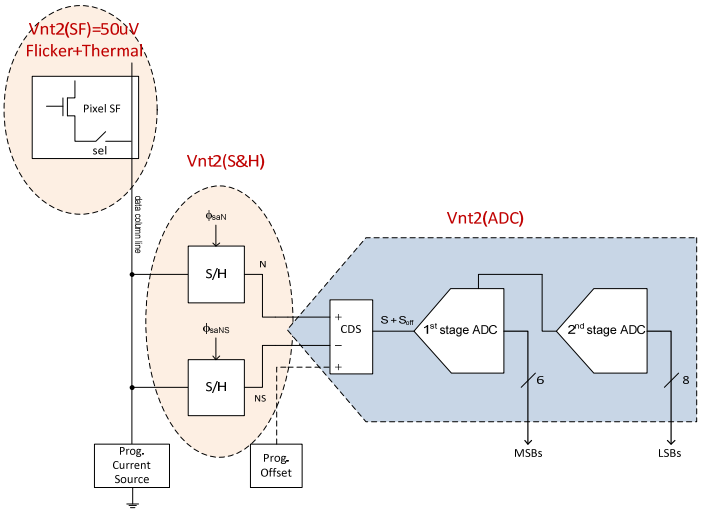

Figure 5. Readout channel noise contributions

LINE MEMORY

The Line Memory noise contribution is one of the most important noise sources of the overall readout channel. Assuming that Rsw<<1/gm so that:

- thermal noise of switches is not dominant compared to thermal noise of OTA;
- settling of switches is not limiting compared to settling of OTA,

the total noise contribution of the Line memories circuitry in case the **offset capacitor is connected** is calculated as:

$$Vntot^2 = \frac{Vnsainn^2 + g^2.Vnsaosn^2 + Vnsains^2 + g^2.Vnsaoss^2}{1^2}$$

$$Vntot^2 = \frac{\alpha kT/Cin + g^2.\alpha kT/Cos + \alpha kT/Cin + g^2.\alpha kT/Cos}{1^2}$$

Where g= Cos/Cin, K is the Boltzamm constant (1.23x10-23 J/K), and T is the temperature in Kelvin (K). The total noise contribution of the Line memories circuitry in case the **offset capacitor is not connected** (current implementation of LoNIS) is calculated as:

$$Vntot^2 = \frac{Vnsainn^2 + Vnsains^2}{1^2}$$

$$Vntot^2 = \frac{\alpha kT/Cin + \alpha kT/Cin}{1^2}$$

The estimated and simulated values of Line Memory noise contribution are shown in Table 1.

Table 1. Line Memory noise estimation- Cos connected

				estimated	simulated						
Cin	4	pF	alpha	4.00	1.60	Vnsainn	44.8	uVrms	Vntot (lm)	63.3	uVrms
k	1.381E-23										
T	90	C	alpha	4.00	1.60	Vnsains	44.8	uVrms	kT/Cin	35.4	uVrms
kT	5.0151E-21										

1ST STAGE A/D CONVERTER

It is evaluated by accumulating noise errors at the different circuit states. By so doing and assuming R<<1/gm so that:

- Thermal noise of switches is not dominant compared to thermal noise of OTA.
- Settling of switches is not limiting compared to settling of OTA.

The total noise contribution of the 1st stage A/D is given by:

$$Vntot^2 = \frac{\left(g1^2.Vn0a^2 + g2^2.Vn0b^2 + Vn0c^2 + Vn1^2\right)}{g1^2} + (G-1)\frac{\left(g1^2.Vn2a^2 + g2^2.Vn2b^2 + Vn1^2\right)}{g1^2} + \frac{\left(g2^2.Vn3b^2 + Vn4^2\right)}{g1^2} + \left(Vn3a^2 + Vn5^2\right)}{G^2}$$

$$Vntot^2 = \frac{\left(g1^2.\alpha kT/C_{11} + g2^2.\alpha kT/C_{12} + \alpha kT/C_2 + \alpha kT/C_2\right)}{g1^2} + (G-1)\frac{\left(g1^2.\alpha kT/C_{11} + g2^2.\alpha kT/C_{12} + \alpha kT/C_2\right)}{g1^2} + \frac{\left(g2^2.\alpha kT/C_{12} + \alpha kT/C_2\right)}{g1^2} + \left(\alpha kT/C_{11} + \alpha kT/C_3\right)}{G^2}$$

The estimated and simulated values of Line Memory noise contribution are shown in Table 2.

Table 2. Noise estimation- 1st stage A/D converter

C11	150	fF
C12	150	fF
C2	300	fF
C3	200	fF
g1	0.5	
g2	0.5	
G	64	
k	1.381E-23	
T	90	C
kT	5.0151E-21	

	estimated	simulated
alpha	5.0	1.51
alpha	5.0	1.46
alpha	3.0	1.75
alpha	5.0	2.06
alpha	5.0	1.54
alpha	5.0	1.62
alpha	3.0	1.45
alpha	3.0	1.52
alpha	3.0	2.17
alpha	7.0	5.78

Vn0a	224.7	uVrms
Vn0b	220.9	uVrms
Vn0c	171.0	uVrms
Vn1	185.6	uVrms
Vn2a	226.9	uVrms
Vn2b	232.7	uVrms
Vn3a	220.2	uVrms
Vn3b	225.4	uVrms
Vn4	190.5	uVrms
Vn5	380.7	uVrms

1.Vn0a	224.7	uVrms
(g2/g1).Vn0b	220.9	uVrms
(1/g1).Vn0c	342.1	uVrms
(1/g1).Vn1	371.1	uVrms
1.Vn2a	226.9	uVrms
(g2/g1).Vn2b	232.7	uVrms
1.Vn3a	220.2	uVrms
(g2/g1).Vn3b	225.4	uVrms
(1/g1).Vn4	380.9	uVrms
1.Vn5	380.7	uVrms

Vntot	62.4	uVrms
kT/C11	182.8	uVrms
kT/C12	182.8	uVrms
kT/C2	129.3	uVrms
kT/C3	158.4	uVrms

4 OPTICAL PERFORMANCE RESULTS

SUMMARY OF RESULTS

The optical performance has been measured on 3 devices. A summary of the results at ~33ºC under the operation of rolling shutter, 60fps and PWC trigger is shown in Table 3. Whenever applicable, the symbol or acronym used in EMVA Standard 1288 is displayed for guidance.

Table 3. – Optical performance(1) in rolling-shutter operation

	EMVA 1288 symbol	DUT1	DUT 7	DUT 8	Mean	Std Dev	UNITS
Dynamic Range (LoNIS SoW)	DR	78.05	76.27	79.16	77.83	1.46	dB
Dynamic Range (EMVA)	DR_{1288}	75.03	73.88	76.14	75.02	1.13	dB
Signal-to-Noise Ratio	SNR_{max}	41.00	41.01	40.92	40.98	0.05	dB
Dark-Signal Non-Uniformity	$DSNU_{1288}$	0.51	0.68	0.57	0.587	0.085	e-
Photo-Response Non-Uniformity	PRNU	0.99(2)	0.41	0.43	0.420	0.008	%
Vertical Fixed-Pattern Noise (dark) $VFPN_{dark}$	-	0.003	0.004	0.003	0.003	0.001	%FS
Horizontal Fixed-Pattern Noise (dark) $HFPN_{dark}$	-	0.0013	0.0006	0.0007	0.0009	0.0004	%FS
Temporal Noise (dark)	$\sigma_{y.dark}$	2.04	2.50	1.79	2.11	0.36	DN
Noise-Equivalent Electrons (NEE_e)	-	1.64	2.03	1.43	1.70	0.30	e-
Overall system gain (or conversion gain)	K	1.24	1.23	1.23	1.23	0.01	DN/e
Saturation Level	$\mu_{y.sat}$	15715	15510	15549	15591	108.8	DN
Dark Level	$\mu_{y.dark}$	117	119	116	117	1.4	DN
Saturation capacity	$\mu_{e.sat}$	12579	12513	12547	12546	33	e-
Full-Well Capacity	FWC	13213	13320	13320	13285	62	e-
Linearity Error	LE	0.76	0.70	0.80	0.75	0.05	%
Responsivity (at 550nm)	R	2.6E+6	2.4E+6	2.4E+6	2.5E+6	69.9E+3	DN/(uJ/cm^2)
Fill-Factor x Quantum Efficiency (for averaged K)	η	74.9	71.4	71.4	72.57	2.02	%
Junction Temperature	T	33.5	33.4	33.3	33.4	0.1	degC

(1) Results after HFPN and VFPN calibration & correction and readout channel linearization

(2) PRNU in sample DUT1 is pessimistic. DUTs used for these measurements are prototypes without glass lids, and the sensing area can be dirty and cannot be cleaned without risking of damaging the units. PRNU on samples DUT7 and 8, which are cleaner, are below 0.5%.

For completeness, results without calibration/correction obtained from raw images are compiled in Table 4. It can be seen that calibration and correction improves DSNU and H/VFPN while keeping the remaining figures nearly unaffected. Differences in the dark level between corrected and raw results are justified by the particular setting of the calibration correction algorithm, but they can be avoided if required.

SPECTRAL RESPONSE

Figure 6 shows the spectral dependence of the Responsivity and Fill-Factor Quantum Efficiency of the 3 samples tested. Note that among the samples tested, DUT1 shows a higher responsivity above red (650nm) and in the IR (accompanied of an increase in FFxQE at these wavelengths). The origin of this discrepancy is still unclear, although it could be due to that fact that the first part board displayed an unexpected current sink caused by a wrong assembly so that its results are not 100% reliable. Further devices must be characterized to assessing these effects.

Table 4. Optical performance in rolling-shutter operation (raw images)

	EMVA 1288 symbol	DUT1	DUT 7	DUT 8	Mean	Std Dev	UNITS
Dynamic Range (LoNIS SoW)	DR	77.23	76.78	79.76	77.92	1.61	dB
Dynamic Range (EMVA)	DR_{1288}	74.34	74.22	76.51	75.02	1.29	dB
Signal-to-Noise Ratio	SNR_{max}	40.83	41.02	40.93	40.93	0.10	dB
Dark-Signal Non-Uniformity	$DSNU_{1288}$	2.45	2.52	2.48	2.483	0.035	e-
Photo-Response Non-Uniformity	PRNU	1.00[(2)]	0.41	0.42	0.418	0.005	%
Vertical Fixed-Pattern Noise (dark) $VFPN_{dark}$	-	0.020	0.019	0.019	0.019	0.001	%FS
Horizontal Fixed-Pattern Noise (dark) $HFPN_{dark}$	-	0.0020	0.0011	0.0000	0.0010	0.0010	%FS
Temporal Noise (dark)	$\sigma_{y.dark}$	2.25	2.37	1.68	2.10	0.37	DN
Noise-Equivalent Electrons (NEE_e)	-	1.80	1.91	1.35	1.69	0.29	e-
Overall system gain (or conversion gain)	K	1.25	1.24	1.24	1.24	0.01	DN/e
Saturation Level	$\mu_{y.sat}$	15126	15428	15470	15341	187.7	DN
Dark Level	$\mu_{y.dark}$	19	17	20	19	1.6	DN
Saturation capacity	$\mu_{e.sat}$	12085	12428	12460	12324	208	e-
Full-Well Capacity	FWC	13107	13213	13213	13178	61	e-
Linearity Error	LE	0.77	0.70	0.80	0.76	0.05	%

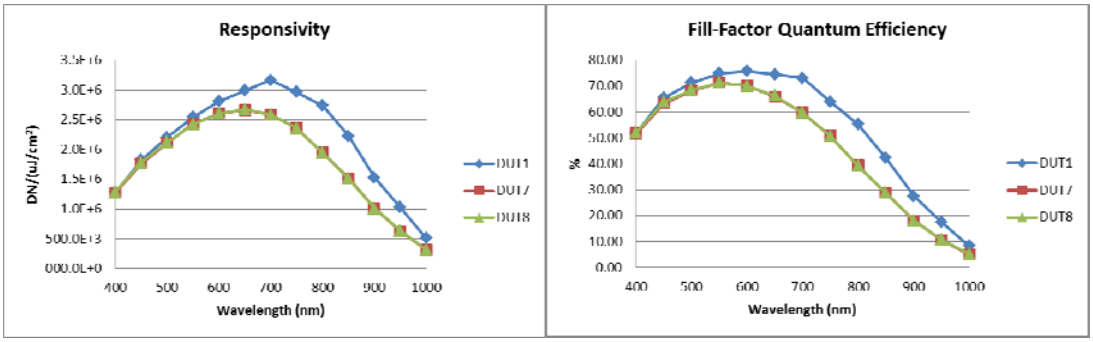

Figure 6. Responsivity (left) and FFxQE (right) as a function of wavelength

5 ACKNOWLEDGMENTS

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REFERENCES

[1] Yole Development. http://www.yole.fr/.
[2] AnaFocus Ltd. http://www.anafocus.com/.
[3] *Proc. of Image Sensors and Imaging Systems 2014* . SPIE Electronic Imaging 2014. San Francisco, February 2014.
[4] *Proc. of Image Sensors 2014*. London, March 2014.
[5] *Proc. 2013 Image Sensing Workshop*. Salt-Lake City, June 201