An Adaptive Approach to On-Chip CMOS Ramp Generation for High Resolution Single-Slope ADCs

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***Abstract*—Many image sensors employ column-parallel ADCs in their readout structures. Single-slope ADCs are ideally suited for these multi-channel applications due to their simplicity, low power and small overall area. The ramp generator, shared by all the converters in the readout architecture, is a key element that has a direct effect in the transfer characteristic of single-slope ADCs. Because a digital counter is inherently present in this conversion scheme, one common practice is to use a digital-to-analog converter driven by the counter to generate the ramp. Given the direct relationship between the DAC and the ADC transfer characteristics, one of the main issues is to ensure a sufficient linearity of the DAC, with special emphasis on its monotonicity. Very often, in particular when medium to high resolutions are aimed, this requires calibration of the DAC, which must be repeated every once in a while to account for temperature, process, power supply, and aging variations. This paper presents an inherently monotonic ramp generator with high levels of linearity and stability against any expected source of variations, combined with a very efficient realization and an inherent automatic adaptability to different resolutions. The ramp generator has been designed using radiation hardening by design (RHBD) techniques, allowing its use in space applications.**

Keywords—Ramp generator; single-slope ADCs; CMOS mixed-signal ASICs; image sensors; aerospace electronics.

I. INTRODUCTION

Column-parallel ADCs are gaining importance in modern image sensors. Several ADC architectures are available for these applications. One of the most used solutions is the single-slope ADC as they are ideally suited for multi-channel applications due to their simplicity, low power and small overall area [1]. To obtain a good performance with single-slope ADCs in these applications, the ramp generator must have good driving capability, high power supply rejection ratio (PSRR), high linearity and good noise rejection [2].

Furthermore, most of the applications require good performance in terms of power consumption and area, the latter being related to a high level of scalability with the increase of resolution. Several approaches for the design of a ramp generator are available in the literature, mostly based on the progressive variation of a voltage, current or charge signal in both continuous and discrete time [3]. Digital-to-analog converters (DACs) with several configurations are the most used option. Main tradeoffs in these approaches are generally due to the need to calibrate the DAC to ensure the monotonicity of the ramp when working at high resolutions. Additional calibrations may also be necessary to set the range of the ramp perfectly defined. The stability with temperature as well as the noise rejection can be other important tradeoffs.

This paper presents a new architecture for an inherently monotonic ramp generator with a high level of scalability to work with high resolutions as well as high level of stability versus any expected source of variations. The ramp generator has been designed in a 0.35 µm CMOS technology from Austria Microsystems (AMS). As a first design, the ramp generator is part of a set of four single slope ADCs and it has been designed by using radiation hardening by design (RHBD) techniques in order to be used in multiple space applications.

The following sections present the architecture and circuit description of the ramp generator. The main design tradeoffs are disclosed and both simulation and experimental results are presented.

II. DESCRIPTION OF THE PROPOSED RAMP GENERATOR

A. Architecture Description

The proposed architecture consists of an integrator driven by a voltage-controlled current source, as shown in Fig. 1. The generation of the ramp is controlled by a feedback loop that modifies the end value of the ramp to the reference voltage by regulating the input voltage of the current source, in turn modified according to the difference between the final value of the ramp and its reference goal value. Thus, after starting up the ramp generator, several cycles of generation of the ramp are needed until the ramp is stabilized and reaches the reference end value (V_{REF_LAST}). For each iteration of the adaptation loop, the variation of the driving current of the integrator is given by:

$$\delta I = g_m \cdot \delta V_G \tag{1}$$

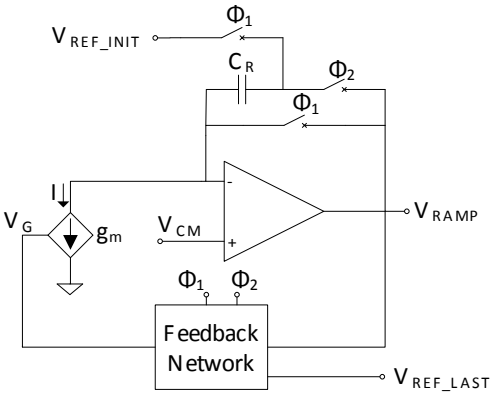

Fig. 1. Proposed architecture for the ramp generator.

where gm and δV_G are respectively the transconductance and the input voltage variation of the voltage-controlled current source. Assuming for simplicity that the ramp starts at ground level (V_{REF_INIT} = 0), the end voltage of the ramp signal for each iteration is:

$$V_{RAMP\_END} = I \cdot \frac{T_{RAMP}}{C_R} \tag{2}$$

where T_{RAMP} is the time duration of the ramp and C_R is the capacitor of the integrator. The error voltage that determines the value of δV_G for the next cycle is:

$$V_\varepsilon = V_{RAMP\_END} - V_{REF\_LAST} \tag{3}$$

with V_{REF_LAST} being the goal value of V_{RAMP_END}.

The generation of the ramp is divided into two phases, as shown in Fig. 2. During the first phase, ϕ_1, the feedback network determines the error voltage V_ε, used to adapt the value of V_G for the next phase, the capacitance C_R is reset, and the output of the ramp generator is driven to an intermediate reference V_{CM}. During the second phase, ϕ_2, the integrator generates the ramp signal starting from V_{REF_INIT} with a driving current value that depends on the voltage V_G determined in the previous phase. After several cycles of adaption, the error voltage V_ε is ideally zero and the range of the ramp signal is stablished between V_{REF_INIT} and V_{REF_LAST}.

B. Circuit Description

Fig. 3 shows the schematic of the circuit proposed for the ramp generator. The voltage-controlled current source is implemented by an NMOS transistor with a capacitor (C_G) that keeps the polarization of the gate during the ramp generation phase (ϕ_2). The feedback loop comprises a capacitor (C_F) and two pairs of switches controlled by ϕ_1 and ϕ_2, resulting in a modification of the gate voltage of the current-source transistor as a function of the error voltage at the end of the previous ramp cycle.

An operational amplifier in a follower configutarion (OA2) is used to provide driving capability to the gate voltage of the current-source transistor (preventing the discharge of capacitor

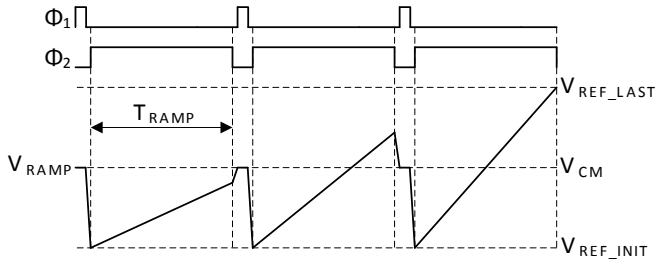

Fig. 2. Time diagram of the operation of the ramp generator with the feedback loop until the ramp is adapted.

C_G during phase ϕ_2). The operational amplifier in the integrator (OA1) is implemented using a rail-to-rail Miller topology with a folded-cascoded first stage, its main requirements being high PSRR and low noise.The integrator is insensitive to the opamp (OA1) offset voltage.

A low drop-out (LDO) internal voltage regulator driven by a band-gap circuit is used to generate an internal supply voltage independent of the external power supply. Voltage references for both the initial and the end values of the ramp are derived from the regulated internal power supply. A non-overlapping two-phase generator, shown in Fig. 4, generates signals ϕ_1 and ϕ_2. For each ramp generation cycle, the final voltage values stored in capacitors C_F and C_G at the end of phase ϕ_2 are given by:

$$V_{C_G} = V_G\big|_{\phi_2} \tag{4}$$

$$V_{C_F} = V_{RAMP\_END} - \left(V_G\big|_{\phi_2} + V_{OFF2}\right) \tag{5}$$

where V_{OFF2} is the offset voltage of the operational amplifier OA2. During the next phase ϕ_1, the voltage values stored in the capacitors change to:

$$V_{C_G} = V_G\big|_{\phi_1} \tag{6}$$

$$V_{C_F} = V_{REF\_LAST} - V_G\big|_{\phi_1} \tag{7}$$

Therefore, capacitor voltage increments associated with transitions from ϕ_2 to ϕ_1 are:

$$\Delta V_{C_G} = \delta V_G \tag{8}$$

$$\Delta V_{C_F} = V_{OFF2} - \left(V_\varepsilon + \delta V_G\right) \tag{9}$$

Using charge conservation and equations (1) to (9) yields the following expressions for the increments in the gate voltage of the current-source transistor and the end value of the ramp:

$$\delta V_G = \frac{C_F}{C_F + C_G} \cdot \left(V_{OFF2} - V_\varepsilon\right) \tag{10}$$

$$\delta V_{RAMP\_END} = \frac{g_m \cdot T_{RAMP}}{C_R} \cdot \frac{C_F}{C_F + C_G} \cdot \left(V_{OFF2} - V_\varepsilon\right) \qquad (11)$$

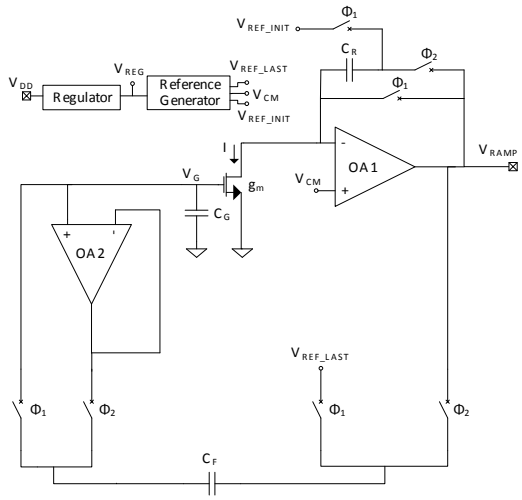

Fig. 3. Circuit description of the ramp generator.

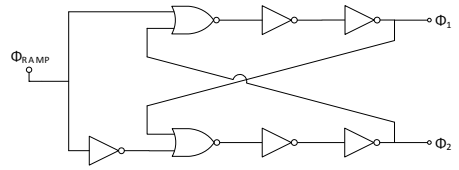

Fig. 4. Non-overlapping two-phase generator.

A constant transconductance g_m is assumed for simplity. At the equilibrium point, when the ramp is fully adapted, the voltage increments will be cero. Using either (10) or (11) shows that the error in the final value of the ramp voltage with respect to its goal value is reduced to the offset voltage of operational amplifier OA2. This steady state error is generally acceptable, but offset correction schemes are possible and may be implemented when required. The stability of the feedback loop can be analyzed in the Z domain. System poles are independent of the specific output or input considered, allowing us to consider the following transfer function obtained from (3) and (11):

$$\frac{V_\varepsilon(z)}{V_{OFF2}} = \frac{\alpha \cdot z}{z - (1-\alpha)}; \quad with \quad \alpha = \frac{g_m \cdot T_{RAMP}}{C_R} \cdot \frac{C_F}{C_F + C_G} \qquad (12)$$

Equation (12) shows that the feedback loop will be stable if $|1-\alpha| < 1$. This condition implies a design compromise between adaptation speed and loop stability, as usual. Thus, a too large transconductance of the current-source transistor could make the loop unstable. On the other hand, a small transconductance increases the stability of the loop, but implies a slow convergence to the equilibrium point. Weak inversion is a good choice for the operation of the current-source transistor, given the proportionality between transconductance and current in that region, which according to (2) yields the condition independent of T_{RAMP} and therefore invariant with the programmed resolution of the ADC. Temperature and ramp excursion do have an effect and must be considered.

The adaptive nature of this ramp generation makes it insensitive to any possible source of variations, except for the reference voltages defining the ramp excursions. These are obtained from a band-gap, as usual in most conversion circuits. The inherent low pass filtering operation of the integrator allows a good noise rejection with respect to other approaches based on DACs.

The resolution of the ADC is determined by the time duration of phase ϕ_2, easily configurable through the control of the input signal of the phase generator (ϕ_{RAMP}). This signal is easily generated with programmable finite state machine (FSM) including a digital counter. This provides a good level of scalability with resolution: the only hardware that must be scaled is the digital counter.

Monotonicity is inherent. Integral linearity is expected to be very high, limited only by capacitor linearity and opamp gain variations along its output swing.

A ramp generator following this approach has been designed in a 0.35 μm CMOS technology from Austria Microsystems (AMS). In this design example, the ramp generator is part of a set of several single-slope ADCs for space applications, specifically for payload sensors temperature measurements for missions to Mars.

All converters share the same ramp generator. Each converter has a self-biasing comparator, all of them controlled by the same signals (ϕ_1 and ϕ_2) that control the common ramp generator. Therefore, all converters are controlled by the same ϕ_{RAMP} signal (Fig. 4), generated by a FSM which is basically composed of a counter that determines the duration of phase ϕ_1 and ϕ_2 depending on the selected resolution.

The resolution is configurable from 10 to 15 bits by a configuration register in the FSM. The internal clock frequency, generated by a simple relaxation oscillator, is also configurable between 25 MHz and 100 MHz. For this specific application, the required voltage range of the ramp is from 50 mV to 2.5 V. The (internally regulated) supply voltage is 3.0 V. The maximum time duration of the ramp is around 1.3 ms, corresponding to a maximum resolution of 15 bits at a frequency of 25 MHz.

A close to optimal design of the ramp generator, with a sufficient margin of stability while ensuring a short adaptation-time of few cycles, has been obtained with a capacitors ratio of $C_G \approx C_R \approx 150 \cdot C_F \approx 20$ pF. The current-source transistor operates in moderate inversion, close to weak inversion.

As the ASIC has been designed for on-board space applications using standard CMOS technology, RHBD techniques have been used and previous technology characterization was required [4] to deal with the extreme environmental conditions in terms of radiation and temperature. Area restrictions were not severe, and therefore, ringed-source layouts [5] were used in every case for NMOS transistors. PMOS devices use a standard layout. Concerning single event latchup (SEL), complete guard-rings have been used around every transistor.

Some amendments have been introduced in the standard design kit, including additional p-cell for radiation-hardened NMOS transistors that translate into an equivalent width for electrical simulation, a RHBD digital library, modifications in the extraction and LVS scripts and additional layout rules and layers for the proper verification of the layout.

III. RESULTS

A. Simulation Results

Fig. 5 shows the evolution of the adaptive loop of the ramp generator. After a few cycles of adaption, the output ramp is stabilized to its final value. Fig. 6 shows the INL error of the ramp generator for a resolution of 15 bits and a clock frequency of 100 MHz. The INL error is always less than 1 LSB for the required voltage range (50 mV – 2.5 V). This range could be extended to the whole range in wich the operational amplifier of the integrator operates in its linear region, that is, approximately 50 mV above the gnd value and 50 mV beyond the regulated supply voltage (3 V).

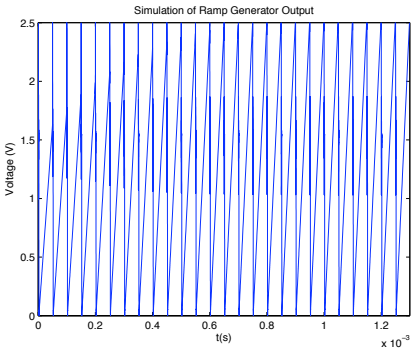

Fig. 5. Simulation of the ramp output voltage during adaptation.

B. Experimental Results

The ramp generator has been functionally verified. Fig. 7 shows the output of the ramp as measured with an oscilloscope. Preliminary experimental tests have been performed for lower resolutions (between 10 and 12 bits) and typical environmental conditions. In these conditions the ramp generator is monotonic and the INL is lower than 1 LSB.

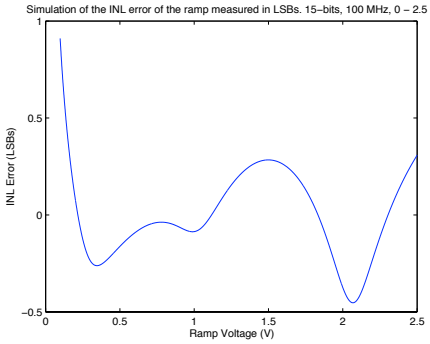

Fig. 6. Simulation of the INL error measured in LSBs versus ramp output voltage for a resolution of 15 bits and a clock frequency of 100 MHz.

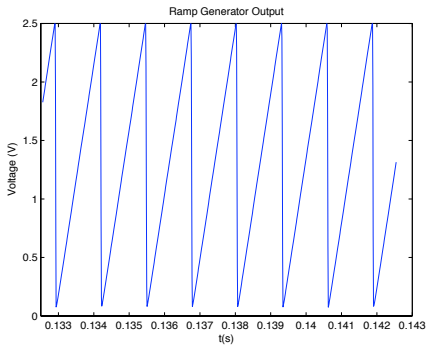

Fig. 7. Output of the ramp generator measured with an oscilloscope.

More accurate and detailed tests are presently underway to check the performance of the ramp generator for higher resolutions as well as to verify its invariability with temperature, radiation and other sources of variation.

IV. CONCLUSIONS

A new architecture for an inherently monotonic ramp generator, with a high level of scalability for high resolutions as well as high insensitivity to virtually any variation source has been presented. It has been designed in a 0.35 µm CMOS technology as part of a set of single-slope ADCs with resolution up to 15 bits. The circuit has been described and the key design aspects have been commented. Simulation and preliminary experimental results have been shown.

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