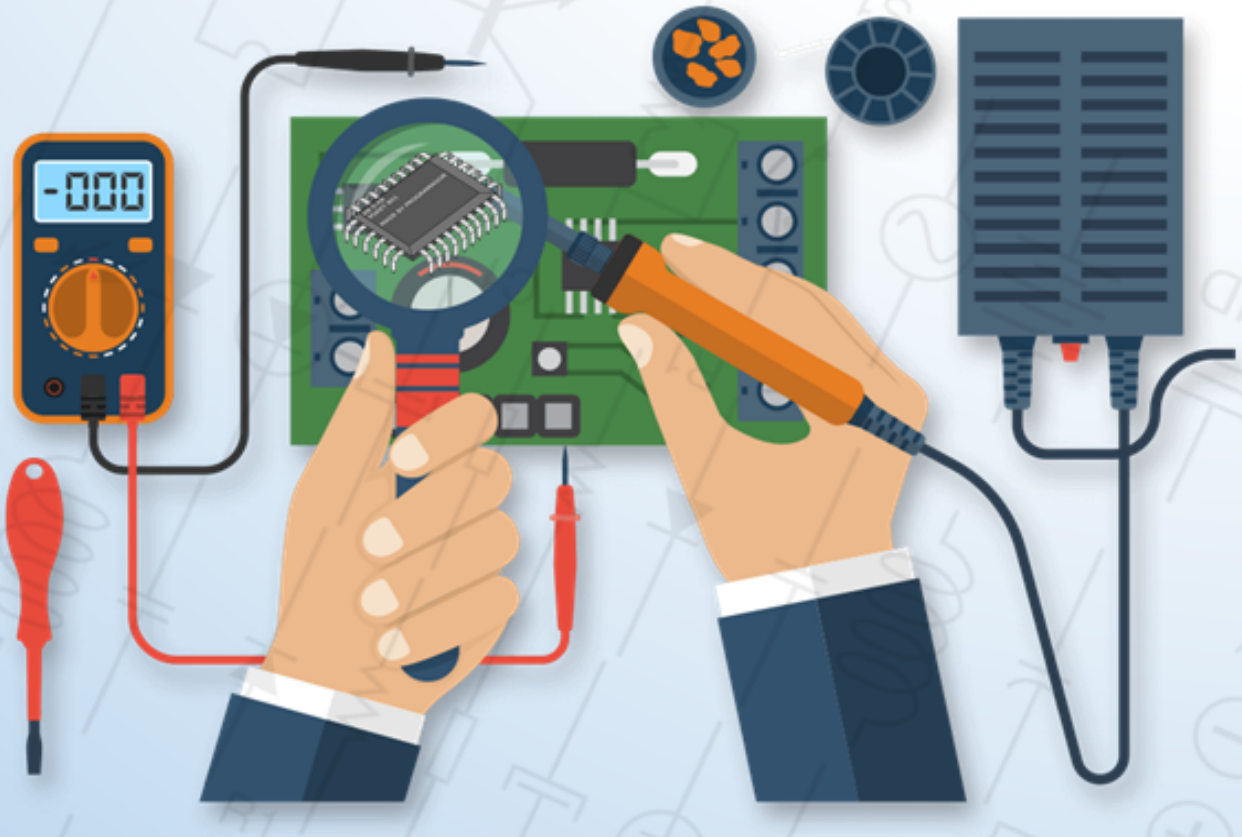
HO CHI MINH CITY UNIVERSITY OF TECHNOLOGY
COMPUTER ENGINEERING

Electronic Device Component

Lab's Report



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CHAPTER 1

Operational Amplifier - OPAMP

1 Introduction

Operational Amplifiers, also known as Op-amps, are basically a voltage amplifying device designed to be used with components like capacitors and resistors, between its in/out terminals. They are essentially a core part of analog devices. Feedback components like these are used to determine the operation of the amplifier. The amplifier can perform many different operations, giving it the name Operational Amplifier.

One key to the usefulness of these little circuits is in the engineering principle of feedback, particularly negative feedback, which constitutes the foundation of almost all automatic control processes. The principles presented in this section, extend well beyond the immediate scope of electronics. It is well worth the electronics student's time to learn these principles and learn them well.

Operational amplifiers can have either a closed-loop operation or an open-loop operation. The operation (closed-loop or open-loop) is determined by whether or not feedback is used. Without feedback the operational amplifier has an open-loop operation. This open-loop operation is practical only when the operational amplifier is used as a cooperator (a circuit which compares two input signals or compares an input signal to some fixed level of voltage). As an amplifier, the open-loop operation is not practical because the very high gain of the operational amplifier creates poor stability. (Noise and other unwanted signals are amplified so much in open-loop operation that the operational amplifier is usually not used in this way.) Therefore, most operational amplifiers are used with feedback (closed-loop operation).

2 Closed Loop Operation

Operational amplifiers are used with degenerative (or negative) feedback which reduces the gain of the operational amplifier but greatly increases the stability of the circuit. In the closed-loop configuration, the output signal is applied back to one of the input terminals. This feedback is always degenerative (negative). In other words, the feedback signal always opposes the effects of the original input signal. One result of degenerative feedback is that the inverting and non-inverting inputs to the operational amplifier will be kept at the same potential.

Closed-loop circuits can be of the inverting configuration or non-inverting configuration.

2.1 Non inverting configuration

The typical circuit for this configuration is shown in the figure bellow:

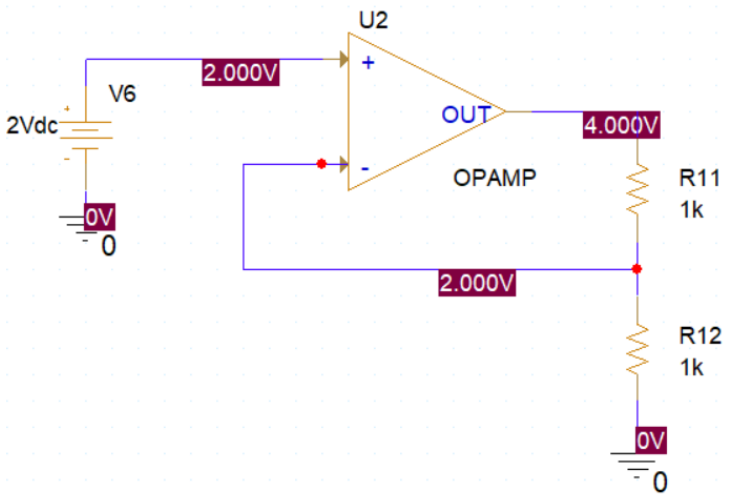

Figure 1.1: Non inverting configuration

The new component, named also OPAMP (Operational Amplifier) is easily found in the favorite list of the PSPICE.

In order to explain the 4V at the ouput, it is obviously that $V(+) = V(-) = 2V$ in a closed loop configuration. Therefore, from a resistor bridge at the output, $V_{OUT} = 4V$.

2.2 Inverting configuration

In this configuration, the output is connected directly to a pin of the opamp as follow:

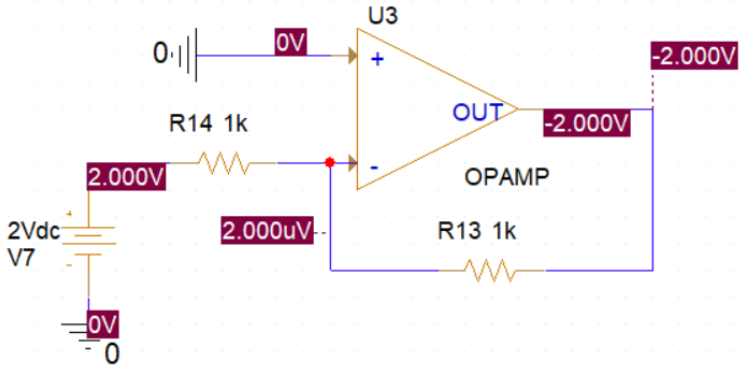

Figure 1.2: Inverting configuration

As the output voltage is negative, which is inverted to the input, the name of this circuit is the invert connection. Students are proposed to perform calculations to confirm the output, which is $-2V$.

The circuit has negative feedback. So we can obtain that:

$V_{(+)} = V_{(-)} = 0(V)$

$$I = \frac{2 - V_{(-)}}{R_{14}} = \frac{2-0}{1000} = 2(mA)$$

$V_{(-)} - V_{out} = I \times R_{13} = 2 \times 10^{-3} \times 1000 = 2(V)$

$=> V_{out} = -2(V)$

3 Exercise and Report

3.1 Voltage Follower

Voltage follower is one of the simplest uses of an operational amplifier, where the output voltage is exactly same as the input voltage applied to the circuit. In other words, the gain of a voltage follower circuit is unity. The connections are proposed as follows:
A voltage follower has low output impedance and extremely high input impedance, and this makes it a simple and effective solution to problematic impedance relationships. If a high-output-impedance sub-circuit must transfer a signal to a low-input-impedance sub-circuit, a voltage follower placed between these two sub-circuits will ensure that the full voltage is delivered to the load.

Students are propose to run the simulation with bias mode to confirm that $V_{OUT} = V(+)$. The feedback resistance is also required to change.

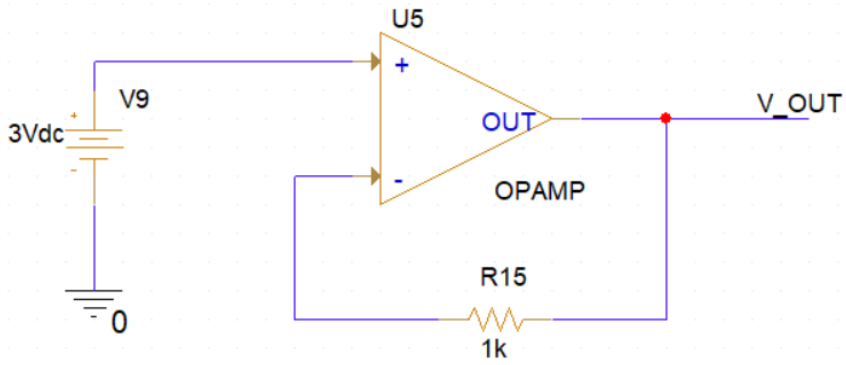

Figure 1.3: Opamp follower circuit

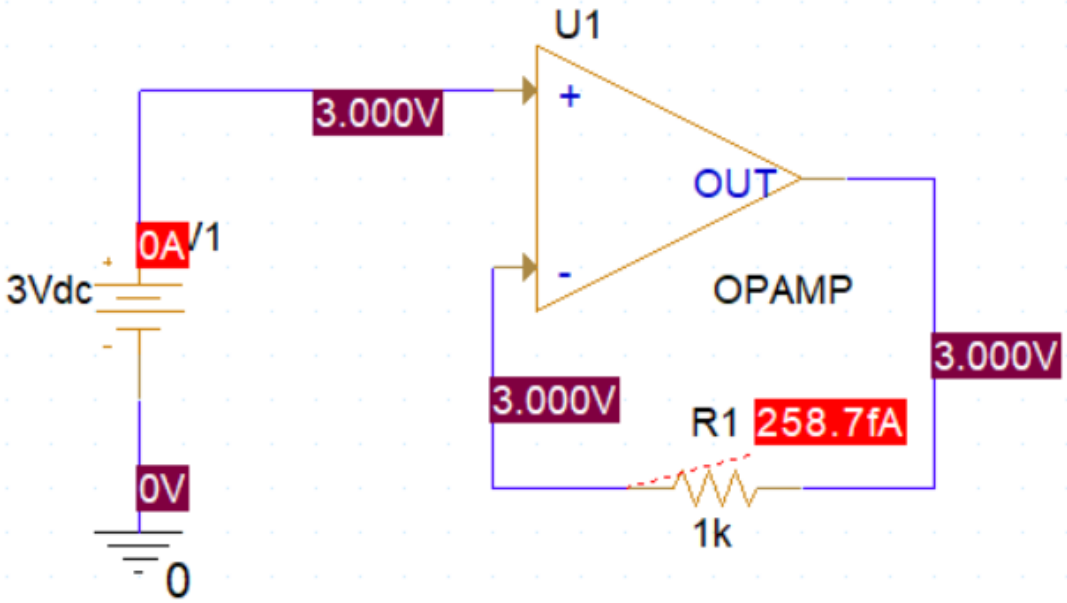

Figure 1.4: The bias point simulation when feedback resistance is 1kΩ.

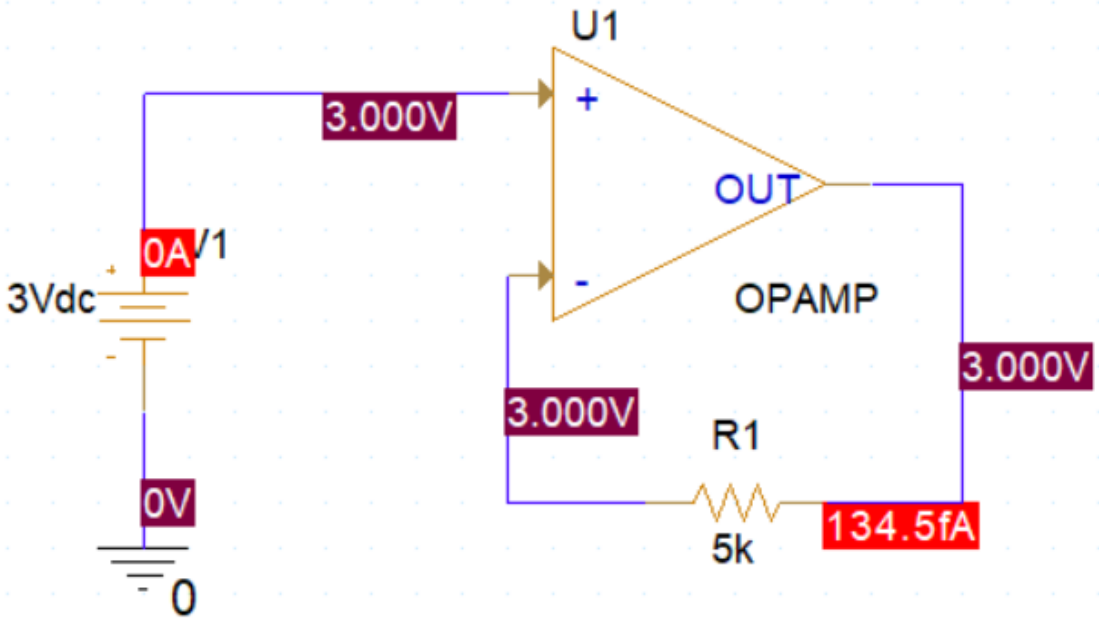

Figure 1.5: The bias point simulation when feedback resistance is 5kΩ.

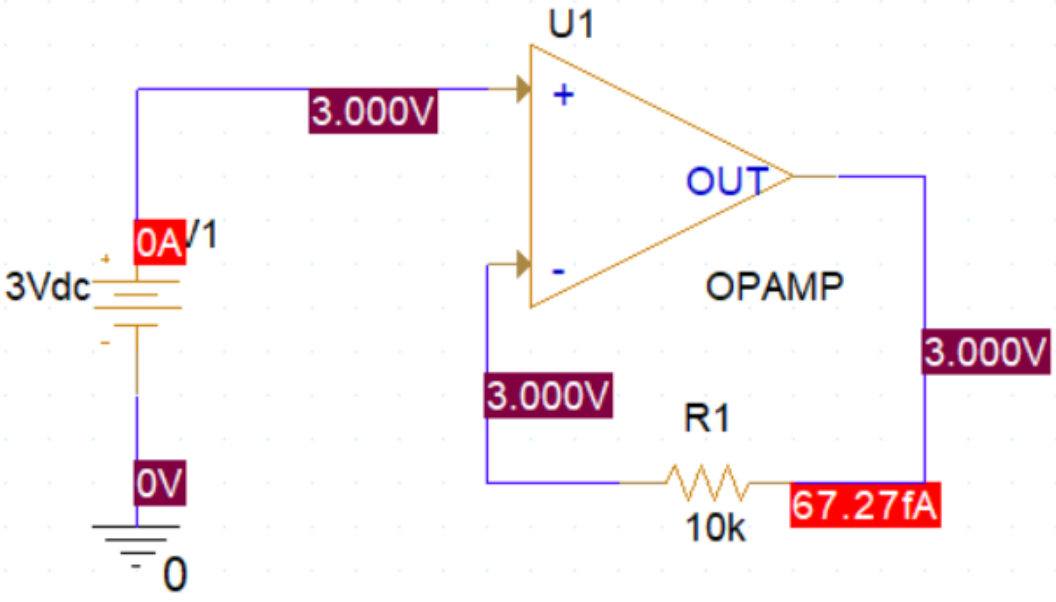

Figure 1.6: The bias point simulation when feedback resistance is 10kΩ.

Your calculations are presented here to prove $V_{OUT} = V(+)$ with any value of R15.

In any case, whenever we change the value of R_{15}, there is no current pass through it. Thus we always have $V_{(+)} = V_{(-)} = V_{out} = 3(V)$

3.2 High-Current Voltage Follower

The voltage follower's low output impedance makes it a good circuit for driving current into a low-impedance load, but it's important to remember that most op-amps are not designed to deliver large output currents. The most basic circuit for buffering an op-amp's output current is the following:

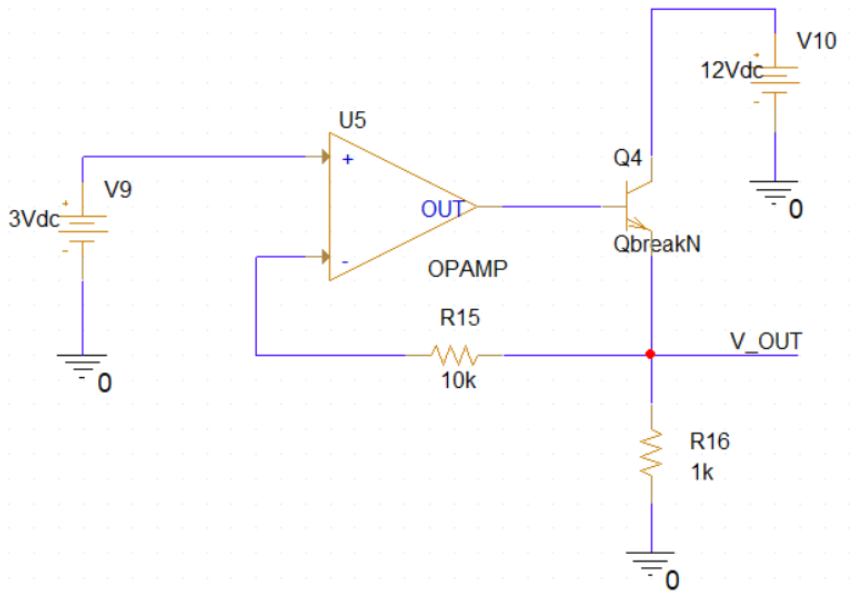

Figure 1.7: Opamp follower circuit

The voltage at the positive pin of the Opamp is copied to V_{OUT}. In this schematic, R16 is used to simulate a load device, which can be a motor or an high power LED. However, in this case, there is a high current can pass the load.

Students are proposed to run the simulation with bias configuration, capture the results and place them in the report.

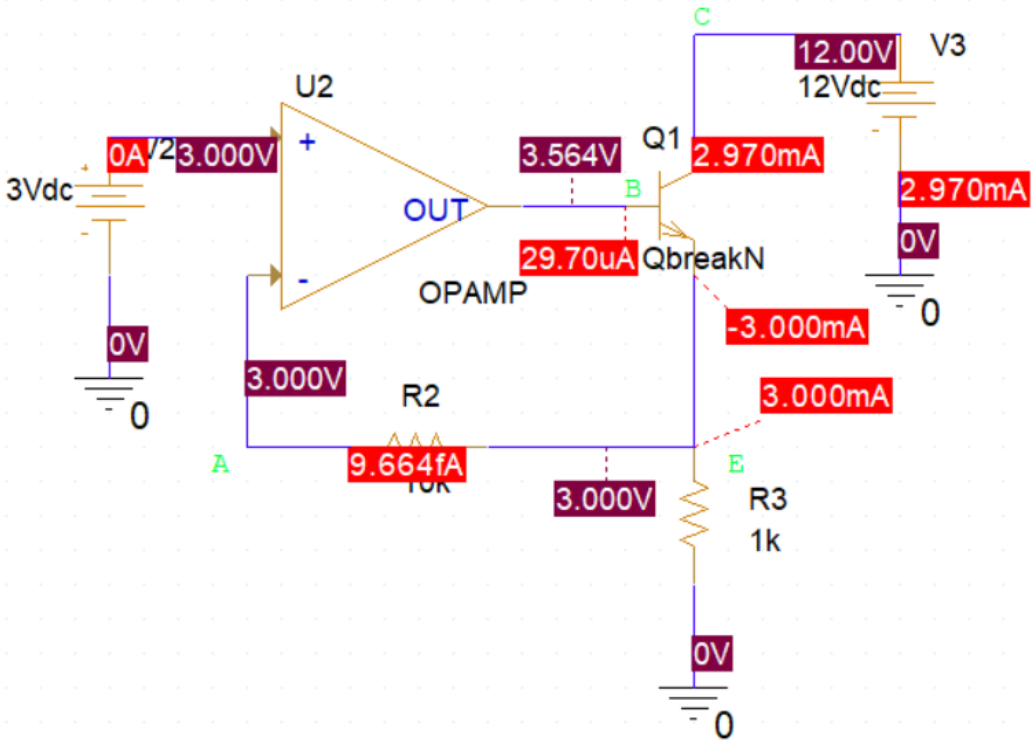

Figure 1.8: The bias point simulation.

Finally, your computations go here to explain the results.

Since there is no current pass through the $10k\Omega$ resistor, $V_{(+)} = V_{(-)} = V_E = 3(V)$

$$I_E = \frac{V_E - 0}{R_3} = \frac{3-0}{1000} = 3(mA)$$

$$I_C = \alpha \times I_E = \frac{\beta}{\beta+1} \times I_E = 2.97(mA)$$

$$I_B = I_E - I_C = 3 - 2.97 = 29.7(\mu A)$$

$$V_B = V_E + 0.7 = 3.7(V)$$

The result is exactly the same with those obtained by simulation

3.3 Voltage Follower with Gain

This basic circuit is not limited to the unity-gain configuration. As with a non-buffered op-amp, you can insert resistors into the feedback path to create overall gain from the input to the load voltage. Here is the non-unity-gain version of the circuit:
Students are proposed to implement this circuit on PSPICE with input is 2V and the gain is 3. The voltage supply for the load side is 12VDC. Value of R_{LOAD} is 1K.

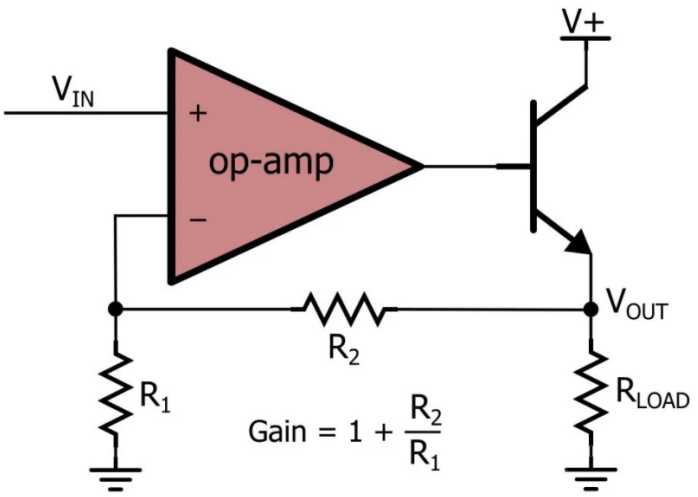

Figure 1.9: Opamp follower with gain for the output

The simulation results in PSPICE (bias configuration) are presented here. Moreover, a short explanations are required in this report to explain the gain of the output follower voltage.

We have the gain is 3. So $3 = 1 + \frac{R_2}{R_1}$

$=> \frac{R_2}{R_1} = 2 => R_2 = 2 \times R_1$

In order to verify that $V_{out} = 3 \times V_{in}$, we can choose two different values for R_2 and R_1.

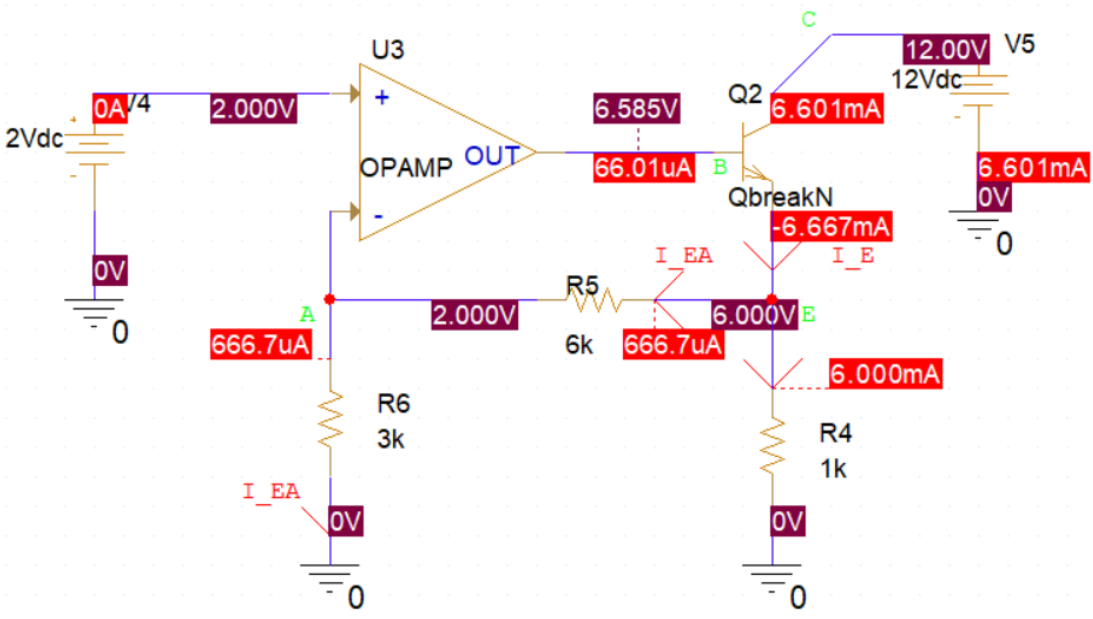

Figure 1.10: The bias point simulation when $R_2 = 6(k\Omega)$ and $R_1 = 3(k\Omega)$.

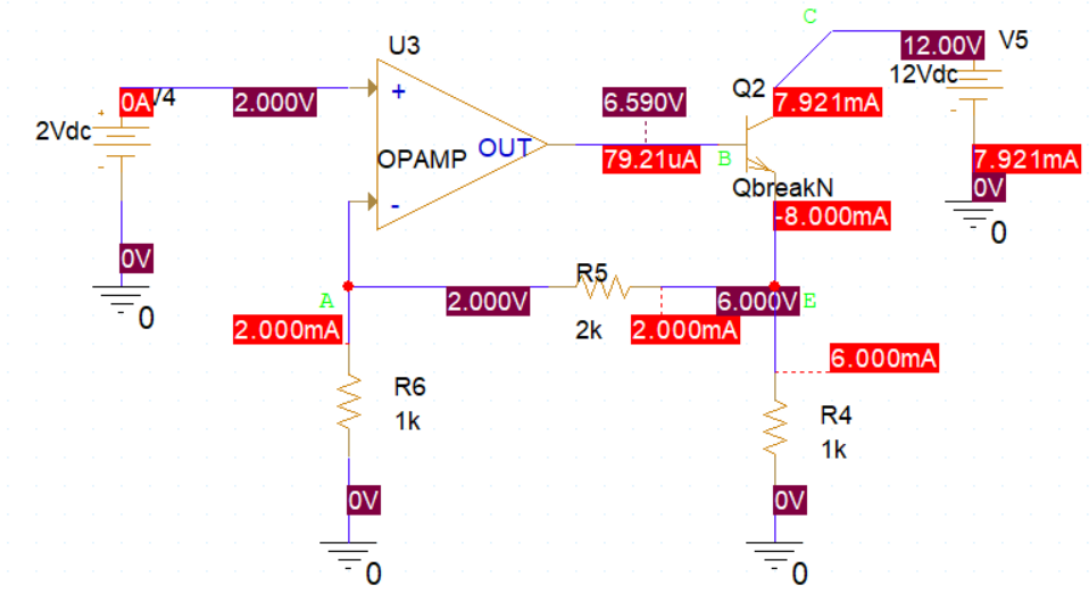

Figure 1.11: The bias point simulation when $R_2 = 2(k\Omega$ and $R_1 = 1(k\Omega)$.

For the theoretical calculation, we can define the direction of the current as shown in the following diagram:

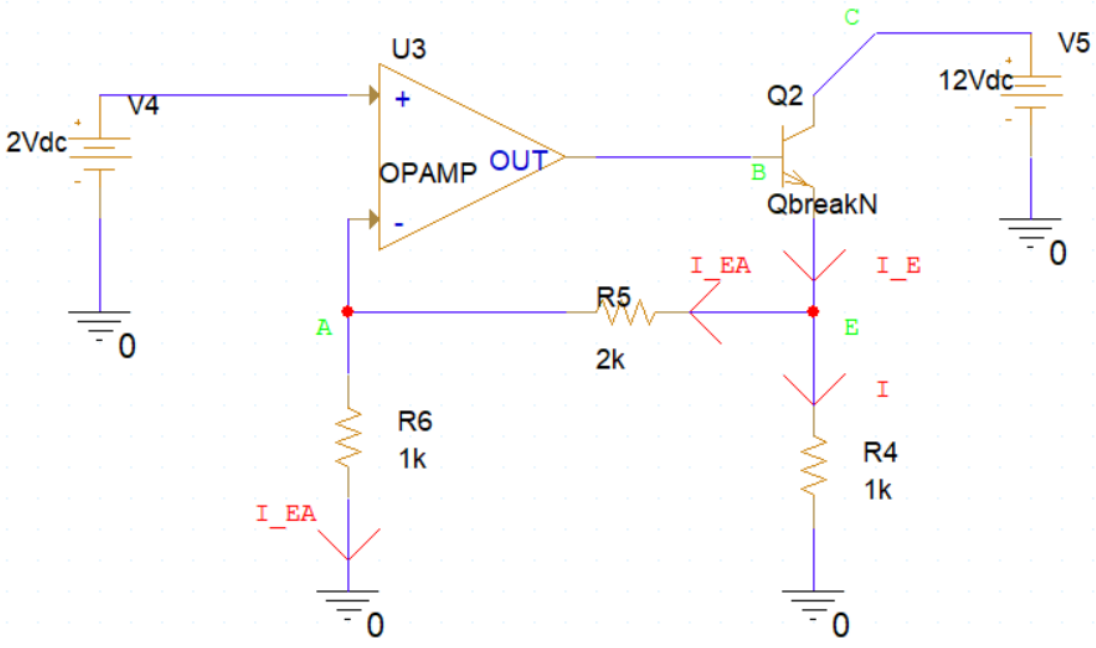

Figure 1.12: The flow of the current.

The Op-amp has negative feedback so $V_A = V_{(+)} = 2(V)$

$$I_{EA} = \frac{V_A - 0}{R_1} = \frac{2}{R_1}$$

$$V_E - V_A = I_{EA} \times R_2 \Rightarrow V_E = V_A + I_{EA} \times R_2 = 2 + \frac{2}{R_1} \times R_2 = 2 + \frac{2}{R_1} \times 2R_1 = 2 + 4 = 6(V)$$

It is obvious that as long as the values of R_2 and R_1 still follow the relation $\frac{R_2}{R_1} = 2$, we always have $V_{out} = 3 \times V_{in} = 6(V)$

3.4 Summing Amplifier

Students are proposed to implement following schematic in PSPICE and run the simulation with R1 = 1K, R2 = 2K, R3 = 5K, Rf = 9K, Ri = 1K. There inputs are V1 = 1V, V2 = 2V and V3 = 3V. This circuit is a non inverting summing configuration using opamp.

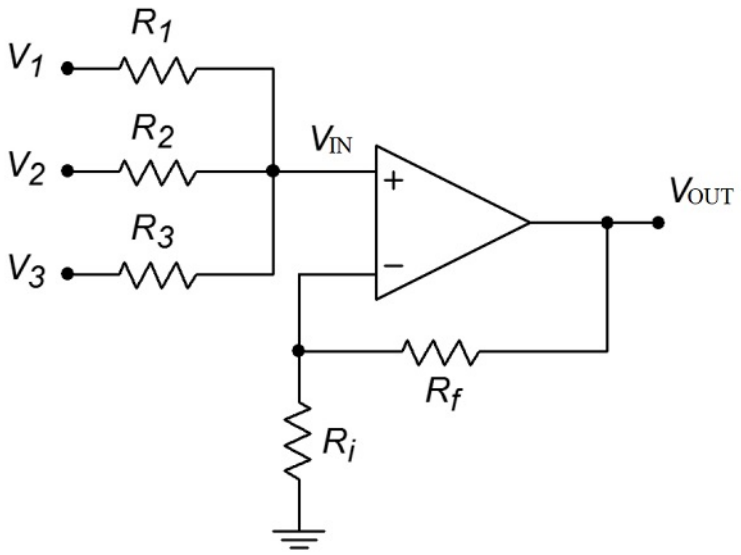

Figure 1.13: Non inverse summing using OPAMP

Students are proposed to design the schematic and place the results in this report.

Your image goes here

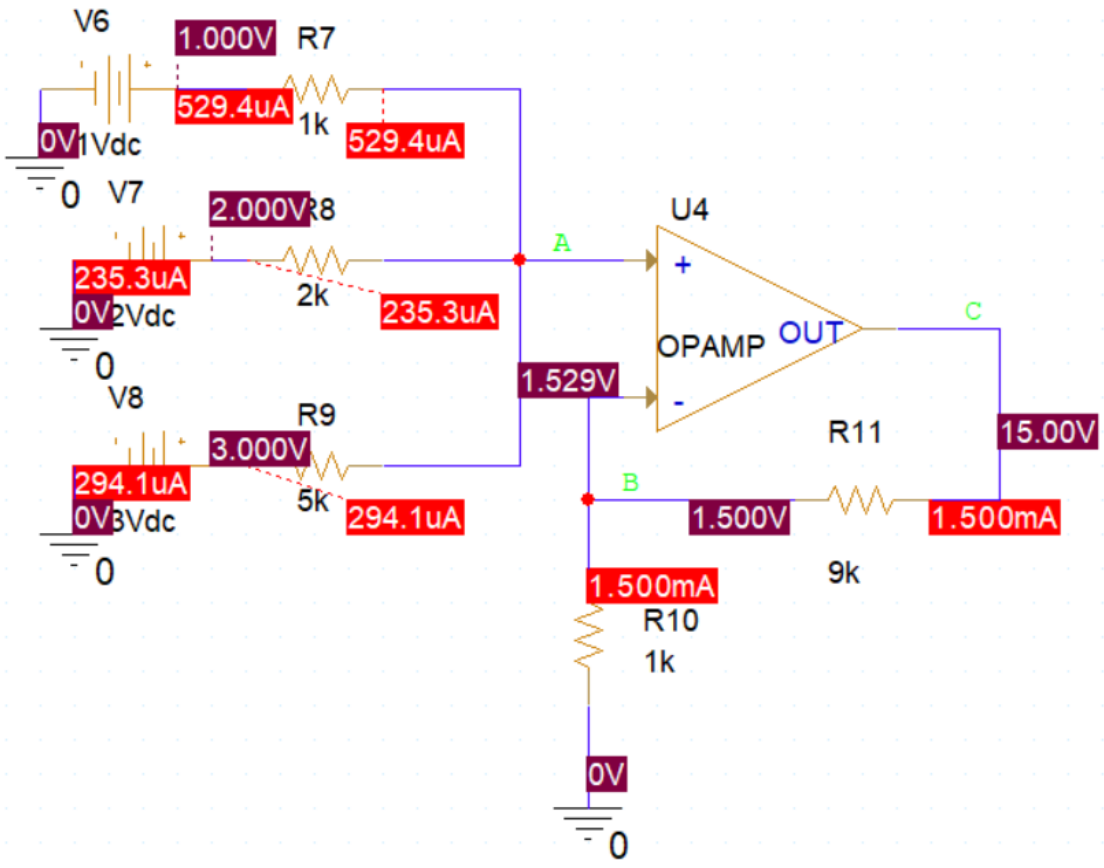

Figure 1.14: The bias point simulation.

Your calculations go here to explain the value of V_{OUT}

Let I_1, I_2 and I_3 denote the current through R_1, R_2 and R_3, respectively. And assume that the direction of these current are from A to their sources. We have the following system of 4 equations with 4 unknowns:

$$\begin{cases} V_A - V_1 = 1000I_1 \\ V_A - V_2 = 2000I_2 \\ V_A - V_3 = 5000I_3 \\ I_1 + I_2 + I_3 = 0 \end{cases}$$

The last equation is the property of the Op-amp when it has negative feedback, $I_{(+)} = 0(A)$

=>

$$\begin{cases} 1000I_1 - V_A = -1 \\ 2000I_2 - V_A = -2 \\ 5000I_3 - V_A = -3 \\ I_1 + I_2 + I_3 = 0 \end{cases}$$

=>

$$\begin{cases} I_1 = 529.41(\mu A) \\ I_2 = -235.29(\mu A) \\ I_3 = -294.11(\mu A) \\ V_A = 1.529(V) \end{cases}$$

The negative values of I_2 and I_3 simply indicate that their directions are from the source to A.

Because of the negative feedback, $V_B = V_A = 1.529(V)$

$$I = \frac{V_B - 0}{R_i} = \frac{1.529 - 0}{1000} = 1.529(mA)$$

$$=> V_{out} = V_B + I \times R_f = 1.529 + 1.529 \times 10^{-3} \times 9000 = 15.29(V)$$

This value is matched with the simulation.

The second type of the summing amplifier is proposed as follows:

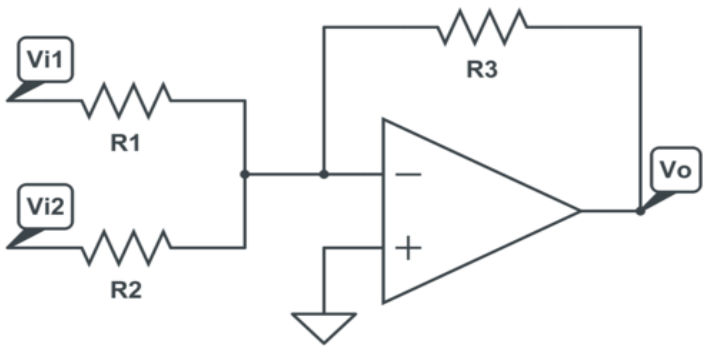

Figure 1.15: Inverse summing using OPAMP

Students are proposed to do the same steps above, with R1 = 1K, R2 = 2K, R3 = 10K and V1 = 1V, V2 = 5V.

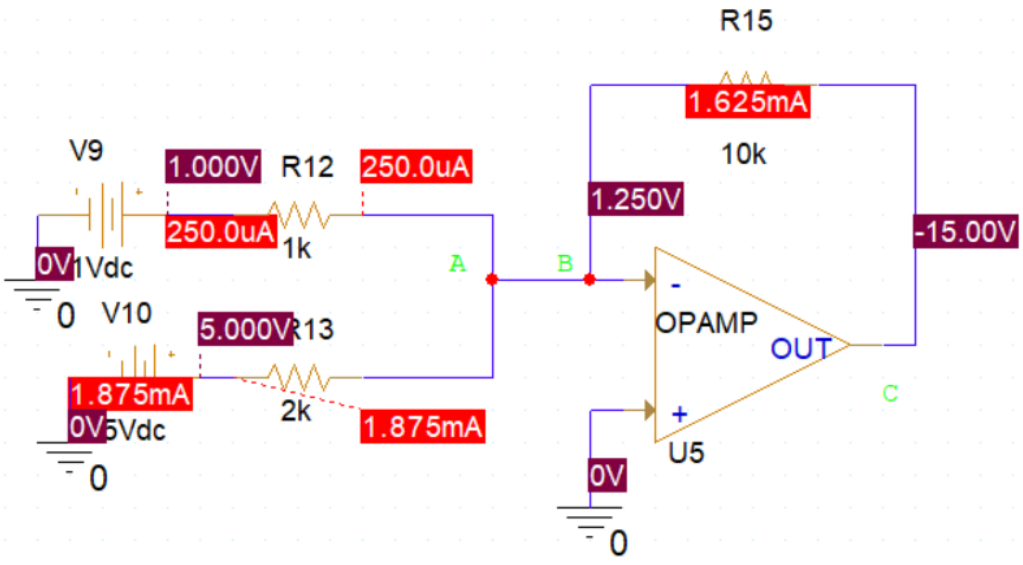

Figure 1.16: The bias point simulation.

Because of negative feedback of the Op-amp, we have $V_A = V_B = V_{(+)} = 0(V)$

$$I = I_1 + I_2 = \frac{V_1 - V_A}{R_1} + \frac{V_2 - V_A}{R_2} = \frac{1-0}{1000} + \frac{5-0}{2000} = 1 \times 10^{-3} + 2.5 \times 10^{-3} = 3.5(mA)$$

$$V_{out} = V_B - I \times R_3 = 0 - 3.5 \times 10^{-3} \times 10000 = -35(V)$$

This results is different from what we have seen in the simulation since the simulation did not consider the values of V_A and V_B as 0 V like the theoretical aspect.

3.5 Low Pass Filter

Low pass filter is a filter which passes all frequencies from 0Hz (DC current) to upper cut-off frequency f_H and rejects any signals above this frequency. A picture to demonstrate a low pass filter behavior is shown in the figure bellow:

Similar to the closed loop configuration, there also 2 types of low pass filter, including the inverting and non-inverting low pass filter. The figure bellow is an inverting low pass filter.

The cut-off frequency is determined by this equation:

$$f_H = \frac{1}{2\pi R_2 C}$$

By applying the value of $R2 = 10KOhm$ and $C = 1nF$, the cut-off frequency is around $16KHz$. In order to see the results, students are proposed to run the AC Sweep simulation profile (**Linear Type, Start and Stop frequency are 1Hz and 50kHz, 200 points**), as follows:
The final results can be archived like the figure bellow:

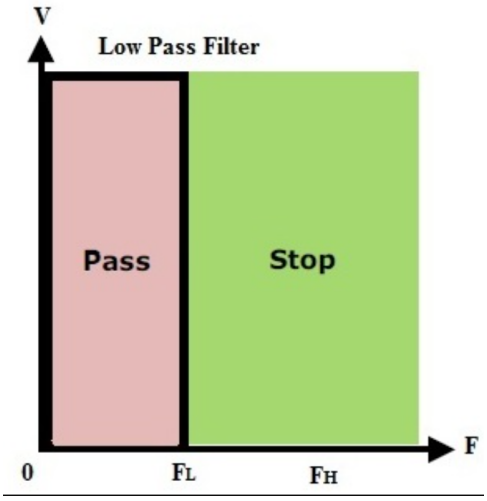

Figure 1.17: Low pass filter principles

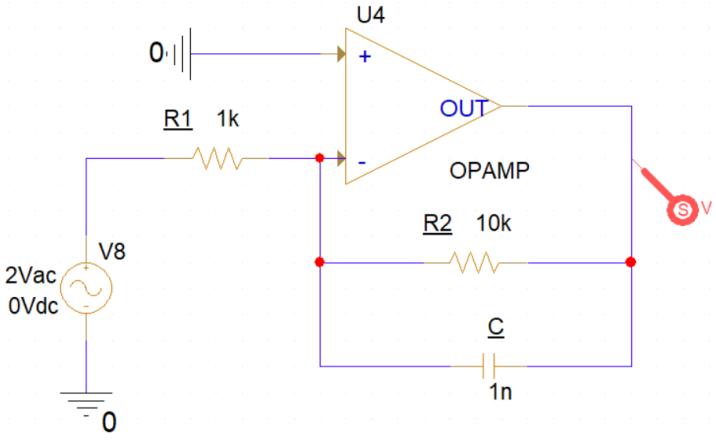

Figure 1.18: Inverting low pass filter

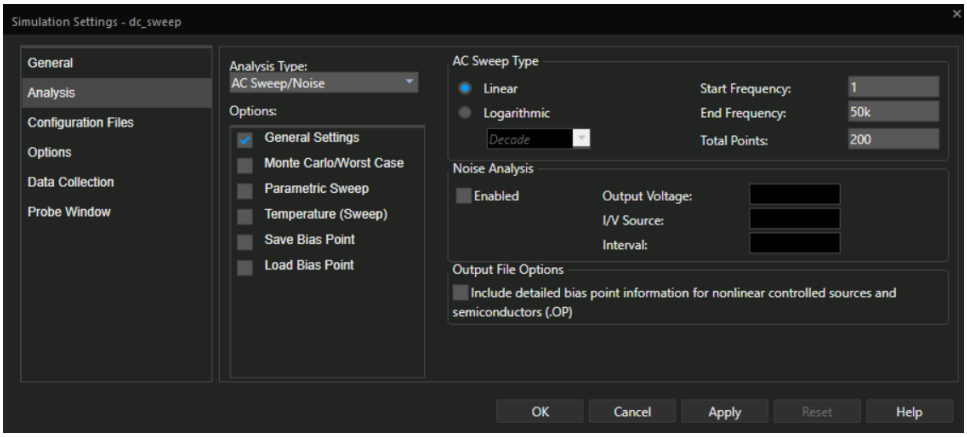

Figure 1.19: AC Sweep simulation profile

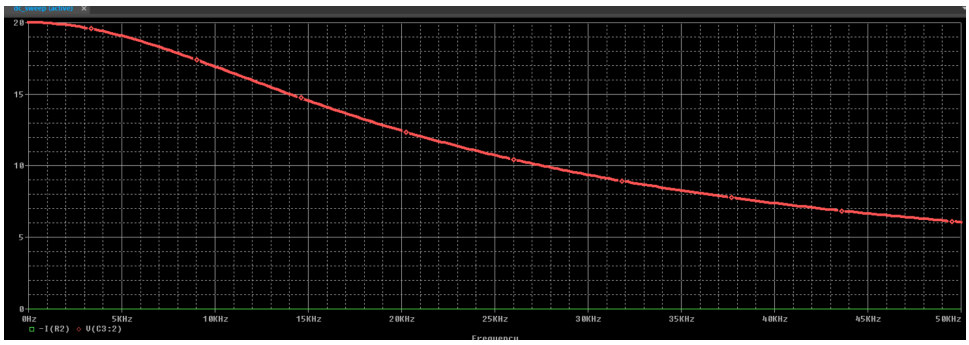

Figure 1.20: Simulation results

It is said that the cut-off frequency point having the gain reduced 3dB. The gain at 0Hz is 10 (input voltage is 2V and output voltage is 20V), or $20log(10) = 20dB$, meanwhile, the gain at 16kHz is 7 (input voltage is 2V and output voltage is 14V), or $20log(7) = 16.9$.

The second type of a low pass filter, the non-inverting configuration, is presented as follows:

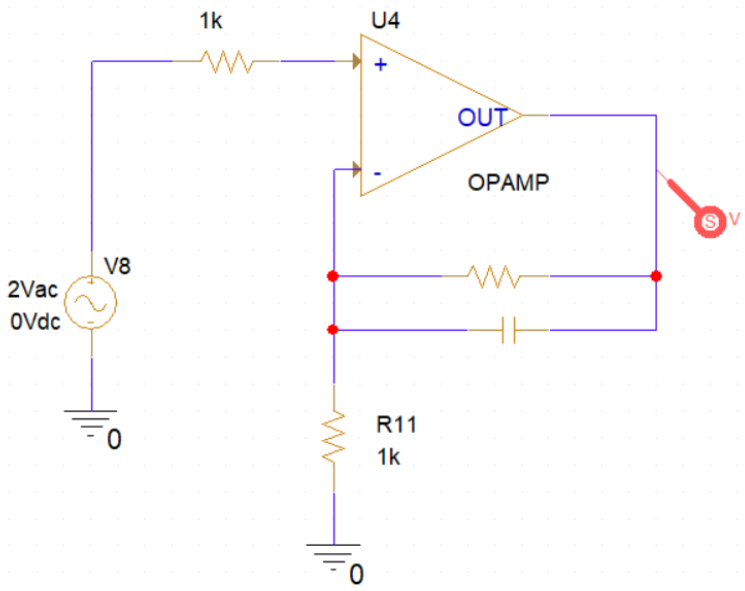

Figure 1.21: Non-inverting low pass filter

Students are proposed to calculate the value of R and C to have the amplifier factor equal to 10 and the cut-off frequency is the same as the previous example. The simulation result with AC Sweep mode is required to plot in this report as well.

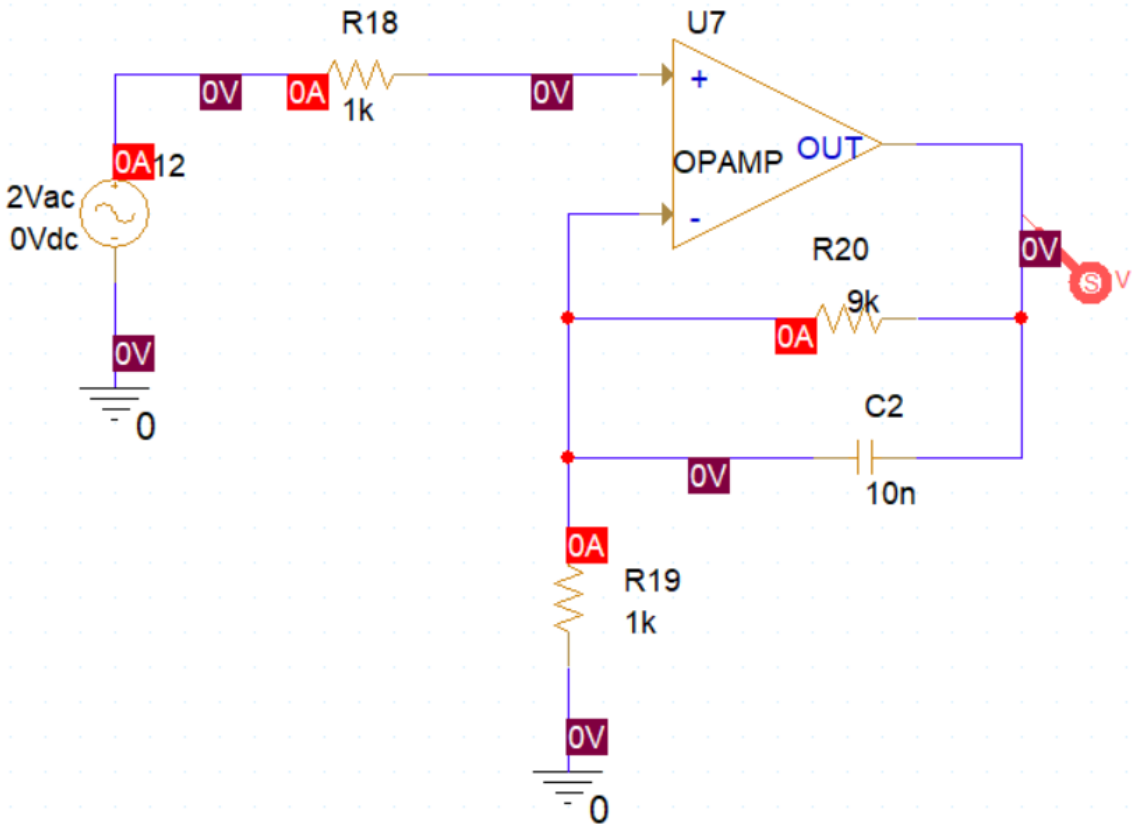

Figure 1.22: Non-inverting low pass filter with value of resistor and capacitor.

The voltage gain of a non-inverting operational amplifier is given as:

$$A_f = 1 + \frac{R_{20}}{R_{19}}$$

$$\Rightarrow 10 = 1 + \frac{R_{20}}{1000}$$

$$\Rightarrow R_{20} = 9(k\Omega)$$

The cut-off frequency is given as being 16 kHz with an input impedance R_{18} of 1kΩ. This cut-off frequency can be found by using the formula:

$$f_C = \frac{1}{2\pi R_{18} C_2}$$

$$\Rightarrow C_2 = \frac{1}{2\pi f_C R_{18}} = \frac{1}{2\pi \times 16000 \times 1000} = 10(nF)$$

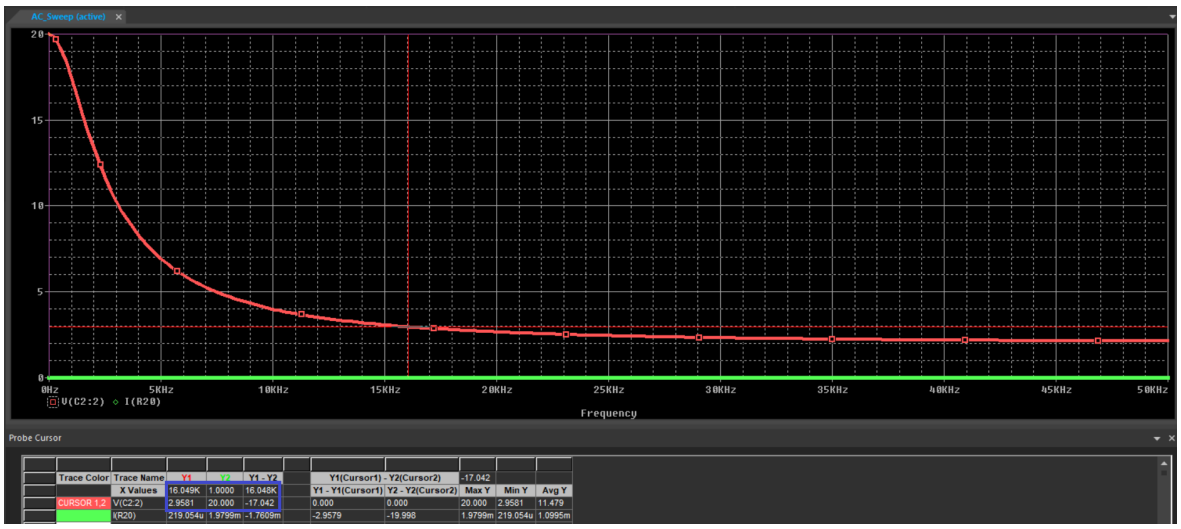

Figure 1.23: The AC Sweep result.

For this circuit the cut-off frequency point having the gain reduced nearly 16.6 dB. The gain at 0 Hz is 10 (input voltage is 2V and output voltage is 20V) or $20 \times log(\frac{V_{out}}{V_{in}}) = 20(dB)$, meanwhile, the gain at 16 kHZ is 3.4 dB (input voltage is 2V and output voltage is 2.9581V) or $20 \times log(\frac{V_{out}}{V_{in}}) = 3.4dB$

Here due to the position of the capacitor in parallel with the feedback resistor R_{20}, the low pass frequency is set as before but at high frequencies the reactant of the capacitor dominates shorting out R_{20} reducing the amplifiers gain.

At a high enough frequency the gain bottoms out at unity (0 dB) as the amplifier effectively becomes a voltage follower so the gain equation $1 + \frac{0}{R_{19}}$ which equals 1 (unity).

3.6 High Pass Filter

In contrast to the low pass filter, there is a high pass filter. which can be referred from this link:

https://www.allaboutcircuits.com/video-tutorials/op-amps-low-pass-and-high-pass-active-filters/

Students are proposed to implement a high pass filter in Pspice and explain the behaviours of your high pass filter.

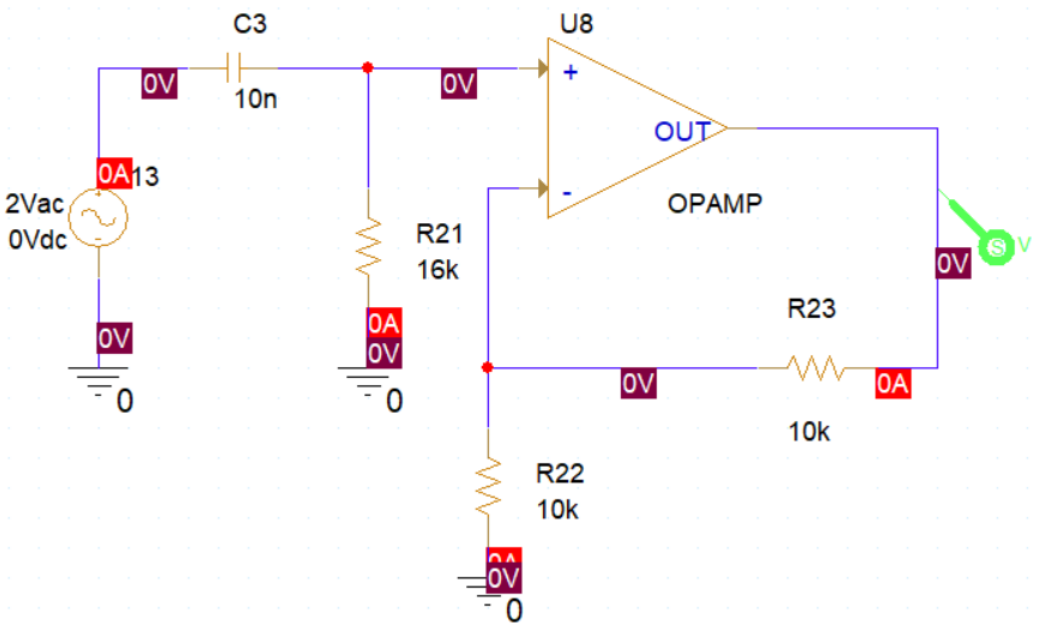

Figure 1.24: Active high pass filter with amplification.

The pass band gain of this non-inverting operational amplifier is $A_f = 2$.

The cut-off frequency is $f_c = 1(kHz)$

The capacitance C_3 is 10 (nF).

We have the formula of the cut-off frequency is: $f_c = \dfrac{1}{2\pi \times R_{21} \times C_3}$

$$\Rightarrow R_{21} = \frac{1}{2\pi \times f_C \times C_3} = \frac{1}{2\pi \times 1000 \times 10 \times 10^{-9}} = 15.92(k\Omega)$$

or 16 kΩ to the nearest preferred value.

The pass band gain of the filter, A_f is 2.

$$A_f = 1 + \frac{R_{23}}{R_{22}}$$

$$\Rightarrow \frac{R_{23}}{R_{22}} = 1$$

We can therefor select a suitable value for the two resistors of say, 10 kΩ each for both feedback resistors.

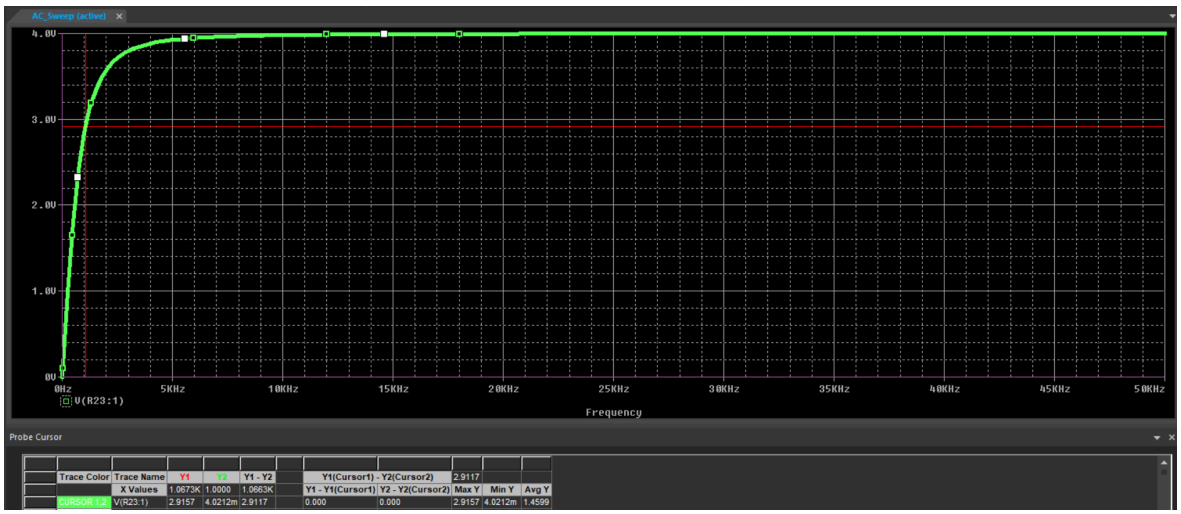

Figure 1.25: The AC sweep result.

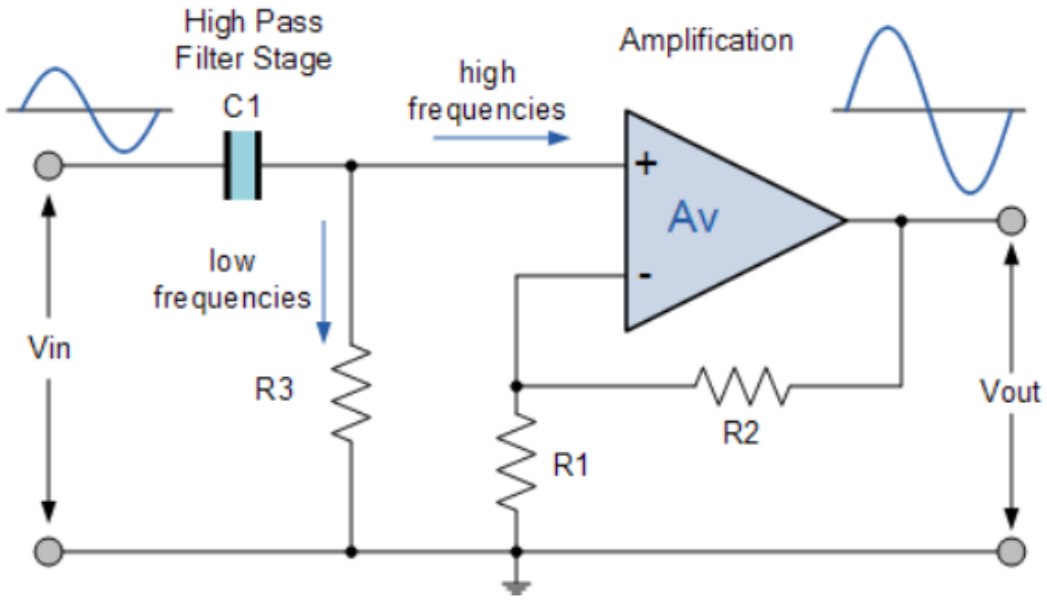

Figure 1.26: The behaviour of the active high pass filter.

This first-order high pass filter,consists simply of one op-amp, one capacitors and three resistors. The amplitude of the signal in increased by the gain of the amplifier.

It only allows the frequencies that are higher than the cut-off frequency to pass through and all of those which are lower than f_C will be filtered out.

Low frequencies are then shorted to grounf through R_3, and high frequencies are passe to the input of the op-amp. In both case, the op-amp produces a buffered version of the ouput.

3.7 Comparator with Hysteresis (Schmitt Trigger)

The two resistors R1 and R2 act only as a "pure" attenuator (voltage divider). The input loop acts as a simple series voltage summer that adds a part of the output voltage in series to the circuit input voltage. This series positive feedback creates the needed hysteresis that is controlled by the proportion between the resistances of R1 and the whole resistance (R1 and R2). The effective voltage applied to the op-amp input is floating so the op-amp must have a differential input.

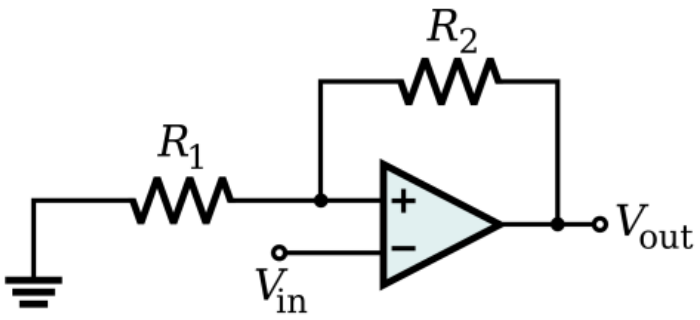

Figure 1.27: Inverting Schmitt trigger

The circuit is named inverting since the output voltage always has an opposite sign to the input voltage when it is out of the hysteresis cycle (when the input voltage is above the high threshold or below the low threshold). However, if the input voltage is within the hysteresis cycle (between the high and low thresholds), the circuit can be inverting as well as non-inverting. The output voltage is undefined and it depends on the last state so the circuit behaves like an elementary latch.

In PSPice, this trigger is implemented as follows, with 3 voltage markers:

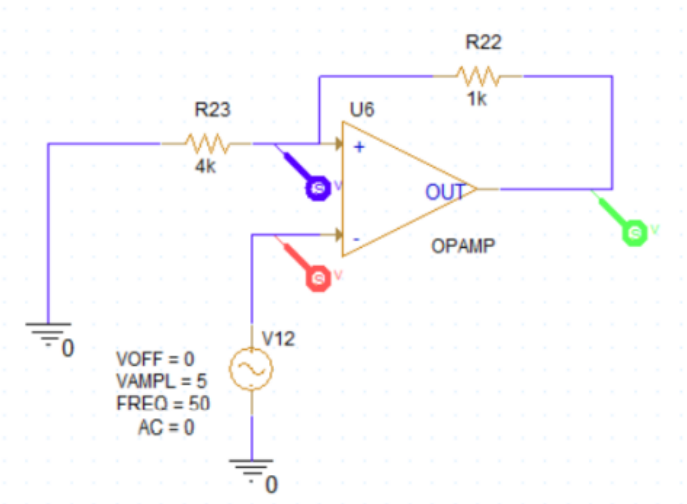

Figure 1.28: Schmitt trigger in Pspice

The OPAMP device is modified in the **Properties** windows (right click on the component and chose Edit Properties or double click on the component), in order to set the VPOS and VNEG to +5V and -5V, as follows:

The simulation profile in this exercise is the **Time Domain**, and is configured as follows:
Finally, the simulation results can be archived as follows:
Students are proposed to explain the signal at the output of the op-amp. Why the signal is toggled at +4V and -4V.

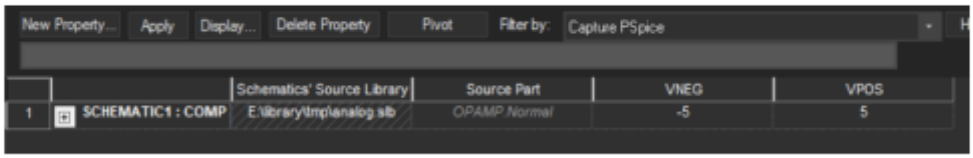

Figure 1.29: Schmitt trigger in Pspice

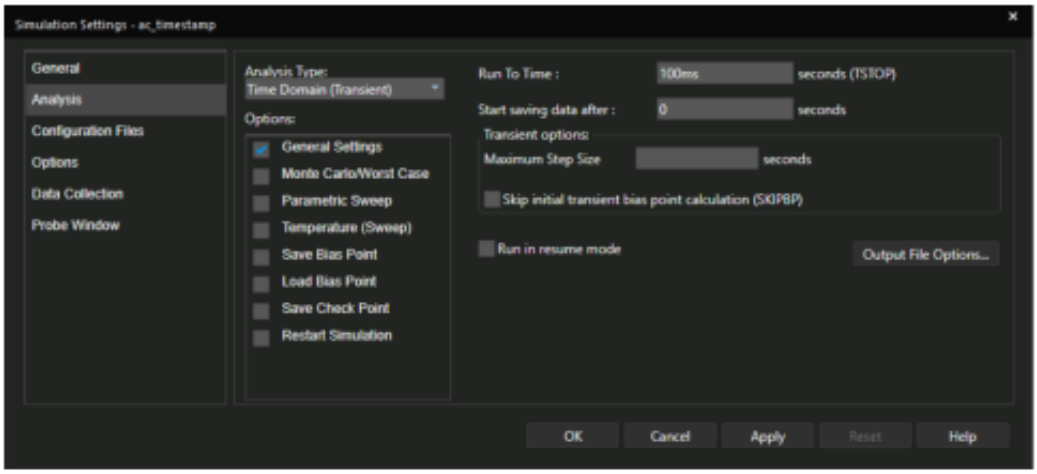

Figure 1.30: Simulation profile

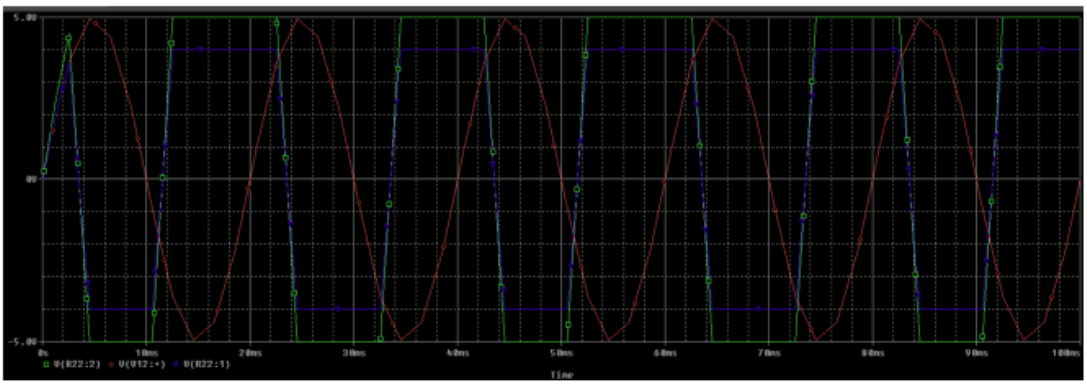

Figure 1.31: Schmitt trigger simulation results

The signal is toggled at +4V and -4V because the input loop act as a simple series voltage summer that adds a part of the output voltage in series to the circuit input voltage.

This series positive feed back creates the needed hysteresis that is controlled by the proportion between the resistances of R_1 and the whole resistance.

That is $\frac{R_1}{R_1+R_2} = \frac{4}{4+1} = 0.8$

$\frac{V_{out}}{V_{in}} = 0.8 => V_{out} = 4(V)$

4 Altium Designer

4.1 LED Driver

In this project, we will show how to build a simple LED driver circuit. A simple driver based on BJT is proposed in this section.

4.1.1 Schematic design

The manual for the schematic is posted in this link:

https://www.youtube.com/watch?v=ftiX8peTsiw

Students are proposed to design the schematic and place the results in this report.

Your image goes here

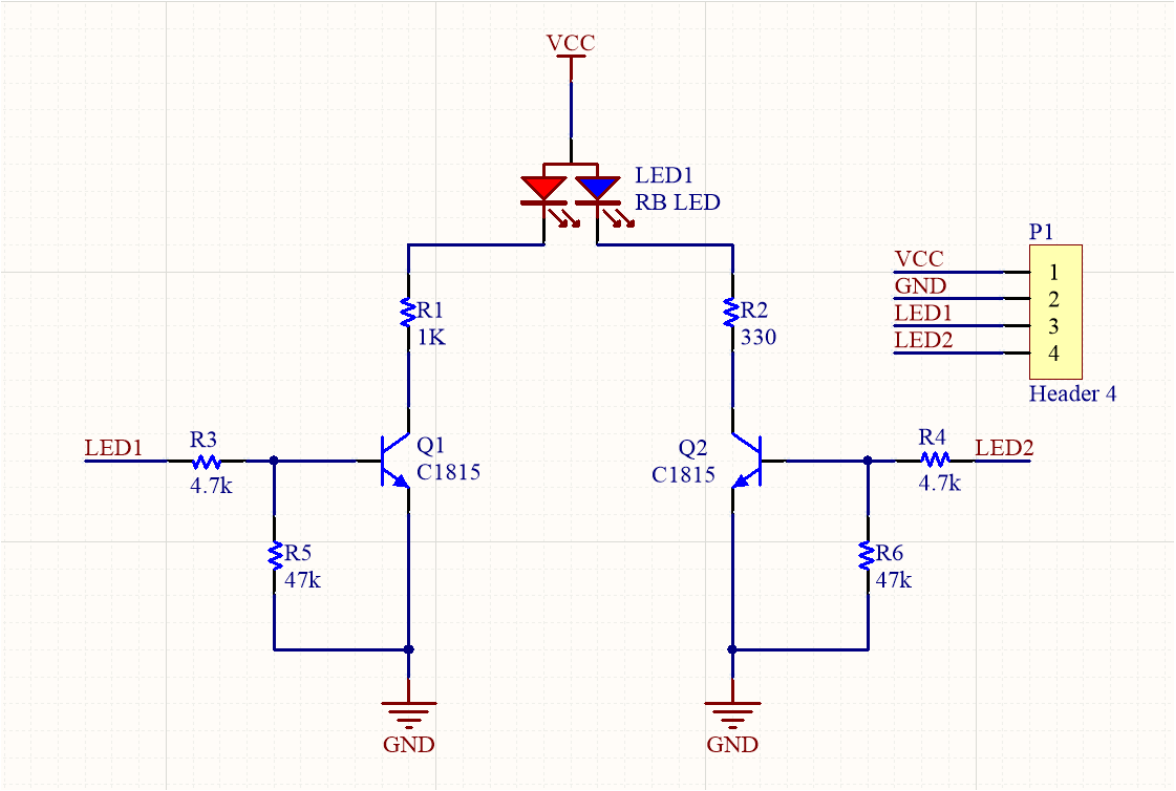

Figure 1.32: The schematic design of the LED Driver.

4.1.2 PCB layout

The manual for PCB layout is posted in this link:

https://www.youtube.com/watch?v=btpAoh3nmBU

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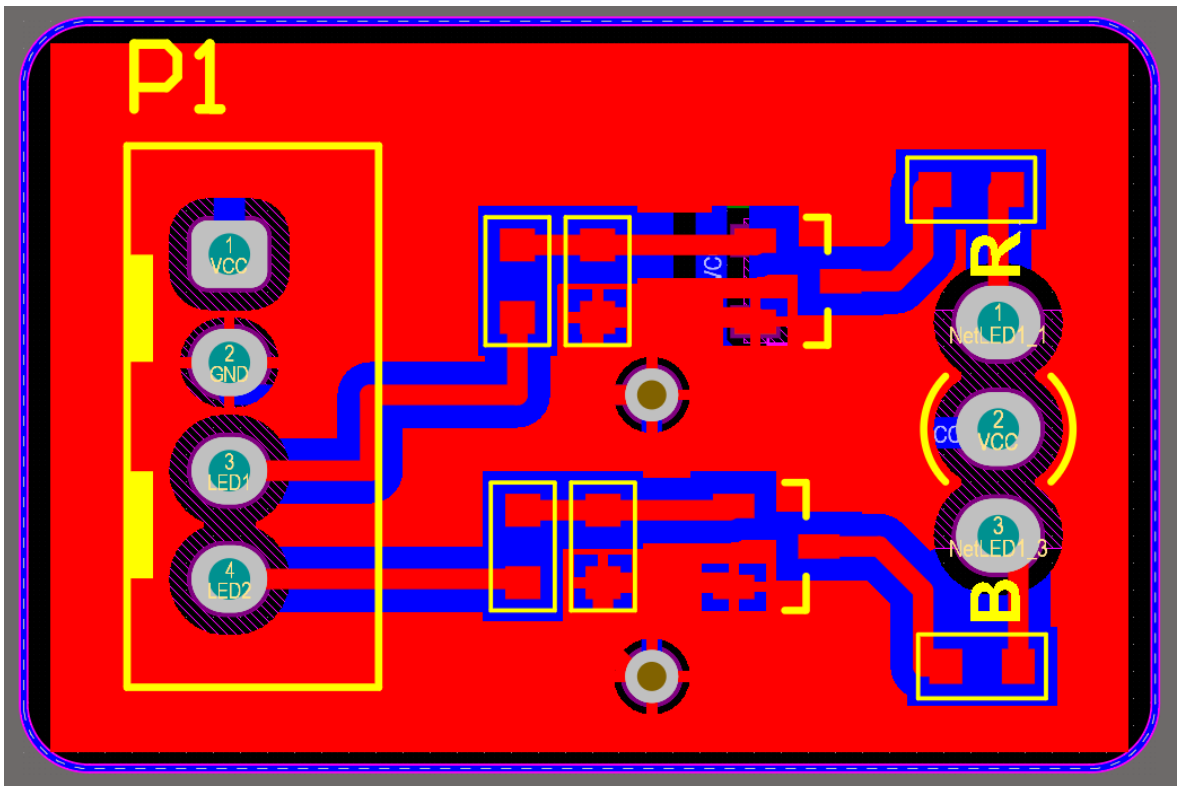

Figure 1.33: The top layer of the PCB layout.

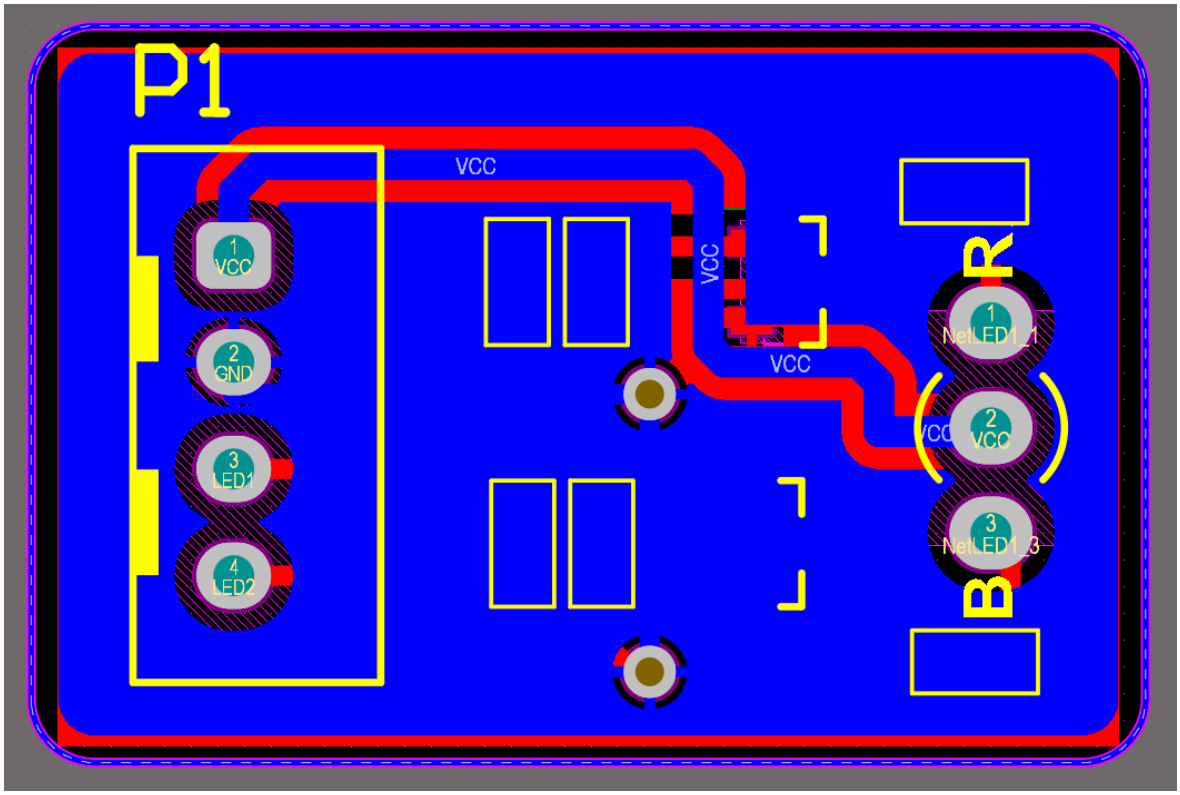

Figure 1.34: The bottom layer of the PCB layout.

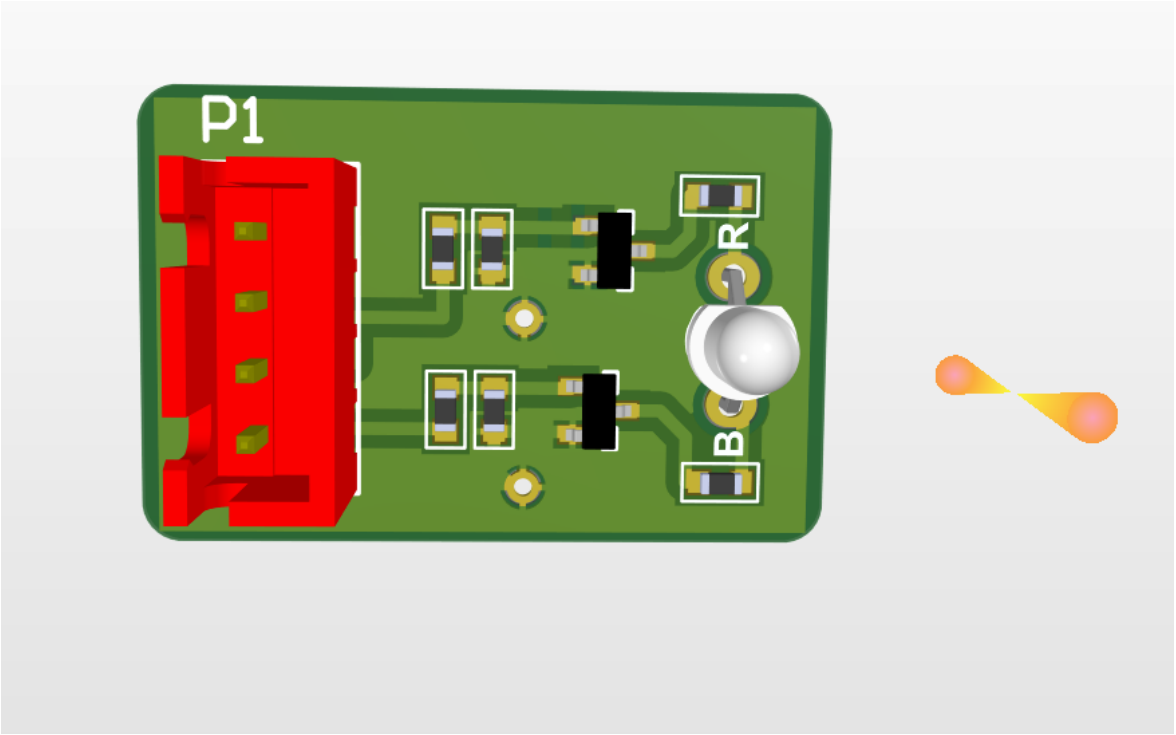

Figure 1.35: The top view of the LED Driver in 3D.

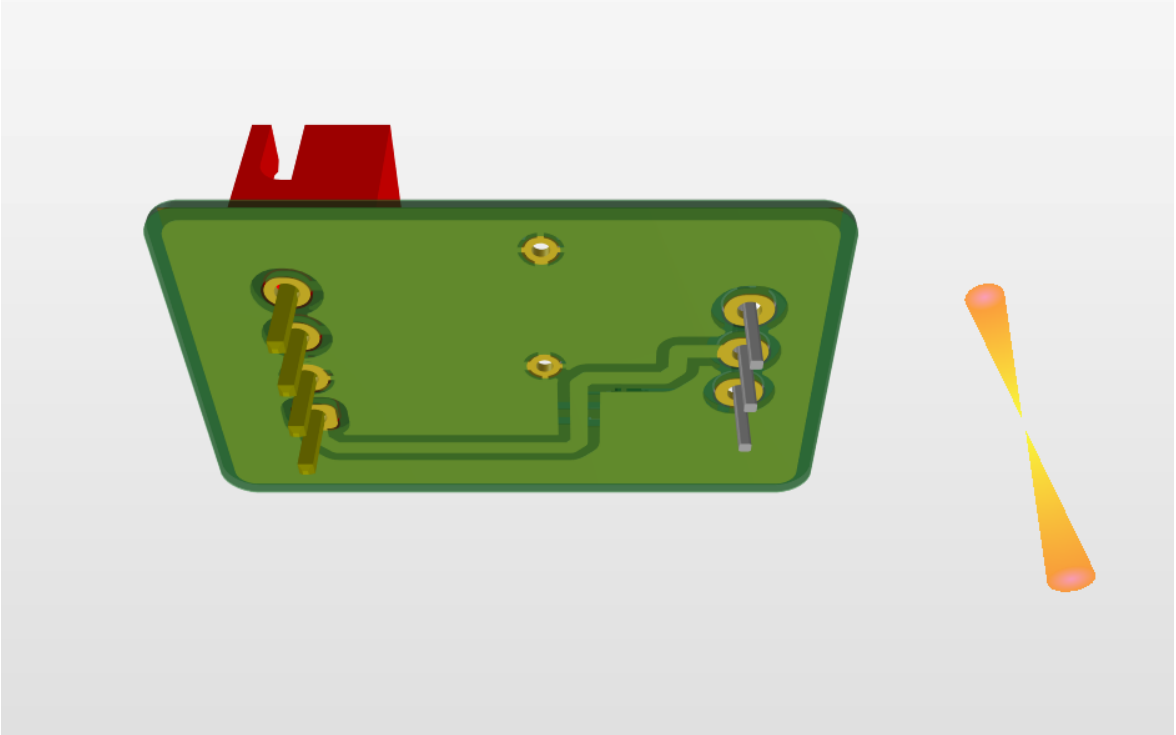

Figure 1.36: The bottom view of the LED Driver in 3D.

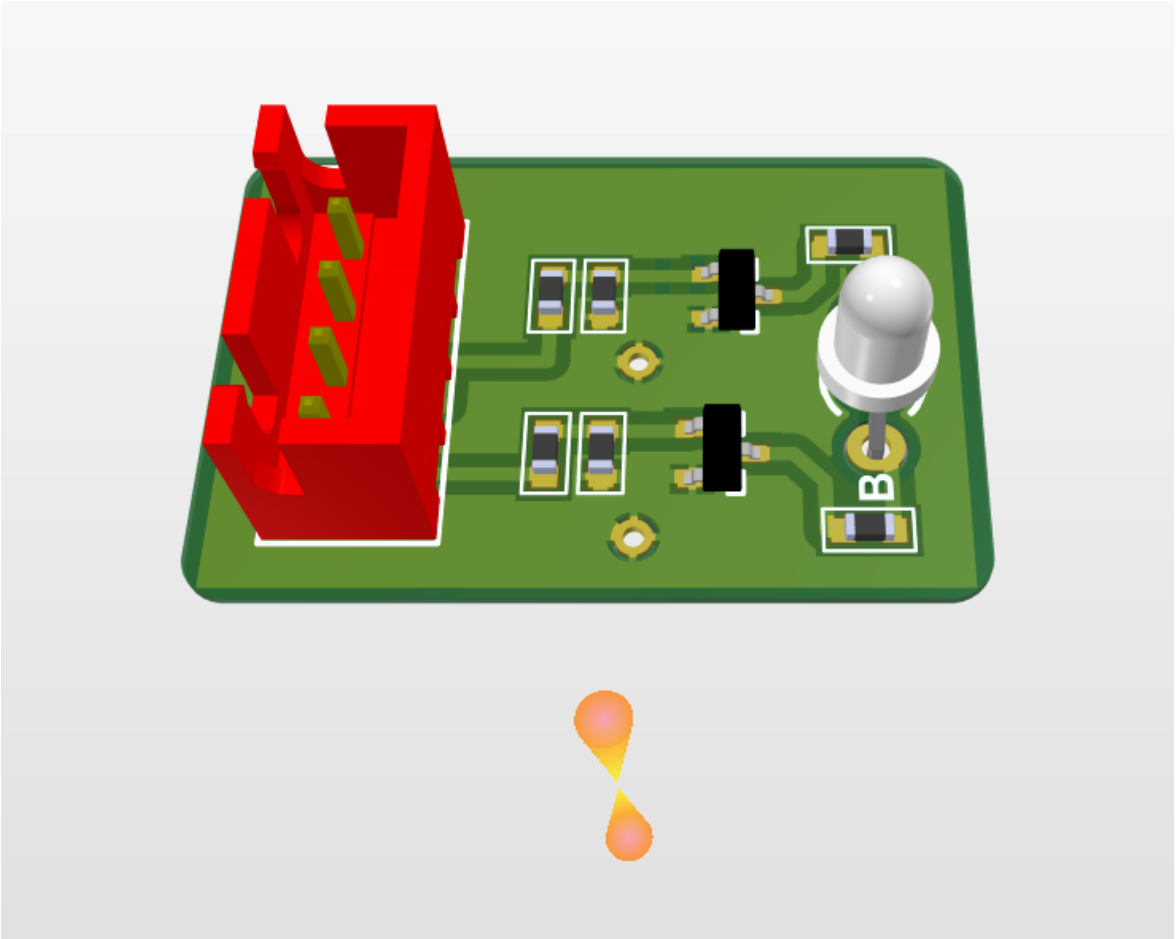

Figure 1.37: The LED Driver in 3D.

4.2 Relay Controller

4.2.1 Schematic design

The manual for the schematic is posted in this link:

https://www.youtube.com/watch?v=VcO_F97ydFM

Students are proposed to design the schematic and place the results in this report.

Your image goes here

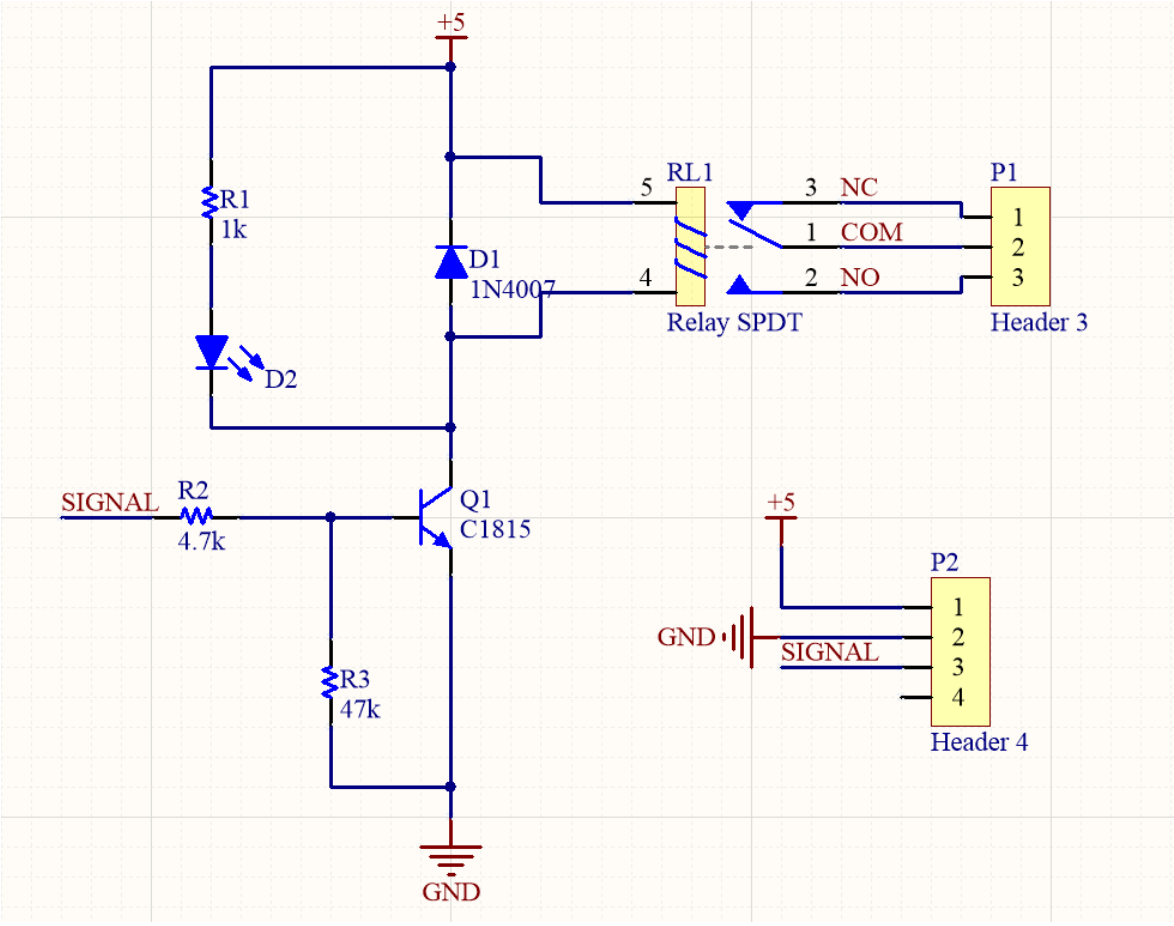

Figure 1.38: The schematic design of the Relay Controller.

4.2.2 PCB layout

The manual for PCB layout is posted in this link:

https://www.youtube.com/watch?v=5qhReO4SxCI

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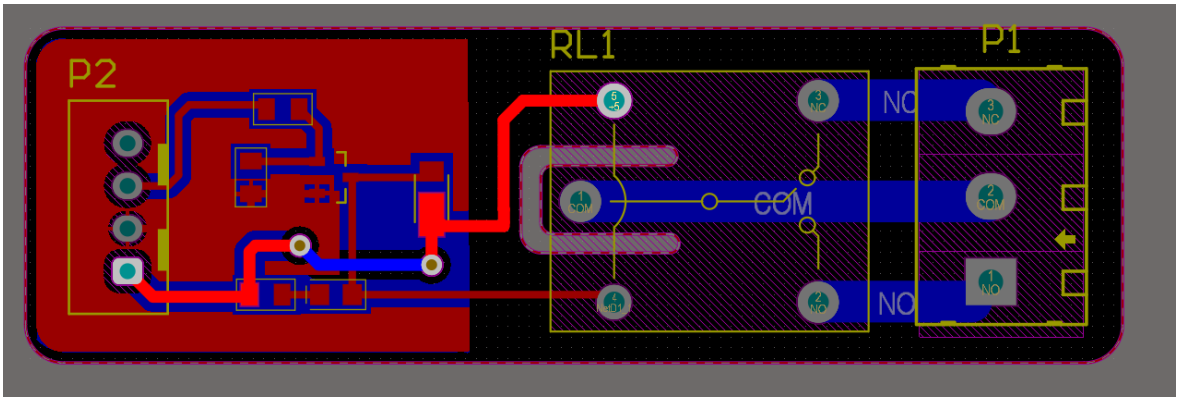

Figure 1.39: The top layer of the PCB layout.

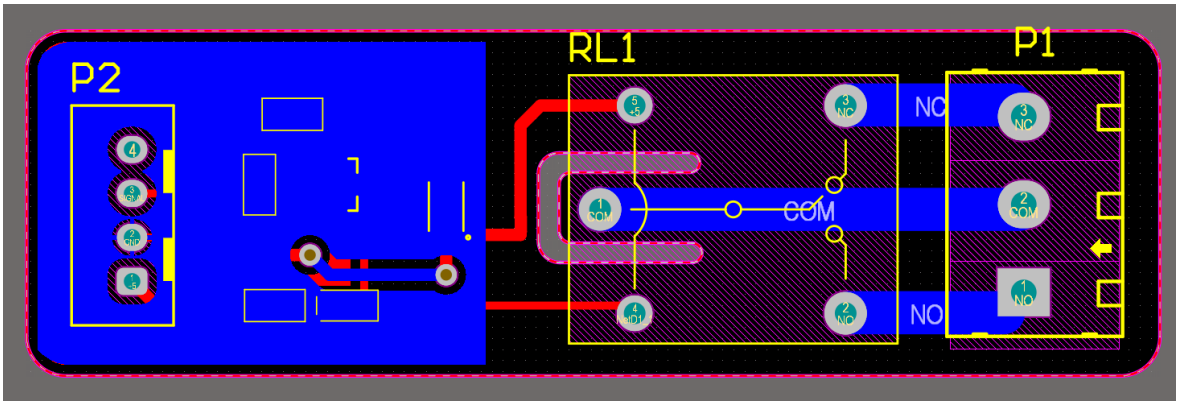

Figure 1.40: The bottom layer of the PCB layout.

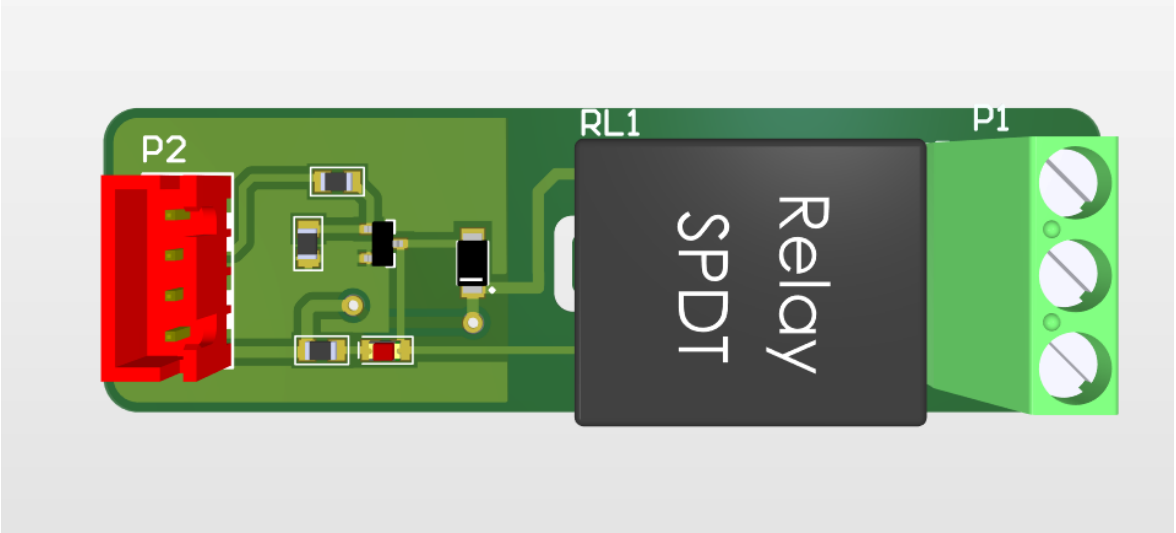

Figure 1.41: The top view of the Relay Controller in 3D.

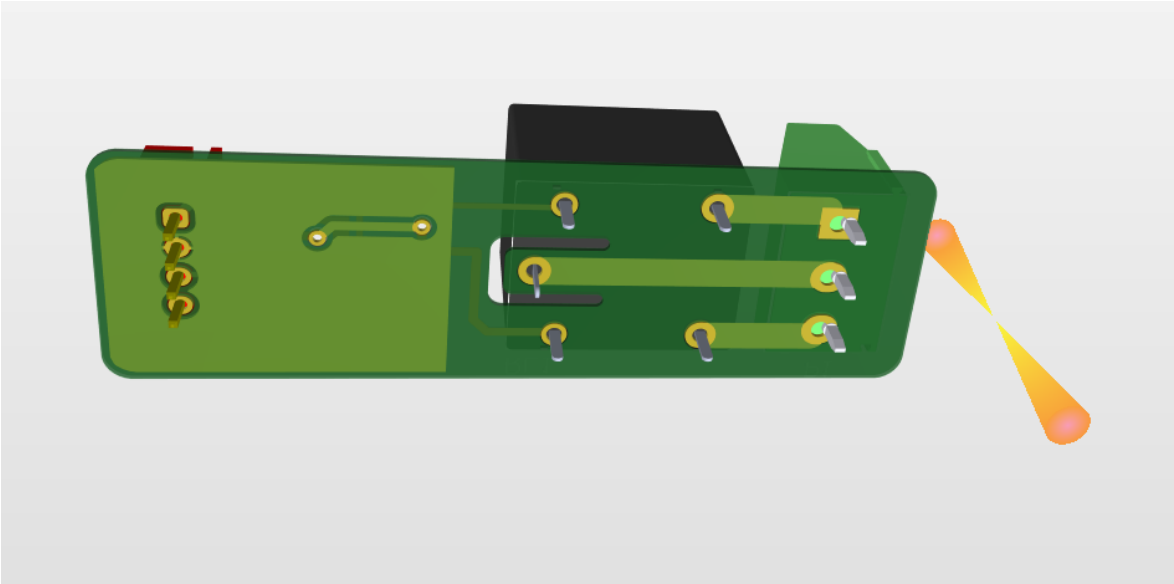

Figure 1.42: The bottom view of the Relay Controller in 3D.

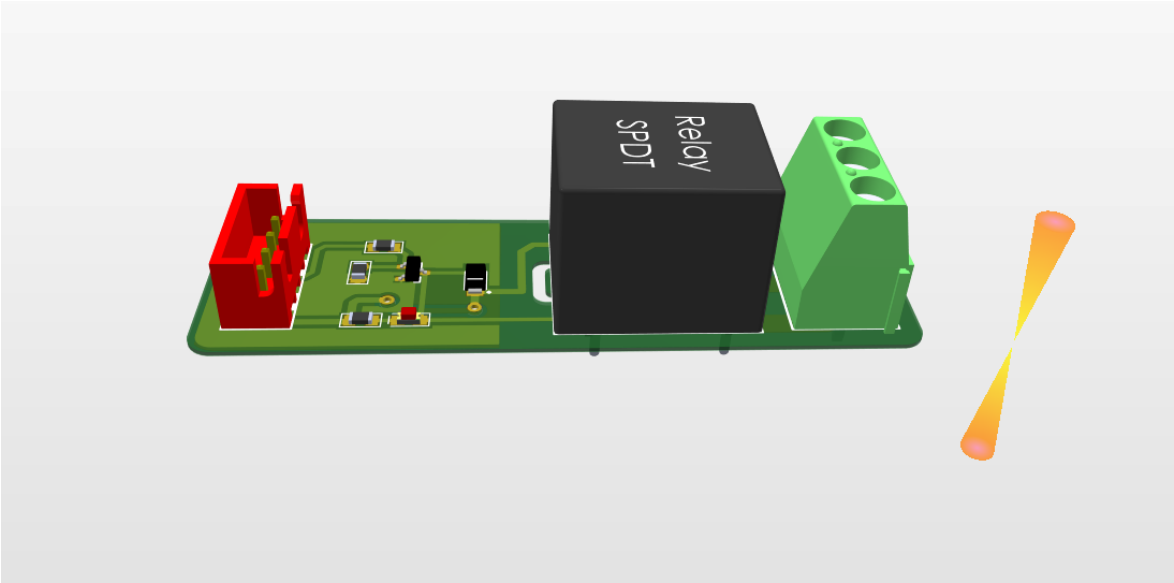

Figure 1.43: The Relay Controller in 3D.

THE END