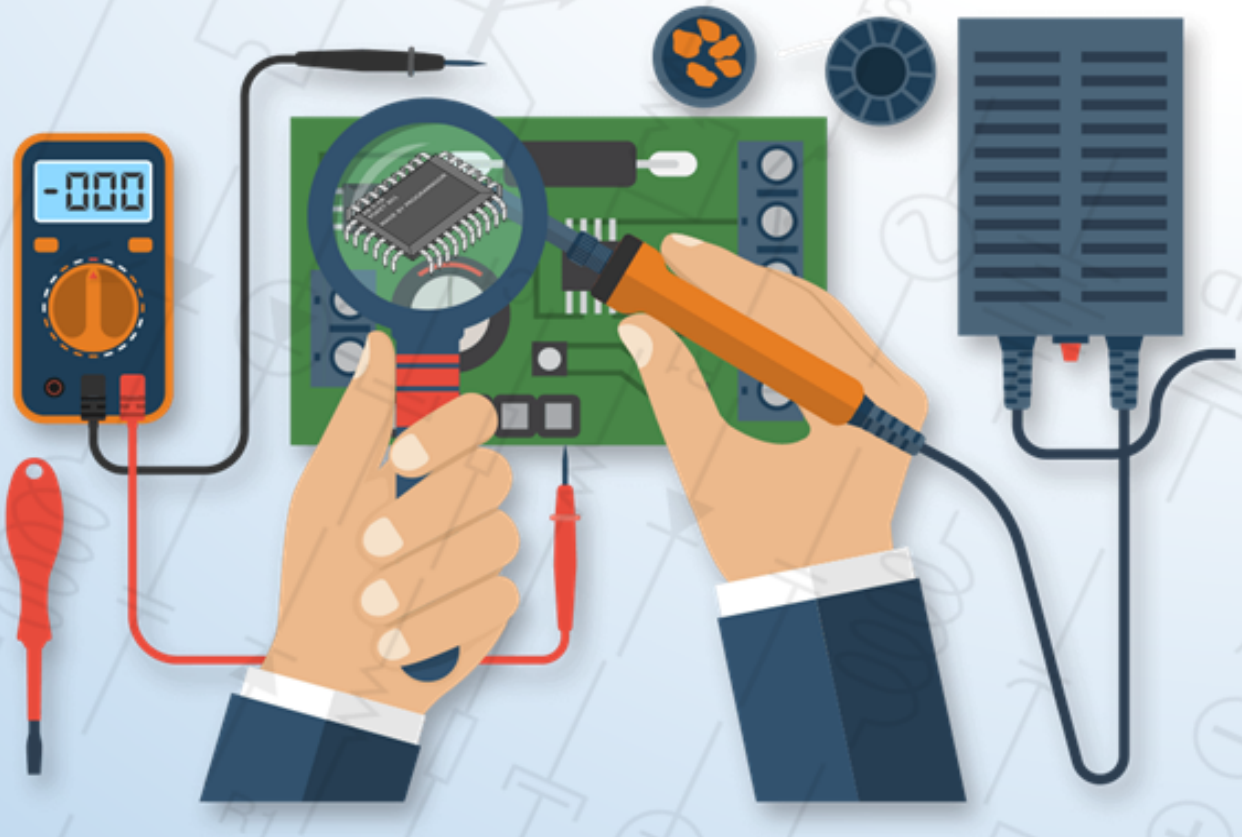
HO CHI MINH CITY UNIVERSITY OF TECHNOLOGY
COMPUTER ENGINEERING

Electronic Device Component

Lab's Report



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Contents

CHAPTER 1

Bipolar Junction Transistor

1 Introduction

In the diode tutorials we saw that simple diodes are made up from two pieces of semiconductor material to form a simple pn-junction and we also learnt about their properties and characteristics.

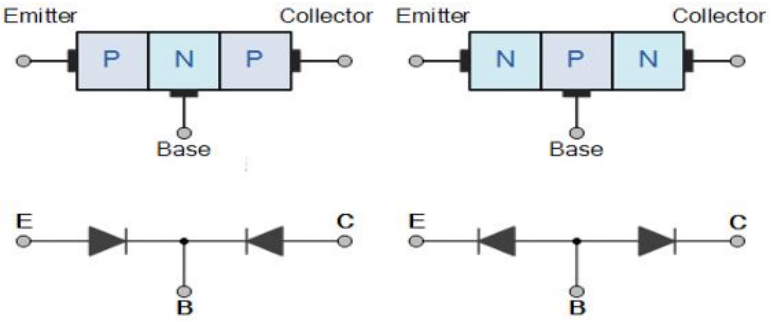

Figure 1.1: *Bipolar transistor construction*

If two individual signal diodes are joined together back-to-back, this will form a two PN-junctions connected together in series which would share a common Positive, (P) or Negative, (N) terminal. The fusion of these two diodes produces a three layer, two junction, three terminal device forming the basis of a Bipolar Junction Transistor (BJT), which is shown in the figure above.

Considering the symbol of the transistor in the schematic, the direction of the arrow always points from the positive P-type region to the negative N-type region for both transistor types, exactly the same as for the standard diode symbol.

The transistor is ability to change between these two states enables it to have two basic functions: “switching” (digital electronics) or “amplification” (analogue electronics). Then bipolar transistors have the ability to operate within three different regions:

- Active region: The transistor operates as an amplifier and $I_C = \beta I_B$
- Saturation: The transistor is “Fully-ON” operating as a switch and $I_C = I_{Sat}$
- Cut-off: The transistor is “Fully-OFF” operating as a switch and $I_C = 0$

2 BJT simulation circuit

Implement the following circuit in PSPICE. The new component used is **QBreakN NPN**, which can be found in the Favorites list. The default transistor gain is $\beta = 100$, and the saturated voltage $V_{CE(Sat)} = 0.65V$

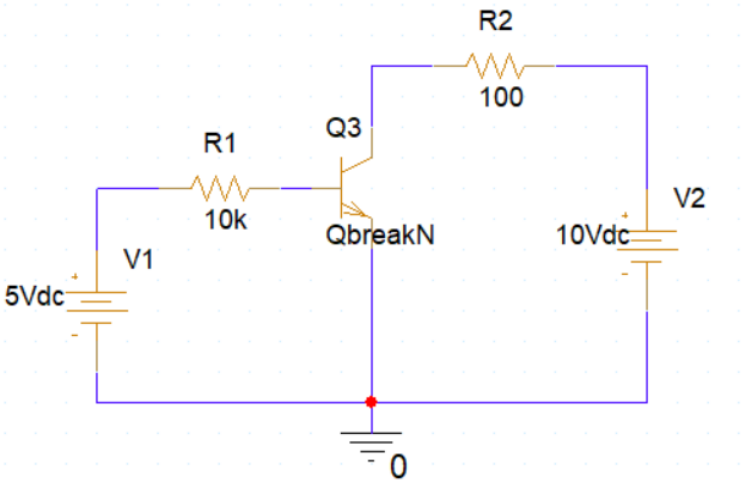

Figure 1.2: Simple connection with transistor

For a bias point simulation profile, the following results are expected:

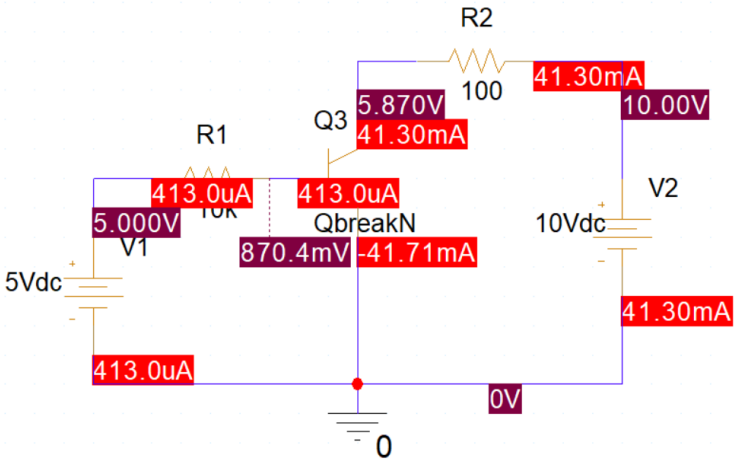

Figure 1.3: Bias profile simulation results

It is assumed that $V_{BE} = 0.7V$, the simulation results in PSPice are explained as follows:

- According to the Ohm Low, $I_B = (V_{BB} - V_{BE})/R1$ = (5V - 0.7V)/10k = 0.43mA
- It is assumed that the transistor is in linear (or active) mode, $I_C = \beta * I_B$ = 43mA
- Finally, in order to confirm the assumption above, $V_{CE} = V_{CC} - I_C * R2$ = 10V - 43mA * 100Ohm = 5.7V

Since $V_{CE} > V_{CE(Sat)}$, the transistor is working in the linear mode, to confirm our assumption. Moreover, the theory calculation is very close to the PSpice simulations.

3 Exercise and Report

3.1 BJT in Saturation Mode

Change the value of **R1 to 1k** and run the simulation again. Capture the simulation results and explain the values of I_B, I_C, V_{CE}. The default transistor gain is $\beta = 100$, and the saturated voltage $V_{CE(Sat)} = 0.65V$ and $V_{BE} = 0.7V$.
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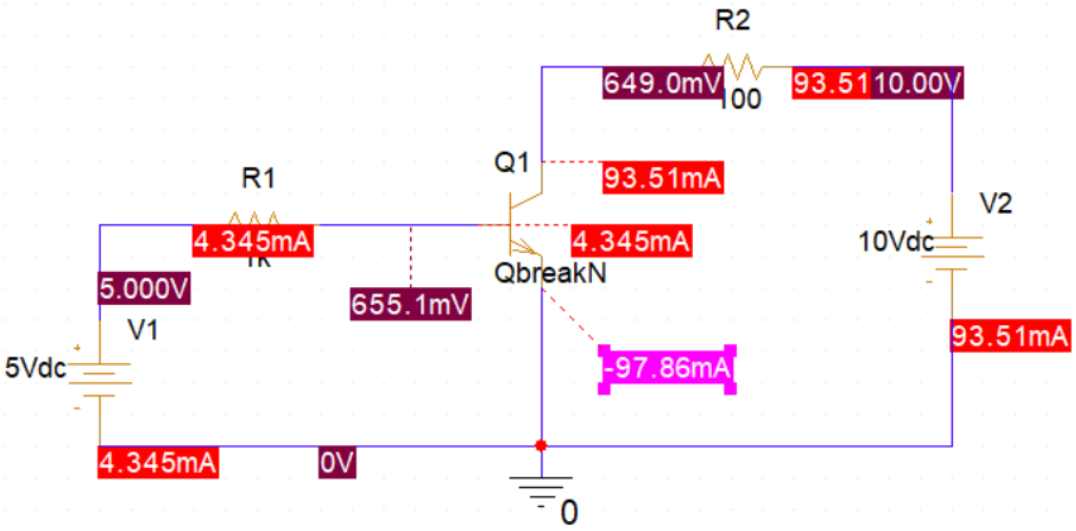

Figure 1.4: The bias point simulation of the circuit.

The results in PSpice are explained as follows:

- According to the Ohm Low, $I_B = \dfrac{V_1 - V_{BE}}{R_1} = \dfrac{5 - 0.7}{1000} = 4.3$ (mA)
- It is assumed that the transistor is in linear (or active) mode, $I_C = \beta * I_B = 100 \times 4.3 \times 10^{-3} = 0.43$ (A)
- Finally, in order to confirm the assumption above, $V_{CE} = V_{CC} - I_C * R2 = 10 - 0.43 \times 100 = -33$ (V)

Since $V_{CE} < 0$, our assumption is not correct. The transistor stays in saturation mode. Therefore, I_C is determined as follows:

$$I_C = (V_{CC} - V_{CE(Sat)})/R2 = \frac{10 - 0.65}{1000} = 93.5 \text{ (mA)}$$

3.2 DC Sweep Simulation

The schematic in the first exersice with **R1 = 1k** is re-used in this exercise. However, a DC-Sweep simulation mode is performed with V1 is varied from 0V to 5V (0.1V for the step), as follows:

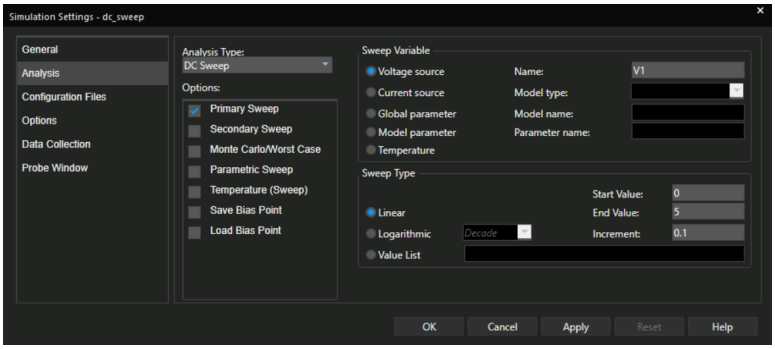

Figure 1.5: *DC-Sweep profile for simulation*

Run the simulation and trace for the current I_C according to the value of V1. Capture your screen and plot it in the report. Please increase the width of the curve.
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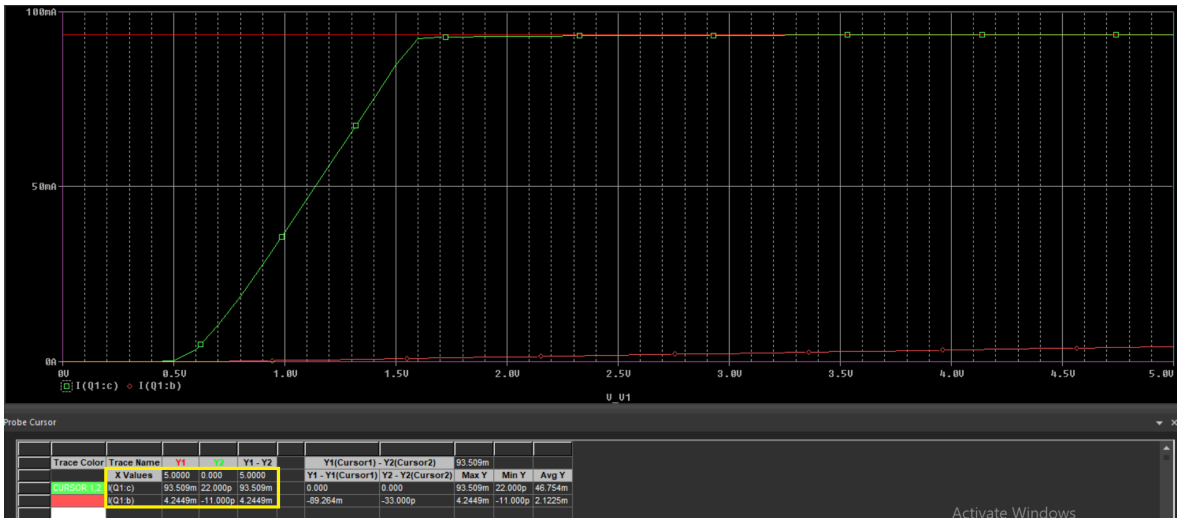

Figure 1.6: The V-I characteristic graph.

When the transistor becomes saturation, the value of V1 is 5 (V)

At this value, the value of I_B is 4.2449 (mA)

And the value of $I_{C(Sat)}$ is 93.5 (mA)

3.3 BJT used as a Switch

For a given BJT circuit, determine R1 and R2 to have IC saturated at 50mA. In this saturation mode, $V_{CE(Sat)}$ is 30mV.

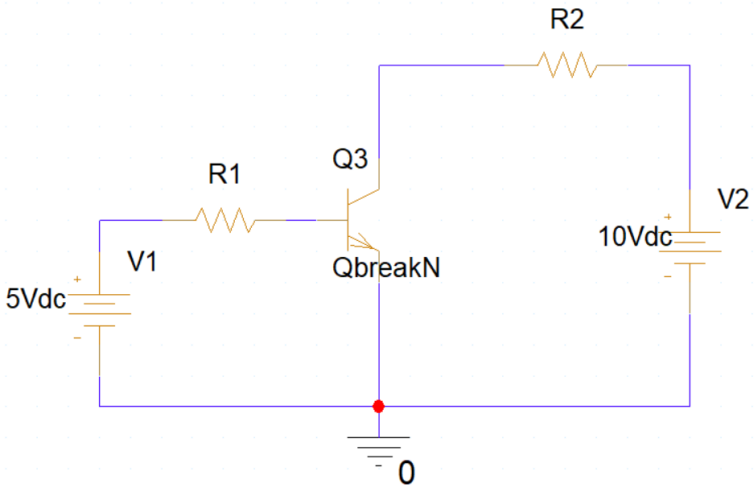

Figure 1.7: BJT used as switch in saturation mode

Present your solution to determine R1 and R2. Perform the simulation in PSpice to confirm the results. Capture the screen in PSpice and present in the report.

$$R_2 = \frac{V_{CC} - V_{CE(sat)}}{I_{C(sat)}} = \frac{10 - 30 \times 10^{-3}}{50 \times 10^{-3}} = 199.4(\Omega)$$

The maximum value of I_B in order for the circuit still works in the linear mode is:

$$I_{B_{max}} = \frac{I_{C(sat)}}{100} = 500(\mu A)$$

So whenever $I_B > I_{B_{max}} = 500(\mu A)$ the circuit will be in the saturation mode.

$$R_1 = \frac{V_{BB} - 0.7}{I_B} => R_1 < \frac{5 - 0.7}{500 \times 10^{-6}} = 8600(\Omega)$$

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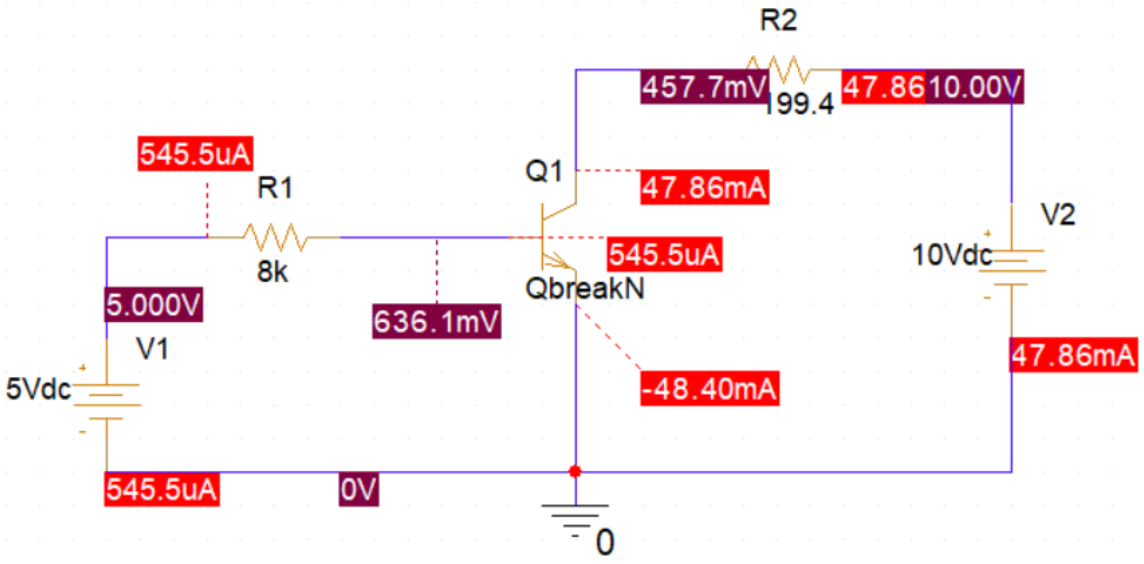

Figure 1.8: The simulation with $R_1 = 8000(\Omega)$.

3.4 Drive a device with an NPN BJT

This exercise has a $5V$ logic output (the V_{ter} in Figure 1.9) that can source up to $10mA$ of current without a severe voltage drop and stand a maximum current of $20mA$. If the logic terminal sources a current larger than $20mA$, it would be damaged. Or, if it sources a current larger than $10mA$, the V_{ter} voltage will drop to less than $4V$. We should avoid this drop in many cases. However, this logic terminal has to be used to drive an electrical component with an equivalent internal resistance of 5 ohms (the LOAD in Figure 1.9) and requires a current of at least $300mA$ and not exceeding $500mA$ to function normally. Given that we have an NPN transistor with the current gain β equals 100, the maximum I_C current is $400mA$, and the barrier potential at the BE junction is $V_{BE} = 0.7V$, select a resistor available in the market to replace the resistor R_B revealed in Figure 1.9. to make the circuit function well. After that, perform a simulation to double-check your selection.

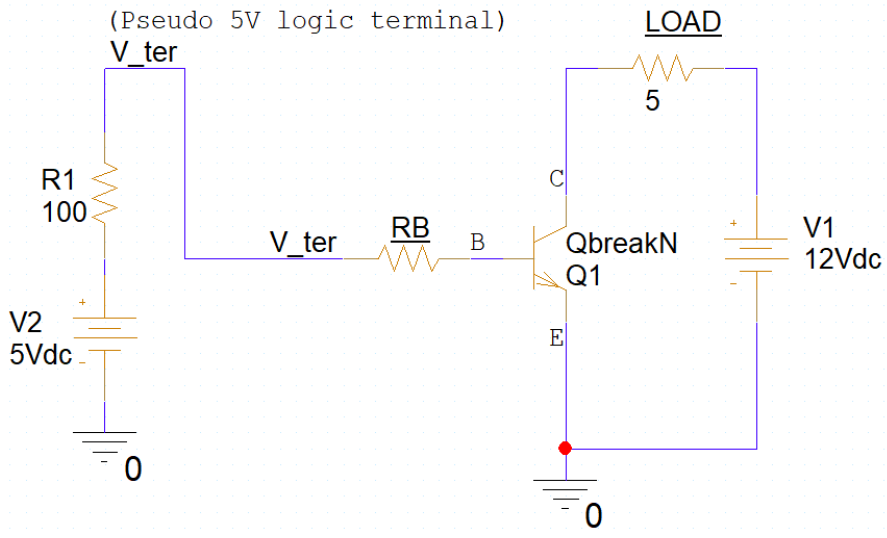

Figure 1.9: Select a resistor available in the market for R_B

3.4.1 Theory calculations

Notes:
Explanations, formulas, and equations are expected rather than only results.

According to the limits of the LOAD and the transistor, we have:

300 mA (min) $< I_C <$ 400mA(max)

3 mA (min) $< I_B <$ 4 mA (max)

With $I_B(min) = 3mA$ we have: $V_2 - I_B(min).R_1 - I_B(min).R_B - 0.7 = 0$

$$R_B(max) = \frac{V_2 - 0.7 - I_B(min).R_1}{I_B(min)} = \frac{5 - 0.7 - 3 \times 10^{-3} \times 100}{3 \times 10^{-3}} = 1333.3(\Omega)$$

With $I_B(max) = 4mA$ we have: $V_2 - I_B(max).R_1 - I_B(max).R_B - 0.7 = 0$

$$R_B(min) = \frac{V_2 - 0.7 - I_B(max).R_1}{I_B(max)} = \frac{5 - 0.7 - 4 \times 10^{-3} \times 100}{4 \times 10^{-3}} = 975(\Omega)$$

So:

$$975\ \Omega\ (\text{min}) < R_B < 1333.3\ \Omega(\text{max})$$

$$R_B \text{ selected:} 1300\Omega$$

3.4.2 Simulation

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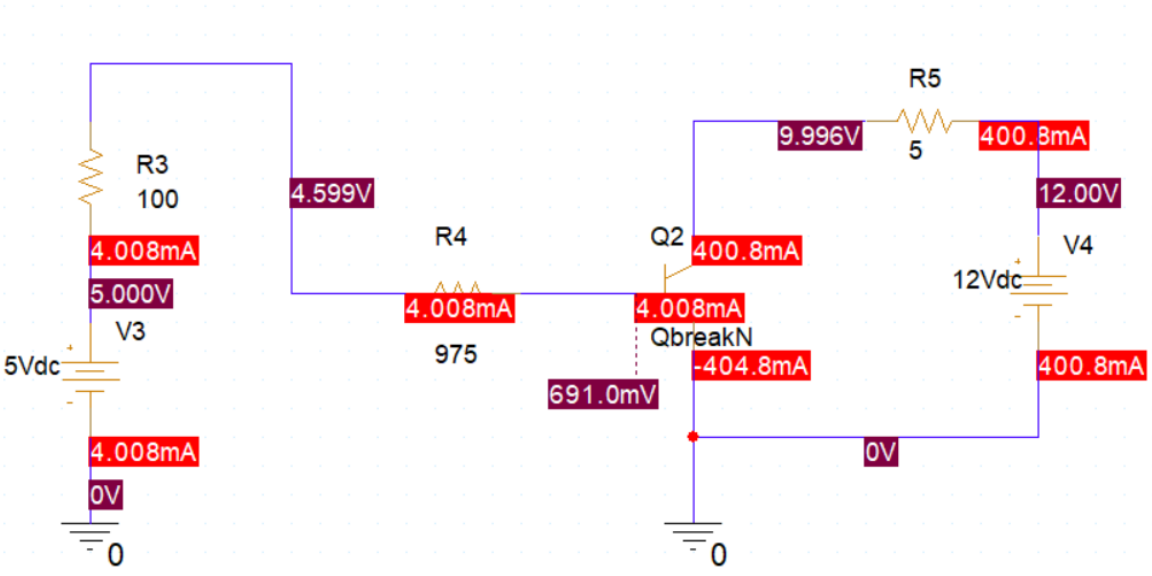

Figure 1.10: The simulation with minimum value of R_B.

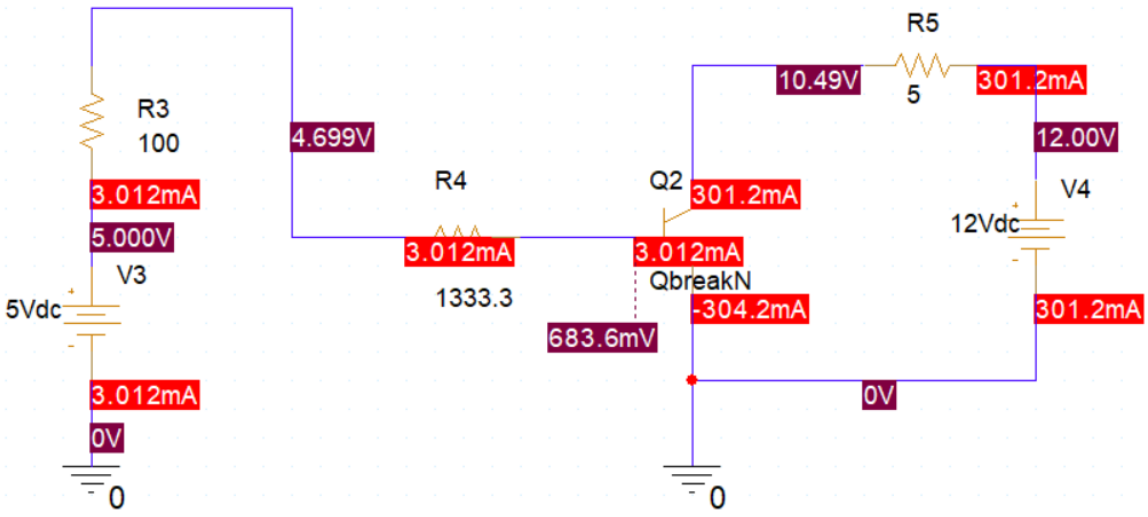

Figure 1.11: The simulation with maximum value of R_B.

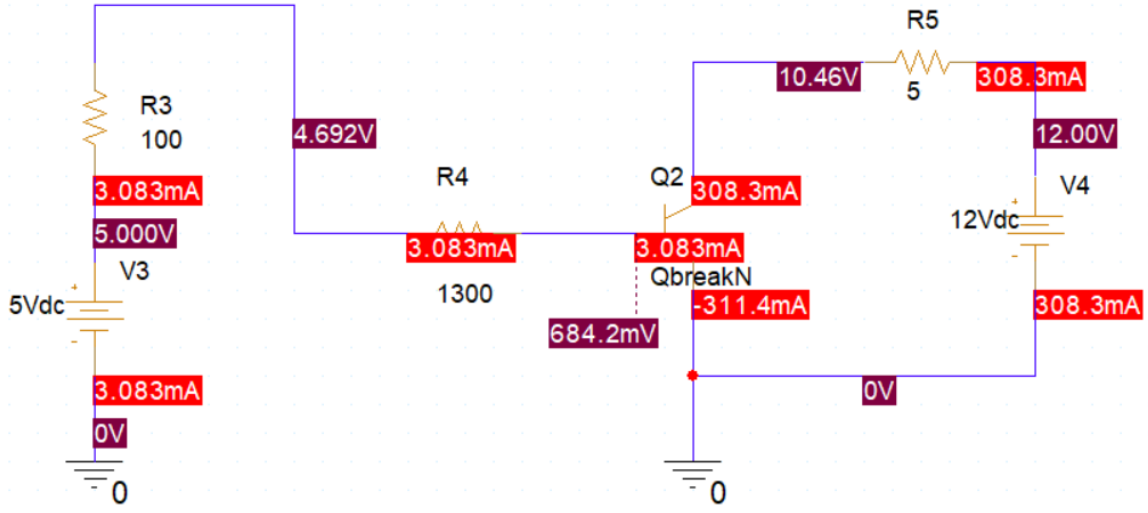

Figure 1.12: The simulation with selected value of R_B.

3.4.3 Compare

		Theory			PSpice		
	$R_B(\Omega)$	$V_{BE}(V)$	$I_B(mA)$	$I_C(A)$	$V_{BE}(V)$	$I_B(mA)$	$I_C(A)$
$R_B(min)$	975	0.7	3	0.3	0.691	4.008	0.4008
$R_B(max)$	1333.3	0.7	4	0.4	0.6836	3.012	0.3012
$R_B(selected)$	1300	0.7	3.07	0.307	0.6842	3.083	0.3083

3.5 Simple bias configuration

The circuit given in Figure 1.13 is known as a simple kind of NPN bias configuration. First, students simulate the circuit with two values of RC, respectively 10 Ohms and 1k Ohms. Then, give your statement on the change of the current I_E and explain the phenomena.

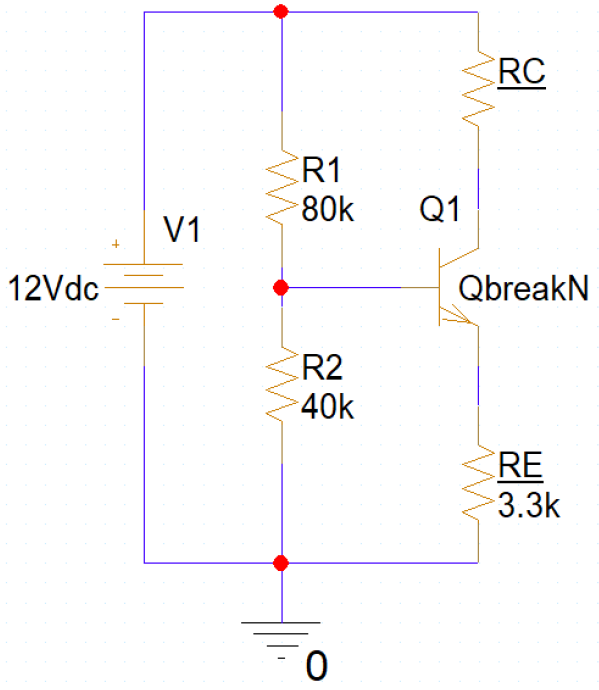

Figure 1.13: Simple bias configuration

3.5.1 Simulation

Your images go here (2 images)
Step 1: Simulate the circuit with R_C = 10 Ohms.

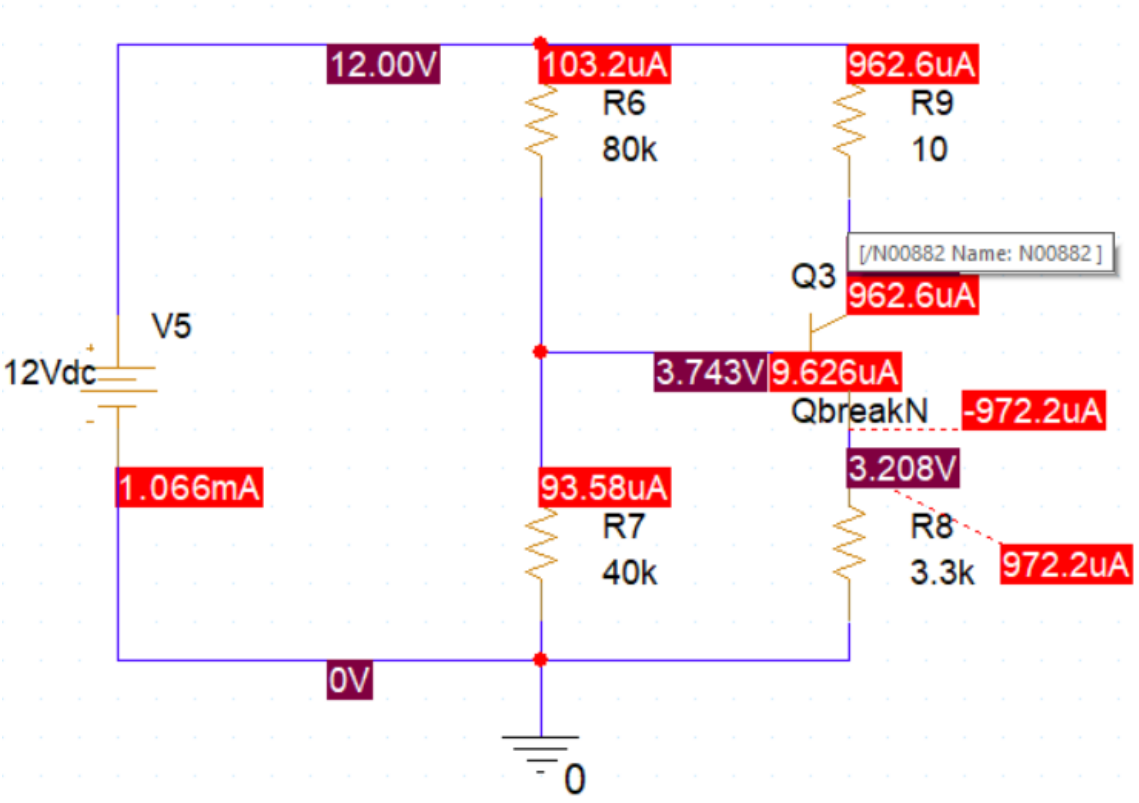

Figure 1.14: The simulation with $R_C = 10Ohms$.

Step 2: Simulate the circuit with R_C = 1k Ohms.

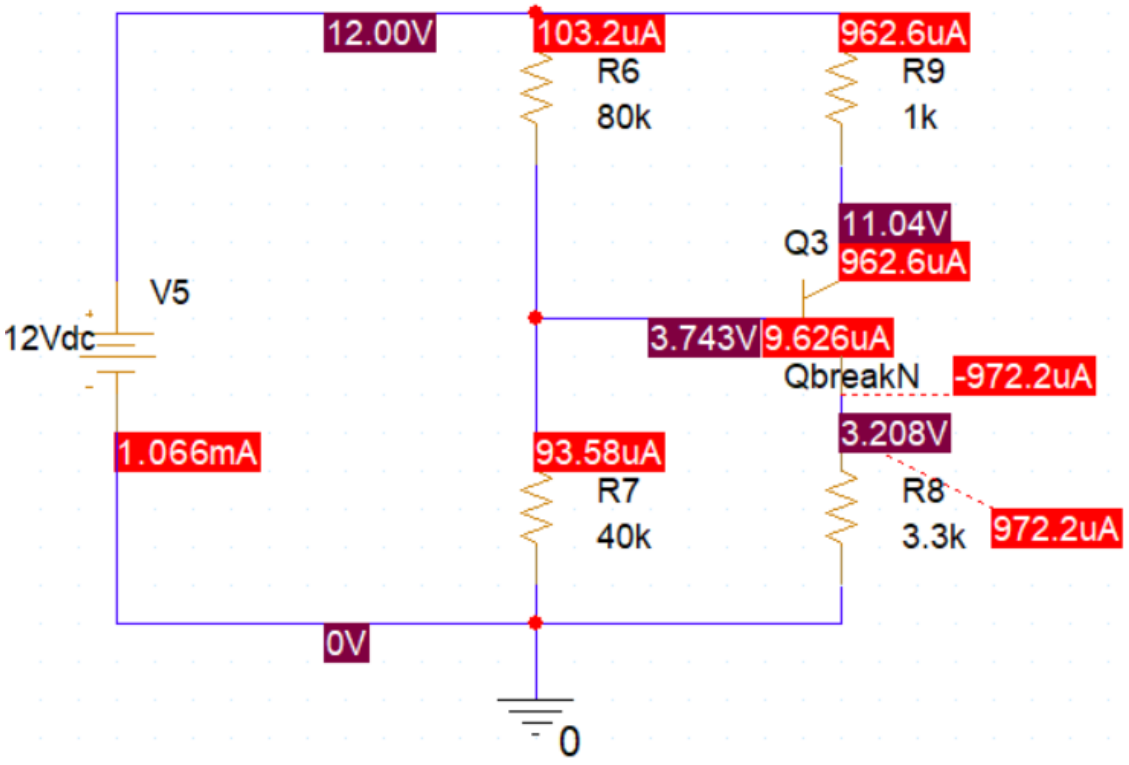

Figure 1.15: The simulation with R_C =1k Ohms.

3.5.2 Circuit analysis

Conduct some theoretical calculation to explain for the phenomena you have observed from the simulation.

First, we name the 3 nodes at middle as A,B,C from top to bottom respectively.

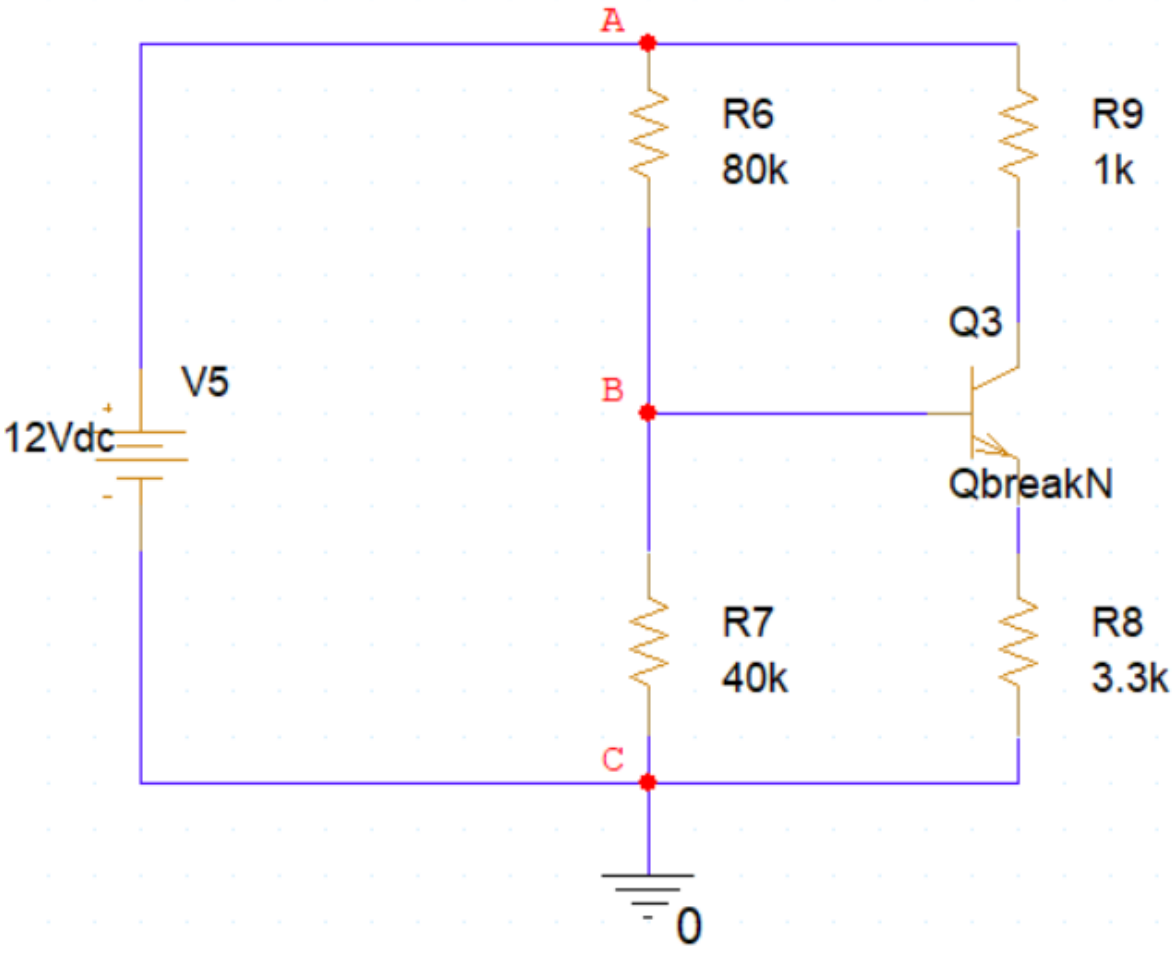

Figure 1.16: Simple bias configuration.

We have:

$$V_{AC} = V_{AB} + V_{BC} = I.R_1 + I.R_2 \Rightarrow I = \frac{V_{AC}}{R_1 + R_2} = \frac{12}{(80+40)\times 10^3} = 100(\mu A)$$

As the current I_B is relatively small so we consider it as 0 A. Thus, we would obtain:

$$V_{AB} = I.R_1 = 100 \times 10^{-6} \times 80000 = 8(V) \Rightarrow V_B = V_A - V_{AB} = 12 - 8 = 4(V)$$

$$V_E = V_B - V_{BE} = 4 - 0.7 = 3.3(V) \Rightarrow I_E = \frac{V_E}{R_E} = \frac{3.3}{3300} = 1(mA)$$

After all calculation, it is obvious that the value of I_E does not depend on R_C since we compute I_E base on V_B and the value of V_B does not change because R_1 and R_2 are kept the same in both cases.

3.6 PNP Circuit

Figure 1.17 shows a very typical PNP transistor circuit. Calculate I_B, I_E, and I_C then simulate the circuit to double-check your calculation. Assume the current gain $\beta = 100$.

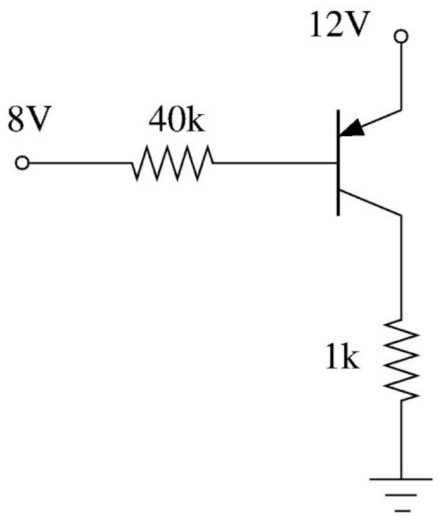

Figure 1.17: A PNP Circuit

3.6.1 Theoretical calculation

Notes:
Explanations, formulas, and equations are expected rather than only results.

$V_{EB} = 0.7(V)$

$12 - 0.7 - I_B.R_B = 8 \Rightarrow I_B = \dfrac{12 - 0.7 - 8}{R_B} = 82.5(\mu A)$

$I_C = \beta \times I_B = 100 \times 82.5 \times 10^{-6} = 8.25(mA)$

$I_E = I_B + I_E = 82.5 \times 10^{-6} + 8.25 \times 10^{-3} = 8.3325(mA)$

3.6.2 Simulation

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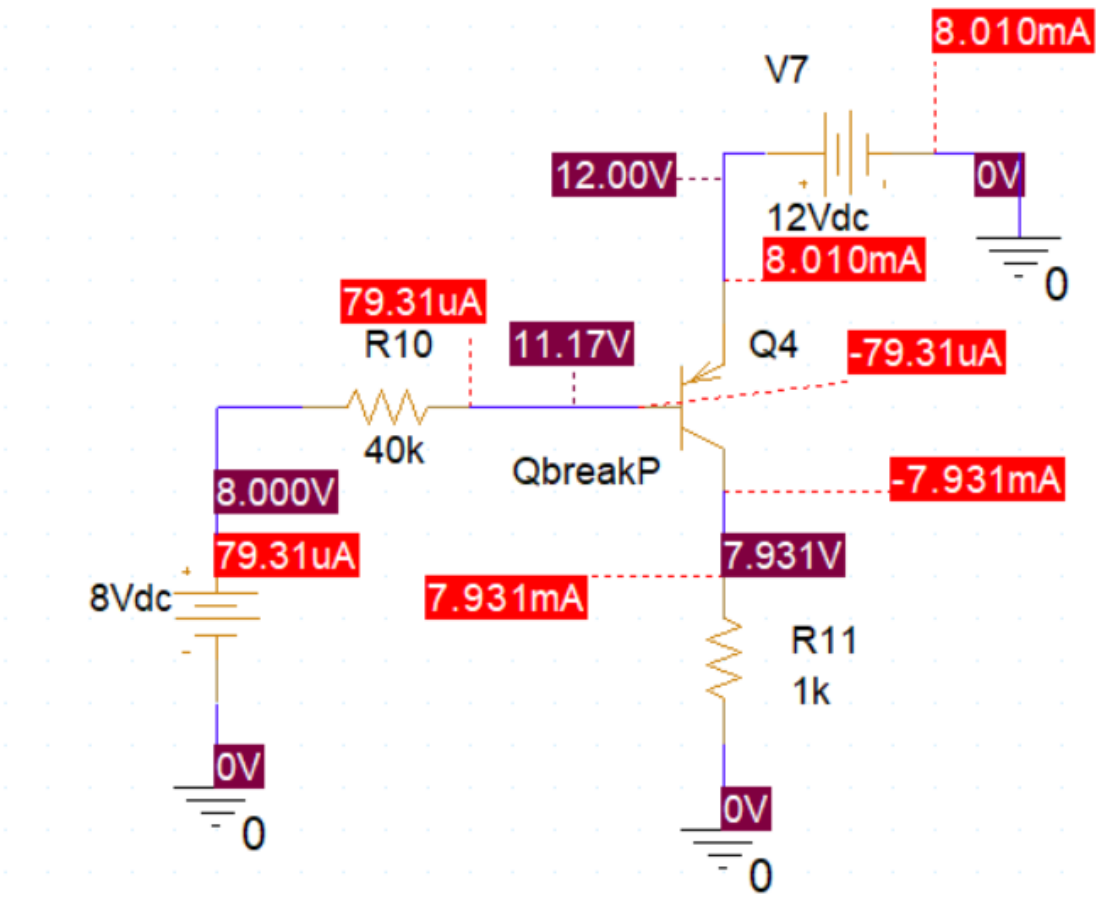

Figure 1.18: The simulation results is quite close to which obtain by theory.

3.6.3 Comparison

I_B (In theory) = 82.5(μA) I_B (simulation) = 79.31(μA)

I_C (In theory) = 8.25(mA) I_C (simulation) = 7.931(mA)

I_E (In theory) = 8.3325(mA) I_E (simulation) = 8.010(mA)

3.7 Circuit with NPN and PNP bipolar junction transistors

Give the circuit in Figure 1.19. Calculate the Voltage at all nodes and the current in all branches. Assume the current gain of both transistors is the same at β = 100. Then perform a simulation and compare the result with the theoretical calculation.

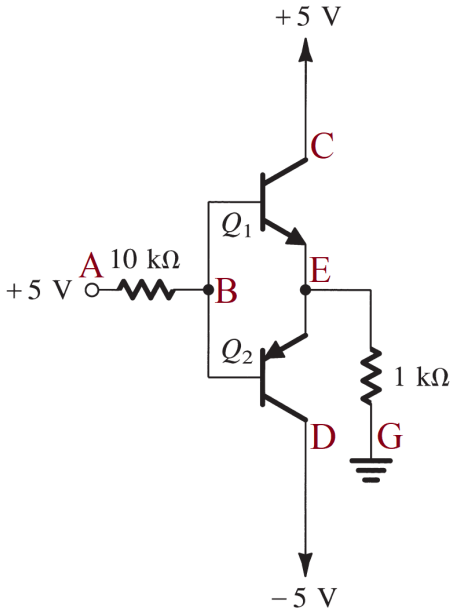

Figure 1.19: Circuit with NPN and PNP bipolar junction transistors

3.7.1 Theoretical calculation

Notes:
Explanations, formulas, and equations are expected rather than only results.

We have V_E (compare to) is less than V_B, therefore the transistor Q_2 is in cut-off mode.

According to the Kirchoff Voltage and Current Law and the properties of transistors, we have the following system of 3 equations:

$$\begin{cases} 5 - R_B.I_{BE} - 0.7 - R_E.I_{EG} = 0 \\ I_C = \beta \times I_{BE} \\ I_{EG} = I_C + I_{BE} \end{cases}$$

=>

$$\begin{cases} I_{BE} = I_B = 38.73(\mu A) \\ I_C = 3.873(mA) \\ I_{EG} = 3.91(mA) \end{cases}$$

$V_E = I_{EG}.R_E = 3.91 \times 10^{-3} \times 1000 = 3.91(V)$

$V_B = 5 - I_B.R_B = 5 - 10000 \times 38.73 \times 10^{-6} = 4.6127(V)$

3.7.2 Simulation

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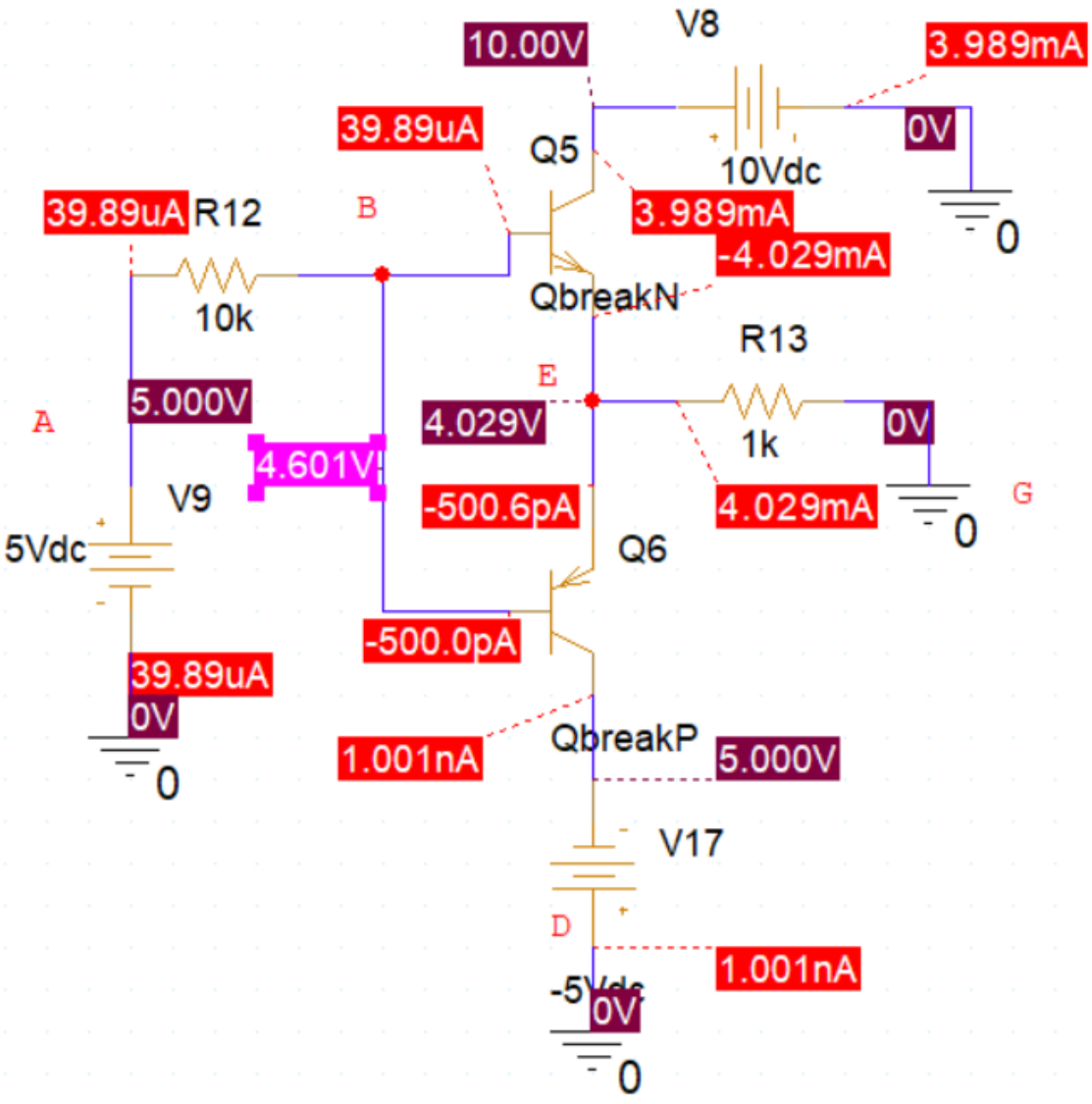

Figure 1.20: The bias point simulation.

3.7.3 Comparison

I_B (In theory) = 38.73(μA) I_B (simulation) = 39.89(μA)

I_C (In theory) = 3.873(mA) I_C (simulation) = 3.989(mA)

I_{EG} (In theory) = 3.91(mA) I_{EG} (simulation) = 4.029(mA)

V_E (In theory) = 3.91(V) V_E (simulation) = 4.029(V)

V_B (In theory) = 4.6127(V) V_B (simulation) = 4.601(V)

3.8 NPN Circuit with E resistance

In Figure 1.21, calculate all the values of I_B, I_C, I_E, V_E, and V_C. Assume the voltage drop V_{BE} = 0.7V and the current gain coefficient of the transistor is β = 100. Then, perform a simulation to double-check your theoretical calculations.

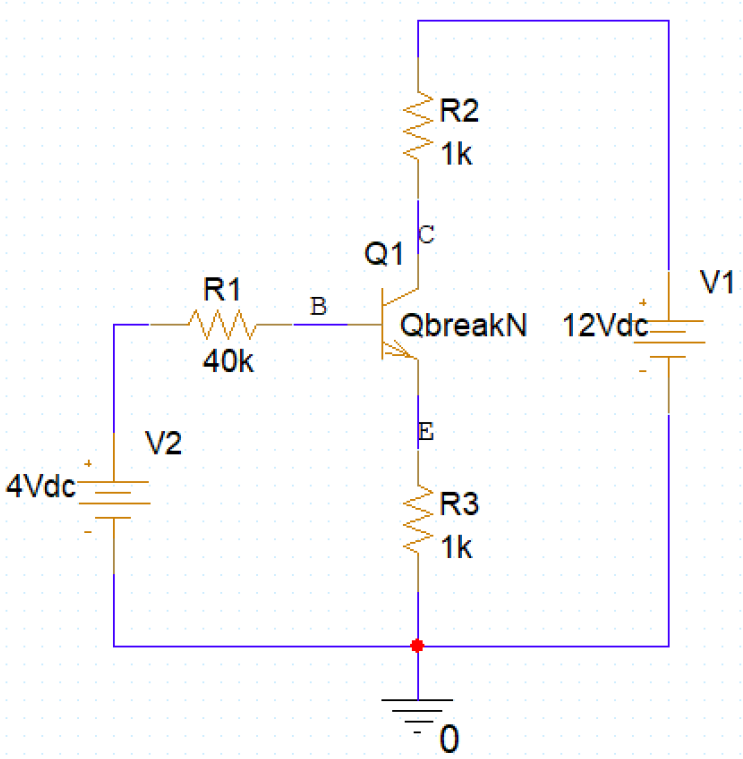

Figure 1.21: NPN Circuit with E resistance

3.8.1 Theoretical calculation

Notes:
Explanations, formulas, and equations are expected rather than only results.

According to the Kirchoff Voltage and Current Laws and the properties of transistors, we have the following system of three equation:

$$\begin{cases} 4 - R_1.I_B - 0.7 - R_3.I_E = 0 \\ I_C = \beta \times I_B \\ I_E = I_C + I_B \end{cases}$$

=>

$$\begin{cases} I_B = 23.4(\mu A) \\ I_C = 2.34(mA) \\ I_E = 2.36(mA) \end{cases}$$

$V_{CE} = V_2 - I_C.R_C - I_E.R_E = 12 - 2.34 \times 10^{-3} \times 1000 - 2.36 \times 10^{-3} \times 1000 = 7.3(V)$

$V_E = I_E.R_3 = 2.36 \times 10^{-3} \times 1000 = 2.36(V)$

$V_C = V_E + V_{CE} = 2.36 + 7.3 = 9.66(V)$

3.8.2 Simulation

Your image goes here

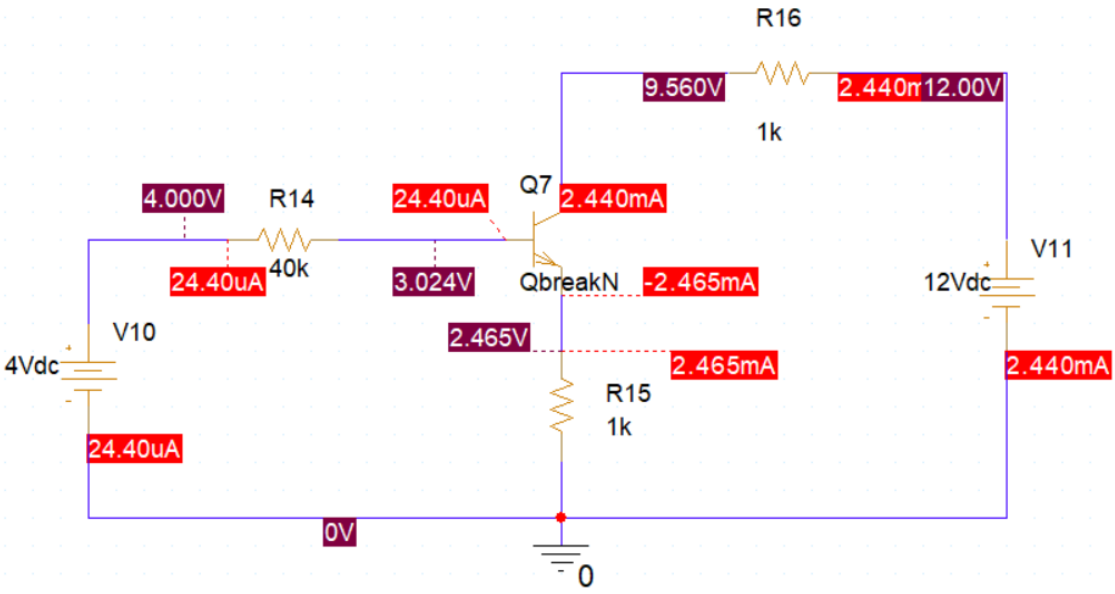

Figure 1.22: The bias point simulation.

3.9 Darlington circuit

The circuit given in Figure 1.23 is known as a darlington circuit. Calculate I_{BE}, I_{AC}, I_{AL}, and the overall current gain $\frac{I_{AL}}{I_{BE}}$. After that, simulate the circuit to double-check your theoretical calculations. Assume both transistors have the same current gain coefficient $\beta = 100$.

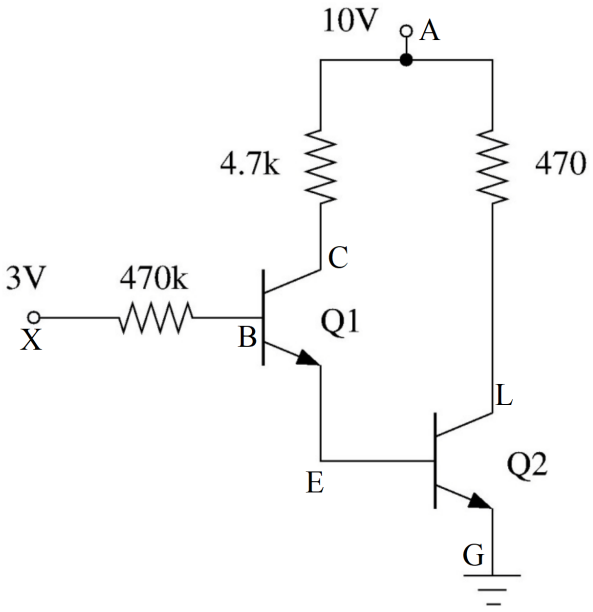

Figure 1.23: Darlington circuit

3.9.1 Theoretical calculation

Notes:
Explanations, formulas, and equations are expected rather than only results.

We have: $3 - I_B.R_B - 0.7 - 0.7 = 0 \Rightarrow I_B = \dfrac{3 - 0.7 \times 2}{470000} = 3.4(\mu A)$

Assume that Q1 is in linear mode, we have:

$I_{AC} = \beta \times I_B = 100 \times 3.4 \times 10^{-6} = 0.34(mA)$

$I_{BE} = I_B + I_{AC} = 0.3434(mA)$

$V_C = 10 - 4700.I_{AC} = 10 - 4700 \times 0.34 \times 10^{-3} = 8.402(V) > 0$

=> Our assumption is correct.

Assume that Q2 is in linear mode, we have:

$I_{AL} = \beta \times I_{BE} = 34.34(mA)$

$V_L = 10 - 470.I_{AL} = 10 - 470 \times 34.34 \times 10^{-3} = -6.1398(V) < 0$

=> Q2 is working in saturation mode.

$\Rightarrow I_{AL} = \dfrac{10 - 0.65}{470} = 19.89(mA)$

$\dfrac{I_{AL}}{I_{BE}} = \dfrac{19.89}{0.3434} = 57.92$

3.9.2 Simulation

Your image goes here

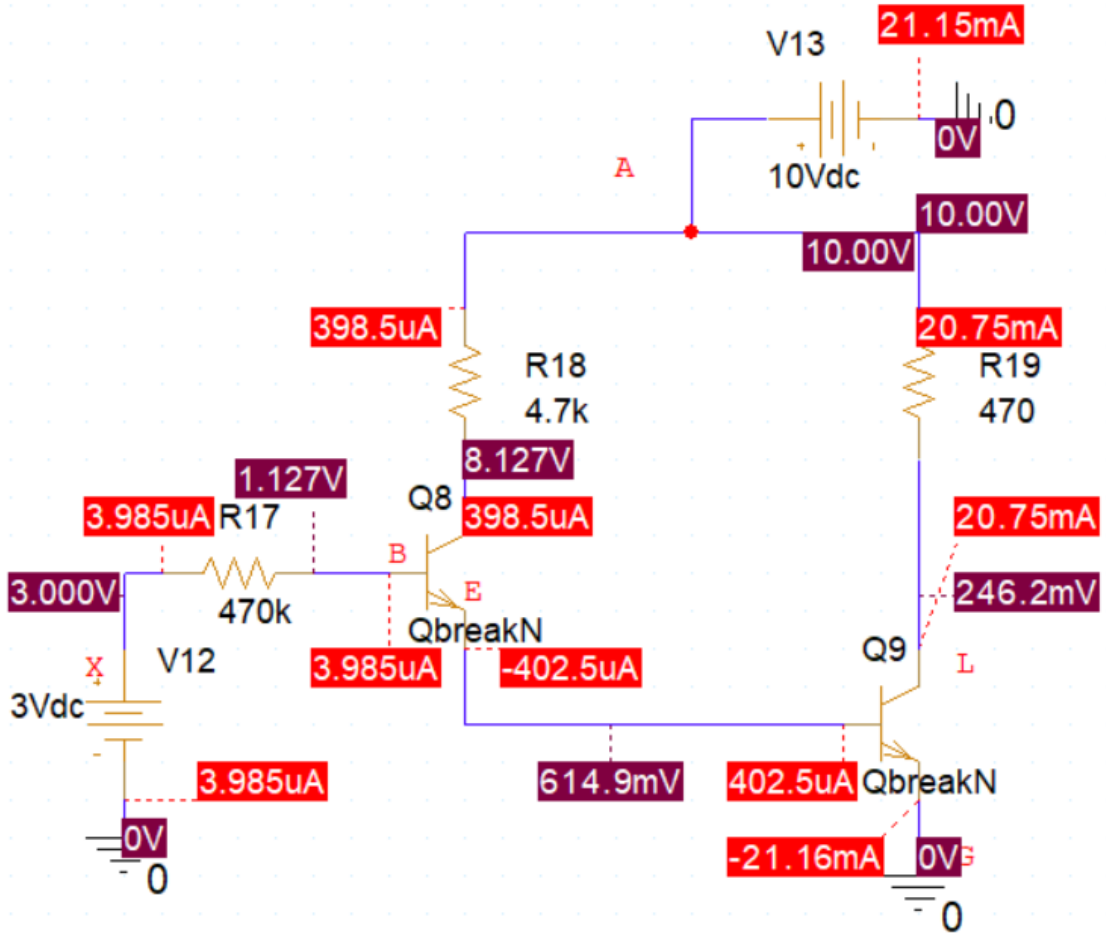

Figure 1.24: The bias point simulation.

3.10 Common base

Figure 1.25 shows a bias techniques named common base bias. Calculate the values of I_E, I_B, I_C, and V_{CE}. Then simulate the circuit to double-check your theoretical calculations. Assume the current gain coefficient β = 100.

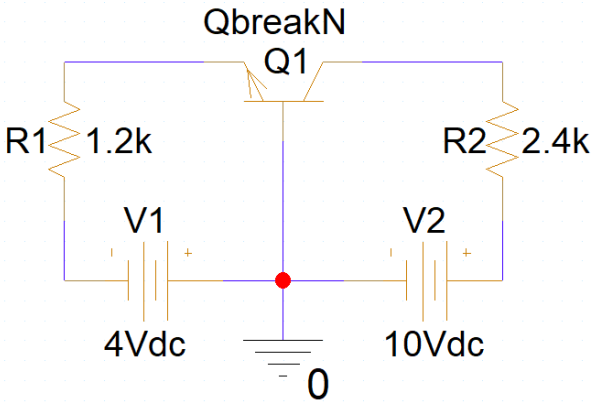

Figure 1.25: Common base

3.10.1 Theoretical calculation

Notes:
Explanations, formulas, and equations are expected rather than only results.

According to the properties of transistors we have:

$$I_E = \frac{V_1 - 0.7}{R_1} = \frac{4 - 0.7}{1200} = 2.75(mA)$$

$$I_C = \alpha \times I_E = \frac{\beta}{\beta + 1}.I_E = \frac{100}{101} \times 2.75 \times 10^{-3} = 2.723(mA)$$

$$I_B = I_E - I_C = (2.75 - 2.723) \times 10^{-3} = 27(\mu A)$$

$$V_{CB} = V_2 - I_C.R_2 = 10 - 2.723 \times 10^{-3} \times 2400 = 3.4648(V)$$

$$VCE = V_{CB} + V_{BE} = 3.4648 + 0.7 = 4.1648(V)$$

3.10.2 Simulation

Your image goes here

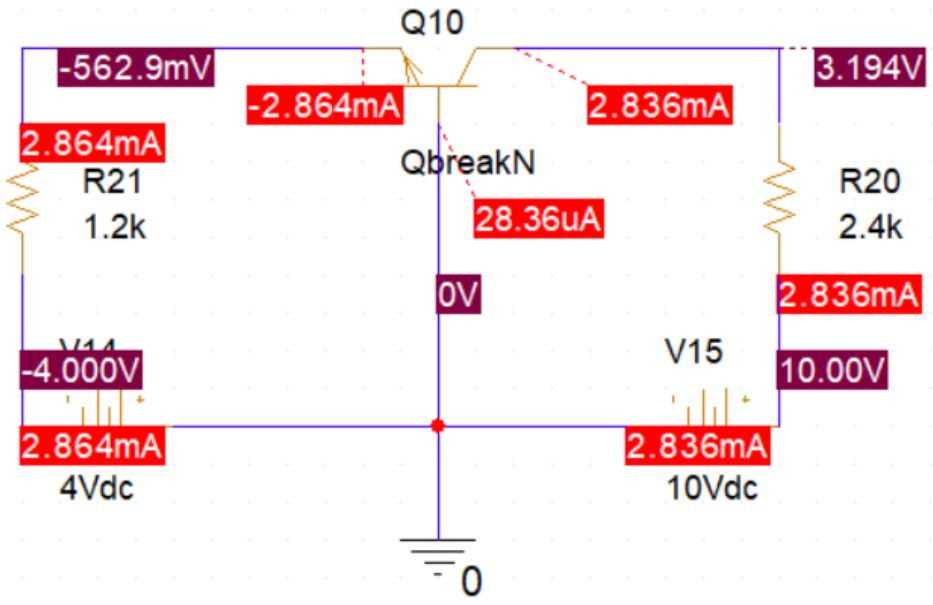

Figure 1.26: The bias point simulation.

3.11 Current mirror

The circuit shown in Figure 1.27 is known as a current mirror circuit. First, students do some theoretical calculations to get an understanding of it. After that, perform a simulation to double-check its principles and your analysis. Assume that the two transistors Q1 and Q2, are the same type and the current gain $\beta = 100$.

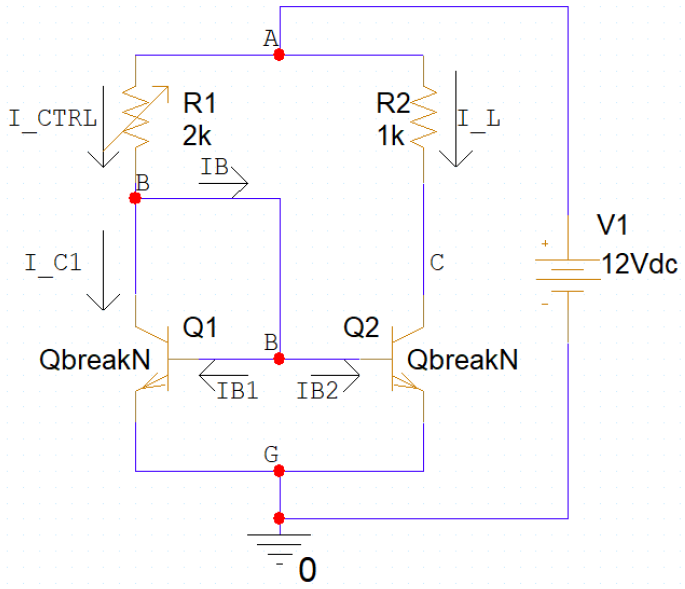

Figure 1.27: Current mirror circuit example

3.11.1 Theoretical calculation

Notes:
Explanations, formulas, and equations are expected rather than only results.

According to the Kirchoff Voltage Law, we have:

$$12 - I_{CTRL}.R_1 - 0.7 = 0 \Rightarrow I_{CTRL} = \frac{12 - 0.7}{2000} = 5.65(mA)$$

According to the Kirchoff Current Law and the properties of transistor, we can obtain the following system of 3 equations:

$$\begin{cases} I_{CTRL} = I_{C1} + I_{B1} + I_{B2} \\ I_{C1} = \beta \times I_{B1} \\ I_{B1} = I_{B2} \end{cases}$$

=>

$$\begin{cases} I_{C1} = 5.53(mA) \\ I_{B1} = I_{B2} = 35.4(\mu A) \end{cases}$$

$$I_L = \beta \times I_{B2} = I_{C1} = 5.53(mA)$$

3.11.2 Simulation

Your image goes here

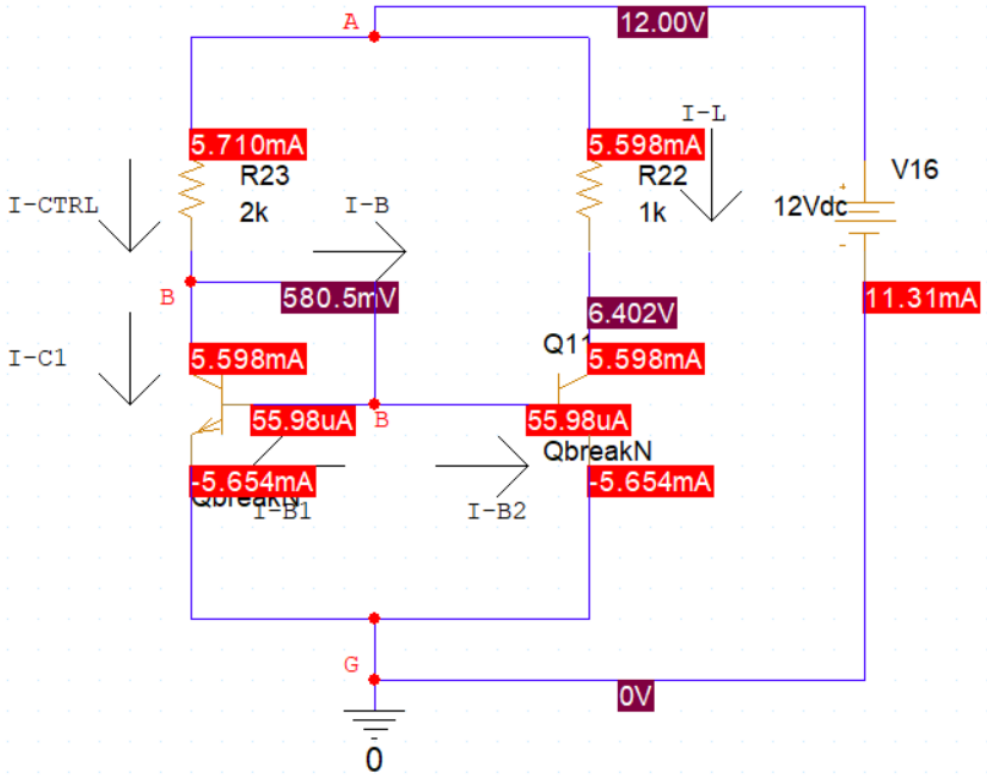

Figure 1.28: The bias point simulation.

Why is the circuit in Figure 1.27 called circuit mirror?

-> The reason why this circuit is called current mirror is that the current through 2 outer branches I_{C1} and I_L are equal. Besides, the value of the currents enter two transistors are also the same.

Now, replace the resistor R_1 with a 100-Ohms one. Next, calculate all the values again. Then, finally, simulate the new circuit and explain the phenomena you've observed.

Using the same technique we can obtain:

$$I_{CTRL} = \frac{12 - 0.7}{100} = 113(mA)$$

$$I_{C_1} = 110.78(mA)$$

$$I_{B_1} = I_{B_2} = 1.1078 \text{ (mA)}$$

Assume that Q2 is in linear mode, we have:

$$I_L = 110.78(mA)$$

$V_C = 12 - 1000.I_L = 12 - 1000 \times 110.78 \times 10^{-3} = -98.78(V) < 0$, so Q2 is working in saturation mode.

$$=> I_L = \frac{12 - 0.65}{1000} = 11.35(mA)$$

The 2nd simulation result goes here:

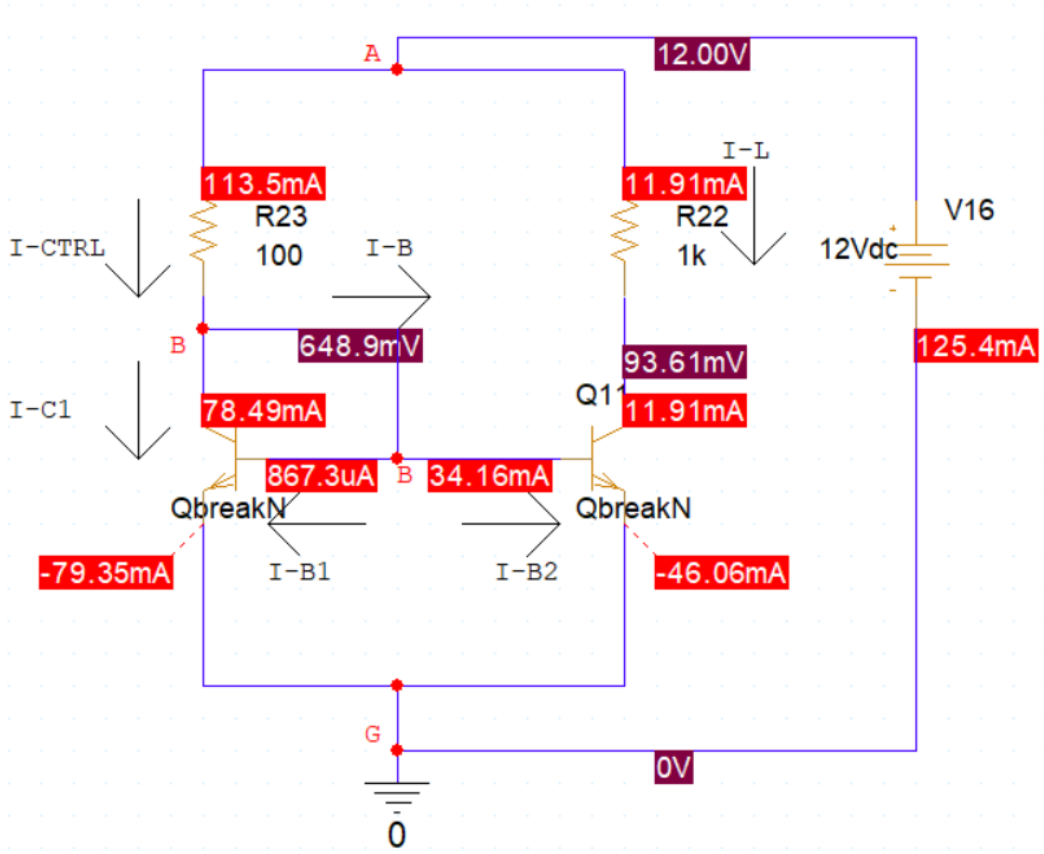

Figure 1.29: The bias simulation when $R_1 = 100\Omega$.

What is the phenomena?

-> We can see that in this case the values of I_{C1} and I_L are no longer equal, in fact the difference between them is significant. Furthermore, the current I_B is also not close to 0 as it was in the previous case but now its value is high enough to take into account and the current division at B is also not the same.

Explain:

The reason that has made this circuit lost its "mirror" properties is that we have decrease the resistance of R_1 too much. This leads to the effect that the current would prefer to pass this branch much more than the other since its resistance is lower.

3.12 BJT's logic gate application

Figure 1.30 describes a straightforward NOT gate theoretical implementation using an NPN bipolar junction transistor. In the circuit, the NPN junction transistor operates in the saturation mode.

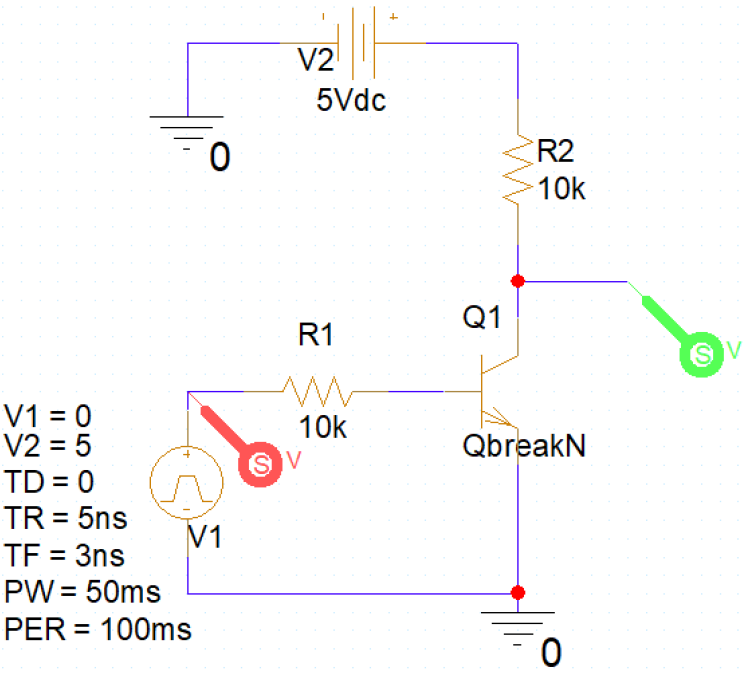

Figure 1.30: NPN theoretical NOT gate

V1 = 0 When the source is off, the voltage would be 0V.
V2 = 5 When the source is on, the voltage would be 5V.
TD = 0 Delay time. This exercise assumes that there is no delay.
TR = 5ns The rise time of the pulse (from off to on stage).
TF = 3ns The fall time of the pulse (from on to off stage).
PW = 50ms Pulse width: The time in which the source keeps on.
PER = 100ms The period of the signal.

Tips:

To get the Voltage Pulse Source component in the PSpice for TI, go to ***Place*** -> ***Pspice Compoment...*** -> ***Source*** -> ***Voltage Sources*** -> ***Pulse.***

3.12.1 Simulation

Your image goes here

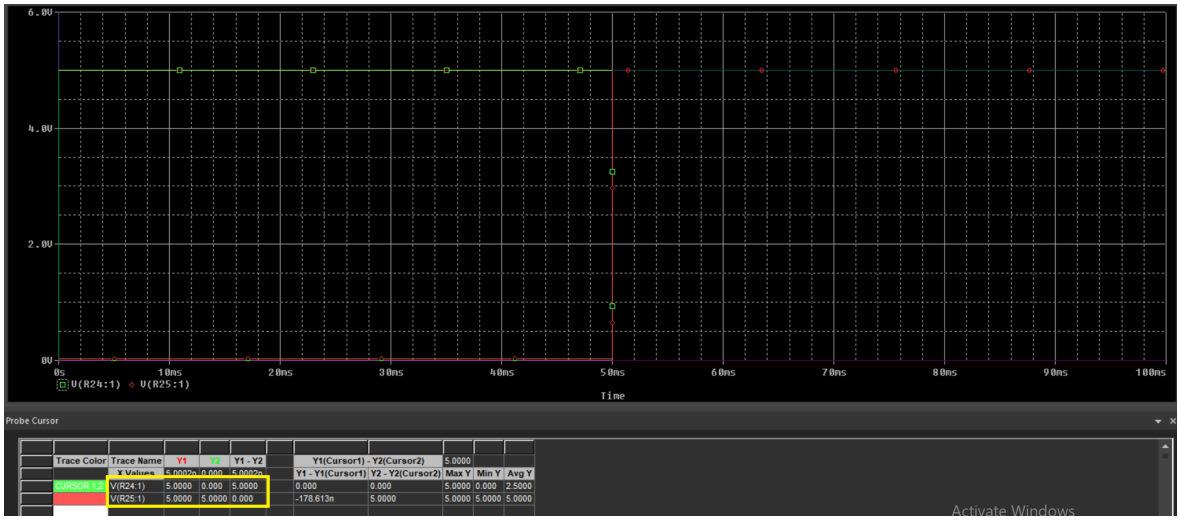

Figure 1.31: The graph of measured voltage by time.

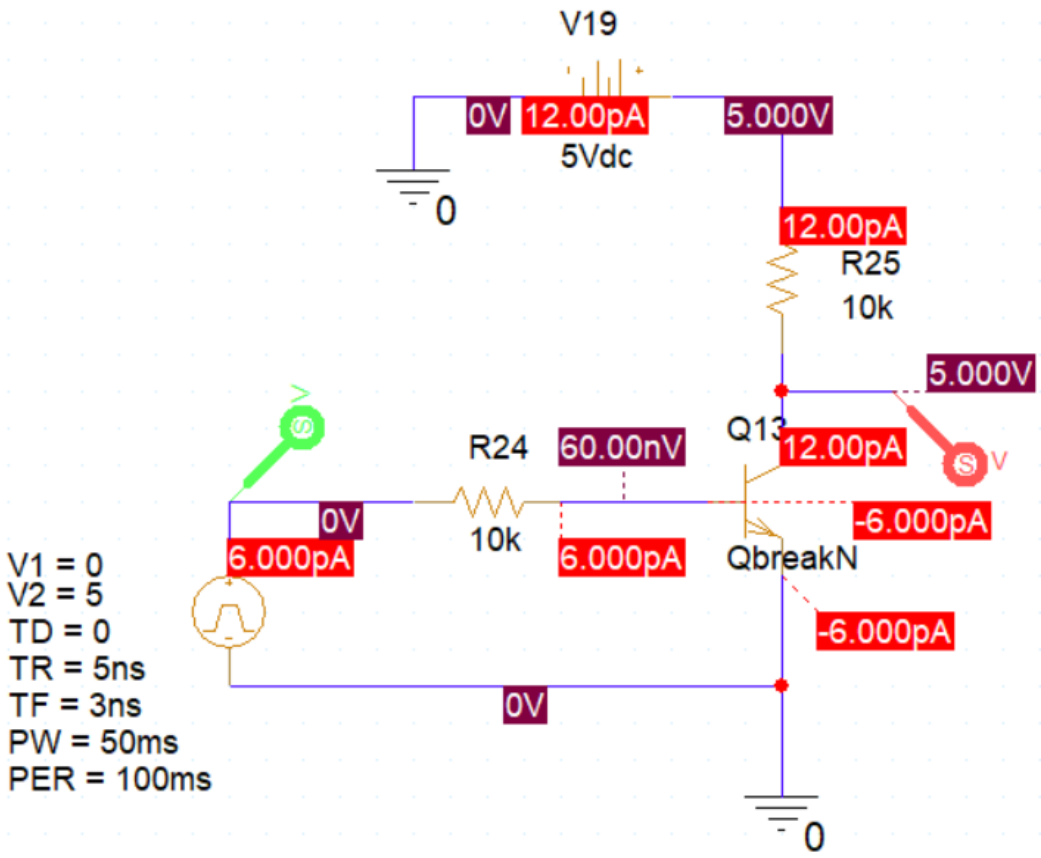

Figure 1.32: The bias point simulation.

But, wait! How large is the maximum current this NOT gate can source? Of course, it cannot exceed 5V/10kOhm. How tiny it is! So, what if we want to use it to drive an LED? Just put an additional 220 Ohm resistor in parallel with the existing 10k one. And in this case, the 10k resistor is quite useless. Therefore, in many cases, people let the collector pin of the transistor open. This design is called open-collector output, as shown in Figure 1.33.

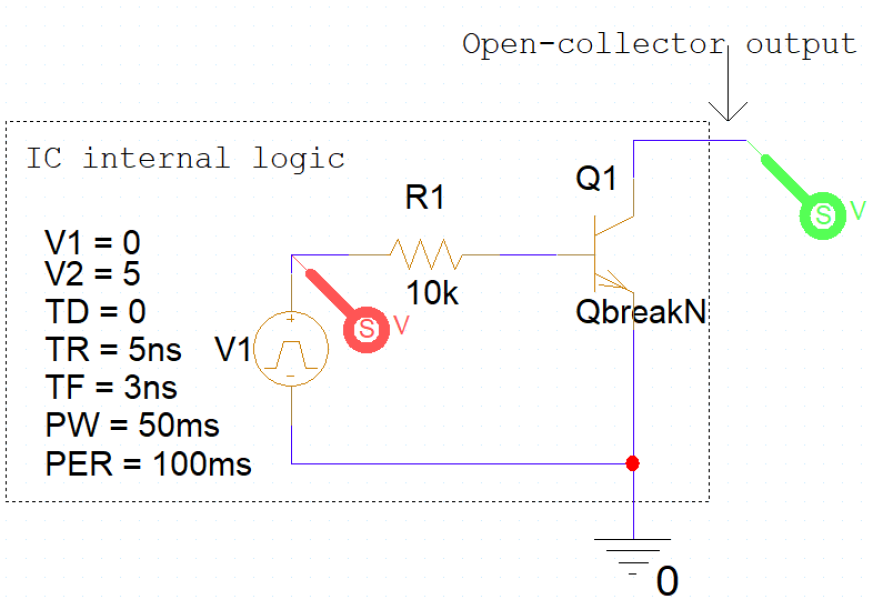

Figure 1.33: Open-collector output example

But, with this design, the input of another IC can't read the voltage of this output. Because without a pull-up resistor, the voltage V_C is floating. To read this voltage, the users have to pull it up using a resistor. There advantage here is to let the users choose the value of the pull-up resistor as their desire.

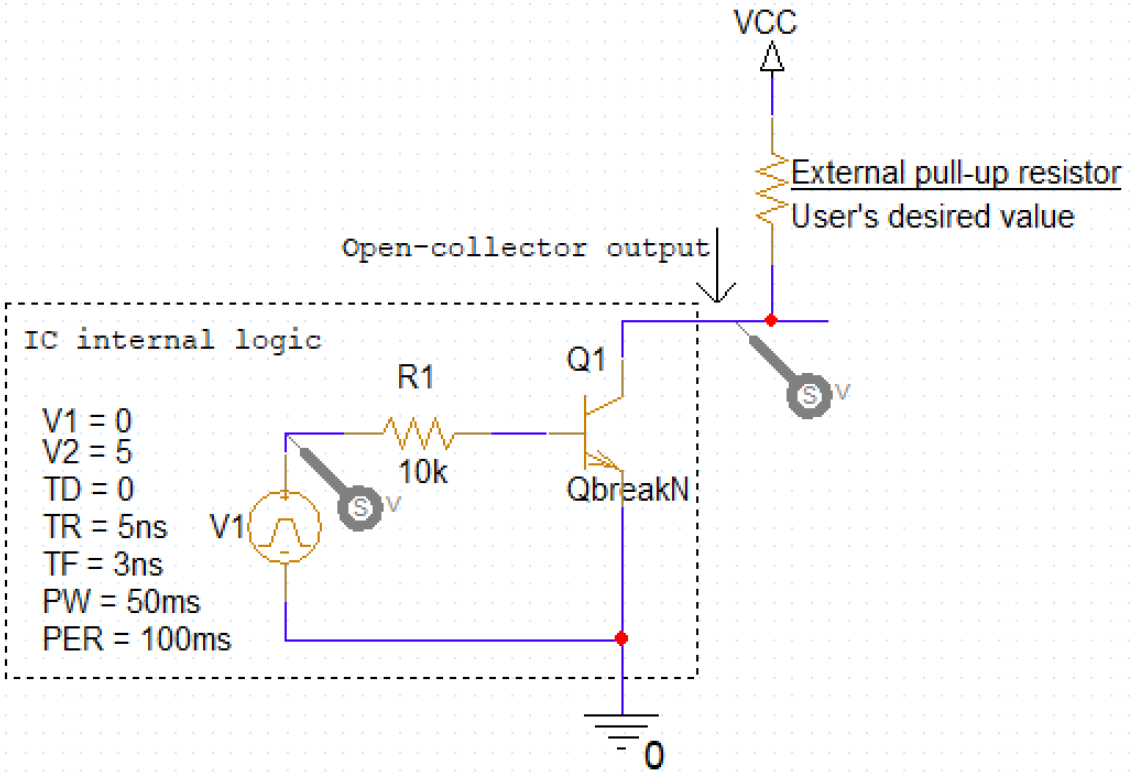

Figure 1.34: External pull-up resistor whose value selected by the users

By the side, the open-collector design manner gives an exciting way of the use of these outputs, as shown in Figure 1.35. The open-collector wired output is at the LOW level if one of the elements is LOW and is HIGH only when all the elements output HIGH.

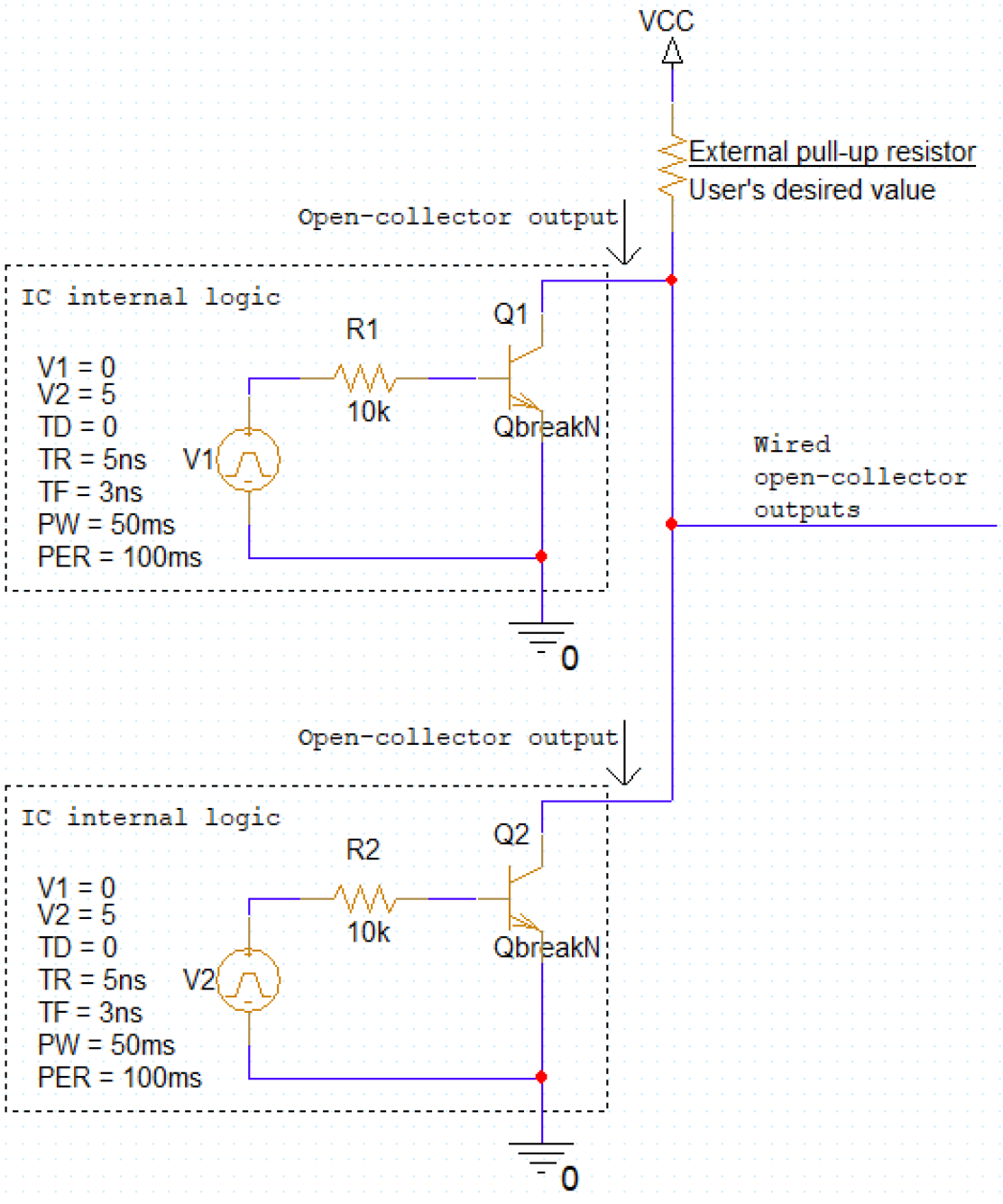

Figure 1.35: Wired open-collector outputs

3.13 Opto

The element OK_1 in Figure 1.36 is an optocoupler, which includes a light-emitting diode (LED) and a photodiode. The photodiode's conductivity depends on the intensity of the light emitted by the LED, and of course, depends on the current intensity through the LED. When the voltage across the LED is lower than its barrier potential, the Opto is cut-off. When there is current through the LED, the Opto is in the transfer mode. Like the current gain β of a BJT, the Opto also has the current transfer ratio (CTR). Assume the LED has its own barrier potential $V_F = 1.7V$, and the Opto has the CTR = 2. Calculate the voltage V_{OUT} when the switch is closed. Finally, give your idea about what we may use an Opto for, and how to use it?

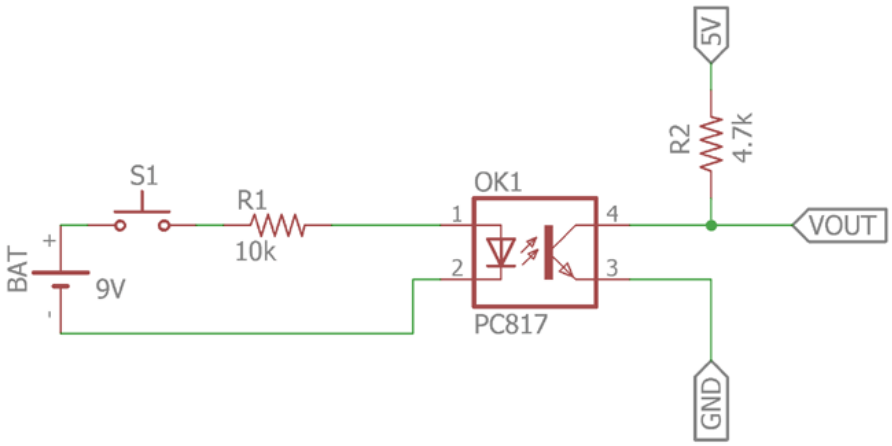

Figure 1.36: Voltage isolation with opto

$$I_F = I_{R_1} = \frac{V_{BAT} - V_F}{R_1} = \frac{9 - 1.7}{10000} = 730(\mu A)$$

When the switch is closed, the pin 4 and 3 are connected, then the value of the current passing through R_2 is:

$$I_{R_2} = \frac{5}{R_2} = \frac{5}{4700} = 1.06(mA)$$

$$V_{OUT} = 5 - V_{R2} = 5 - I_{R_2} \times R_2 = 5 - 1.06 \times 10^{-3} \times 4700 = 0(V)$$

If we're designing an electronic device that will be susceptible to voltage surges, lighting strikes, power suply strikes, etc. then we'll need a way to protect sensitive, low-voltage devices. When used correctly, an Optocoupler can effectively:

- Remove electrical noise from signals

- Isolate low-voltage devices from high-voltage circuits

- Allow using small digital signals to control larger AC voltages.

Optocouplers can either be used on their own as a switching device, or used with other electronic devices to provide isolation between low and high voltage circuits. We may typically find these devices being used for:

- Microprocessor in/out switching

- DC and AC power control

- Communications equipment protection

- Power supply regulation

With these applications, we'll encounter various configurations. Some examples include:

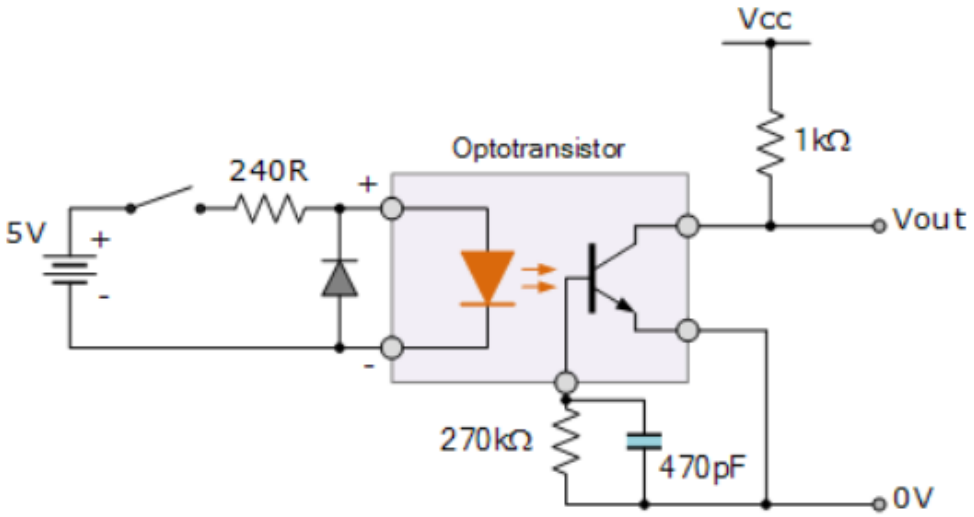

Figure 1.37: Opto Transistor DC Switch.

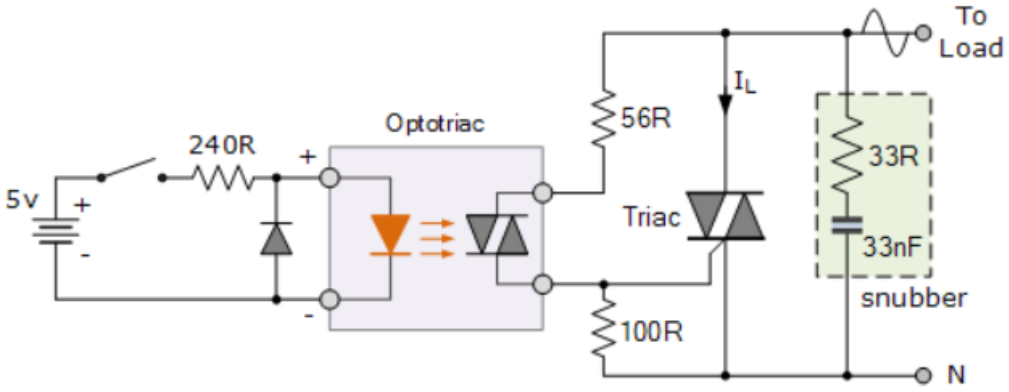

Figure 1.38: Triac Optocoupler.

THE END