东亚时区RISC-V双周会

2021年04月29日·第011次

https://github.com/cnrv/RISCV-East-Asia-Biweekly-Sync

Organizer: Wei Wu wuwei2016@iscas.ac.cn

会议议程(15:00 - 16:00)

- 自我介绍、等待参会者接入、非技术话题八卦(5分钟)
- 东亚地区小伙伴的项目更新
- 全体:过去两周RVI的新消息(10分钟)
- 自由讨论(5分钟)

- 注意:RVI 开始重视版权问题，GitHub 提交逐渐开始要求使用单位邮箱进行提交。后续如果有需要在 github/riscv/ 名下的repos进行merge的话，则默认需要使用 任何一个已经是RVI会员单位的邮箱。
  - 贡献非 RVI 的repos不受影响，由开源社区决定。

RISC-V in East Asia

- 全志的D1开始有小规模铺货，PLCT实验室拿到了20块（后仰），
  还有部分开源开发者都拿到了D1，在进行适配。
  我知道的就有2个团队已经跑起来了GUI和简单的浏览器
  - Fedora 还在路上（fuwei乐观的估计是五一假期之后）
  - Debian 已经有了demo在RISC-V讨论群里（ww还没拿到）
  - Gentoo 紧随其后还在贴着debian追赶
  - 自带的 TinaLinux 用于桌面还是不太行，适用于只能 语音设备等AIoT的
- RISC-V中国峰会，明天大概会公开录用信息
- 如果各位有新闻稿件想要发表到riscv.org（基金会官方网站）
  - 可以联系ww（发邮件到 china@riscv.org 我会收到，可以中文 发送）

RISC-V LLVM Biweekly Sync-up Call

- 取消了一次

RISC-V GNU Toolchain sync-up call

- **Should binutils require at least C99? Alan Modra, all yes.**
- Kito Cheng talk about the primary things to do in psABI meeting on monday.

  https://github.com/riscv/riscv-elf-psabi-doc/pull/185

- Jiawei Chen report the status update of B,K,P extensions in RISCV GNU Toolchain.
- Christoph Mueller introduce the atomic compute application in libc++

Nelson Chu via sourceware.org
to binutils, amodra, nickc, jimw, kito.cheng, andrew, palmer

Tue, Mar 30, 5:38 PM (5 days ago)

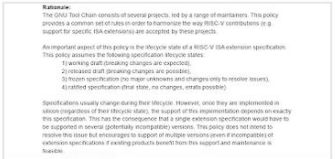
Hi Guys,

The original discussions were from here,
https://sourceware.org/pipermail/binutils/2020-December/114439.html

And this is the current policy of vendor and draft extensions,
https://docs.google.com/document/d/1Gj-ZCmWZGFgqGjtrdfC00tpULNIs1-wwjie9vdoKB9E/edit

RISC-V GNU binutils will have another two FSF develop branches to let developers can contribute their works, but these works are not ratified yet, so they aren't allowed to merge into mainline. The two branches are integration branch and working branch. The series of patches are the prototypes for these two develop branches, and they won't be applied to the mainline. Please see the details in the comments of the patches, and feels free to share any thought and suggestion, if you are interested.

Thanks
Nelson


Rationale:
The GNU Tool Chain consists of several projects, led by a range of maintainers. This policy provides a common set of rules in order to harmonize the way RISC-V contributions (e.g. support for specific ISA extensions) are accepted by these projects.

An important aspect of this policy is the lifecycle state of a RISC-V ISA extension specification. This policy assumes the following specification lifecycle states:
1) working draft (breaking changes are expected),
2) released draft (breaking changes are possible),
3) frozen specification (no major unknowns and changes only to resolve issues),
4) ratified specification (final state, no changes, errata possible)

Specifications usually change during their lifecycle. However, once they are implemented in silicon (regardless of their lifecycle state), the support of this implementation depends on exactly this specification. This has the consequence that a single extension specification would have to be supported in several (potentially incompatible) versions. This policy does not intend to resolve this issue but encourages to support of multiple versions (even if incompatible) of extension specifications if existing products benefit from this support and maintenance is feasible.

GNU Tool Chain Br...

K-ext Support: GNU, LLVM, Spike, QEMU, SAIL

- GNU: GCC部分对builtin进行了补充，添加了GCC和binutils的测试用例，重新发起review

  https://github.com/WuSiYu/riscv-gcc/pull/3

  https://github.com/riscv/riscv-binutils-gdb/pull/254

- LLVM: intrinsic 实现接近尾声
- Spike: 暂无更新
- QEMU: 暂无更新
- SAIL:
- Intrinsics：

P-ext Support: GNU, LLVM, Spike, QEMU, SAIL

- GNU: 提交了GCC和Binutils的PR到riscv-experiment branch, 感谢Andes-tech对GCC部分给出的修改建议，修复了Binutils的测试用例错误

  https://github.com/riscv/riscv-gcc/pull/258

  https://github.com/riscv/riscv-binutils-gdb/pull/257

- LLVM:
- Spike: fix了一些bug（andes合作的大学）
- QEMU: 暂无更新（阿里巴巴）
- SAIL:
- Intrinsics：

V-ext Support: GNU, LLVM, Spike, QEMU, SAIL

- GNU: 暂无更新
- LLVM:

  https://reviews.llvm.org/D100577 LGTM

  https://reviews.llvm.org/D100286 LGTM

  https://reviews.llvm.org/D100284 LGTM
- Spike: 暂无更新
- QEMU: 暂无更新
- SAIL:
- Intrinsics：

B-ext Support: GNU, LLVM, Spike, QEMU, SAIL

- GNU: 修复了Binutils中的测试用例bug，更新了GCC中的测试用例，感谢大家的帮助

  https://github.com/riscv/riscv-binutils-gdb/pull/255

- LLVM: Zbb/Zbc/Zbr IR intrinsic patches have been committed to Monorepo
- Spike: 暂无更新
- QEMU:更新了v5版本，v0.9.3
- SAIL:
- Intrinsics：

Zfinx Support: GNU, LLVM, Spike, QEMU, SAIL

- GNU: 暂无新更新，准备将GCC和Binutils移植至新版本
- LLVM:
- Spike: 无新更新
- QEMU: 无新更新
- SAIL:
- Intrinsics：
- Tariq 发了邮件说想要 Freeze，目前有四五个人进行了回复

V8 for RISC-V 更新

- Upstreaming status:

☆	2853282	[riscv64]skip atomic test case regress-1196837	Merged	Lu Yahan
☆	2848732	[riscv64] Optimize add/sub with immediate	Merged	Lu Yahan
☆	2848100	[riscv64] Alter rs to t6 in CallCfunction	Merged	Lu Yahan
☆	2847673	[riscv64] Optimize xori and branch in FloatMinMaxHelper	Merged	Lu Yahan
☆	2848735	[riscv64][sparkplug]Port Use EnterFrame/LeaveFrame with StackFrame::BASELINE	Merged	Lu Yahan
☆	2814723	[riscv64][wasm][liftoff] Record correct offset in StoreTaggedPointer	Merged	Lu Yahan
☆	2814726	[riscv64]Clean call/jump register	Merged	Lu Yahan
☆	2814724	[riscv64] Re enable constant pool	Merged	Lu Yahan
☆	2834632	[riscv64][codegen] Add static interface descriptors	Merged	Lu Yahan
☆	2839546	[riscv64] Fix IsConstantPoolAt and typo	--	Ji Qiu
☆	2848476	[riscv64] fix PushAllRegistersAndIterateStack	Merged	Ji Qiu
☆	2822631	[riscv64] Change one of the owners for RISCV.	Merged	Ji Qiu

- V8课程：Security Strategies in V8(Part1): Spectre Mitigation (https://b23.tv/qJB8OV)

OpenJDK for RISC-V

OpenJDK RV32G目前已经初步移植完成了解释器、汇编器和宏汇编器的移植，目前在调试fast-debug版本的java -version。

过去两周发生的一些值得关注的事情

- **[RISC-V] [tech-toolchain] Kick-off psABI TG meeting**

I am pleased to announce that Jessica and I are running the psABI TG now, and we would like to start a monthly meeting to discuss any psABI-related topics.

The time of the kick-off psABI TG meeting is: 4/19/2021 UTC+0 14:00/PDT 07:00/CST 22:00

Please join the meeting if you are interested in ABI-related issues.The agenda for the kick-off psABI TG meeting:
1) Discuss the policy for merging PRs
2) Discuss the priorities for work items; in particular:
 - [New] compact code model
 - [New] Draft for z[fdq]inx ABI
 - [New] Vendor or Non-standard Extension Compatibility.
 - [New] Review ABI for overlay.
 - [Doc Improve] ELF Attributes spec.
 - [Doc Improve] Pseudo-code for calling convention.
3) Open discussion

-

RISC-V Software Standing Committee

- 这两周没有，是每个月一次

RVI 的新消息

- gh/riscv/riscv-gnu-toolchain QEMU bump to 5.2.0; glibc/kernel bumped too.
- RISC-V CI Lab
  - 软件所，南京，≥2000 个RISC-V开发板，提供给全球开源软件社区使用（as CI Infrastructure）

RISC-V Toolchain & Runtime Meeting

- PLCT更新了在RISCV GNU Toolchain上的工作状况并在上周四GNU双周会进行了分享
- WDC更新了Overlay的工作状况

overlay status

Ofer Shinaar

Hi Christoph,
Following our corresponding, I will modify the Overlay Standard/Spec to be agnostic to target.
That was the porpoise from the beginning, same as you mentioned we need to separate imple

I will work to clean it up this week. The HLD is the implementation based on RISCV; for that, w
you see any blockers?

I wish to get T&R blessing for the Standard (not the HLD) to start working on patch submissior
There are few things to clean up before the relocation topic; for that, we need approval for HLI
Please note that Craig and I have more queries on the email thread related to your questions.

Thanks,
Ofer

RISC-V GNU Toolchain work status

jiawei

Hello everyone:

Here is the recently works status of RISCV GNU Toolchain from PLCT-lab:

Finished:

1. Update Zfinx RISCV GNU Toolchain with the new spec Z[fdq]inx.

2. Support Scalar Crypoto extension(K-ext) support on RISCV GNU Toolchain and P

3. Adding remaining work with ISA Bitmanip extension in Binutils part, sync the GCC

Doing

Porting Signal Digital Processing extension(P-ext) form Andes-tech v0.50 into v0.93

Code Optimization Group (formerly code size TG)

- Tariq会在本周给出Zce的encoding草案
- 大家正在激烈讨论压缩指令的一些汇编语法问题
- WDC提供了GCC RISC-V [Code-density-test-bench]

GCC RISCV test cases

Mr. Nidal Faour

Hi all,
I would like to share with you the test cases we worked on at WDC.
These test cases have been extracted from the real life embedded product where the GCC com
upstream.
You can find the test cases at our github repo:
https://github.com/westerndigitalcorporation/riscv32-Code-density-test-bench

feel free to explore these test cases and give your feedback, also this is to encourage others wh
benefit from it.

One more thing, in the near future these test cases will be integrated into the Embench system.

Best Regards,

Nidal Faour
Staff Engineer, R&D Engineering – Firmware & Toolchain, CTO Group

Wording of compact vs. non-compact assembler syntax

Anders Lindgren

Hi!

As discussed in the last meeting, some assemblers automatically convert normal instructions (like "add a0, a0, a1") into compact instructions ("c.add a0, a1"). However, not all assemblers has opted to do this.

It is important that the wording in the proposed extension allow, but don't mandate, this behavior.

I suggest that 1) we use the compact format of the instructions in all examples and in the syntax description. 2) somewhere in the beginning of the document we include a text like:

"When the non-compact syntax is used, and there is a corresponding compact instruction, an assembler is allowed to emit the compact version."

QEMU / Linux Kernel 社区的新消息

- Ren Guo?
- 李威威？王俊强？

CHISEL/FIRRTL 项目的进展

- PLCT两位实习生同学直接都在上游提交，感谢Sequencer耐心指导
- CCC2021 workshop
  - 16个talk！(^o^)/
  - Full day event
  - Co-located w/ RVWC2021

自由讨论 / AOB

- 欢迎报名参加 RISC-V World Conference China 2021！
- 报名链接:
- https://www.bagevent.com/event/7314534
-

AOSP 进展：这两周没进展

- 尚未看到平头哥有公开技术报告的计划
- Call for Sharing：欢迎看过代码的小伙伴进行讨论