注意今天有 Open Hours，请同步更新英文的 slides

欢迎第一次加入的伙伴（开会时请从下一页开始展示）

- 开放编辑，直接点击 request for edit 然后在东亚时区群里at吴伟
- 如果没有找到自己的内容分类，可以添加1-2页在最开始或中间
- 欢迎在开始的前5分钟进行自我介绍
- 日常八卦在东亚时区RISC-V双周同步微信群中，欢迎加入

东亚时区RISC-V双周会

2022年06月09日·第037次

https://github.com/cnrv/RISCV-East-Asia-Biweekly-Sync

Host: 邢明杰

Organizer: PLCT Lab wuwei2016@iscas.ac.cn

会议议程（15:00 - 16:00）

- 自我介绍、等待参会者接入、非技术话题八卦（5分钟）
- RVI 的更新和八卦（基本上跟东亚双周会群内消息同步）
- Unratified Specs 的参考实现进展
- 东亚地区小伙伴的项目更新
- 自由讨论

RISC-V International 同步、全球开源社区八卦

- RISC-V 中国峰会开始征集演讲，欢迎大家报名
- 中科院软件所张洪滨同学作为 RISC-V国际基金会mentorship代表做了一次mentor分享
- 今天上午举行了 RISC-V Open Hours
- 东京的 RISC-V Day 有没有小伙伴参加了？
- Profiles 的潜在问题和推广的缓慢

AOSP for RISC-V - 汪辰、陆旭凡

这两周的工作主要仍然是继续对 Andorid 上的 Bionic 库解决故障和优化工作，现在支持完整的 mmm bionic：

RVI upstream:

1. fixed TLS issues and pass unit tests: https://github.com/riscv-android-src/platform-bionic/pull/26
2. roll-back temp changes: https://github.com/riscv-android-src/platform-bionic/pull/27
3. redefine ucontext: https://github.com/riscv-android-src/platform-bionic/pull/28
4. fixed benchmark for link reloc: https://github.com/riscv-android-src/platform-bionic/pull/29
5. updated android 12 download steps: https://github.com/riscv-android-src/riscv-android/pull/4
6. use clang integrated as: https://github.com/riscv-android-src/platform-build-soong/pull/4

aosp-riscv development

1. update env and add 8.log: https://gitee.com/aosp-riscv/test-riscv/pulls/21
2. added build of run-as: https://gitee.com/aosp-riscv/test-riscv/pulls/22
3. added 9.log: https://gitee.com/aosp-riscv/test-riscv/pulls/23
4. 与 RVI upstream 的同步工作

RISC-V GCC进展

- RVV的built-in系列patch已经发送至上游，正在review中

  [PATCH 00/34] RISC-V: Add RVV (RISC-V 'V' Extension) support

  https://github.com/riscv-collab/riscv-gcc/tree/riscv-gcc-rvv-next

- Linux Plumbers & GNU Cauldron 2022会议将于今年九月召开
- RISC-V profile规范讨论

  Handling profiles in the tools

  riscv-profiles docs introduction

- Zicntr and Zihpm扩展讨论

  zicntr and zihpm issue on github

  Kito Cheng's slides introduce about this topic

- Zfh and Zhinx扩展的binutils部分已经支持, gcc部分的工作仍在开发中
- CMO扩展的gcc部分已经通过review合入上游
- Slides for RISC-V GNU Toolchain会议slides

  RISC-V GNU Toolchain Biweely sync-up 06-02

Clang/LLVM 进展 (PLCT)

被合并的patch:

1. **[RISCV] Add ISD::EH_DWARF_CFA : https://reviews.llvm.org/D126181**
2. **[RISCV] Add more patterns for FNMADD: https://reviews.llvm.org/D126852**
3. **[RISCV] Change GPRPF64's hwmode and spill alignment : https://reviews.llvm.org/D126652**

Clang / LLVM 社区的更新（廖春玉、陆旭凡）

1. D126843 [RISCV] Support (addi (addi globaladdr, C1), C2) in RISCVMergeBaseOffset.
2. D126729 [RISCV] Support LUI+ADDIW in RISCVMergeBaseOffsetOpt::matchLargeOffset.
3. D126861 [RISCV] Fix missing stack pointer recover
4. D126968 [RISCV] Support LUI+ADDIW in doPeepholeLoadStoreADDI.
5. D126576 [RISCV] Add custom isel for (add X, imm) used by load/stores.

Philip Reames : https://github.com/preames/public-notes/blob/master/llvm-riscv-status.rst

QEMU/Spike/Sail/ACT进展 (PLCT)

- Qemu: zmmul支持更新第3版PR, 已被接收, 等待合并至上游
  - https://lists.gnu.org/archive/html/qemu-riscv/2022-05/msg00441.html
- Spike: CMO支持修复了反汇编相关的问题,已合并至上游
  - https://github.com/riscv-software-src/riscv-isa-sim/pull/1024
  - https://github.com/riscv-software-src/riscv-isa-sim/pull/1026
- Sail和ACT: 对CMO的支持进行了相应更新
  - https://github.com/riscv/sail-riscv/pull/137
  - https://github.com/riscv-non-isa/riscv-arch-test/pull/226
  - 相关更新:
    - https://github.com/riscv-software-src/riscof/pull/46
    - https://github.com/riscv-software-src/riscv-config/pull/79
    - https://github.com/riscv-software-src/riscv-ctg/pull/22
    - https://github.com/riscv-software-src/riscv-isac/pull/43

V8 for RISC-V 更新（邱吉、陆亚涵）

- Upstream Update：
  - [riscv64] Fix return value of lazy compile runtime function | https://chromium-review.googlesource.com/c/v8/v8/+/3669661
  - [riscv64] Fix name ambiguous | https://chromium-review.googlesource.com/c/v8/v8/+/3673913
  - [riscv64] Optimize call/jump code instr | https://chromium-review.googlesource.com/c/v8/v8/+/3676880
  - [riscv64] Port Improve gap resolver algorithm | https://chromium-review.googlesource.com/c/v8/v8/+/3677327
  - [riscv64][wasm-simd] Prototype relaxed integer Dot product instructions | https://chromium-review.googlesource.com/c/v8/v8/+/3687424
  - [riscv64][heap] Remove write barrier builtin for incremental marking | https://chromium-review.googlesource.com/c/v8/v8/+/3696492
  - [riscv64] Using SystemPointerSize to index address for PrologueFillFrame | https://chromium-review.googlesource.com/c/v8/v8/+/3669660
  -

- RV32G Porting: in progressing
  - Going on bug fix for the V8 embedded unittests and cctest
  - All the 4000 unitests pass
  - 77% cctest case pass(5699 out of 7435)
  - Porting process can be tracked and open sourced on https://github.com/riscv-collab/v8/

OpenJDK for RISC-V 更新(RV64及upstream)

1. 8287418: riscv: Fix correctness issue of MacroAssembler::movptr

   https://github.com/openjdk/jdk/pull/8913/files

2. 8287552: riscv: Fix comment typo in li64

   https://github.com/openjdk/jdk/pull/8950/files

OpenJDK for RISC-V 更新(RV32/PLCT)

1. Fix Matcher::isSimpleConstant64 on riscv32.ad

   https://github.com/openjdk-riscv/jdk11u/pull/399

2. Fix incorrect register mask in call_native_base according to JDK-8285303

   https://github.com/openjdk-riscv/jdk11u/pull/404

3. Update the storeval_barrier with RV64 11.0.11

   https://github.com/openjdk-riscv/jdk11u/pull/405

4. Fix codeblob pointing error in C2 compilation

   https://github.com/openjdk-riscv/jdk11u/pull/406

openEuler RISC-V

- oerv OBS 构建
  - openEuler:22.03 :4075+/4220 ?/+36
    - 自构建:新建obs工程openEuler:selfbuild:repo 和仓库openEuler_2203_self
  - openEuler:22.03:Epol : 599/679 +1/0
  - Factory:RISC-V:Python : 1431/1434 +5/0
  - 新obs工程:Factory:RISC-V:Mozilla : 3/3
  - 新obs工程:Factory:RISC-V:Kernel:15/15
- PR 新增 17个
  - https://gitee.com/openeuler/RISC-V/blob/master/archive/weeklyreports/2022-05-19.md
- RISC-V 软件源&每日镜像计划
  - 每日镜像:已经初步能够生成qemu、D1、unmatched、Visionfive 镜像
    :https://repo.tarsier-infra.com/openEuler-RISC-V/devel/20220609/v0.1/（定期构建更新，以最新 为准）
  - 更新ORSP004 openEuler RISC-V 定时快照构建 规范
- 测试/验证
  - 镜像测试验证

Gentoo for RISC-V 的情况更新（Gentoo小队）

- A total of 64 keywording commits: https://whale.plctlab.org/riscv/RISC-V-双周会/20220609/commits.txt
  - app-admin/salt: keyword for riscv
    - commit: gentoo/gentoo@96241ffa021b565647f234bdb834c1b07dc0d50a
    - bug: https://bugs.gentoo.org/835717
  - x11-wm/fvwm3: keyword for riscv
    - commit: gentoo/gentoo@a91eec1b27ce7d819b775e3724c9180eaa1e2297
- riscv overlay
  - New packages: app-emulation/{nemu-xiangshan,nemu-nju}, gentoo/riscv#5
- RISC-V binhost progress
  - Images for MangoPi MQ Pro and VisionFive
    - Links
      - MQ Pro: https://github.com/Rabenda/riscv-calculate/releases/tag/gentoo-mq-pro-20220607040010
      - VisionFive: https://github.com/Rabenda/riscv-calculate/releases/tag/gentoo-visionfive-20220609041048
    - Usage

```
# unzstd *.img.zst
# dd if=xxxx.img of=/dev/sdX bs=1M status=progress
```

Arch Linux RISC-V（东东）

1. 移植进度

   [extra] 2592 / 3030 (85.54%)

   [community] 7180 / 9192 (78.11%)
2. Archriscv-packages merged 58 PR. highlights

   Updpkg: firefox to 101.0
3. 更新 archriscv-packages wiki
4. 新增 VisionFive 编译机（感谢 RVI）

Fedora for RISC-V（傅炜）

SRPM打包编译进度

- [fc36] **144000 / 22832 (65%)**
- [rawhide]【**TODO**】
- 现在主要以主要模块化软件手工补包为主，图形化桌面环境目标为辅。
- **firefox**/chromium【**On Going**】

F36 highlights:

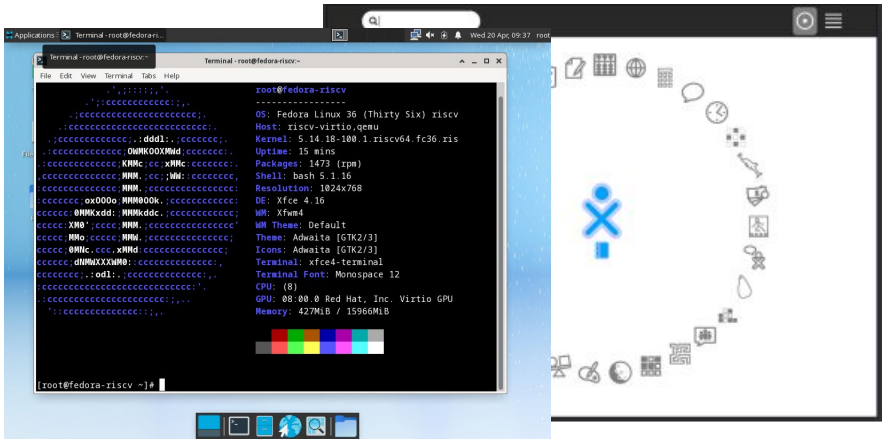
- koji + mock build supported
- QEMU **multi graphic desktop** supported

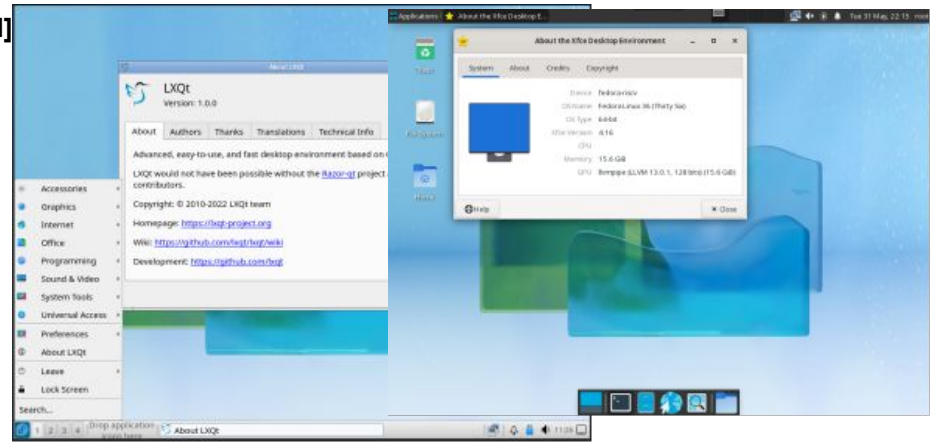
软件版本:

- GCC 12.0.1 / Glibc 2.35
- Binutils 2.38→ 2.39 **[need to update for opensbi/uboot/kernel]**
- Python 3.10.4 → 3.11[rawhide]
- **Perl 5.34.2**
- **LLVM/Clang 14.0-1**
- **Rust 1.61-1 [need qemu fix from Felix]**
- **QT-5.15.3 and QT-6**

Images:

- minimal/developer Image
- **LXQT/LXDE/XFCE/Sugar/ Image**
- **Workstation (GNOME&KDE/Deepin) Image: 预计7月**
- **New koji builder Image (F36) 3GB**





Debian for RISC-V（于波）

[Ready to official ports] https://wiki.debian.org/Ports/riscv64

[suricata confirm]https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1012031

[cpufetch todo upstream]https://github.com/Dr-Noob/cpufetch/issues/133

[jimtcl -2 upload]https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1012029

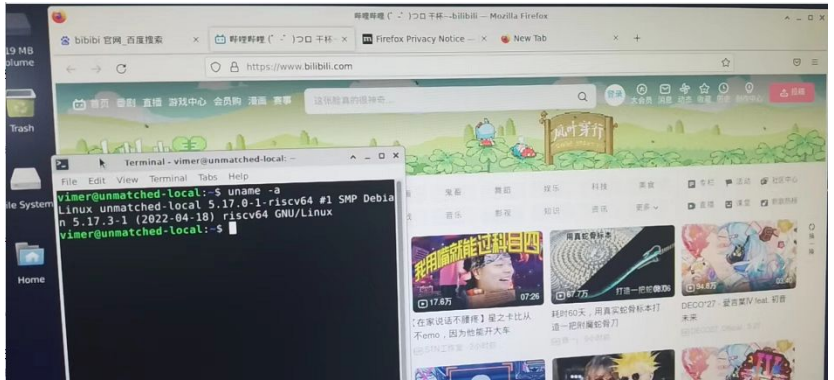
[debhelper help]https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1012058

[firefox patch]https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1012218

[rush packaging] https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1012292

[abps done] https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1012302

[coredns itp]https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1012251



FW相关更新（王翔）

- opensbi
  - 改进变地址的csr读写操作，通过动态生成指令来实现。讨论中：
    - 需要fence.i来确保指令存储一致性，有性能问题
    - 此方法需要用到W^X的数据段有安全风险
  - 删除不必要的封装get_platform_ticks
  - 修正illegal_insn_table为只读，此表运行时不需要修改
  - 为OpenC906模拟fence.tso
  - 为改善putchar性能，添加debug console扩展，正在讨论

RISCV性能跟踪小队 - 陈小欧

1. Run SPECjbb on unmatched (on going)

Using OpenJDK19 on unmatched.

Problem: PR is under limit

香山开源RISC-V处理器 - ICT / PCL

- 取指前端
  - 修复若干性能 Bug
  - 针对 trace cache、stream fetch 等技术进行预研
  -
- 后端流水线
  - 讨论和细化 V 扩展的微架构设计
  -
- 访存模块
  - 通过 microbenchmark 调试 dcache sride 预取
  - 研究 load 指令 LSU 重发性能下降问题
  -
- 缓存模块
  - 针对 ACE、CHI 总线预研

MLIR RISC-V Vector (RVV) Dialect Proposal - 张洪滨

相关链接

- RFC Patch - https://reviews.llvm.org/D108536
- RFC Post - https://discourse.llvm.org/t/rfc-add-risc-v-vector-extension-rvv-dialect/4146/32
- MLIR + RVV 集成测试环境搭建文档 - https://gist.github.com/zhanghb97/ad44407e169de298911b8a4235e68497
- 工具链和集成测试状态 - https://buddy-compiler.github.io/Pages/DisplayBoards/RVVStatus.html

Google/IREE 伙伴的反馈

- https://discourse.llvm.org/t/rfc-add-risc-v-vector-extension-rvv-dialect/4146/39
- 他们大多依赖于VLS (Vector Length Specific) 向量化，希望把VLS 和 RISC-V Scalable Intrinsic 结合
- 目前的设计抽象层级太低，尝试使用更高抽象层级的设计来提供 RVV 的特性，并且能够支持 VLS 和 VLA 两种向量化
- 确实需要找一个方法在MLIR 中支持动态指定 vl，但是应该用硬件不相关的抽象来增加可重用性和通用性
- 尾端处理他们倾向于使用 Mask 实现，因为没有看到决定性的理由使用strip-mining

面向 RISC-V 的 OpenCV 情况更新 - 韩柳彤

- **为 Universal Intrinsic 增加可变长向量指令的支持**

  Google Summer of Code 2022: Optimizing OpenCV Universal Intrinsic for RISC-V Vector

  示例项目：https://github.com/hanliutong/rvv-ui

  为了与现有接口兼容，引入了新的包装层

  - 修改OpenCV中的用户代码
  - 复用单元测试用例

  欢迎讨论：Issue#21829

Chisel and Additional Technology / Sequencer

- 郑鉉壬:
  - RISC-V Vector的Montgomery Modular Multiplication实现
    - https://github.com/ZenithalHourlyRate/rvv-mmm
    - https://github.com/openssl/openssl/pull/18479
- 程光辉:
  - 完成 SRT-4 和 SRT-16 除法
    - https://github.com/sequencer/arithmetic/pull/3
- 徐金焱:
  - Bug report to open source RISC-V cores
    - https://github.com/openhwgroup/cva6/issues/900
    - https://github.com/openhwgroup/cva6/issues/906
    - https://github.com/openhwgroup/cva6/issues/905
    - https://github.com/openhwgroup/cva6/issues/904
    - https://github.com/openhwgroup/cva6/issues/901
    - https://github.com/openhwgroup/cva6/issues/899
    - https://github.com/openhwgroup/cva6/issues/898
    - https://github.com/riscv-boom/riscv-boom/issues/606
    - https://github.com/riscv-boom/riscv-boom/issues/605
- 杨砚祺:
  - Debug Spec 会议
- 陈春昀:
  - CVA6+Arvine 后端报告
  - 探索 Rocket-Chip的后端设计
- 摸了:
  - 申奥 王瑞康 陈泱宇 刘晓义 罗云千 廖杰 韩博阳 苑浩然 刘思皓 张露承

自由讨论 / AOB

- 各位工作生活都还顺利？

Backups

Spidermonkey for RISC-V - 吴伟

- 过去两周没有新的进展
  - 重新加入了 PLCT Roadmap 2022 计划
  - 但是这次并没有重新放入到 LFX Mentorship（专业对口的太少了）
  - https://github.com/plctlab/gecko-dev-riscv/pull/3
- 欢迎感兴趣移植的小伙伴通过实习、兼职或全职形式加入
  - https://github.com/lazyparser/weloveinterns/blob/master/open-internships.md
  -

RISC-V 笔记本计划的进展 / 吴伟

- 过去2周硬件部分没有观察到有新的动作
  - 但是有了新的传言～
- 软件部分，目光开始看向
  - LibreOffice：我们很高兴有一位全职员工 **钱耀津** 同学 all in！
    - ArchRV小队也有小伙伴开始参与
    - Debian小队的**于波**开始尝试
  - LuaJIT：呼唤勇士
  - DynamoRIO：呼唤勇士
  - Valgrind：呼唤勇士
  - DartVM：呼唤了！还没来……
  - Mono：需要么？
  - Chromium：SUSE上ok但是其它发行版还不行，呼唤勇士