#### 欢迎第一次加入的伙伴(开会时请从下一页开始展示)

- 开放编辑, 直接点击 request for edit 然后在东亚时区群里at吴伟
- 如果没有找到自己的内容分类, 可以添加1-2页在最开始或中间
- 欢迎在开始的前5分钟进行自我介绍
- 日常八卦在东亚时区RISC-V双周同步微信群中,欢迎加入

# 东亚时区RISC-V双周会

2023年09月28日 · 第065次

https://github.com/cnrv/RISCV-East-Asia-Biweekly-Sync

Host: 陈逸轩

Organizer: PLCT Lab <u>plct-oss@iscas.ac.cn</u>

### 会议议程(15:00 - 16:00)

- 自我介绍、等待参会者接入、非技术话题八卦(没有的话就直接跳过)
- RVI 的更新和八卦(基本上跟东亚双周会群内消息同步)
- Unratified Specs 的参考实现进展
- 东亚地区小伙伴的项目更新
- 自由讨论

#### RISC-V International 同步、全球开源社区八卦

- GNU Tools Cauldron 2023 (陈逸轩、陈嘉炜、吴伟、Kito、Palmer 等参会)
  - David给 gcc 新手的教程: https://gcc-newbies-guide.readthedocs.io/en/latest/index.html
- OSEEU 2023 上 openEuler RISC-V 带着 Milk-V Pioneer 和 Sipeed LicheePi
   4A

#### RISC-V 韩语社区的同步与八卦

- 最近两周没有韩国本土社群的新闻
- 但是韩国媒体对华为Mate 60 Pro进行了广泛的报道
  - 内容上主要提及华为在美国制裁,没有EUV等设备的情况下解决了7nm代工的困难
  - 提到7nm是18年TSMC已经可以量产的技术
  - 韩媒"华为的技术自立成功成为其他中国企业的催化剂"

### RISC-V 日语社区的同步与八卦

● Codasip 和美国硬件安全公司 Verilock 宣布了合作实现多种应用于RISCV SoC的安全功能,包括设备身份验证、固件签名、基于EED 的 OTP 。

## RISC-V 俄语社区的同步与八卦

最近没有八卦

#### RISC-V GCC进展

#### RISC-V BoF in GNU Cauldron 2023

- 介绍了过去一年里RISC-V GNU社区的进展, Intel, Ventana, Eswin等新的开发者伙伴加入社区
- 介绍了GCC13至目前GCC upstream的更新,包括自动向量化,RVV intrinsic工作, inline sub-word atomics, Zc\*, Zicond, Ztso, Xthead等扩展的支持
- 讨论了GCC14支持的新特性:
  - 更全面的RVV intrinsic支持(zvfh, zvfbf, rounding mode)
  - 消除不必要的符号扩展
  - 添加新的cost model支持(Zicond, RVV)
  - 对已有的cost model进行优化(RVV)
  - 长跳转分支支持
  - 指令融合支持
  - 更多的厂商自定义扩展(已规范Binutils中厂商自定义扩展添加的行为)
  - Profiles支持

## Clang/LLVM 进展 (PLCT)

- upstream 合并的patch
  - 进一步优化D156238中当谓词为==/!=时的折叠 [InstCombine] Fold icmp eq/ne min|max(X, Y), Z https://github.com/llvm/llvm-project/pull/67087
  - 将icmp eq/ne (A ^ Cst), B规范化为icmp eq/ne (A ^ B), Cst以暴露更多优化机会, 修复
     https://github.com/llvm/llvm-project/issues/65968 [InstCombine] Canonicalize icmp eq/ne (A ^ B), C https://github.com/llvm/llvm-project/pull/67273
- RVV 0.7.1,第一个instrinsic patch
  - [LLVM] [RVV 0.7.1] add vsetvl and vsetvlmax intrinsic <a href="https://github.com/ruyisdk/llvm-project/pull/12">https://github.com/ruyisdk/llvm-project/pull/12</a>

## QEMU/Spike/Sail/ACT进展 (PLCT)

## V8 for RISC-V 更新(邱吉、陆亚涵、荆培杨)

#### Port 上游更新

- 1. 4895850: [riscv][interpreter] Cache FBV in the stack frame | https://chromium-review.googlesource.com/c/v8/v8/+/4895850
- 2. 4884597: [riscv][wasm] Use Builtin ids instead of RuntimeStubId ids for calls | https://chromium-review.googlesource.com/c/v8/v8/+/4884597
- 3. 4868010: [riscv][compiler] Generalize InstructionSelectorT for Turboshaft (part 17) | <a href="https://chromium-review.googlesource.com/c/v8/v8/+/4868010">https://chromium-review.googlesource.com/c/v8/v8/+/4868010</a>

删除maglev公共代码里的condtion code, 以便port maglev到riscv上

1. 4876814: [maglev] Replace CompareInt32 by CompareInt32AndJumpIf | https://chromium-review.googlesource.com/c/v8/v8/+/4876814

### Spidermonkey for RISC-V更新(邱吉、陆亚涵)

#### 修复fixfox wasm相关问题,以下patch扔在review中

- 1. [riscv]wasm: Generalize load/store instructions for multiple memories. r=jseward https://phabricator.services.mozilla.com/D188222
- 2. [riscv]Port wasm return calls implementation. r=jseward https://phabricator.services.mozilla.com/D187967
- 3. [riscv]Fix register conflict in Mull64.r=jseward https://phabricator.services.mozilla.com/D188068
- 4. [riscv]wasm: Generalize load/store instructions for multiple memories. r?jseward https://phabricator.services.mozilla.com/D187968

## OpenJDK for RISC-V 更新(RV64及upstream) 杨飞

#### 1. Reviewed JDK-mainline PRs:

- https://github.com/openidk/idk/pull/14991 (8312569: RISC-V: Missing intrinsics for Math.ceil, floor, rint)
- https://github.com/openjdk/jdk/pull/15119 (8313592: RISC-V: Link libatomic statically)
- https://github.com/openidk/jdk/pull/15156 (8313779: RISC-V: use andn / orn in the MD5 instrinsic)
- https://github.com/openidk/idk/pull/15226 (8314117: RISC-V: Incorrect VMReg encoding in RISCV64Frame.java)
- https://github.com/openjdk/jdk/pull/15356 (8314618: RISC-V: -XX:MaxVectorSize does not work as expected)
- https://github.com/openjdk/jdk/pull/15437 (8315070: RISC-V: Clean up platform dependent inline headers)
- https://github.com/openidk/idk/pull/15464 (8315206: RISC-V: hwprobe query is set return wrong value)
- https://github.com/openjdk/jdk/pull/15465 (8315195: RISC-V: Update hwprobe query for new extensions)
- https://github.com/openidk/jdk/pull/15211 (8314020: Print instruction blocks in byte units)
- https://github.com/openjdk/jdk/pull/15285 (8314268: Missing include in assembler\_riscv.hpp)
- https://qithub.com/openidk/idk/pull/15248 (8313419: Template interpreter produces no safepoint check for return bytecodes)
- https://github.com/openidk/idk/pull/15428 (8315020: The macro definition for LoongArch64 zero build is not accurate)
- https://github.com/openjdk/jdk/pull/15443 (8315073: Zero build on macOS fails after JDK-8303852)
- https://github.com/openjdk/jdk/pull/15468 (8315069: Relativize extended\_sp in interpreter frames)
- 2. Finished building & regression testing of the initial jdk11u riscv port from Alibaba:
- https://github.com/openidk/riscv-port-jdk11u/pull/3 (8276799: Implementation of JEP 422: Linux/RISC-V Port)
- 3. Proposed JDK11u upstream backport PRs:
- https://github.com/openjdk/jdk11u-dev/pull/2099 (8292407: Improve Weak CAS VarHandle/Unsafe tests resilience under spurious failures)
- https://github.com/openjdk/jdk11u-dev/pull/2125 (8292713: Unsafe.allocateInstance should be intrinsified without UseUnalignedAccesses)
- 4. Proposed riscv-port-jdk11u backport PRs:
- https://github.com/openjdk/riscv-port-jdk11u/pull/4 (8283929: GHA: Add RISC-V build config)
- 5. Fei Yang is nominated as JDK Updates Reviewer:
- https://mail.openjdk.org/pipermail/jdk-updates-dev/2023-July/023701.html
- https://mail.openjdk.org/pipermail/jdk-updates-dev/2023-August/024467.html
- 6. OpenJDK Committer Voting:
- https://mail.openidk.org/pipermail/jdk-updates-dev/2023-July/024067.html
- https://mail.openjdk.org/pipermail/jdk-dev/2023-August/008056.html

## OpenJDK for RISC-V 更新(RV64及upstream)张定立

## JDK11U for RV32G 更新(RV32及upstream) 曹贵

#### Merged & New JDK-mainline PRs:

<a href="https://github.com/openidk/idk/pull/15911">https://github.com/openidk/idk/pull/15911</a> | 8316933: RISC-V: compiler/vectorapi/VectorCastShape128Test.java fails when using RVV

#### Backport jdk21u:

<a href="https://github.com/openjdk/jdk21u/pull/165">https://github.com/openjdk/jdk21u/pull/165</a> | 8315931: RISC-V: xxxMaxVectorTestsSmokeTest fails when using RVV

#### JDK11U for RV32:

- 1. 修复 C2 调用 intrinsics 过程中栈帧错位的问题
- 2. 修复 C2 Long 类型数据左移节点逻辑

### openEuler RISC-V(周嘉诚)

- Preparing the latest release of 23.09
  - Ironing out final details and procedures of release
- Approaching milestones of the "LLVM Parallel Universe Project"
- Brief work recap
  - <u>qt5-qtwebkit: add riscv64 enablement patch [distro] [merged]</u>
  - <u>iotop: add a fix for riscv64 [distro] [merged]</u>
  - kubernetes: refresh enablement patch [distro] [open]
  - kubeedge: add a patch for riscv64 support [distro] [merged]
  - mailit-framework: add a upstream fix [distro] [merged]
  - kf5-kirigami2-addons: init package [distro] [merged]
  - Many other packaging changes, and more fixes for the "LLVM Parallel Universe Project"

### Gentoo for RISC-V 的情况更新(Gentoo 小队)

● 暂无更新

#### Arch Linux RISC-V(潘瑞哲、Felix)

[core] 256 / 263 (97.34%) [extra] 12578 / 13365 (94.11%)

Package update count: 5590

Distinct package update count: 3788

Arch	[core]			[extra]		
	Up-to-date (Ratio%)	Outdated	Missing	Up-to-date (Ratio%)	Outdated	Missing
x86_64	263	0	0	13359	0	0
i486	142 (53.99%)	113	8	3920 (29.34%)	5541	3898
i686	169 (64.26%)	89	5	6004 (44.94%)	5899	1456
pentium4	169 (64.26%)	89	5	5880 (44.02%)	5931	1548
aarch64	239 (90.87%)	12	12	10902 (81.61%)	296	2161
armv7h	240 (91.25%)	10	13	10611 (79.43%)	412	2336
riscv64	248 (94.3%)	7	8	11262 (84.3%)	1265	832
loong64	150 (57.03%)	110	3	6697 (50.13%)	3543	3119

```
linux - 6.4.10.arch1-1.1 --> 6.5.2.arch1-1
glibc - 2.37-3 --> 2.38-3.1
qcc - 13.1.1-2 --> 13.2.1-3.2
clang - 15.0.7-9 --> 16.0.6-1
firefox - 116.0.3-1 --> 118.0-1
ire-openidk - 20.0.2.u9-3 --> 21.u35-3
rust - 1:1.71.1-1 --> 1:1.72.1-1
libreoffice-fresh - 7.5.5-1 --> 7.6.1-1
electron24 - 24.8.0-1 --> 24.8.3-1
electron25 - 25.5.0-1 --> 25.6.0-1
electron - never been built --> 1:25-1
code - 1.81.1-1 --> 1.82.2-2
chromium - 116.0.5845.96-1 --> 117.0.5938.92-2
```

### Arch Linux RISC-V(潘瑞哲、Felix)

#### 125 PRs merged: ref

- Code OSS
- Chromium 117.0.5938.92
- OpenSSL: reconfigure to enable RISC-V optimization codes
- Electron 25
- Electron 24
- Linux 6.5.2.arch1
- go 2:1.21.1 Workaround AUIPC+JALR mis-optimized
- rust 1.72.1
- gcc 13.2.1 cherry-pick for fixing glibc compatibility

#### Arch Linux RISC-V(潘瑞哲、Felix)

 openssl: SSL related tests are failing with high HARNESS\_JOBS

https://github.com/openssl/issues/22166

- cockatrice: qemu-user segfaults in tcg interval\_tree\_insert
  - o qemu 8.1.0 regression, bisect:
  - o commit 2d708164e

```
linux-user/riscv/target_mman.h []

... ... @@ -1 +1,8 @@

1 + /*
2 + * arch/loongarch/include/asm/processor.h:
3 + * TASK_UNMAPPED_BASE PAGE_ALIGN(TASK_SIZE / 3)
4 + */
5 + #define TASK_UNMAPPED_BASE \
6 + TARGET_PAGE_ALIGN((1ull << (TARGET_VIRT_ADDR_SPACE_BITS - 1)) / 3)
7 +

1 8 #include "../generic/target_mman.h"
```

- rust 1.72: <u>https://github.com/felixonmars/archriscv-packages/pull/2950</u>
- Pin cc dependency of src/bootstrap to 1.0.77. src/bootstrap/llvm.rs relies on internal implementation details of cc crate and cc 1.0.78 contains a change that breaks llvm.rs's assumptions.
- code: <u>https://github.com/felixonmars/archriscv-packages/pull/3022</u>
- need to build native node extensions in debug mode or they still segfaults even in electron25

### Fedora for RISC-V status update (20230928)

- RPM packaging
  - Status: Updating Fedora 38
    - 22816/23293 [97.95%] srpm have been built.
  - Spin: Server/Workstation/Cloud
  - WIP Spin: IoT/CoreOS [ONGING]
- main package version:
  - Toolchain(up-to-date for F38)
    - gcc-13.2.1 -1[DONE]
    - glibc-2.37.4[DONE]
    - Binutils 2.39-15[DONE]
  - libffi-3.4.4-2(up-to-date)
  - java-latest-openjdk-19.0.2.0.7
  - perl-5.36.1-497(up-to-date)
  - $\circ$  Python 3.11.4-1(up-to-date)  $\rightarrow$  3.12
  - LLVM/Clang 16.0.6-2(up-to-date)
  - o golang-1.20.7-1(up-to-date)
  - rust-1.72.0-1(up-to-date)

- Desktop support:
  - DONE: XFCE/LXDE/LXQT/GNOME/
     Budgie/Cinnamon/Mate/Sugar/Sway/KDE
  - Building: Deepin(will try to maintain it)
  - Key Desktop App
    - firefox-116.0-1[DONE]
    - Libreoffice 7.5.5.2-2[DONE]
    - Thunderbird 102.12.0[DONE]
    - Chromium 116[DONE]
- Image :
  - Sophgo SG2042 EVB/Milk-V[DONE]
  - TH1520 BeagleV/<u>LPi4A</u>/\*\*\*[DONE]
  - StarFive JH7110 boards[ONGOING]
- ROS/ROS2 upgraded to F38
  - ROS2 packaging is ongoing
- function testing:
  - Podman[pass], Image: <u>fedora-rv64</u>
  - Ceph[pass]
  - K8s [pass]demo in RISC-V summit

### Fedora for RV32 (20230928) working on 64ILP32

- Create a new bootstrap framework, target on multi-arch rpm-based Linux distro bootstrap
  - https://github.com/fedora-riscv/bootstrap
- Download srpm automatically by a given list
  - https://github.com/fedora-riscv/srpm-get
- Automated build script using yaml
  - https://github.com/fedora-riscv/rpm-builder
- All the documents for this bootstrap
  - https://github.com/fedora-riscv/bootstrap-development-log
  - https://github.com/fedora-riscv/rpmbuild-fedora-log

Core group DONE!

**DNF works well!!** 

The current status: building stage4 rpms for the standard Fedora minimal image, 84/149[56%].

Stage1: Native toolchain build



Stage2: minimal rootfs (with make)

Stage3: native build packging tools: rpmbuild

Cross build



Stage6: koji Image builder rpms

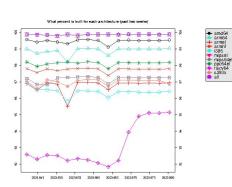


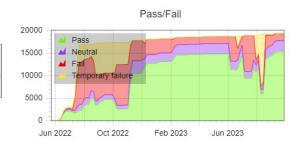
Stage5: koji rpm builder rpms



#### Debian for RISC-V(于波)

- Official porting update
  - 1. Installed: ><u>16K</u>
  - 2. BD-Uninstablled: < 500
  - 3. Architecture percent: > 95%
  - 4. testing suite will be coming
- Debci\_update
  - Over 25K binary for britney's job
- Some works
  - 1. Chromium 116.0.5845.<u>180-1</u> [Debian upstream]
  - 2. <u>python-pyface</u>, <u>ceph</u>, <u>libobd</u>, <u>yubioath-desktop</u> [ftbfs done]
  - 3. nodejs(18.18.0) MR, golang-github-zyedidia-tcell/terminal/micro
  - 4. python filecheck package







#### FW相关更新 (王翔)

#### opensbi

- ➤ 离散hartid支持合并, 重构 last\_hartindex\_having\_scratch/hartindex\_to\_hartid\_table/hartindex\_to\_scratch\_table 节约一些内存开销
- ➢ 修正文档fw\_payload.md
- ➤ 对sbi\_pmu\_ctr\_cfg\_match添加索引检查防止溢出
- ➤ 修复sbi\_domain\_get\_assigned\_hartmask中的整数移位溢出 问题
- 简化dt\_parse\_isa\_extensions,移除判断sbi\_scratch\_offset\_ptr返回值为空
- ➤ 修正SET\_ISA\_EXT\_MAP,do ... while的包裹使得continue无效

## 固件相关更新(洛佳)

● 本周暂无更新

## RISCV性能跟踪小队 - 陈小欧

● 暂无更新

#### 香山开源RISC-V处理器 - ICT / PCL

- 取指前端
  - 修复 Predecode 部分时序问题(#2291)
  - 修复 IFU 的 redirect 的 predecode 检查指令有效性问题(#2300)
  - 修复 BPU 模块的 target 通路时序问题(#2324)
  - 实现 FTQ 中提前一拍接收后端的 redirect 信号,减少 redirect penalty (#2329)
- 乱序调度&向量
  - 实现推测 BusyTable, 以支持快速唤醒和取消(#2290)
  - 重构 PcTargetMem, 修复 Jump 误预测问题(#2318)
  - 实现提前一拍反馈重定向信号给前端(#2329)
- 访存
  - 完成向量访存 Load Flow Queue 的代码、向量访存测试环境的搭建,向量 Store 新方案正在开发中
  - 完成 TLB 结构变化的修改(#2289)
  - 完成 BOP with delay queue 的代码(#2239)
  - 实现 SMS 预取优化(#2314)
- 缓存
  - 定位并解决请求融合的性能 bug,请求融合合入主线(#2337)

#### MLIR 结合 RISC-V 相关工作 - 张洪滨

- Buddy Compiler 端到端 LLaMA2-7B 推理
  - 自定义 Torch Dynamo 编译后端
  - 优化: Vector Dialect, OMP Dialect, Affine Dialect, ...
  - WIP: 修复已知 Bug, 打磨代码合入主线
  - WIP: RVV Specific Optimization, Gemmini Accelerator Support
  - Authors: @weilinquan, @xTayEx, @EllisLambda, @Lester-1, @qingqing12138
  - Mentors: @zhanghb97, @xlinsist, @SForeKeeper, @LHY-24

### Chisel and Additional Technology / Sequencer

暂无更新

## OpenHW & OpenHW Aisa Working Group

## ROCm bootstrapping for RISC-V (陆言, PLCT Tariser)

● 本周暂无更新

## 自由讨论 / AOB

# **BACKUP**

## 准备加入更多的国际开源组织进行同步观测

欢迎追加或提议