

欢迎第一次加入的伙伴(开会时请从下一页开始展示)

- 开放编辑, 直接点击 request for edit 然后在东亚时区群里at吴伟
- 如果没有找到自己的内容分类, 可以添加1-2页在最开始或中间
- 欢迎在开始的前5分钟进行自我介绍
- 日常八卦在东亚时区RISC-V双周同步微信群中, 欢迎加入

东亚时区RISC-V双周会

2023年03月30日·第054次

<https://github.com/cnrv/RISCV-East-Asia-Biweekly-Sync>

Host: 陈嘉炜

Organizer: PLCT Lab plct-oss@iscas.ac.cn

会议议程(15:00 - 16:00)

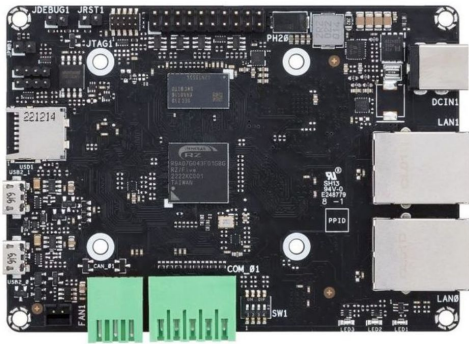
- 自我介绍、等待参会者接入、非技术话题八卦(没有的话就直接跳过)
- RVI 的更新和八卦(基本上跟东亚双周会群内消息同步)
- Unratified Specs 的参考实现进展
- 东亚地区小伙伴的项目更新
- 自由讨论

RISC-V International 同步、全球开源社区八卦

Ashling and Imagination announce [Ashling RiscFree C/C++ SDK](#) support for RISC-V-based Catapult family.

[ASUS Tinker Board V](#) will be using a RISC-V processor

全球首款RISC-V笔记本电脑[ROMA](#)正式发布！



RISC-V 韩语社区的同步与八卦

- 之前提过的韩国公司Zaram Technology，专注于开发监控、可穿戴设备等基于RISC-V的嵌入式SoC，预计今年推出自家的NPU，现在正在韩国IPO。
- 韩国公司Codaship的高性能RISC-V产品（A70）被韩国公司Siliconarts采用，预计在该社的PC GPU产品中使用。

RISC-V 日语社区的同步与八卦

- 有趣的开源项目 : 日本Cybozu Labs的开发者用Rust写了一个RISC-V Emulator, 支持rv32imac/rv64imac
- [Alignof/carron: RV64IMAC emulator \(github.com\)](https://github.com/Alignof/carron)

RISC-V 俄语社区的同步与八卦

两起俄罗斯开发人员被禁止公开开发 FOSS 代码的事件

1. Yadro的员工Alexander Amelkin的GitHub账户被无缘无故封禁，仓库[GitHub - ipmitool/ipmitool: An open-source tool for controlling IPMI-enabled systems](#)被归档
2. Baikal Electronics的员工Sergey Semin对Linux内核的贡献被拒绝
[Re: \[PATCH net 00/13\] net: stmmac: Fixes bundle #1 - Jakub Kicinski](#)

AOSP for RISC-V 进展

- Google AOSP upstream PR
 - Android (RISC-V) Review 双周报 第 13 期(in Chinese): <https://zhuanlan.zhihu.com/p/618145179>
 - Toolchain 部分, Enable targeting riscv64-linux-android 补丁已经合入 LLVM/Clang 上游。
 - ART 部分本周期提交的补丁不多, 主要来自国内 RISC-V 大厂阿里平头哥以及合作伙伴 xcvmbyte 的贡献。
 - Bionic 方面的主要工作集中在 SCS (Shadow Call Stack) 的实现., 另外来自中国的公司 ESWIN 也为 bionic 提交了一个优化补丁。
 - 在模拟器 cuttlefish 方面, 基于最新 (至少 3 月 23 日后) 的 aosp 代码, 尝试构建并使用 cuttlefish 已经成功, 具体见邮件列表 topic : <https://lists.riscv.org/g/sig-android/topic/97534045>
- RVI Android SIG upstream:
 - Chromium for Android apk 从 93/96 升级到 109.0.5414.87 Status update
 - <https://github.com/aosp-riscv/chromium/pulls?q=is%3Apr+is%3Aclosed>
- 技术文章
 - 链接处理过程中的"符号解析(Symbol Resolution)": <https://zhuanlan.zhihu.com/p/616183375>

RISC-V GCC进展

RVV目前除了segment 外其他intrinsic已经全部在上游支持了。RV64 连续测了约一个月基本稳定没有BUG, google/highway也在测试中被使用了。

临近gcc13 release, 正在协助修复回归测试中发现得错误:

<https://gcc.gnu.org/pipermail/gcc-patches/2023-March/614396.html>

<https://gcc.gnu.org/pipermail/gcc-patches/2023-March/614678.html>

<https://gcc.gnu.org/pipermail/gcc-patches/2023-March/614847.html>

ZC扩展GCC中发现一个中断导致的load/store匹配错误问题, 正在处理中:

<https://github.com/openhwgroup/corev-gcc/issues/30>

Android-SIG提出保留寄存器的使用需求, 目前Kito提出了几种解决方案, 还在讨论中:

<https://github.com/riscv-non-isa/riscv-elf-psabi-doc/issues/370>

Clang/LLVM 进展 (PLCT)

- 基于LNT搭建了测评平台, 欢迎使用, 提需求 <https://lnt.rvperf.org>

Active Machines

Machine	Latest Submission	Results
rv32gc-O3-thinlto:6	2 hours ago	View Results
rv64gc-O3-thinlto:2	34 minutes ago	View Results
rv64gc-Os-thinlto:3	8 minutes ago	View Results
rv64gcxx-O3-thinlto:5	1 hour ago	View Results

- 被合并的patch
 - [LegalizeTypes][RISCV] Add a special case for (add X, -1) to ExpandIntRes_ADDSUB <https://reviews.llvm.org/D146635>
 - [Local] Preserve !nonnull only when K dominate J and K has a !noundef <https://reviews.llvm.org/D146799>
 - [Local] Use most generic range if K does not dominate J or K doesn't have a !noundef <https://reviews.llvm.org/D142687>
 - [flang][nfc] Remove unused codes in idioms.h <https://reviews.llvm.org/D146709>

Clang / LLVM 社区的更新 (廖春玉、陆旭凡)

1. <https://reviews.llvm.org/D143708> [RISCV] Support emulated TLS
2. <https://reviews.llvm.org/D146946> [RISCV][MC] Add support for experimental zicond extension
3. <https://reviews.llvm.org/D147086> [RISCV][GlobalSel] Add lowerCall for calling convention
4. <https://reviews.llvm.org/D146463> [CodeGen][RISCV] Change Shadow Call Stack Register to X3

QEMU/Spike/Sail/ACT进展 (PLCT)

- Qemu

- RVH相关检查以及代码格式优化

- <https://github.com/plctlab/plct-qemu/tree/plct-virtfix-upstream>

- <https://lists.nongnu.org/archive/html/qemu-riscv/2023-03/msg00716.html>

- PM相关bug修复以及指令pm的支持

- <https://github.com/plctlab/plct-qemu/tree/plct-pm-fix-v2>

- <https://lists.nongnu.org/archive/html/qemu-riscv/2023-03/msg00824.html>

- 其它bug修复

- <https://lists.nongnu.org/archive/html/qemu-riscv/2023-03/msg00832.html>

- <https://lists.nongnu.org/archive/html/qemu-riscv/2023-03/msg00874.html>

V8 for RISC-V 更新(邱吉、陆亚涵)

Port 上游更新

1.4344114: [riscv] Remove the unused kOffHeapTrampolineRegister |

<https://chromium-review.googlesource.com/c/v8/v8/+4344114>

2.4347985: [riscv] Move data fields from InstructionStream to Code | <https://chromium-review.googlesource.com/c/v8/v8/+4347985>

3.4348677: [riscv] Clean up api callback stack access | <https://chromium-review.googlesource.com/c/v8/v8/+4348677>

4.4293541: [riscv] Enable the vector extension as default on simulator mode |

<https://chromium-review.googlesource.com/c/v8/v8/+4293541>

5.4355044: [riscv] Allocate builtin Code objects in RO space | <https://chromium-review.googlesource.com/c/v8/v8/+4355044>

other update:

实现rvv vslide指令

jingpeiyang@eswincomputing.com:

1.4351855: [riscv] Improve vslide* instruction and test | <https://chromium-review.googlesource.com/c/v8/v8/+4351855>

Spidermonkey for RISC-V更新（邱吉、陆亚涵）

Port 上游：

1. <https://phabricator.services.mozilla.com/D172760>

OpenJDK for RISC-V 更新(RV64及upstream) 杨飞(离线)

1. Authored JDK-mainline PRs:

- <https://github.com/openjdk/jdk/pull/12849> (8303562: Remove obsolete comments in os::pd_attempt_reserve_memory_at)
- <https://github.com/openjdk/zgc/pull/16> (RISC-V: Only use conditional far branch in copy_memory for ZGC)
- Added more RISC-V-Specific changes for JDK-8291555:
<https://github.com/openjdk/jdk/pull/10907/commits/0ad01c1d794bbbfbfef911c1ef4d8601f2e48302>

2. Reviewed JDK-mainline PRs:

- <https://github.com/openjdk/jdk/pull/12547> (8302368: [ZGC] Client build fails after JDK-8300255)
- <https://github.com/openjdk/jdk/pull/12553> (8302453: RISC-V: Add support for small width vector operations)
- <https://github.com/openjdk/jdk/pull/12616> (8302776: RISC-V: Fix typo CSR_INSTERT to CSR_INSTRET)
- <https://github.com/openjdk/jdk/pull/12670> (8302780: Add support for vectorized arraycopy GC barriers)
- <https://github.com/openjdk/jdk/pull/12753> (8303210: [linux, Windows] Enable UseSystemMemoryBarrier by default if possible)
- <https://github.com/openjdk/jdk/pull/12869> (8302976: C2 intrinsification of Float.floatToFloat16 and Float.float16ToFloat yields different result than the interpreter)
- <https://github.com/openjdk/jdk/pull/12950> (8303863: RISC-V: TestArrayStructs.java fails after JDK-8303604)
- <https://github.com/openjdk/jdk/pull/12969> (8303955: RISC-V: Factor out the tmp parameter from copy_memory and copy_memory_v)
- <https://github.com/openjdk/jdk/pull/13053> (8304293: RISC-V: JDK-8276799 missed atomic intrinsic support for C1)
- <https://github.com/openjdk/jdk/pull/13071> (8304387: Fix positions of shared static stubs / trampolines)
- <https://github.com/openjdk/jdk/pull/12551> (8302384: Handle hsdis out-of-bound logic for RISC-V)
- <https://github.com/openjdk/jdk/pull/12778> (8301995: Move invokedynamic resolution information out of ConstantPoolCacheEntry)
- <https://github.com/openjdk/jdk/pull/12324> (JDK-8301496: Replace NULL with nullptr in cpu/riscv)
- <https://github.com/openjdk/jdk/pull/13202> (8305008: RISC-V: Factor out immediate checking functions from assembler_riscv.inline.hpp)

3. OpenJDK17u backport update:

- Reviewed and merged 27 backport PRs: <https://github.com/openjdk/riscv-port-jdk17u>
- Daily builds are available here: <https://builds.shipilev.net/openjdk-jdk17-riscv>
- Tier1-4 tested on SiFive Unmatched board (with release build)
- Tested non-trivial benchmark workloads on SiFive Unmatched board: SPECJVM, SPECJBB, Renaissance, Dacapo, etc.
- Need to backport several more patches for enabling RVC extension by default

OpenJDK for RISC-V 更新(RV64及upstream) 张定立

Merged & New JDK-mainline PRs:

- <https://github.com/openjdk/jdk/pull/13202> | (8305008: RISC-V: Factor out immediate checking functions from assembler_riscv.inline.hpp)

Backport jdk17u:

- <https://github.com/openjdk/riscv-port-jdk17u/pull/7> | (8287552: riscv: Fix comment typo in li64)
- <https://github.com/openjdk/riscv-port-jdk17u/pull/13> | (8291893: riscv: remove fence.i used in user space)
- <https://github.com/openjdk/riscv-port-jdk17u/pull/17> | (8301313: RISC-V: C2: assert(false) failed: bad AD file due to missing match rule)
- <https://github.com/openjdk/riscv-port-jdk17u/pull/18> | (8299847: RISC-V: Improve PrintOptoAssembly output of CMovEl/L nodes)
- <https://github.com/openjdk/riscv-port-jdk17u/pull/25> | (8300109: RISC-V: Improve code generation for MinI/MaxI nodes)
- <https://github.com/openjdk/riscv-port-jdk17u/pull/26> | (8297715: RISC-V: C2: Use single-bit instructions from the Zbs extension)

OpenJDK for RISC-V 更新(RV64及upstream) 曹贵

Merged & New JDK-mainline PRs:

- <https://github.com/openjdk/jdk/pull/12778> | (8301995: Move invokedynamic resolution information out of ConstantPoolCacheEntry)(as co-author)

Backport jdk17u:

- <https://github.com/openjdk/riscv-port-jdk17u/pull/15> | (8291947: riscv: fail to build after JDK-8290840)
- <https://github.com/openjdk/riscv-port-jdk17u/pull/19> | (8304293: RISC-V: JDK-8276799 missed atomic intrinsic support for C1)
- <https://github.com/openjdk/riscv-port-jdk17u/pull/22> | (8297644: RISC-V: Compilation error when shenandoah is disabled)
- <https://github.com/openjdk/riscv-port-jdk17u/pull/27> | (8305006: Use correct register in riscv_enc_fast_unlock())

OpenJDK8 backporting (章翔)

- [Fix the ARCH and SRCARCH](#)
- [Add riscv64 for sys_clock_getres](#)
- [Fix vmIntrinsics::_linkToVirtual](#)
- [Fix bs->try_resolve_jobject_in_native for release javac](#)
- [Fix resolve_jobject](#)
- [Add riscv64 for test](#)
- [Fix const static int InterpreterCodeSize = 208 * 1024;](#)
- [Fix codeCahe in oerv](#)
- [Fix dacapo-eclipse&tomcat](#)
- [Fix stack_guard_state_offset](#)
- [Fix set_mdp_flag_at](#)
- [Fix lbu in g1_write_barrier_post](#)
- [Fix WARNINGS_ARE_ERRORS for oerv](#)
- [Fix profile_return_type due to intrinsic_id_offset_in_bytes](#)

- [Fix ExternalAddress in branch](#)
- [Fix lwu for form_address in c1](#)

测试集: SPECjvm通过情况与x86保持一致 ([SPECjvm2008测试记录 · Issue #261 · zhangxiang-plct/jdk8u \(github.com\)](#))

dacapo (通过率: 71.4% <https://github.com/zhangxiang-plct/jdk8u/issues/253#issuecomment-1378447521>)

jtreg-tier1 (通过率: 95% [jtreg调试记录 · Issue #321 · zhangxiang-plct/jdk8u \(github.com\)](#))

openEuler RISC-V

- [WIP] openEuler 23.03创新版:测试镜像已出
 - [https://build.tarsier-infra.com/project/show/openEuler:23.03_4300\(4300+\)](https://build.tarsier-infra.com/project/show/openEuler:23.03_4300(4300+))
 - [https://build.tarsier-infra.com/project/show/openEuler:23.03:Epol_1234\(1100+\)](https://build.tarsier-infra.com/project/show/openEuler:23.03:Epol_1234(1100+))
 - 测试镜像: <https://mirror.iscas.ac.cn/openeuler-sig-riscv/openEuler-RISC-V/testing/20230322/v0.1/>
 - 测试列表: <https://docs.qq.com/sheet/D5m93aWhQVUIpT0VJ?tab=kwi6yq>
 - XFCE、UKUI、DDE、Kiran、GNOME、Cinnamon 六种桌面环境均可运行
- PR(23个): <https://gitee.com/openeuler/RISC-V/blob/master/archive/weeklyreports/2023-03-23.md>
 - openresty:升级到最新release 并初步支持 riscv64 @Jingwiw
 - risc-v-kernel:清理spec增加配置 @laokz
 - lwip:修复riscv64上的构建 @laokz
 - pytorch:rebase中间仓补丁 @laokz
 - qemu:增加user模式模拟器 @laokz
 - openmpi:Upgrade OpenMPI to 4.1.5 @arielheleneto
 - mozilla:升级并添加 riscv64 架构的 JIT 支持 @Jingwiw
 - openssl:修复riscv64上的构建 @laokz
 - libpox:将"GLIBC_2.27"加入test/dlwrap.c @laokz
 - libvirt:增加riscv构建支持 @laokz
 - libaio:删除补丁2的架构隔离宏 @laokz
 - isomd5sum:[手工sync] PR-10: 增加riscv支持并使能%check @laokz
 - isula-build:riscv64去除-static-pie @laokz
 - jnr-ffi:修复riscv64上的有关构建测试错误 @laokz
 - jffi:应用上游补丁修复riscv64上的有关构建测试错误 @laokz
 - apache-commons-daemon:Fix build failed on openEuler RISC-V @misaka00251
 - gazelle:[WIP] Fix deprecated ETH_LINK macros @misaka00251
 - fence-virt:Enable build on riscv64 @misaka00251
 - obs-server:Fix build on riscv64 @misaka00251
 - color-fs:Add riscv64 support for color filesystem @misaka00251
 - obs-bundled-gems:Fix build on riscv64 @misaka00251
 - gn:Add risc-v and loongarch support @misaka00251

Gentoo for RISC-V 的情况更新 (Gentoo 小队)

- Support statistics (7761/18687, 41.53%) : <https://whale.plctlab.org/riscv/support-statistics/>
- A total of 11 keywording commits: <https://whale.plctlab.org/riscv/RISC-V-双周会/20230330/commits.txt>
 - app-containers/docker-buildx: Keyword 0.10.4 riscv
 - kde-apps/kgpg: keyword 22.12.3 riscv
 - kde-apps/kleopatra: keyword 22.12.3 riscv
 - x11-misc/rofi: keyword 1.7.5 for ~riscv
- doing riscv keyword on firefox
 - <https://bugs.gentoo.org/903411>

Arch Linux RISC-V (东东、潘瑞哲)

- Report generated on: 20230330
- Package update count: 1800
- [core] 256 / 263 (97.33%)
- [extra] 2992 / 3099 (96.54%)
- [community] 9100 / 10123 (89.89%)
- firefox - 110.0.1-1 --> 111.0-1 no patchset change since last update
- nodejs - 19.7.0-1 --> 19.8.1-1 no patchset change since last update
- sbcl - WIP (bootstrapping) 挺难搞的
 - reverted commit e50eda73 from 2.2.3
 - its backend misused A7 reg

Arch Linux RISC-V (东东、潘瑞哲)

- percona-server (see: [felixonmars/archriscv-packages #2390](#))
 - Adds various memory barrier methods:
 - `mb()`, `rmb()`, `wmb()` according to RISC-V unprivileged specs section A.5
 - `xcng()` from Linux kernel source code
 - `cpu_pause()` using Zihintpause's `pause`
- luajit (see: [felixonmars/archriscv-packages #2362](#))
 - Upstream maintainer: we should use clang to avoid some issues with ffi. Also disable LTO.
- mold
 - Disable test `z-dynamic-undefined-weak` because clang hangs
 - Disable `MOLD_USE_MOLD` because gcc does not pass default library path
 - causes linking issues for mold
 - bfd automatically searches conventional paths, so it works fine
 - consider modifying gcc specs to add `-L/usr/lib/`

Fedora for RISC-V (傅炜)

- 本周暂无更新

Debian for RISC-V(于波)

- [Official porting update](#)

Waiting FTP team to add riscv64 on unstable(many pings but no replies)

Filing a request against the ftp.debian.org(WIP)

- [Debci update](#)

[debci riscv64 alerts page](#) (fixed: timeout; false positive;exception)

- Some works

1. firefox [110.0.0-1](#), [111.0.0-1](#)

2. thunderbird [110.0](#)

3. <https://github.com/numba/llvmlite/issues/923> [help]

4. [#1033629](#) [ruby-devise pass debci]

Deepin for RISC-V

本周暂无进度

FW相关更新（王翔）

❖ opensbi

- Startfive JH7110添加i2c驱动，并添加电源管理芯片支持实现重启和关机
- 优化sbi_scarch内存申请时的对齐操
- 修正如何检测domain是否包含fw_region
- 添加一个计数器分别在sbi_hsm_init之前和sbi_hsm_hart_start_finish之前计数器，防止hotplug hart_start唤醒以启动的核心
- 添加CPPC扩展，这个扩展和ACPI配合用于性能调节，主要定义了一些寄存器给ACPI读写
- 修正fw_jump.md文档中用于检测内核太大的示例代码

固件相关更新(洛佳)

- RustSBI原型设计系统的更新
 - d1-rom-rt: 重构项目, 并启动ddr控制器 ([#3](#))
 - xtask: 完成tui控制的编译框架 ([#5](#))
 - aw-soc: 完成了com、phy、uart和gpio, spi已完成部分 ([#4](#), [#8](#))
 - flashes: 增加新模块, 读闪存元数据 ([#9](#), [#10](#))
 - bootstrap: 增加ddrinit、hello world和spi flash示例 ([#6](#), [#7](#))
- RustSBI子项目: 正在迁移到RustSBI原型设计系统
- 下周目标
 - 整理SBI运行环境, 适配fast-trap
 - d1-rom-rt、aw-soc项目独立管理, base-address项目发布首个版本
 - 跳转到内核态UEFI服务入口

RISCV性能跟踪小队 - 陈小欧

Flutter/Dart在RISC-V上的支持现状

1. Flutter支持情况

Flutter在2022年3月就有开发者提议添加对RISC-V的支持, 其中包括[linux平台的支持](#), [Android平台的支持](#)。

添加RISC-V支持主要的工作有:

- patches in the engine and Flutter tool to handle RISC-V
- pre-built Engine snapshots for RISC-V

[Issue 117973](#)中开发者提到Flutter针对RV支持的开发, 受阻于开发板的性能,

2. Dart SDK支持情况

Dart SDK目前已经有支持RISC-V的Beta版本(3.0.0-290.3.beta)发布, 下载地址

同时, 也可以自己从源码构建, 目前是需要交叉编译, 构建指导可以参考:

<https://github.com/dart-lang/sdk/wiki/Building-Dart-SDK-for-ARM-or-RISC-V>

Dart SDK的回归测试可以参考: <https://github.com/dart-lang/sdk/wiki/Testing>

	x64 (s)	unmatched (s)	rv64/x64
dart create	6.546	23.704	3.62
dart run	0.761	20.102	26.42
dart test	12.253	253.844	20.72
dart compile	3.167	50.829	16.05
hello.exe	0.005	0.041	8.20

3. Dart SDK Beta for RISCV试用

在Linux上可以创建和运行cli和server的程序, 做了简单的cli性能对比(创建和运行一个简单的hello程序)

4. Dart SDK的回归测试还没有跑通

5. 知乎文档: <https://zhuanlan.zhihu.com/p/618200990>

香山开源RISC-V处理器 - ICT / PCL

- 南湖进展
 - 在 FPGA 上图形界面启动 glmarks、GLXGears、x11perf、firefox 等应用（感谢 PLCT 的帮助）
 - 开始香山的 UEFI 的开发工作
- 昆明湖进展
 - 前端:L2 FTB 实现完成开始性能调优, 探索 FDIP 的优化和 BATAGE 的实现
 - 后端:实现简单的 ROB 压缩;完成新版的 move 指令消除
 - 访存:向量 Load 初版实现完成;探索 Store 预取的实现
 - 缓存:实现新版 L2 去除 Set 阻塞、early release 等性能优化

MLIR 结合 RISC-V 相关工作 - 张洪滨

注: 提交人不在线 hongbin2019@iscas.ac.cn

完善 MLIR Vector Dialect Dynamic Vector Length Support Proposal (更新了一版 Draft RFC, 已提交给 Google 团队讨论)

- Integrate vector length configuration with the current mask operation.
- Create a standalone vector length operation
- Insert an optional argument in the existing operations.

RVV Co-Design

- <https://github.com/buddy-compiler/buddy-mlir/commit/cc57e60f073d769224a334b4df10c16b43eb2711>
- <https://github.com/sequencer/vector/commit/2c898e014eba73d30b2ade7db4c7b7239d7ae1ce>
- <https://github.com/sequencer/vector/commit/ea8412c50a0ff4c4f71ae36972e0ce5ee2fec134>

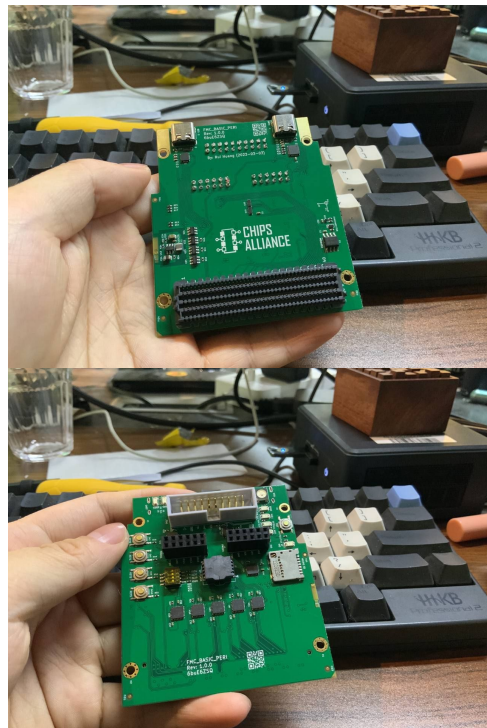
Gemmini Dialect

- <https://github.com/buddy-compiler/buddy-mlir/commit/6104e6a6f683dad89ac272ed8baba5e5716fe65b>
- WIP: 各种 Operation Benchmark Cases
- WIP: 完成完整神经网络推理

Chisel and Additional Technology / Sequencer

咕子

- Vector RTL开始和Buddy小队进行性能联合调试
 - buddy提了很多需求, 已经逐步开始安排优化了
 - 跑过了基于MLIR的strip mining/mat mul的例子
- RTL code review
 - 进行组内/跨组的架构+代码 review 针对性提出架构优化点
- Rocket PCB
 - <https://github.com/chipsalliance/rocket-pcb>
 - 用于Chisel外设IP板级验证测试



OpenHW & OpenHW Aisa Working Group

Hello AWG members

OpenHW Group is organizing a technical session presenting OpenHW/ RISC-V projects at the upcoming Embedded World conference at the Shanghai World Expo Exhibition & Convention Center from June 14-16.

This session will comprise three technical presentations on development of OpenHW technology. The presenters should be physically present at the conference. Any of our projects would be suitable presentation topics, with a thematic focus on embedded systems. The focus should be on the open-source projects and technology, not on product promotion. The languages of this conference are Chinese and English.

To have a sense of the focus of the conference, other sessions are listed here

https://www.embedded-world.com.cn/en/conference_call%20for%20papers

I think this is a great opportunity for Asian regional members to present work they are driving within OpenHW Group. Could you please let me know as soon as possible if you may be interested in presenting one of these three presentations, and the topic of course?

Thank you!

Duncan

自由讨论 / AOB

- 听说ARM要涨价了...
- [OpenEuler Developer Day 2023](#)

BACKUP

准备加入更多的国际开源组织进行同步观测

欢迎追加或提议