欢迎第一次加入的伙伴(开会时请从下一页开始展示)

- 开放编辑，直接点击 request for edit 然后在东亚时区群里at吴伟
- 如果没有找到自己的内容分类，可以添加1-2页在最开始或中间
- 欢迎在开始的前5分钟进行自我介绍
- 日常八卦在东亚时区RISC-V双周同步微信群中，欢迎加入

东亚时区RISC-V双周会

2022年09月01日·第042次

https://github.com/cnrv/RISCV-East-Asia-Biweekly-Sync

Host: 邱吉

Organizer: PLCT Lab plct-oss@iscas.ac.cn

会议议程（15:00 - 16:00）

- 自我介绍、等待参会者接入、非技术话题八卦（5分钟）
- RVI 的更新和八卦（基本上跟东亚双周会群内消息同步）
- Unratified Specs 的参考实现进展
- 东亚地区小伙伴的项目更新
- 自由讨论

RISC-V International 同步、全球开源社区八卦

- 第二届 RISC-V 中国峰会顺利结束，惊喜超多
- 北美RISC-V峰会改成了 RISC-V Global Summit，跟 RISC-V China Summit 区分和同品牌化
  - 感觉今年特别强调透明性，并且将审稿责任等交给TSC下属各个技术工作组织的chair/co-chairs。
  - 还有10天截稿，9月9日截稿，注意看 Michele 的邮件！
- PLCT Lab 又开始搞大新闻：用廉价交换机和RISC-V开发板搭建超过1000个节点的RISC-V集群
  - 开始征集想要运行的软件或者demo https://github.com/plctlab/riscv-cluster
-

AOSP for RISC-V - 汪辰、陆旭凡

- 参加第二届 RISC-V 中国峰会并与 RVI Android SIG 主席 - 毛晗做联合报告，幻灯片：https://github.com/aosp-riscv/working-group/blob/master/docs/slides/202208-rvsc2022-rvi-aosp-report.pdf
- RVI 上游 PR 贡献：
  - skip ptrace testing cases：https://github.com/riscv-android-src/platform-bionic/pull/35
  - Backport commits to support fe_getround and fe_raise_inexact in builtins：https://github.com/riscv-android-src/toolchain-llvm-project/pull/6
- Bionic/CTS 测试（基于模拟器）状态更新：
  - 数学库圆整问题：已解决，参考 https://gitee.com/aosp-riscv/working-group/issues/I5BV63
  - Signal Stack unwinding 问题：参考 https://gitee.com/aosp-riscv/working-group/issues/I5D6NY，根源发现是由于当前 LLVM/libunwind 不支持 signal frame unwinding。向 RVI 上游汇报后，T-head 提出补丁方案，现等待新版本发布并验证。
  - “-nan” 的 sprintf 问题：参考：https://gitee.com/aosp-riscv/working-group/issues/I5CKA4 已得到 rootcause，但考虑到处理的优先级问题，暂不考虑修改，计划向 Google 报告后看看他们对此有何评论。
  - sys_ptrace 失败问题：已解决，参考 https://gitee.com/aosp-riscv/working-group/issues/I5NL9M。
- 技术类文章分享：
  - 《聊一聊 Linux 上信号处理过程中的信号栈帧》：https://zhuanlan.zhihu.com/p/555659009
  - 《用于栈回溯的一些库》：https://zhuanlan.zhihu.com/p/556211455
  - 《和 ptrace 有关的一些笔记》：https://zhuanlan.zhihu.com/p/559140687

RISC-V GCC进展

RVV GCC upstream在持续推进中，目前钟居哲已有数个patch merge进upstream:

https://gcc.gnu.org/git/?p=gcc.git&a=search&h=HEAD&st=author&s=juzhe

Zmmul的binutils patch已merge进upstream:

https://sourceware.org/git/?p=binutils-gdb.git;a=commit;h=0938b032daa52129b4215d8e0eedb6c9804f5280

宋教授删除了两个RISC-V中不会用到的relocation type:

https://sourceware.org/git/?p=binutils-gdb.git;a=commit;h=453595283c323e106a60b229999756b45ae6b2d8

Christoph添加了AIA(Advanced Interrupt Architecture)扩展的binutils支持：

[PATCH] riscv: Add AIA extension support (Smaia, Ssaia)

https://lists.riscv.org/g/tech-aia

通过测试更新了gcc12.1-binutils中rv64gc-lp64d/lp64,rv32gc-ilp32d/ilp32, newlib与glibc的allowlist,
记录了部分新修复的和已知的 FAIL testcases:

https://github.com/riscv-collab/riscv-gnu-toolchain/pull/1116

RISC-V GCC进展

git://gcc.gnu.org / gcc.git / search

summary | shortlog | log | commit | commitdiff | tree
first · prev · next

middle-end: Add MULT_EXPR recognition for cond scalar reduction

5 hours ago	*zhongjuzhe*	**RISC-V: Add vector registers in TARGET_CONDITIONAL_REGISTER_...**	commit | commitdiff | tree
5 hours ago	*zhongjuzhe*	**RISC-V: Add csrr vlenb instruction.**	commit | commitdiff | tree
5 hours ago	*zhongjuzhe*	**RISC-V: Add RVV constraints.**	commit | commitdiff | tree
5 hours ago	*zhongjuzhe*	**RISC-V: Fix comment in riscv.h**	commit | commitdiff | tree
5 hours ago	*zhongjuzhe*	**RISC-V: Fix riscv_vector_chunks configuration according...**	commit | commitdiff | tree
23 hours ago	*zhongjuzhe*	**middle-end: Fix unexpected warnings for RISC-V port.**	commit | commitdiff | tree
3 days ago	*zhongjuzhe*	**RISC-V: Add RVV registers**	commit | commitdiff | tree
3 days ago	*zhongjuzhe*	**RISC-V: Add RVV instructions classification**	commit | commitdiff | tree
9 days ago	*zhongjuzhe*	**middle-end: Fix issue of poly_uint16 (1, 1) in self...**	commit | commitdiff | tree
2022-08-18	*zhongjuzhe*	**RISC-V: Add runtime invariant support**	commit | commitdiff | tree

Clang/LLVM 进展 (PLCT)

Gollvm:

1. [merged]gollvm跨平台编译支持 https://go-review.googlesource.com/c/gollvm/+/425199?usp=dashboard
2. [new] 优化跨平台编译 https://go-review.googlesource.com/c/gollvm/+/425854
3. [new] 向内置汇编器传入平台信息 https://go-review.googlesource.com/c/gollvm/+/425556

Upstream llvm:

1. [merged] 支持zihintntl拓展 https://reviews.llvm.org/D121670
2. [merged] 标量优化，x > 1 ? x : 1 -> x > 0 ? x : 1 https://reviews.llvm.org/D132211
3. [merged] lldb, 修复一个注释中的FIXME：将m_target_arch设置成private成员 https://reviews.llvm.org/D132353
4. [New] lldb, 为模拟器增加更多操作解 码 https://reviews.llvm.org/D132789
5. [New] 标量优化，fold 1 - X == X to false https://reviews.llvm.org/D132989
6. [New] zcmp子拓展，https://reviews.llvm.org/D132819

Clang / LLVM 社区的更新（廖春玉、陆旭凡）

1. D132365 [DSE] Support looking through memory phis at end of function.
2. D132771 [RISCV] Apply DeMorgan to (beqz (and/or (seteq), (xor Z, 1))) to remove the xor.
3. D132798 [RISCV] Add more invertible setccs to tryDemorganOfBooleanCondition.
4. D131958 [VP][RISCV] Add vp.fabs intrinsic and RISC-V support.
5. D133063 [docs] Add a RISC-V Usage page

QEMU/Spike/Sail/ACT进展 (PLCT)

- Qemu
  - Vector 反汇编支持v2
    - https://lists.gnu.org/archive/html/qemu-riscv/2022-08/msg00343.html
  - CORE-V MCU整理 支持优化
    - https://github.com/plctlab/plct-qemu/tree/plct-corev-upstream
    - https://github.com/plctlab/plct-qemu/tree/plct-corev-upstream-sync-dma

GEM5进展 (PLCT)

- V拓展开发进展
  - 新增指令
    - 定点饱和运算(vsadd.vv等)
    - 整数拓宽(vzext_vf2等)
    - 整数收缩位移指令(vnsrl.wv等)
    - 整数平均运算指令(vaaddu等)
    - 浮点转换指令(vfcvt.*, vnfcvt.*, vwfcvt.*)
    - 浮点单操作数指令(vfsqrt.v, vfrec7.v等)
    - gather指令(vrgather.* vrgatherei16.vv)
    - 位运算指令(vmand.mm等)
  - 为所有已实现的指令添加vtu/vmu支持
  - 修复vle*.v与vse*.指令uop拆分错误的问题
  - 还剩41条指令未实现

V8 for RISC-V 更新（邱吉、陆亚涵）

- V8 常规更新
  - 3867138: [riscv]Port [wasm] Keep call_indirect index on the stack | https://chromium-review.googlesource.com/c/v8/v8/+/3867138
  - 3857980: Reland "[riscv] Port [heap] Add shared barrier to RecordWrite builtin" | https://chromium-review.googlesource.com/c/v8/v8/+/3857980
  - 3844663: [riscv64][wasm-relaxed-simd] Implement relaxed i16x8.q15mulr_s | https://chromium-review.googlesource.com/c/v8/v8/+/3844663
  - 3835293: Reland "[WATCHLISTS] Add riscv watch" | https://chromium-review.googlesource.com/c/v8/v8/+/3835293
  - 3822761: [riscv] Fix wasm/generic-wrapper test failed | https://chromium-review.googlesource.com/c/v8/v8/+/3822761
  - 3831142: [riscv] Separate single and double precision zero to different registers to avoid misuse. | https://chromium-review.googlesource.com/c/v8/v8/+/3831142（from sifive ChouTing）

- 参加第二届 RISC-V 中国峰会并做了关于RV32GC V8 porting的报告

Spidermonkey for RISC-V - 邱吉、陆亚涵

- 提交了一些列patch, 目前汇编器、模拟器、反汇编、宏汇编等模块初步移植完成
  https://github.com/plctlab/gecko-dev-riscv
- Test jit-test status

  Pass 5914 Failed 3897 Timeout 29
  https://github.com/plctlab/gecko-dev-riscv/issues/27

OpenJDK for RISC-V 更新（RV64及upstream）杨飞

- GHA support for RISC-V (Based on Ubuntu 22.04):
  - -- https://github.com/openjdk/jdk/pull/10086 (8283929: GHA: Add RISC-V build config)

- Merged jdk-mainline PRs:
  - -- https://github.com/openjdk/jdk/pull/10079 (8293050: RISC-V: Remove redundant non-null assertions about macro-assembler)
  - -- Two WIP PRs pending.

- Reviewed jdk-mainline PRs:
  - -- https://github.com/openjdk/jdk/pull/9889 (8292407: Improve Weak CAS VarHandle/Unsafe tests resilience under spurious failures)
  - -- https://github.com/openjdk/jdk/pull/9970 (8292713: Unsafe.allocateInstance should be intrinsified without UseUnalignedAccesses)
  - -- https://github.com/openjdk/jdk/pull/9889 (8292867: RISC-V: Simplify weak CAS return value handling)
  - -- https://github.com/openjdk/jdk/pull/10056 (8293007: riscv: failed to build after JDK-8290025)
  - -- https://github.com/openjdk/jdk/pull/9936 (8292575: riscv: Represent Registers as values)
  - -- https://github.com/openjdk/jdk/pull/10057 (8293011: riscv: Duplicated stubs to interpreter for static calls)
  - -- https://github.com/openjdk/jdk/pull/10075 (8293065: Zero build failure on AArch64 and RISCV64 after JDK-8293007)
  - -- https://github.com/openjdk/jdk/pull/10065 (8293035: Cleanup MacroAssembler::movoop code patching logic aarch64 riscv)

- Reviewing jdk-mainline PRs:
  - -- https://github.com/openjdk/jdk/pull/9587 (8290154: [JVMCI] partially implement JVMCI for RISC-V)

- Reported JBS issue:
  - -- https://bugs.openjdk.org/browse/JDK-8292859 (test/hotspot/jtreg/gc/shenandoah/compiler/BarrierInInfiniteLoop.java timeouts after JDK-8292285)

- JDK regression test:
  - -- Tier1-3 test clean.
  - -- Tier4 need more testing and bugfixing.

- Loom RV64 port:
  - -- GC-related changes has been upstreamed, need rebase before start debugging

OpenJDK for RISC-V 更新（RV32/PLCT 史宁宁）

1、Fix the instructs in riscv32.ad
1)Fix the subL_reg_reg https://github.com/openjdk-riscv/jdk11u/pull/474
2)Fix the mulL() https://github.com/openjdk-riscv/jdk11u/pull/475
3)Fix the loadConL https://github.com/openjdk-riscv/jdk11u/pull/476
4)Fix the divL/modL https://github.com/openjdk-riscv/jdk11u/pull/479
5)Fix the storeL and storeimmL0 https://github.com/openjdk-riscv/jdk11u/pull/480
6)Fix loadConD0 https://github.com/openjdk-riscv/jdk11u/pull/482
7)Fix the storeLConditional https://github.com/openjdk-riscv/jdk11u/pull/485
8)Fix the compareAndSwapL https://github.com/openjdk-riscv/jdk11u/pull/487
9)Fix the compareAndSwapLAcq() https://github.com/openjdk-riscv/jdk11u/pull/488
10)Fix the compareAndExchangeL https://github.com/openjdk-riscv/jdk11u/pull/489
11)Fix the compareAndExchangeLAcq https://github.com/openjdk-riscv/jdk11u/pull/490
12)Fix the weakCompareAndSwapL https://github.com/openjdk-riscv/jdk11u/pull/492
13)Fix the weakCompareAndSwapLAcq https://github.com/openjdk-riscv/jdk11u/pull/493
14)Fix the get_and_setI/F https://github.com/openjdk-riscv/jdk11u/pull/494
15)Fix the get_and_setIAcq/setLAcq https://github.com/openjdk-riscv/jdk11u/pull/495
2、Rewrite the div system https://github.com/openjdk-riscv/jdk11u/pull/478
3、Improve the code style of loadUS2L https://github.com/openjdk-riscv/jdk11u/pull/486
4、Improve the xchg system https://github.com/openjdk-riscv/jdk11u/pull/496
5、Improve the atomic_add system https://github.com/openjdk-riscv/jdk11u/pull/497

OpenJDK for RISC-V 更新（RV64及upstream）张定立

Merged jdk-mainline PRs:

- https://github.com/openjdk/jdk/pull/10057 | (8293011: riscv: Duplicated stubs to interpreter for static calls)
- Three WIP PRs pending.

Technical article:

- https://zhuanlan.zhihu.com/p/552839183 | 启用OpenJDK20的RVV特性

OpenJDK for RISC-V 更新（RV64及upstream）曹贵

代码提交：

- [Reuse runtime call trampolines] (https://github.com/DingliZhang/jdk/commit/8635e01206ffa60e3054569444e0411e8c3e4b88)

项目调研：

- 主要在调研和调试OpenJDK Vector API（aarch64）实现，计划下周一左右 产出调研报告，规划riscv OpenJDK Vector API 的实现。

OpenJDK8 backporting（章翔）

- 构建OpenJDK8的rv64支持：

1. https://github.com/zhangxiang-plct/jdk8u/pull/1
2. https://github.com/zhangxiang-plct/jdk8u/pull/4
3. https://github.com/zhangxiang-plct/jdk8u/pull/5
4. 构建过程：https://github.com/zhangxiang-plct/jdk8u/issues/2

- make过程

1. https://github.com/zhangxiang-plct/jdk8u/pull/13
2. https://github.com/zhangxiang-plct/jdk8u/pull/14
3. https://github.com/zhangxiang-plct/jdk8u/pull/15
4. https://github.com/zhangxiang-plct/jdk8u/pull/17
5. https://github.com/zhangxiang-plct/jdk8u/pull/19
6. https://github.com/zhangxiang-plct/jdk8u/pull/20
7. https://github.com/zhangxiang-plct/jdk8u/pull/22
8. https://github.com/zhangxiang-plct/jdk8u/pull/23
9. https://github.com/zhangxiang-plct/jdk8u/pull/24
10. https://github.com/zhangxiang-plct/jdk8u/pull/26
11. https://github.com/zhangxiang-plct/jdk8u/pull/27
12. https://github.com/zhangxiang-plct/jdk8u/pull/29
13. https://github.com/zhangxiang-plct/jdk8u/pull/30

openEuler RISC-V

- 移植进度：
  - 核心包：4130 / 4240 97.10%
  - 扩展包：2355 / 4269 55.17%
  - 三方包：未开始
- oerv OBS 构建：
  - openEuler:22.03 4119(+6)/4240
  - 22.09工程修包：4096(+63)/4239(+4)　　failed：79 (-53)
  - Factory:RISC-V:KDE　: 173(+71)/176
- PR：
  - 中间仓：+18　详见：https://github.com/isrc-cas/tarsier-oerv/blob/main/biweekly/2022-08-25.md
- Porting
  - 测试：VLC、Thunderbird 、chromium、eclipse
  - 本地成功，整理提交中：KDE、DDE、LibreOffice
  - WIP：tensorflow
- 工具
  - Tarsier-OBS构建状态跟踪及展示：https://github.com/ArCyanic/Internship/blob/main/monthly/2022-8.md
  - 按照giteeid查询PR：https://github.com/iamtwz/tarsier-oerv/tree/pr-track-tools/scripts/GiteePRTracker
- 测试
  - GIMP测试说明：https://github.com/YunxiangLuo/testing/blob/main/GIMP/GIMP_userguide.md
  - VLC测试说明：https://github.com/YunxiangLuo/testing/blob/main/GIMP/README.md
  - 自动化工具开发实现了基于多qemu的多线程测试：https://github.com/brsf11/mugen-riscv

Gentoo for RISC-V 的情况更新（Gentoo小队）

- A total of 58 keywording commits: https://whale.plctlab.org/riscv/RISC-V-双周会/20220901/commits.txt
  - dev-util/crash: add riscv support
    - patch: gentoo/gentoo@70b109c , keyword: gentoo/gentoo@565e20c
- media-rv/kodi: keyword and atomic issue fixed
  - fix commit: gentoo/gentoo@7342318 , keyword: gentoo/gentoo@65ad3fb
  - Upstream pull request: xbmc/xbmc#21743
- deepin-overlay
  - other deepin apps riscv keywording: deepin-community/deepin-overlay#24
- riscv overlay
  - dev-qt/qtwebengine updated
    - patch and keyword: gentoo/riscv/@ee1fce2
  - sys-apps/kexec-tools, fix memory location issue
    - patch: gentoo/riscv@9bd3aae
  - www-firefox/firefox updated
    - patch and update: gentoo/riscv@5183cfd (pr: gentoo/riscv#8)

Arch Linux RISC-V（东东）

1. 移植进度

   [extra] 2670 / 3032 (88.06%)

   [community] 8185 / 9415 (86.93%)
2. Archriscv-packages merged 31 PR.
3. Updpkg: firefox 104.0
4. Updpkg: chromium 103.0
5. Addpkg: mkinitcpio
6. Blog: RV64 板子更换 rootfs 指南

Fedora for RISC-V（傅炜）

- SRPM打包编译进度
  - [fc36] 144000 / 22832 (70%) [https://openkoji.iscas.ac.cn/repos/fc36dev/]
  - [rawhide]【On Going】重点工作
- 以 server 和 desktop 的功能包为目标:
  - Libreoffice has been built, need testing
  - firefox [104, patches fixing]
  - Chromium [103, patch fixing, 102 patch is fixed by 文宇]
- 软件版本:
  - Toolchain gcc-12.1.1-3 / Glibc 2.36.9000-2 (up-to-date)
  - Binutils 2.39-1(up-to-date)
  - Rust 1.63.0-1 [need qemu fix from Felix](up-to-date)
  - OpenJDK17 with JIT (DONE，the patch is fixed by 文宇), OpenJDK18 (up-to-date)
  - LLVM/Clang 14.0.0-1→ 14.0.5-3[rawhide](updating)
  - Python 3.10.4 → 3.11[rawhide] (updating)
  - Perl 5.34.2→ 5.36.0-490[rawhide](updating)
  - Go 1.18-1→ 1.19-1[rawhide](updating)
- Images:
  - QEMU/D1/Icicle/Unmatched/JH7110 Images
  - New koji builder Image (rawhide 更新中)
  - Workstation (GNOME&KDE) Image: will be tested on JH7110

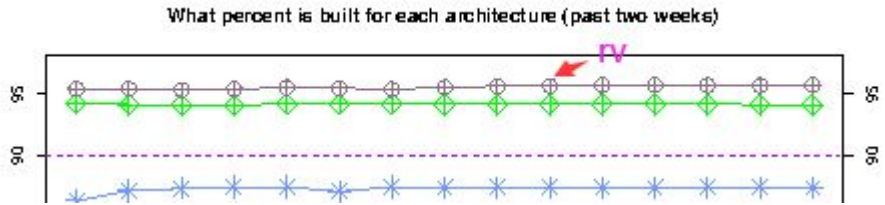
Debian for RISC-V I（于波）

- debci on riscv64

2022-08-31 17:59:39 UTC	booth	unstable	riscv64	pass	22m 35s	migration-reference/0

- buildd on riscv64

  Installed: 15200+



- Fix issues：

Debian for RISC-V II

1. https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1017374 [neochat close]
2. https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1017684 [tiledb-r patch]
3. https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1017771 [gridengine patch]
4. https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1017965 [telegram-desktop patch]
5. https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1018292 [ncrystal patch]
6. https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1018799 [wishlist workround]
7. https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1015885 [lz4-java patch]
8. https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1011628 [rust-fasteval patch]
9. https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1018157 [wsclean patch]
10. https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=952159 [rust-nodrop-union patch]
11. https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1017863 [numactl patch]
12. https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1015715 [libtree patch]
13. https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1018688 [pygame patch]
14. https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1018860 [pygame patch]

Debian for RISC-V II

FW相关更新（王翔）

- opensbi
  - 使用官方AIA M-Mode扩展名Smaia
  - 移除CSR sideleg sedeleg，这两个CSR已经从标准中移除了
  - opensbi pmu改进，优化内存使用（删除了fw_event中的event id），添加结构sbi_pmu_device用于非标准pmu的接口，把firmware counter修改为固定的64比特
  - 修正Unmatched关于pmu的文档
- u-boot
  - 修正获取PCIE设备映射地址时，计算BAR偏移量的错误
- openocd
  - 提交了关于trigger用作watchpoint时size的设置，讨论中

RISCV性能跟踪小队 - 陈小欧、陈逸轩

- **Run benchmark (sunspider, octane)on unmatched to test spidermonkey**
- **Working on porting kraken to test spidermonkey**

```
[xyenchi@milk sunspider-0.9.1]$ js91 sunspider-standalone-driver.js
3d-cube: 718
3d-morph: 1151
3d-raytrace: 848
access-binary-trees: 681
access-fannkuch: 1626
access-nbody: 916
access-nsieve: 569
bitops-3bit-bits-in-byte: 509
bitops-bits-in-byte: 838
bitops-bitwise-and: 2720
bitops-nsieve-bits: 908
controlflow-recursive: 702
crypto-aes: 642
crypto-md5: 482
crypto-sha1: 494
date-format-tofte: 727
date-format-xparb: 456
math-cordic: 922
math-partial-sums: 1105
math-spectral-norm: 595
regexp-dna: 372
string-base64: 525
string-fasta: 1523
string-tagcloud: 1095
string-unpack-code: 2381
string-validate-input: 4771
```

```
[xyenchi@milk octane]$ js91 run.js
Richards: 12.3
DeltaBlue: 13.5
Crypto: 24.2
RayTrace: 41.4
EarleyBoyer: 63.0
RegExp: 19.3
Splay: 75.2
SplayLatency: 459
NavierStokes: 59.5
PdfJS: 178
Mandreel: 17.2
MandreelLatency: 99.4
Gameboy: 132
CodeLoad: 2236
Box2D: 86.5
zlib: 66.8
Typescript: 310
----
Score (version 9): 74.5
```

香山开源RISC-V处理器 - ICT / PCL

- 南湖时序迭代优化接近尾声
  - 前端和访存模块在做最后的 Fanout 与逻辑优化
  - 尝试裁剪 L1I/L1D 容量，评估 PR 和对性能造成的影响

- 昆明湖架构进展
  - 前端：将缓存路预测实现进香山中，评估性能收益
  - 后端：推进 V 扩展开发的基础设施（模拟器、译码单元等）
  - 访存/缓存：实现更激进的 SMS 预取器并做性能评估；着手搭建新版缓存框架

MLIR RISC-V Vector (RVV) Dialect Proposal - 张洪滨

注:提交人不在线

相关链接

- RFC Patch - https://reviews.llvm.org/D108536
- RFC Post - https://discourse.llvm.org/t/rfc-add-risc-v-vector-extension-rvv-dialect/4146/32
- MLIR + RVV 集成测试环境搭建文档 - https://gist.github.com/zhanghb97/ad44407e169de298911b8a4235e68497
- MLIR + RVV 环境搭建 - https://github.com/buddy-compiler/buddy-mlir/blob/main/thirdparty/build-rvv-env.sh
- MLIR + RVV 相关实验 - https://github.com/buddy-compiler/buddy-mlir/tree/main/examples/RVVExperiment

WIP

- Google IREE 伙伴提出向 Vector Dialect 中添加 Mask Region 的 RFC（未来合作添加 VL）
  - https://discourse.llvm.org/t/rfc-vector-masking-representation-in-mlir/64964
- 正在测试 VP Intrinsic 完备性（Scalable Vector + RVV 后端）

面向 RISC-V 的 OpenCV 情况更新 - 韩柳彤

- **为 Universal Intrinsic 增加可变长向量指令的支持**

  Google Summer of Code 2022: Optimizing OpenCV Universal Intrinsic for RISC-V Vector

  新的Patch：

  PR#22353 Add more universal intrinsic implementations for RVV.

  PR#22429 Add remaining universal intrinsic implementations for RVV.

  已经被合并，增加了剩余所有 Intrinsic 的实现，并添加了对应的测试用例。

  新的 Universal Intrinsic RVV 后端已经完成，其不仅支持了可变长的寄存器宽度，还解决了原始版本中生成冗余 Load/Store 指令的问题，预计可以获得较大的性能提升。

  接下来将尝试优化 OpenCV 图像处理模块中的部分热点函数，并寻找可用的 RISC-V Vector 硬件设备进行性能测试。

Chisel and Additional Technology / Sequencer

- 申奥: https://github.com/OceanS2000/rocket-chip-fpga-shells/commit/63003a86b8b5997daa649d16d7c9116842bf7ac1
  - 对 Alinx KU040 FPGA 的支持
- 李秦君:https://github.com/qinjun-li/v/pull/1
  - 完成了RVV的Lane设计
- 叶泽文, 郑鉞壬:https://github.com/OpenRigil/rvsc22
  - RV Crypto的FPGA展示
- 杨砚祺:https://github.com/chipsalliance/rocket-chip-blocks/pull/4
  - 添加对UART的文档
- 罗云千:https://github.com/qinjun-li/v/pull/1
  - RVV Lane C++ 通信模型设计
- 匿名实习生0&1:
  - Serdes 控制逻辑
- 匿名实习生2:
  - Serdes Phy
- 苑浩然,张露承,廖杰,程光辉,陈春昀摸了

提交人在另一个会

自由讨论 / AOB

- 各位工作生活都还顺利？
- 成都的朋友们你们冰箱塞满了么？
- 深圳的朋友呢？
- 广州的朋友？
- 还有谁？