欢迎第一次加入的伙伴(开会时请从下一页开始展示)

- 开放编辑，直接点击 request for edit 然后在东亚时区群里at吴伟
- 如果没有找到自己的内容分类，可以添加1-2页在最开始或中间
- 欢迎在开始的前5分钟进行自我介绍
- 日常八卦在东亚时区RISC-V双周同步微信群中，欢迎加入

东亚时区RISC-V双周会

2022年12月22日·第050次

https://github.com/cnrv/RISCV-East-Asia-Biweekly-Sync

Host: 邢明杰

Organizer: PLCT Lab plct-oss@iscas.ac.cn

会议议程（15:00 - 16:00）

- 自我介绍、等待参会者接入、非技术话题八卦（没有的话就直接跳过）
- RVI 的更新和八卦（基本上跟东亚双周会群内消息同步）
- Unratified Specs 的参考实现进展
- 东亚地区小伙伴的项目更新
- 自由讨论

RISC-V International 同步、全球开源社区八卦

- RISC-V Summit 2022召开
- 腾讯加入RISC-V 基金会
- 欧盟将提供 2.7 亿欧元资金，试图通过构建基于开放 RISC-V 指令集架构的芯片来实现技术独立

RISC-V 韩语社区的同步与八卦

- KINTEX: 2022大韩民国科学技术大展(12.02 ~ 12.25)
  - 韩国电子通信研究院(ETRI)：微型LED同时转录、接合（전사・접합）的技术。费用减少到1/10，生产效率提高10倍。
  - 我人不在韩国所以没参加

RISC-V 日语社区的同步与八卦

- 熊本
  - Sony新建传感器厂
    - 旁边是台积电熊本厂
    - 索尼没有先进制程
    - 友商也在这Tokyo Electron Limited (東京威力科创)：设计Logic IC的
  - 索尼新廠將生產智慧手機用的影像传感器，鑑於手機需求放緩，索尼未來也將為自駕車以及自動化工廠生產传感器。
  - 2021年索尼的CMOS影像传感器全球市占率44%，18%三星
- 美国IC Insights预测，2026年全球CMOS图像传感器市场将比2021年增长30%，达到269亿美元
- 来源：日经

RISC-V 俄语社区的同步与八卦

- 暂时没有新闻

AOSP for RISC-V - 汪辰、陆旭凡

- 跳过一次

RISC-V GCC进展

目前仍在讨论profile在-march选项中的规范，我们会及时跟进工具链中的实现：

https://github.com/riscv-non-isa/riscv-toolchain-conventions/pull/26

Intrinsic的讨论已经基本结束，采用“__riscv_指令名”的形式，RVV intrinsic也会保持一致：

https://github.com/riscv-non-isa/riscv-c-api-doc/pull/31

RVV vsetvl pass已经合并至上游：

https://gcc.gnu.org/git/?p=gcc.git;a=commit;h=9243c3d1b63b9092a82178392145f9e9d62423d9

https://gcc.gnu.org/bugzilla/show_bug.cgi?id=108185#c1

弈斯伟计算向上游提交了多个优化的patch：

https://gcc.gnu.org/pipermail/gcc-patches/2022-December/607626.html

https://sourceware.org/git/?p=binutils-gdb.git;a=commit;h=207cc92d92c863298c530498e2dbf71a2b5fd8ae

Clang/LLVM 进展 (PLCT)

- **[LLDB][RISCV] Add RVD instruction support for EmulateInstructionRISCV: https://reviews.llvm.org/D140032**
- **[NFC][LLDB] Using namespace llvm in EmulateInstructionRISCV https://reviews.llvm.org/D140092**
-

Clang / LLVM 社区的更新（廖春玉、陆旭凡）

1. D140421 [RISCV] Add more XVentanaCondOps patterns.
2. D140438 [IR/MachineOutliner] Add a "nooutline" function attr and respect it
3. D140089 [MemCpyOpt] Add a stack-move optimization to opportunistically merge allocas together.
4. D140460 [RISCV][MC] Add support for experimental zfa extension

QEMU/Spike/Sail/ACT进展 (PLCT)

- Spike
  - 改善了rv32u兼容模式的实现
    - https://github.com/riscv-software-src/riscv-isa-sim/pull/1167
  - 修复Zc* 和misa.C读写之间的关系
    - https://github.com/riscv-software-src/riscv-isa-sim/pull/1176

gem5 进展 (PLCT)

-

V8 for RISC-V 更新（邱吉、陆亚涵）

- Port 上游改动

  4119766: [riscv][centry] Remove the unused SaveFPRegsMode parameter | https://chromium-review.googlesource.com/c/v8/v8/+/4119766

- 适应archopcode输入参数顺序的修改

  4114558: [riscv] Fix qfma test fail | https://chromium-review.googlesource.com/c/v8/v8/+/4114558

Spidermonkey for RISC-V更新（邱吉、陆亚涵）

根据review意见进行了修改后，遇上圣诞节放假，暂时review不了了
https://phabricator.services.mozilla.com/D161986

OpenJDK for RISC-V 更新(RV64及upstream) 杨飞

1. Authored jdk-mainline PRs:
- https://github.com/openjdk/jdk/pull/11631 (8298568: Fastdebug build fails after JDK-8296389)
- https://github.com/openjdk/jdk/pull/11505 (8298088: RISC-V: Make Address a discriminated union internally)

2. Reviewed jdk-mainline PRs:
- https://github.com/openjdk/jdk/pull/11502 (8298075: RISC-V: Implement post-call NOPs)
- https://github.com/openjdk/jdk/pull/11577 (8298345: Fix another two C2 IR matching tests for RISC-V)
- https://github.com/openjdk/jdk/pull/11432 (8297851: Add devkit for RISC-V)
- https://github.com/openjdk/jdk/pull/11750 (8299168: RISC-V: Fix MachNode size mismatch for MacroAssembler::_verify_oops*)
- https://github.com/openjdk/jdk/pull/11751 (8299172: RISC-V: [TESTBUG] Fix stack alignment logic in jvmci RISCV64TestAssembler.java)
- https://github.com/openjdk/jdk/pull/11749 (8299162: Refactor shared trampoline emission logic)

3. Foreign-API RISCV Port:
- WIP PR rebased on latest jdk-master: https://github.com/openjdk/jdk/pull/11004 (8293841: RISC-V: Implementation of Foreign Function & Memory API (Preview))
- Passed all jtreg foreign tests with fastdebug build on HiFive Unmatched
- Internal code review in progress, will be ready for public code review at the end of Dec.

4. Generational-ZGC RISCV Port:
- Basic support contributed by Huawei: https://github.com/openjdk/zgc/pull/10
- Pending on gen-ZGC branch rebasing: https://github.com/openjdk/zgc/tree/zgc_generational
- WIP: Add support for RVV extension

OpenJDK for RISC-V 更新（RV32/PLCT 史宁宁）

1、Fix the RFLAGS in riscv32.ad

https://github.com/openjdk-riscv/jdk11u/pull/577

2、Fix the RegisterImpl::number_of_registers in riscv32.ad

https://github.com/openjdk-riscv/jdk11u/pull/578

3、Fix the i2c and c2i adapter according arm 32bit

https://github.com/openjdk-riscv/jdk11u/pull/579

4、risv32.ad中的lfmv_w_x/fmv_x_w 64位数据处理

https://github.com/openjdk-riscv/jdk11u/issues/580

5、gen_i2c_adapter()中，long数据高低位对后续影响问题

https://github.com/openjdk-riscv/jdk11u/issues/581

OpenJDK for RISC-V 更新（RV64及upstream）张定立

Vector-API support:

- RISC-V: Add rvv_compare function
- RISC-V: Add vfmerge_vfm and fix vmerge
- RISC-V: Add CMoveVF and CMoveVD
- RISC-V: expand reduce_add patterns into separate instructions

OpenJDK for RISC-V 更新（RV64及upstream）曹贵

Vector-API support:（提交人发烧咳嗽，不在线）

- Support C2 AbsVB/AbsVS/AbsVI/AbsVF/AbsVD mask node

- Support C2 AddVB/AddVS/AddVL mask node

OpenJDK8 backporting（章翔）

Javac调试（提交人offline）

1. Fix index_check and delete condy_helper
2. Fix CAN_SHOW_REGISTERS_ON_ASSERT by JDK-8004124
3. Fix MethodHandles::verify_klass by KlassHandle replace with Klass
4. https://github.com/zhangxiang-plct/jdk8u/pull/238
5. Fix based on pr 235
6. Fix generate_generic_copy
7. Fix templateInterpreterGenerator_riscv64.cpp
8. Fix stubGenerator_riscv64.cpp
9. Fix vtableStubs_riscv64.cpp
10. Fix some makefiles to support rv64
11. Fix #pr243 by deleting pd_code_size_limit
12. Fix .java to support riscv64
13. Fix HSDB.java to support riscv64
14. Fix LinuxDebuggerLocal.c & libproc.h
15. Fix NativeMovConstReg::set_data

openEuler RISC-V

- PR：新增2个，merged 11个

  https://gitee.com/phoebe-xi/RISC-V/blob/master/archive/weeklyreports/2022-12-15.md

- build
  - Electron（共23；succeeded: 22；failed：1）
  - qt6及相关软件包（共51；succeeded: 36；unresolvable：3；failed：11）
  - KDE：（共281；succeeded: 270；）
  - HPC：（共14：succeeded：11）
- other
  - 矽速科技LicheeRV开发板 openEuler镜像

Gentoo for RISC-V 的情况更新（Gentoo 小队）

- Support statistics (8026/19537, 41.08%)：https://whale.plctlab.org/riscv/support-statistics/
- A total of 10 keywording commits: https://whale.plctlab.org/riscv/RISC-V-双周会/20221222/commits.txt
- dev-util/crash-8.0.2: add riscv64 support
  - https://github.com/gentoo/gentoo/commit/79b1ca7a87db37bd57412bb82a192afe4264d7fc
- New stage3 image for Lichee RV Dock:
  - https://github.com/peeweep/Gentoo-Lichee-RV-Dock

Arch Linux RISC-V（东东、潘瑞哲）

```
[ Arch Linux RISC-V Bi-Week Package
Update Stats Report ]
Report generated on: 20221222
Package update count: 2451
Distinct package update count: 1547
[core] 253 / 261 (96.93%)
[extra] 2859 / 3079 (92.85%)
[community] 8790 / 9829 (89.42%)
```

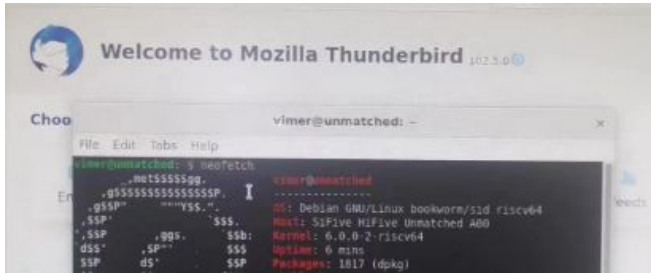
```
Highlight packages:
    firefox - 107.0-1 --> 108.0.1-1
    rust-analyzer - 20221205-1 --> 20221212-1
    nodejs - 19.2.0-1 --> 19.3.0-1
    docker-compose - 2.13.0-1 --> 2.14.1-1
    harfbuzz - 5.3.1-3 --> 6.0.0-1
    qt5-wayland - 5.15.7+kde+r55-1 --> 5.15.7+kde+r56-1
    kwayland - 5.100.0-1 --> 5.101.0-1
    imagemagick - 7.1.0.53-1 --> 7.1.0.54-1
    telegram-desktop - 4.4.0-1 --> 4.4.1-3
    redis - 7.0.5-3 --> 7.0.7-1
    git - 2.38.1-2 --> 2.39.0-1
```

Fedora for RISC-V（傅炜）

-

Debian for RISC-V（于波）

- Buildd status&news
  1. Installed: 15440+ (rebuilt some packages)
  2. Udd FTBFS packages ~299
  3. Official porting news (no reply)
- Debci update
- Some works
  1. https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1025831 [vpb-driver NMU RC done]
  2. https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1025827 [slic3r-prusa reportbug]
  3. https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1026065 [nodejs ftbfs patch]
  4*. https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1026118 [thundbird patch]



Deepin for RISCV

Deepin-riscv-stage2:

succeeded: 5291 failed: 174 unresolvable: 1087

继续解决重构工具链带来的问题

同步deepin主线软件包

deepin-riscv-board：fix star64构建

FW相关更新（王翔）

- opensbi
  - bash在freebsd下目录为/usr/local/bin/bash,修正脚本通过env来调用bash
  - T-Head c9xx添加clint支持，通过添加quirk来指定c9xx mtime特性
  - opensbi添加Zisslpcfi支持
  - 更新冷启动核的选择方法，从预处理修改为fdt
  - 把pmp的权限分为M模式和SU模式（加锁的PMP会对M模式有效，但也会让低特权等级可以访问）

固件相关更新(洛佳)

香山开源RISC-V处理器 - ICT / PCL

- 南湖架构 100% RTL 交付后端进行物理设计流程
  - 在 FPGA 上跑通了各类外设和预期的 workload
-
- 昆明湖进展
  - 前端：FDIP 基本调试完成；开始 Loop Buffer 和 Loop Predictor 的整合调试
  - 后端：推进向量浮点、寄存器、派遣等部分的代码设计；持续添加功能单元
  - 访存：VLSU设计方案基本敲定；LQ 的分解工作开始
  - 缓存：CoupledL2开始进入子系统级联调；调研 CHI 总线

MLIR RISC-V Vector (RVV) Dialect Proposal - 张洪滨

提交人不在线 - hongbin2019@iscas.ac.cn

相关链接

- RFC Patch - https://reviews.llvm.org/D108536
- RFC Post - https://discourse.llvm.org/t/rfc-add-risc-v-vector-extension-rvv-dialect/4146/32
- MLIR + RVV 集成测试环境搭建文档 - https://gist.github.com/zhanghb97/ad44407e169de298911b8a4235e68497
- MLIR + RVV 环境搭建 - https://github.com/buddy-compiler/buddy-mlir/blob/main/thirdparty/build-rvv-env.sh
- MLIR + RVV 相关实验 - https://github.com/buddy-compiler/buddy-mlir/tree/main/examples/RVVExperiment

Update

- [RISCV][VP] Support vp.reduce.mul by ExpandVectorPredication - https://reviews.llvm.org/D139721

Chisel and Additional Technology / Sequencer

- 全军覆没

OpenHW & OpenHW Aisa Working Group

- 暂无新消息

自由讨论 / AOB

-

BACKUP

准备加入更多的国际开源组织进行同步观测

欢迎追加或提议

CHIPS Alliance

风平浪静