欢迎第一次加入的伙伴(开会时请从下一页开始展示)

- 开放编辑，直接点击 request for edit 然后在东亚时区群里at吴伟
- 如果没有找到自己的内容分类，可以添加1-2页在最开始或中间
- 欢迎在开始的前5分钟进行自我介绍
- 日常八卦在东亚时区RISC-V双周同步微信群中，欢迎加入

东亚时区RISC-V双周会

2023年08月17日·第062次

https://github.com/cnrv/RISCV-East-Asia-Biweekly-Sync

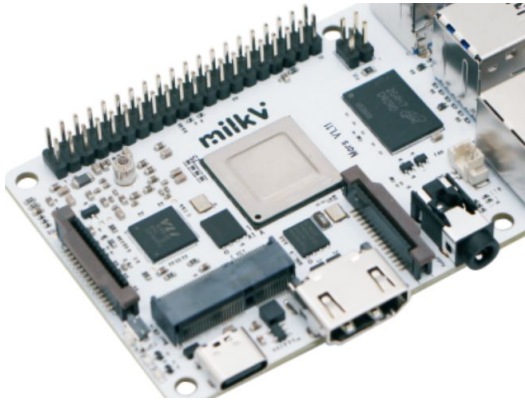
Host: 李威威

Organizer: PLCT Lab plct-oss@iscas.ac.cn

会议议程（15:00 - 16:00）

- 自我介绍、等待参会者接入、非技术话题八卦（没有的话就直接跳过）
- RVI 的更新和八卦（基本上跟东亚双周会群内消息同步）
- Unratified Specs 的参考实现进展
- 东亚地区小伙伴的项目更新
- 自由讨论

RISC-V International 同步、全球开源社区八卦



1. RISC-V 中国峰会日程；8月21日-27日北京
2. 高通参与成立RISC-V芯片公司
3. 首批RISC-V笔记本电脑ROMA已成功交付
4. 平头哥宣布举办玄铁RISC-V应用创新大赛
5. 全球首款信用卡大小的RISC-V单板计算机Mars正式发售
6. RISC-V Expanding In China
7. 赛昉科技重磅发布全新RISC-V处理器内核及多核子系统IP平台

SiFive Open Source Software (Hong-Rong Hsu 許宏榮)

- Android oriented RVV libraries.
  - Upstreamed
    - Libc/Bionic/Glibc/
    - Libyuv
    - Zlib-ng
  - On-going
    - OpenSSL (based on VRULL's patch)
    - zstd
    - ffmpeg
- OpenXLA/IREE
  - Cross build for RISC-V and RVV code-gen
  - e2e Performance dashboard. Run on X280 FPGA

RISC-V 韩语社区的同步与八卦

- 三星联合现代集团投资Tenstorrent一亿美元
  - NPU、车载半导体、Fabless
  - Tenstorrent正在联合LG开发基于RISC-V的用于智能电视的产品
- 三星急于摆脱4纳米制程的良率质疑
  - 7月，”明年年末三星美国泰勒工厂将开始4纳米量产产品的出货，主要服务于美国客户“
  - Groq选择Samsung Foundry
- 三星研究所新一代家电研究组旗下新设了"智能家庭AI实验室"，开发基于AI的智慧家电业务

RISC-V 日语社区的同步与八卦

日语社区本周暂无更新

RISC-V 俄语社区的同步与八卦

UDV集团推出俄罗斯首款基于RISC-V架构的防火墙

RISC-V GCC进展

- Ztso的GCC patch已合入上游： Ztso atomic mapping
- 正在讨论R_RISCV_RELAX在rvc与非rvc下的链接器松弛处理：

  Compressed and Non-compressed Relaxations in the Same Object

- SIG toolchain讨论了RISC-V Profiles中各种新扩展（ziccif, zihintpause等）对工具链的行为影响，近期会产生一份新的关于-march说明的文档
- 更新了密码学标量(Zk*)扩展的intrinsic API规范，添加了Bitmanip使用intrinsic的说明：

  RISC-V B,K扩展 Intrinsic API规范提案

- Zihintntpause的RFC patch正在Review中：RISC-V: Make __builtin_riscv_pause 'Zihintpause' only
- Zc扩展的草案更新至1.0.4-1合并了之前提出的f/d依赖：Add F/D to Zcf/d's depending relations
- Zca/b/f/d的gcc支持已合入上游：RISC-V: Support Zc* extensions
- RVV自动向量化支持持续进行中：RVV auto-vectorazition recently commits
- RVV intrinsic手册发布了新版本

  ：https://github.com/riscv-non-isa/rvv-intrinsic-doc/releases/tag/draft-20230811-a810011071e9e2f630450f01f5fdc9a9ccc3e3be
- RISC-V GNU Toolchain双周会slides链接：

  https://docs.google.com/presentation/d/1F-EhbGGapwUY2JkcxUP7FaBgFVOsBVslwC5SnYVL_1A/edit

Clang/LLVM 进展 (PLCT)

- RVV0.7.1完成大概90%的汇编器支持
  - [RVV 0.7.1] MC support https://github.com/ruyisdk/llvm-project/pull/4
  - [RVV 0.7.1] reject when both v and xtheadv are specified https://github.com/ruyisdk/llvm-project/pull/5
  - [RVV 0.7.1] port assembler tests from binutils https://github.com/ruyisdk/llvm-project/pull/6

- Upstream提交的patch
  - [RISCV] Fix rlist grammar for cm.push, cm.popret, cm.popretz and cm.pop in RISCV zcmp Extension https://reviews.llvm.org/D157847

QEMU/Spike/Sail/ACT进展 (PLCT)

- QEMU
  - 改进 TCG 后端 vector 支持
    - https://github.com/plctlab/plct-qemu/tree/plct-riscv-backend-rvv
  - 更新svadu支持
    - https://lists.gnu.org/archive/html/qemu-riscv/2023-08/msg00291.html
  - milkv duo支持
    - https://github.com/plctlab/plct-qemu/tree/duo-qemu

V8 for RISC-V 更新（邱吉、陆亚涵、荆培杨）

Upstream Port

1. 4779385: [riscv][wasm] Fix memory.fill and memory.init with i64.const args | https://chromium-review.googlesource.com/c/v8/v8/+/4779385
2. 4776621: [riscv][compiler] Generalize InstructionSelectorT for Turboshaft (part 12) | https://chromium-review.googlesource.com/c/v8/v8/+/4776621
3. 4750761: [riscv][sandbox] Reference Code objects (and their entrypoint) through the CPT | https://chromium-review.googlesource.com/c/v8/v8/+/4750761

Clean code:

1. 4778439: [riscv] Reduce the number of vector arch codes (Part 4) | https://chromium-review.googlesource.com/c/v8/v8/+/4778439
2. 4772525: [riscv]Reduce number of vector arch code(Part 3). | https://chromium-review.googlesource.com/c/v8/v8/+/4772525
3. 4768905: [riscv] Reduce the number of vector arch code(Part 2) | https://chromium-review.googlesource.com/c/v8/v8/+/4768905
4. 4763850: [riscv] Reduce the number of vector arch code(Part 1) | https://chromium-review.googlesource.com/c/v8/v8/+/4763850

Bug fix:

1. 4757857: [riscv] Fix incorrect store size | https://chromium-review.googlesource.com/c/v8/v8/+/4757857

Spidermonkey for RISC-V更新（邱吉、陆亚涵）

1. **无**

OpenJDK for RISC-V 更新(RV64及upstream) 杨飞 (offline)

1. Co-authored JDK-mainline PRs:
- More RISC-V update for PR11044: https://github.com/openjdk/jdk/pull/11044#issuecomment-1632158856
- Add RISC-V update for PR14375: https://github.com/openjdk/jdk/pull/14375#issuecomment-1639148430

2. Reviewed JDK-mainline PRs:
- https://github.com/openjdk/jdk/pull/14545 (8308984: Relativize last_sp (and top_frame_sp) in interpreter frames)
- https://github.com/openjdk/jdk/pull/14576 (8308340: C2: Idealize Fma nodes)
- https://github.com/openjdk/jdk/pull/14800 (8311548: AArch64: [ZGC] Many tests fail with "assert(allocates2(pc)) failed: not in CodeBuffer memory" on some CPUs)
- https://github.com/openjdk/jdk/pull/14823 (8311862: RISC-V: small improvements to shift immediate instructions)
- https://github.com/openjdk/jdk/pull/14848 (8311923: TestIRMatching.java fails on RISC-V)
- https://github.com/openjdk/jdk/pull/14888 (8312014: [s390x] TestSigInfoInHsErrFile.java Failure)
- https://github.com/openjdk/jdk/pull/14129 (8301996: Move field resolution information out of the cpCache)
- https://github.com/openjdk/jdk/pull/14991 (8312569: RISC-V: Missing intrinsics for Math.ceil, floor, rint)

3. Reviewed JDK17u upstream PRs:
- https://github.com/openjdk/jdk17u-dev/pull/1565 (8297476: Increase InlineSmallCode default from 1000 to 2500 for RISC-V)
- https://github.com/openjdk/jdk17u-dev/pull/1567 (8309254: Implement fast-path for ASCII-compatible CharsetEncoders on RISC-V)
- https://github.com/openjdk/jdk17u-dev/pull/1613 (8312511: GHA: Bump cross-compile runner to Ubuntu 22.04)
- https://github.com/openjdk/jdk17u-dev/pull/1611 (8311923: TestIRMatching.java fails on RISC-V)

4. riscv-port-jdk11u backport PRs:
- https://github.com/openjdk/riscv-port-jdk11u/pull/1 (8283929: GHA: Add RISC-V build config)

OpenJDK for RISC-V 更新（RV64及upstream）张定立

- 暂无更新

OpenJDK for RISC-V 更新（RV64及upstream）曹贵

Merged & New JDK-mainline PRs:

- https://github.com/openjdk/jdk/pull/14848 | 8311923: TestIRMatching.java fails on RISC-V

Backport jdk21u:

- https://github.com/openjdk/jdk21u/pull/12 | 8311923: TestIRMatching.java fails on RISC-V

openEuler RISC-V（周嘉诚）

- Preparing the next release 23.09, when RISC-V will be officially supported by openEuler
  - Sending RISC-V related changes upstream to distro mainline
  - Expanding test breadth and depth according to distro guidelines
- Approaching milestones of the “LLVM Parallel Universe Project”, preliminary performance test ongoing
- Brief work recap
  - openjdk{8,11,17}: add riscv64 enablement patch (respectively) [distro] [open]
  - openresty: add upstream enablement patch [distro] [open]
  - rust: upgrade to 1.71.0 [distro] [merged]
  - mesa: add OrcJIT and more backend [distro] [merged]
  - qt6: upgrade to 6.5.1 [distro] [merged]
  - Many other packaging changes, and more fixes for the “LLVM Parallel Universe Project”

Gentoo for RISC-V 的情况更新（Gentoo 小队）

- 暂无更新

Arch Linux RISC-V（潘瑞哲）

- Package update count: 3348
- Distinct package update count: 2548
- [core] 257 / 263 (97.72%)
- [extra] 12422 / 13383 (92.82%)

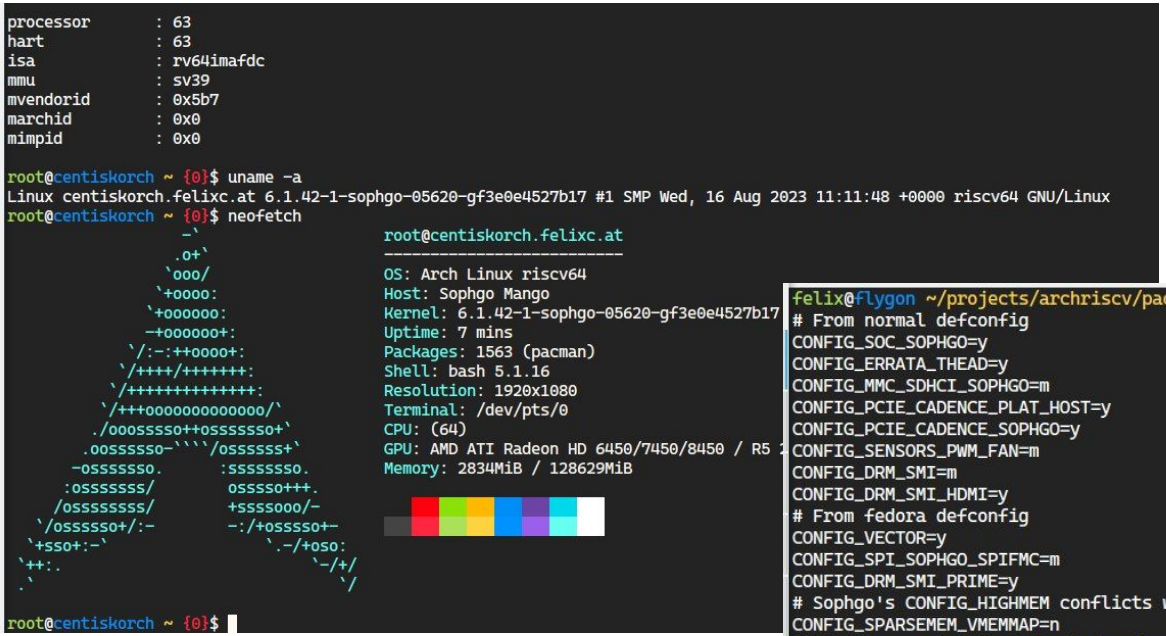
- electron sandbox mode works now:
  - electron22 Fix sandbox patch. Code-OSS can run without the `--no-sandbox` flag after this.
  - electron25 Fix sandbox patch (a7 register should be in clobber list)
  - Revert a problematic upstream workaround that is causing a crash in crash handler. https://bugs.chromium.org/p/chromium/issues/detail?id=1472258
  - Disable RVV in libyuv because the build of libyuv with RVV at this commit is broken on riscv.

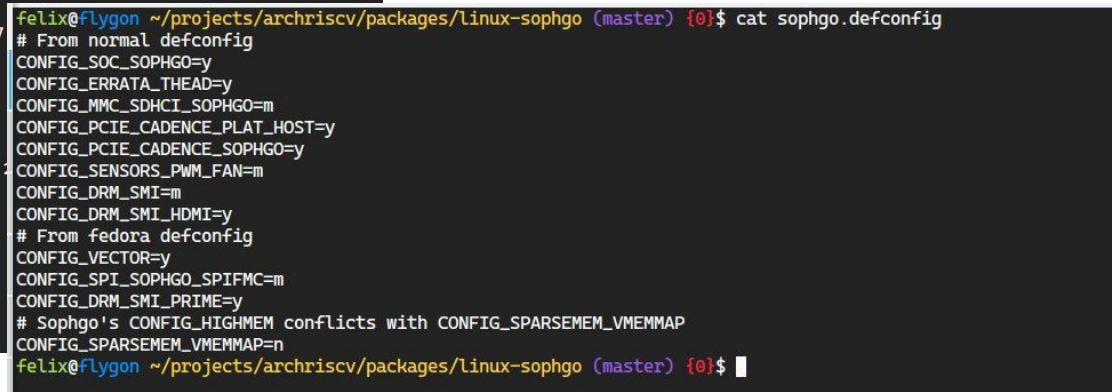
- Highlight packages:
- linux - 6.4.2.arch1-1.1 --> 6.4.10.arch1-1.1
- firefox - 115.0.2-1 --> 116.0-1
- rust - 1:1.70.0-1 --> 1:1.71.1-1
- nodejs - 20.4.0-1 --> 20.5.0-1
- ruby - 3.0.5-1 --> 3.0.6-1
- libreoffice-fresh - 7.5.4-3 --> 7.5.5-1
- electron22 - 22.3.17-1 --> 22.3.18-2
- electron24 - never been built --> 24.6.5-2
- electron25 - never been built --> 25.3.2-2
- code - 1.79.2-1 --> 1.81.1-1
- chromium - 114.0.5735.198-2 --> 115.0.5790.110-1

- linux: `[v5] riscv: entry: set a0 = -ENOSYS only when syscall != -1`. Waiting for approval https://patchwork.kernel.org/project/linux-riscv/list/?series=771708

Arch Linux RISC-V

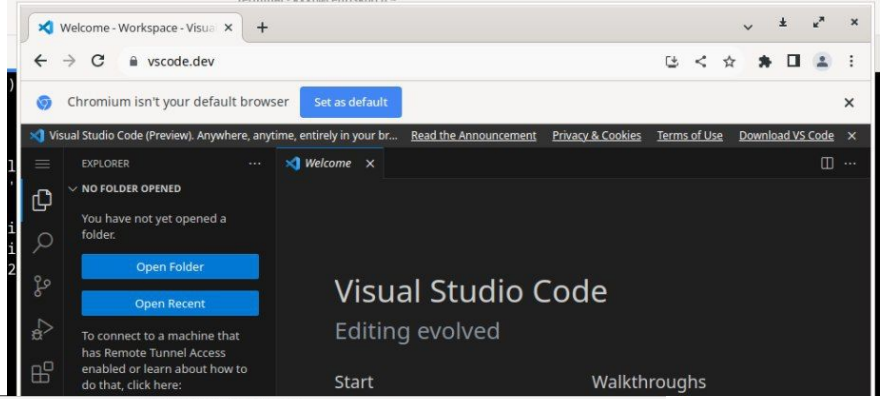
- Arch Linux on Sophgo sg2042 & MilkV Pioneer
- https://github.com/felixonmars/archriscv-packages/pull/2907

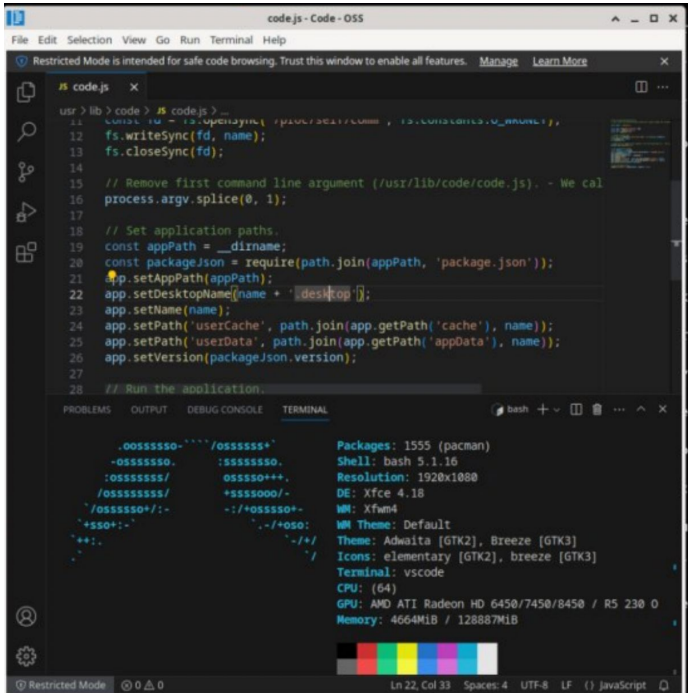


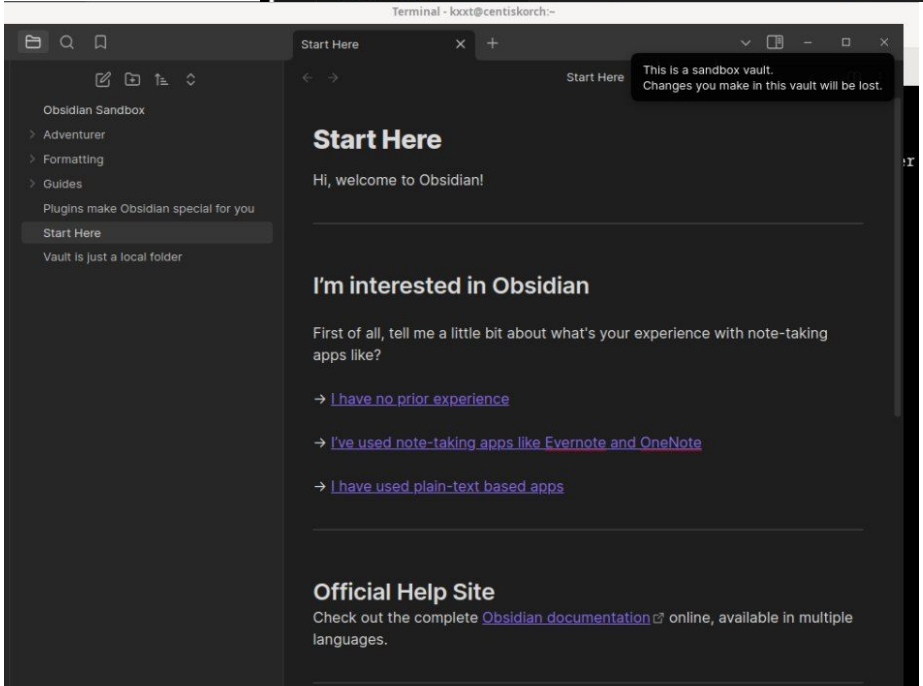


Arch Linux RISC-V

- Code + sandbox; Obsidian
- Chromium (openning https://vscode.dev)





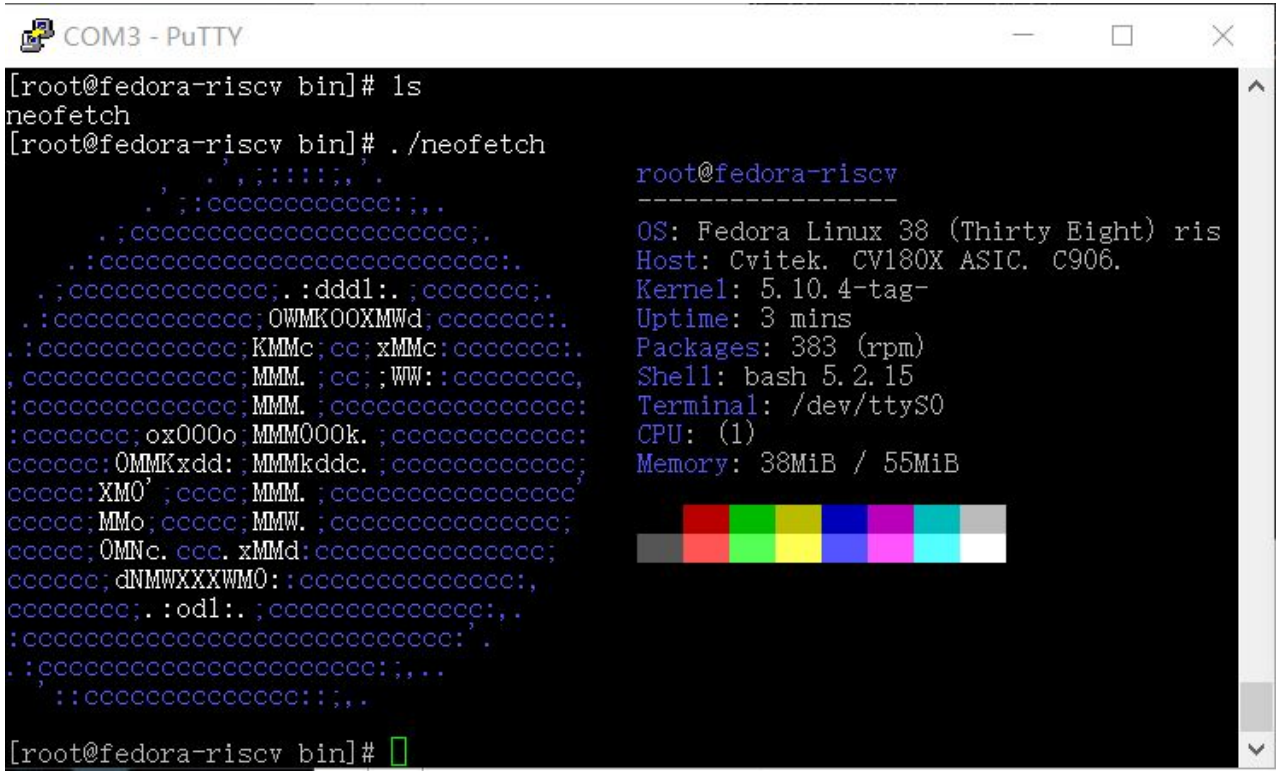


Fedora for RISC-V（傅炜）

- **RPM packaging**
  - Status: **Updating Fedora 38**
    - **22079/22951 [96.20%] srpm have been built.**
  - Spin: Server/Workstation/Cloud
  - WIP Spin: IoT/**CoreOS** [ONGING]
- **main package version:**
  - Toolchain(up-to-date for F38)
    - **gcc-13.2.1 -1[DONE]**
    - glibc-2.37.4[DONE]
    - Binutils 2.39-12[DONE] → 2.40-10 [ONGING]
  - libffi-3.4.4-2(up-to-date)
  - java-latest-openjdk-19.0.2.0.7→20 [ONGING]
  - perl-5.36.1-497(up-to-date)
  - Python 3.11.4-1(up-to-date) → 3.12
  - **LLVM/Clang 16.0.6-2(up-to-date)**
  - **golang-1.20.7-1(up-to-date)**
  - **rust-1.71.1-1(up-to-date)**

- Desktop support:
  - DONE：XFCE/LXDE/LXQT/GNOME/ Budgie/Cinnamon/Mate/Sugar/Sway/KDE
  - Building：Deepin(will try to maintain it)
  - Key Desktop App
    - **firefox-116.0-1[DONE]**
    - **Libreoffice 7.5.5.2-2[DONE]**
    - Thunderbird 102.12.0[DONE]
    - Chromium [ONGOING]
- Image :
  - Sophgo SG2042 EVB/Milk-V[DONE]
    - zsbl→opensbi->edk2→GRUB→Fedora
  - TH1520 BeagleV/LPi4A/***[DONE]
  - StarFive JH7110 boards[ONGOING]
- ROS/ROS2 upgraded to F38
  - ROS2 packaging is ongoing
- function testing:
  - Podman[pass], Image：fedora-rv64
  - Ceph[pass]
  - K8s [pass]will demo in RISC-V summit

Fedora on Duo (Guoguo He)



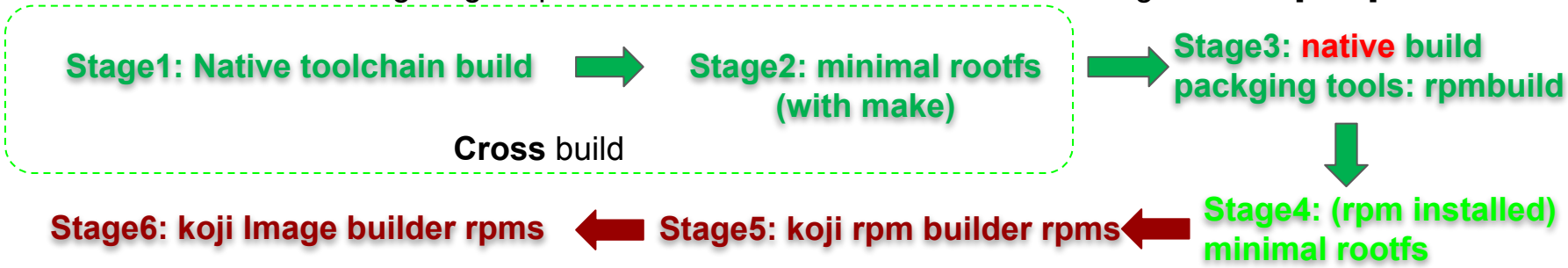
Fedora for RV32（张松松）

- Create a new bootstrap framework, target on multi-arch rpm-based Linux distro bootstrap
  - https://github.com/fedora-riscv/bootstrap
- Download srpm automatically by a given list
  - https://github.com/fedora-riscv/srpm-get
- Automated build script using yaml
  - https://github.com/fedora-riscv/rpm-builder
- All the documents for this bootstrap
  - https://github.com/fedora-riscv/bootstrap-development-log
  - https://github.com/fedora-riscv/rpmbuild-fedora-log

Core group DONE!

DNF works well !!

The current status: building stage4 rpms for the standard Fedora minimal image，84/149[56%]。



Fedora for RV32（张松松）

基于以上成果，正在 bootstrap 64ILP32，

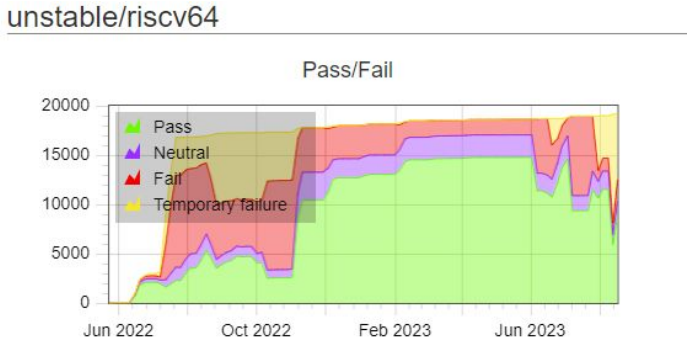
工具链部分感谢 @廖仕华 全力支持！

```
 Package                Architecture           Version                    Repository                Size
================================================================================================================
Installing:
 file                   riscv32                5.44-3.fc38                fedora                    47 k

Transaction Summary
================================================================================================================
Install  1 Package

Total download size: 47 k
Installed size: 92 k
Is this ok [y/N]: y
Downloading Packages:
file-5.44-3.fc38.riscv32.rpm                                               939 kB/s |  47 kB     00:00
----------------------------------------------------------------------------------------------------------------
Total                                                                      644 kB/s |  47 kB     00:00
Running transaction check
Transaction check succeeded.
Running transaction test
Transaction test succeeded.
Running transaction
  Preparing        :                                                                                1/1
  Installing       : file-5.44-3.fc38.riscv32                                                       1/1
  Verifying        : file-5.44-3.fc38.riscv32                                                       1/1

Installed:
  file-5.44-3.fc38.riscv32

Complete!
bash-5.2# file
Usage: file [-bcCdEhikLlNnprsSvzZ0] [--apple] [--extension] [--mime-encoding]
            [--mime-type] [-e <testname>] [-F <separator>]  [-f <namefile>]
            [-m <magicfiles>] [-P <parameter=value>] [--exclude-quiet]
            <file> ...
       file -C [-m <magicfiles>]
       file [--help]
bash-5.2#
```

Debian for RISC-V（于波）

- Official porting update
  1. 2023/07/23，riscv64 becomes Debian official architecture
  2. the rebootstrap process
  3. Installed: 10600+ failed: 200~ finished: 65%
  4. gitlab runner and crossqa support riscv64
- Debci update

  Ready for testing
- Some works
  1. chromium 115.0.5790.170 [rebase]
  2. zynaddsubfx, wsclean, man-db, mmseps2 [ftbfs done]
  3. libsass, mia,xutils-dev, strace [ftbfs done]
  4. yrmcds, wreport,yubioath-desktop [ftbfs patch]
  5. lazy-loader, ubelt [update]



FW相关更新（王翔）

- opensbi
  - 添加smcntrpmf扩展支持
  - 修正sbi_system_suspend的错误返回值，使代码适应spec
  - 添加基于syscon的重启和关机，并移除sifive test重启驱动（这个驱动可以用基于syscon的重启和关机来代替，需要添加dt）
  - 更新gitignore跳过.开头的文件，一些特别需要关注的文件需要特别添加
  - pmu计数器不连续的支持，移除mhpm_count，通过mhpm_mask记录哪些计数器是支持的
  - 修正Makefile中grep的一个警告
  - 修正查找event计数器中的一个拼写错误
  - __fw_rw_offset改为运行时计算，以规避clang16+编译报错
  - 把fdt_parse_isa_extensions移动到coolboot中防止操作系统破坏fdt后再解析isa扩展
  - 平台制定tlb队列长度支持，tlb队列改为通过堆申请
  - 修正c9xx pmu引起hang，允许s-mode访问相关寄存器
- openocd
  - 修正通过progbuf执行fence的问题，fence.i可能不被支持会打断progbuf的执行

固件相关更新(洛佳)

- 本周暂无更新

RISCV性能跟踪小队 - 陈小欧

- 暂无更新

香山开源RISC-V处理器 - ICT / PCL

- 取指前端
  - 修复预译码边界情况处理错误
  - 调试预测器参数，暂无显著效果
- 乱序调度&向量
  - IssueQueue 推测唤醒支取消通路添加完成，可以启动 Linux
  - Move 指令消除：合入新版 RTL 设计，优化时序和面积
  - Vector Perm 和 Reduction 功能单元集成完成
- 访存
  - 添加 Hybrid unit，Load Store 共用流水线
  - 完成 Sbuffer 加入动态阈值机制，针对性优化 spec06 lbm 测试点
  - 完成 L1 stream 预取以及 L1 L2 多级预取和动态调控机制，性能调试中
  - 进行 TLB filter 优化
- 缓存
  - 针对新版 Coupled L2 代码进行时序评估，并解决了部分时序问题
  - 在 MainPipe 模块和总线中添加了更多信息的DB 记录，并在 tl-test 中也添加了 ChiselDB 的支持
  - 完成 CHI-Test 验证框架 RN-F 端和 ICN Agent 的代码实现，并通过了 RN-F 和 ICN 的联合测试

MLIR 结合 RISC-V 相关工作 - 张洪滨

MLIR Vector Dialect Dynamic Vector Length Support

- #1: Integrate vector length configuration with the current mask operation.
- #2: Create a standalone vector length operation.
- ~~#3: Integrate dynamic vector representation into ODS.~~
- 结合 #1 和 #2: 通用 vector.setvl + vector.mask

Operation 优化 & E2E 支持

- Operation Optimization and Benchmark cases - https://github.com/buddy-compiler/buddy-benchmark/tree/main/benchmarks/OpOptimization
- [WIP]: 使用 Spike 构造针对 E2E 模型的 CI 流程
- [WIP]: Bert 模型在 Sequencer Vector Repo 跑通

Gemmini Dialect 进展

- [WIP] RVV + Gemmini + SiFive VCIX Proposal
- [Gemmini Dialect] Gemmini Dialect enhancement on tiled_matmul - https://github.com/buddy-compiler/buddy-mlir/pull/178

Chisel and Additional Technology / Sequencer

暂无更新

OpenHW & OpenHW Aisa Working Group

- AWG工作会议这两个月暂停

ROCm bootstrapping for RISC-V (陆言, PLCT Tariser)

- 本周暂无更新

自由讨论 / AOB

- RISC-V 中国峰会
- RISE 基金会
-

BACKUP

准备加入更多的国际开源组织进行同步观测

欢迎追加或提议