欢迎第一次加入的伙伴(开会时请从下一页开始展示)

- 开放编辑，直接点击 request for edit 然后在东亚时区群里at吴伟
- 如果没有找到自己的内容分类，可以添加1-2页在最开始或中间
- 欢迎在开始的前5分钟进行自我介绍
- 日常八卦在东亚时区RISC-V双周同步微信群中，欢迎加入

东亚时区RISC-V双周会

2023年12月07日·第070次

https://github.com/cnrv/RISCV-East-Asia-Biweekly-Sync

Host: 席静

Organizer: PLCT Lab plct-oss@iscas.ac.cn

会议议程（15:00 - 16:00）

- 自我介绍、等待参会者接入、非技术话题八卦（没有的话就直接跳过）
- RVI 的更新和八卦（基本上跟东亚双周会群内消息同步）
- Unratified Specs 的参考实现进展
- 东亚地区小伙伴的项目更新
- 自由讨论

RISC-V International 同步、全球开源社区八卦（史宁宁）

- RISC-V 软件移植优化锦标赛
  - https://rvspoc.org 报名已开启，赛题公开
- RISC-V Summit North America 2023
  https://www.youtube.com/playlist?list=PL85jopFZCnbMfMRR25ENcRkhhAUGwP5C5
- RISC-V 101
  https://www.youtube.com/playlist?list=PL85jopFZCnbOBxiKAMG00zFyx9g9q5mht
- [mktg-content] Get Your Company Profile In: Opportunity (No cost or sponsored) in The SHD Group's RISC-V Market Report
  https://lists.riscv.org/g/mktg-content/message/611
- Renesas unveils first generation 32-bit RISC-V CPU core
  https://www.eenewseurope.com/en/renesas-unveils-first-generation-32-bit-risc-v-cpu-core/
- 256核！赛昉科技发布全新RISC-V众核子系统IP平台
  https://www.eet-china.com/info/71306.html

RISC-V 韩语社区的同步与八卦

- 韩国嵌入式解决方案公司MDS Tech开设RISC-V开发者支援中心
  - 成立于1998年的中坚公司
  - 目前有开设RISC-V相关的课程
-

RISC-V 日语社区的同步与八卦

- 瑞萨电子（Renasas）于11月30日宣布独立开发出基于RISC-V的32位CPU Core
  - RV32I/RV32E，支持M Extension，A Extension，以及 C Extension

RISC-V 俄语社区的同步与八卦

俄罗斯RISC-V 联盟宣布启动一项资助竞赛，用于开发和实施 RISC-V 技术教育材料。该项目的教育合作伙伴是圣彼得堡国立大学，竞赛的运营商是国立开放大学“INTUIT”。

目的是寻找并支持为俄罗斯大学开设新培训课程的建议，以培训微电子和信息技术领域的专家。

RISC-V GCC进展

- 廖仕华提交了RISC-V Scalar Crypto/Bitmanip intrinsic的实现：https://gcc.gnu.org/pipermail/gcc-patches/2023-November/638238.html
- gcc支持了LP64E ABI，它与ILP32E相似，将整型寄存器的数目限制为16个，面向嵌入式系统 https://gcc.gnu.org/git/?p=gcc.git;a=commit;h=006e90e13441c3716b40616282b200a0ef689376
- Thead添加了自定义厂商扩展指令集XtheadVector：

  https://sourceware.org/git/?p=binutils-gdb.git;a=patch;h=8321007a988ecd3acb354e1374682e79f414dd29

- GNU Cauldron会议介绍：

  https://docs.google.com/document/d/1_01XZvVcbb-IYeQ1B5CW2bE9092105s0udhmYT0_EjU/edit?usp=sharing

- RISC-V GNU Toolchain slides链接：

  https://docs.google.com/presentation/d/1b7kZke1D1xvktcptnbKdhSw6uWr6yEu8SHXEx0hux20/edit?ouid=113624190907107496245&usp=slides_home&ths=true

Clang/LLVM 进展 (PLCT)

- upstream接收的patch
  - [flang][runtime] Add a critical section for LookUpOrCreateAnonymous. https://github.com/llvm/llvm-project/pull/74468

- xtheadvector 的支持，https://github.com/ruyisdk/llvm-project
  - 第一个大佬评论，https://github.com/ruyisdk/llvm-project/pull/30#issuecomment-1835712978
  - 第一个来自社区伙伴的 pr，fix build by changing enum definition https://github.com/ruyisdk/llvm-project/pull/35

- 另附，2023 LLVM Developers Meeting视频：https://www.youtube.com/playlist?list=PL_R5A0lGi1AD9nPVIv7mG8_2mMSiL_0Ik

QEMU/Spike/Sail/ACT进展 (PLCT)

V8 for RISC-V 更新（邱吉、陆亚涵）

实现turboshaft里部分riscv的指令选择优化

1. 5061589: [riscv][turboshaft] Merge EqualOp into ComparisonOp | https://chromium-review.googlesource.com/c/v8/v8/+/5061589
2. 5066071: [riscv] Implement ChangeInt32ToInt64 when input is a load | https://chromium-review.googlesource.com/c/v8/v8/+/5066071

提交部分chromium浏览器的base和angle组件的riscv补丁

3. 5054184: [base][riscv] Add riscv support in ProcessCPUArchitecture | https://chromium-review.googlesource.com/c/chromium/src/+/5054184
4. 5057086: [riscv] Add riscv support | https://chromium-review.googlesource.com/c/angle/angle/+/5057086

还有关于ffmpeg和sandbox两个组件的补丁，因改动加大且加入了非官方支持的架构代码，需要chrome ATLS进行确认,才能开始review

Port 上游更新

5. 5032534: [riscv][compiler] Generalize InstructionSelectorT for Turboshaft (part 19) | https://chromium-review.googlesource.com/c/v8/v8/+/5032534
6. 5051556: [riscv][turboshaft] Port InstructionSelector part4 | https://chromium-review.googlesource.com/c/v8/v8/+/5051556
7. 5055995: [riscv][jspi][arm64] Port JS central stack switch | https://chromium-review.googlesource.com/c/v8/v8/+/5055995
8. 5075020: [riscv][builtins] Avoid reloading undefined value in InterpreterEntryTrampoline | https://chromium-review.googlesource.com/c/v8/v8/+/5075020
9. 5081171: [riscv][builtins][masm] Use CallBuiltin/TailCallBuiltin where possible | https://chromium-review.googlesource.com/c/v8/v8/+/5081171

Spidermonkey for RISC-V更新（邱吉、陆亚涵）

无

OpenJDK for RISC-V 更新(RV64及upstream) 杨飞

1. Correctness and performance testing before Rampdown/Code Freeze.
- OpenJDK-21.0.2 LTS (2024/01/15 GA)
- OpenJDK-17.0.10 LTS (2024/01/06 GA)
- OpenJDK-22 (2024/03/19 GA)

2. Co-authored JDK-mainline PRs:
- https://github.com/openjdk/jdk/pull/16750 (8261837: SIGSEGV in ciVirtualCallTypeData::translate_from)

3. Reviewed JDK-mainline PRs:
- https://github.com/openjdk/jdk/pull/16382 (8318158: RISC-V: implement roundD/roundF intrinsics)
- https://github.com/openjdk/jdk/pull/16417 (8316592: RISC-V: implement poly1305 intrinsic)
- https://github.com/openjdk/jdk/pull/16453 (8319184: RISC-V: improve MD5 intrinsic)
- https://github.com/openjdk/jdk/pull/16481 (8318218: RISC-V: C2 CompressBits)
- https://github.com/openjdk/jdk/pull/16658 (8318219: RISC-V: C2 ExpandBits)
- https://github.com/openjdk/jdk/pull/16500 (8319412: RISC-V: Simple fix of indent in c2_MacroAssembler_riscv.hpp)
- https://github.com/openjdk/jdk/pull/16498 (8319408: RISC-V: MaxVectorSize is not consistently checked in several situations)
- https://github.com/openjdk/jdk/pull/16521 (8319525: RISC-V: Rename *_riscv64.ad files to *_riscv.ad under riscv/gc)
- https://github.com/openjdk/jdk/pull/16557 (8319705: RISC-V: signumF/D intrinsics fails compiler/intrinsics/math/TestSignumIntrinsic.java)
- https://github.com/openjdk/jdk/pull/16657 (8318159: RISC-V: Improve itable_stub)
- https://github.com/openjdk/jdk/pull/16629 (8318217: RISC-V: C2 VectorizedHashCode)
- https://github.com/openjdk/jdk/pull/16703 (8320280: RISC-V: Avoid passing t0 as temp register to MacroAssembler::lightweight_lock/unlock)

4. Proposed JDK21u backport PRs:
- https://github.com/openjdk/jdk21u/pull/338 (8319525: RISC-V: Rename *_riscv64.ad files to *_riscv.ad under riscv/gc)
- https://github.com/openjdk/jdk21u/pull/360 (8319184: RISC-V: improve MD5 intrinsic)

OpenJDK for RISC-V 更新（RV32G移植相关工作）曹贵

RV64 JDK 主线:

- https://github.com/openjdk/jdk/pull/16880 (8320397: RISC-V: Avoid passing t0 as temp register to MacroAssembler::
cmpxchg_obj_header/cmpxchgptr)
- https://github.com/openjdk/jdk21u/pull/399 (8320280: RISC-V: Avoid passing t0 as temp register to MacroAssembler::lightweight_lock/unlock)

JDK11U for RV32:

- Fix use of cr register in URShiftL/LShiftL/RShiftL nodes without kill cr

Async-profiler:

Async-profiler 对RV64的支持已成功合入到主线，并每天拉取最新代码在 LicheePI 4A上测试
https://github.com/async-profiler/async-profiler/pull/644

openEuler RISC-V（周嘉诚）

- Recent official major release: openEuler 23.09 [News] [Download]
  - RISC-V becomes the first new official architecture of openEuler since x86 and ARM
  - Follow-up release is ready for [Download] now, providing addition packages and hardware images
- Making progress of the “LLVM Parallel Universe Project”
- Brief work recap
  - firefox: add upstream riscv64 optimization patch [distro] [merged]
  - pcre2: add sljit enablement patch for riscv64 [distro] [merged]
  - nodejs: upgrade to 20.10.0 [distro] [open]
  - libuv: upgrade to 1.47.0 [distro] [merged]
  - Initialized multiple kde packages (7) [distro] [open]
  - Many other packaging changes, and more fixes for the “LLVM Parallel Universe Project”

Gentoo for RISC-V 的情况更新（Gentoo 小队）

-

Arch Linux RISC-V（潘瑞哲、Felix）（Offline）

- [core] 256 / 263 (97.34%)
- [extra] 12984 / 13511 (96.1%)
- upgpatch: nodejs 21.1.0-1
  - deps: V8: cherry-pick 13192d6e10fa by kxxt · Pull Request #50552 · nodejs/node · GitHub
  - deps: V8: cherry-pick 70caf337c3f6 by kxxt · Pull Request #50506 · nodejs/node · GitHub
- AMD CLR - Compute Language Runtimes rocvirtual: use SIMD memcpy only on x86
- ROCR-Runtime Add RISC-V support
- RadeonOpenCompute/rocminfo: use -m64 only in amd64
- python-zict: lmdb: Platform-specific default map size
- pdal: Fix convention error with xmlErrorPtr caused by libxml2 API change
- clamav-rs: Fix char signedness problem with var virname
- updpkg: linux-sophgo 6.1.61-1
- upgpatch: qt6-webengine

felixonmars commented now

许愿：Zig 的 riscv64 支持
目前有一些进度我更新在了 ziglang/zig#18018
看起来还有不少工作需要做。

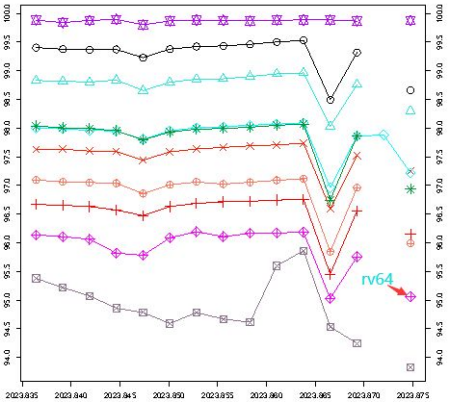
Fedora for RISC-V status update（20231206）

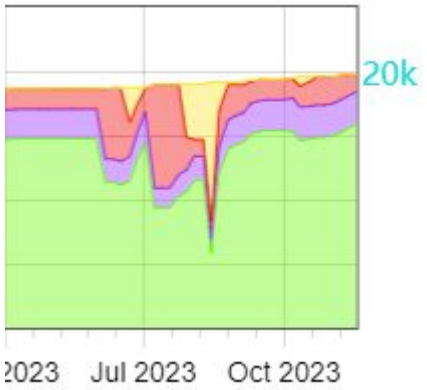
- **RPM packaging**
  - Status: **Updating F39**
    - **21381/23469 [91.1%] srpm have been built.**
    - **Building F40, will do mess build soon**
  - Spin: Server/Workstation/Cloud…
  - WIP Spin: IoT/**CoreOS**
- **main package version:**
  - Toolchain(up-to-date for F39)
    - gcc-13.2.1 -1
    - glibc-2.38-10
    - binutils-2.41-14[rawhide]
  - libffi-3.4.4-2(up-to-date)
  - java-latest-openjdk[ONGING]
  - perl-5.38.0-501(up-to-date)
  - python3.12-3.12.0-1(up-to-date)
  - llvm-17.0.4-1(up-to-date)
  - golang-1.21.3-1(up-to-date)
  - rust-1.74.0-1(up-to-date)
- Desktop support Fedora 39:
  - DONE：XFCE/LXDE/LXQT/GNOME/ Budgie/Cinnamon/Mate/Sugar/Sway/KDE
  - Building：Deepin[ONGING]
  - Key Desktop App
    - firefox-120.0-2[DONE]
    - Libreoffice-7.6.3.1-4[DONE]
    - Thunderbird [ONGING]
    - Chromium [ONGING]
- Image :
  - Sophgo SG2042 EVB/Milk-V[DONE]
    - LiveCD image [ONGING]
  - TH1520 BeagleV/LPi4A/***[DONE]
  - StarFive JH7110 boards[ONGOING]
- ROS/ROS2 upgraded to F39
  - ROS2 packaging is ongoing
- function testing:
  - **Podman[pass], Image：fedora-rv64（f39）**
  - Ceph[ONGING]
  - K8s[ONGING]

Debian for RISC-V（于波）

- Official porting update
  1. Installed: ~16.2K ; BD-Uninstablled: < 350
  2. Architecture percent: ~ 95%
  3. testing suite is coming
  4. Python3.12 WIP
- Debci update

  Over 20K binary testing for Dec I
- Some works
  1. Chromium upstream
  2. vf2 Debian sid image
  3. ldc/bpfcc/yabause for riscv64
  4. python-nss [NMU]/onboard/python-babel





FW相关更新（王翔）

- opensbi
  - 改进sbi_hsm_hart_interruptible_mask加快比特位扫描的速度
  - 通过hsm重启时跳过等待冷启动的核心
  - 添加SEE扩展支持
  - 修正可中断核心不包含RESUME_PENDING
  - 修正汇编文件中一些数据段的类型错误
  - 修正获取PMU计数器信息时返回不存在的计数器信息

固件相关更新(洛佳)

- RISC-V SBI 2.0的扩展可能存在定义不完整的情况：https://lists.riscv.org/g/tech-prs/message/730
  - 社区意见：扩展需要初始化的shared memory长度是固定的
  - 这里存在一个C语言社区和Rust语言社区对同一件事情的不同看法，我们以memcpy为例
    - C语言对memcpy(dst, src, len)的定义是：dst“至少”要有len长度
    - Rust语言对slice::copy_from_slice的定义是：切片是“正好”为len长度的元组
  - 由于存在很多C语言用户的SBI开发者，标准正文里曾经仅采用C语言的表述。对Rust开发者而言，我们应当认为SBI中的共享内存都是定长的，于是修改了标准正文：https://github.com/riscv-non-isa/riscv-sbi-doc/pull/135
  - 其它内容：特殊的指针值由相应SBI扩展决定
  - 希望大家在RISC-V SBI 2.0正式版批准之前多提点意见！SBI是RISC-V特权层软件必不可少的接口规范，建议内核、虚拟化软件和固件开发者引起重视
- RustSBI的RISC-V SBI 2.0支持已经更新（目前支持最新预览版2.0-rc7），等待2.0正式版发布
- RustSBI原型设计系统

RISCV性能跟踪小队 - 陈小欧

- 暂无更新

香山开源RISC-V处理器 - ICT / PCL

- 前端
  - 完成前端 FTQ 面积压缩方案修正
  - 完成 FTB 和 ICache 的 sram 规格拆分（#2493，#2497）
- 后端
  - BusyTable 支持 load 推测快速唤醒（#2502）
  - IssueQueue 时序优化，出队后并行 flush 和 load cancel（#2494）
  - 降低 IQ entry 位宽，减少存储开销（#2500）
  - 优化 IQ 入队唤醒时序，将入队唤醒放在 EnqEntry 完成（#2499）
- **访存**
  - 持续推进时序优化，MemBlock 内部违例减小至 -30ps 左右（#2501）
  - 新 features（实现紧耦合 L1-L2 总线和关键字优先）已跑通 CI 等基本测试
  - MinimalConfig 下的 VLSU 跑通 riscv-vector-tests 全部测试用例
- **缓存**
  - 优化跨模块时序，修改多处 L1D-L2 以及 L1I-L2 的时序违例路径
  - L3 新替换算法进行性能测试，有一定性能倒退，正在分析原因

Chisel and Additional Technology / Sequencer

- T1
  - 对接Compiler团队的Perf Event设计
  - 开始进行与Rocket的SoC集成
    - vsetvl通过
  - 完成动态验证框架
  - 进行了数轮refractor
  - 定义了最后一轮LSU的架构设计
- Chisel
  - MLIR C-API完成
  - 完成了Property与Probe的C-API
- RocketChip
  - RocketX 项目启动
- TN28 PLL设计收敛
- New Infra
  - 本地CI集群setting up

OpenHW & OpenHW Aisa Working Group

-

ROCm bootstrapping for RISC-V (陆言, PLCT Tariser)

- 本周暂无更新

自由讨论 / AOB

- 有没有同样在 RISE 基金会里做事的小伙伴？有空交流交流啊～
  - wuwei2016@iscas.ac.cn
  - 看看能否组合起来互补开会，现在的会议时间都不太友好 :(

BACKUP

准备加入更多的国际开源组织进行同步观测

欢迎追加或提议