欢迎第一次加入的伙伴(开会时请从下一页开始展示)

- 开放编辑，直接点击 request for edit 然后在东亚时区群里at吴伟
- 如果没有找到自己的内容分类，可以添加1-2页在最开始或中间
- 欢迎在开始的前5分钟进行自我介绍
- 日常八卦在东亚时区RISC-V双周同步微信群中，欢迎加入

东亚时区RISC-V双周会

2022年09月29日·第044次

https://github.com/cnrv/RISCV-East-Asia-Biweekly-Sync

Host: 廖春玉

Organizer: PLCT Lab plct-oss@iscas.ac.cn

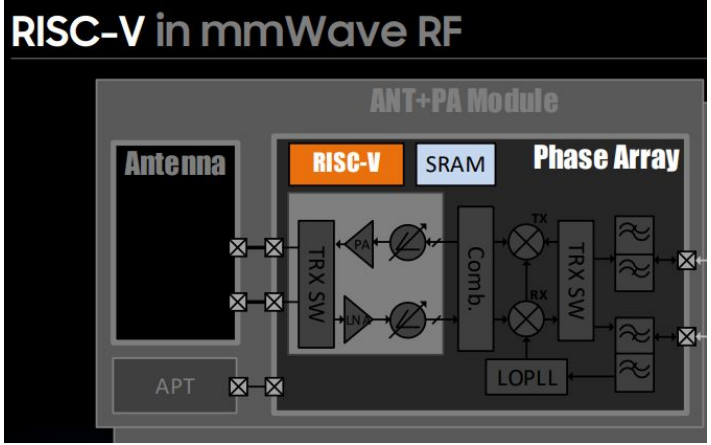
会议议程（15:00 - 16:00）

- 自我介绍、等待参会者接入、非技术话题八卦（5分钟）
- RVI 的更新和八卦（基本上跟东亚双周会群内消息同步）
- Unratified Specs 的参考实现进展
- 东亚地区小伙伴的项目更新
- 自由讨论

RISC-V International 同步、全球开源社区八卦

- Apple to Move a Part of its Embedded Cores to RISC-V, Stepping Away from Arm ISA
  - https://www.techpowerup.com/298936/report-apple-to-move-a-part-of-its-embedded-cores-to-risc-v-stepping-away-from-arm-isa
- [RISC-V] [tech-p-ext] slides on ARC preferences for moving forward with P extension
  - http://www.jhauser.us/RISCV/ext-P/RISCV-20220911-P-extension.pdf
- 谷歌也入局RISC-V，与AI芯片有关
- 欧盟更新《关于创建欧洲开源硬件、软件和RISC-V技术主权的建议和路线图》报告
- OpenCloudOS 社区 RISC-V ARCH SIG 正式成立，致力于RISC-V架构软件生态的共建和推广
- openKylin在RISC-V方向工作论文入选国际会议ICACTE 2022最佳演讲论文

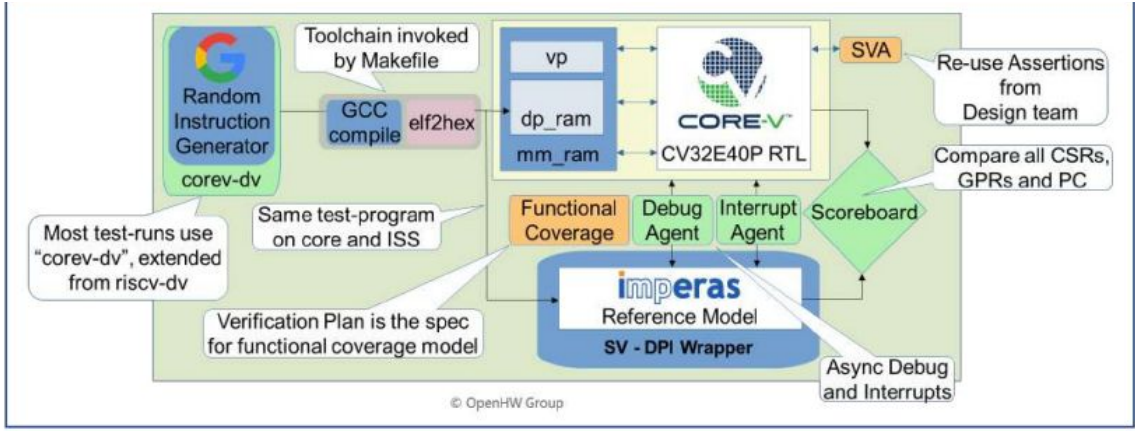
RISC-V 韩国 同步与八卦



- 三星李在镕--下个月与软银孙正义会长讨论ARM收购
- 回顾
- 三星RISC-V开发从2017开始，
- E.g.， 如图在2020推出的 5G RF frontend 模组的 mmWave RF处理用了RISC-V Core
- 自家的RISC-V主要用在
  - (1) RF Calibration, (2) AI Image Sensor, (3) AI Computing Control, (4) Security Management, (5) Safety Island
- 推测
  - 三星要ARM，软银要钱
  - 在Low-power SoC持续投入
  - 三星希望增强Fabless 实力来救这几个亲儿子（e.g.， Samsung Mongoose失败，设计水平低下）
    - 三星电子的系统LSI事业部
    - 半导体代工事业部
    - 移动事业部

RISC-V 韩国 同步与八卦

- 公司COONTEC
  - 主要做design verification，embedded OS还有security产品的
- 和欧洲的SysGo公司开始伙伴关系，希望把这两个用在自己家的产品里
  - RTOS: PikeOS
  - Embedded Linux: ELinOS



2nd generation CV32E40P OpenHW flow (2H2020)
(Imperas model encapsulated in SystemVerilog)

Datacenter/Cloud Computing SIG 2022/09/19 会议纪要:

- Agenda
  - 简单回顾过去半年 DataCenter/Cloud Gap清单的内容;
  -Jeff Maguire(Ventana) 建议DataCenter sig(Roadmap)工作可以参考worksonarm(https://www.arm.com/solutions/infrastructure/works-on-arm), 接下来的工作重点应放在那些未完成的任务上。
- Action Items
  - 修改白皮书的DC软件栈slide;
  - Ravi更新TEE Gap;
  - Michael 更新 Accelerators.

Sig-toolchain Meeting 9.26

1. riscv-gnu-toolchain repo update to GCC 12.2 and plan to clean up the issue tracker.
Jessica Clarke sugguest carrying an upstream issue into the upstream tricker.

2. Plan to convert existing unpriv spec form Latex to AsciiDoc.

3. Updates from Linux Plumbers Conference:
 ●HWCAPinterface
  o Kernel-user space API/AB to query available extensions o Proposal: key/value pairs
 ●ACPI/UEFI
  o Merge changes upstream if ECR(engineering change request)is accepted
 ●Tuningin-kernel mem*/str*functions
  o Selection policy is weak part(no cost-model)
   Benchmarking at bootup(which load)?
   Most likely: fixed order with acceptance of overruling on SoC-level

4. Updates from GUN Cauldron
 ●GCC intrinsic &auto-vectorizationforRISC-V
  o First patches already landed upstream
  o There is still a lot of work ahead
  o Patches are stored in GitHub:
   https://github.com/riscv-collab/riscv-gcc/tree/riscv-gcc-rvv-next
  o Current goals:
        Add support for existing patterns(this will already enable auto-vectorization)

来自香山

介绍香山设计方法的MICRO论文《Towards Developing High Performance RISC-V Processors Using Agile Methodology》定稿了。论文也通过Artifact Evaluation获得三个徽章(Available, Functional, Reproduced)。

我们已将论文分享在了GitHub上，欢迎大家批评指正！

一、论文GitHub链接：https://github.com/OpenXiangShan/XiangShan-doc/raw/main/publications/micro2022-xiangshan.pdf

日语社区的RISC-V更新

招募伙伴进行观测

俄语社区的RISC-V更新

招募伙伴进行观测

AOSP for RISC-V - 汪辰、陆旭凡

- RVI Android SIG 动态更新：
  - add riscv64 for vndk snapshot build script: https://github.com/riscv-android-src/platform-development/pull/2 review 中
  - 配合 CTS 测试移植 chrome 到 android apk for riscv。进行中 ……
  - RISC-V Android Source https://github.com/riscv-android-src 近期会有一次较大更新
  - RISC-V Android on VisionFive/JH7100 项目：https://github.com/android-risc-v，“can barely boot-up to Home Launcher, although it's very slow. UI resolution is 640x480 by Mesa swpipe and Ethernet is working”，最近还在尝试在板子上运行 TensorFlow Lite。如果感兴趣可以加入讨论组 https://groups.google.com/g/android-risc-v

- 技术类文章分享：
  - Android Init Language: https://zhuanlan.zhihu.com/p/564715676
  - Android Early Init Boot Sequence: https://zhuanlan.zhihu.com/p/565027512
  - VNDK 基本概念: https://zhuanlan.zhihu.com/p/567512089

RISC-V GCC进展

GNU Cauldron会议结束了:

RVV : GNU Tools Cauldron - S9 - day 2 58:20 ~ 1:59:10

ZC* & RISC-V BOF : GNU Tools Cauldron - S5 - day 2 1:58:40 ~ 2:49:10

会议视频频道: GNU Tools Cauldron 2022

钟居哲继续在向上游提交RVV的Patch，包括 poly move, machine mode, RVV types等patch已被接受合并

提交了gcc -m[no]-csr-check选项的支持，目前还没有收到修改意见

Zmmul扩展已合入GCC上游，修改了‘g’的定义，现在g的展开项中会包含zmmul (由于m->zmmul)

T-head vendor extension(MemIdx,FMemIdx,Mempair,CMO,Bitmanip,MAC,CondMov,SYNC), Zawr，Ztso 已合入binutils上游

TommyMurphy开始协助清理riscv-gnu-toolchain仓库中的issue，目前已经将issue数减少至100以下（高峰时issue数为300+）

Clang/LLVM 进展 (PLCT)

- Gollvm
  - 针对RISCV的支持大佬还没空帮忙review.
  - 针对than大佬给的测试用例测出了一些问题，已经提了issue以及fix的pr
    - https://github.com/golang/go/issues/55141
    - https://github.com/golang/go/issues/55242
    - Merged, 修复runtime.Reflect中空结构体内存分配https://go-review.googlesource.com/c/gofrontend/+/431735
    - 修复含空成员的结构体的比较运算https://go-review.googlesource.com/c/gofrontend/+/431736

- LLVM upstream
  - Merged, 为lldb模拟器添加完整的RVM和RVA拓展https://reviews.llvm.org/D133670
  - Merged, 标量优化，保留 and X, 0xfff，而不被优化0xff00, https://reviews.llvm.org/D134155
  - Merged, 给llvm-dwarfdump 添加R_RISCV_SET8，R_RISCV_SET16，R_RISCV_SET32 支持 https://reviews.llvm.org/D134408
  - New，提交了关于Zc*的全部MC代码 https://reviews.llvm.org/search/query/n7vyeFKsW.mb/#R

Clang / LLVM 社区的更新（廖春玉、陆旭凡）

1. D134785 [RISCV] Add lowering for llvm.roundeven
2. D134639 [VP][RISCV] Add vp.maxnum and vp.minnum intrinsics and RISC-V support.
3. D134489 [RISCV] Add lowering for scalable @llvm.riscv.masked.strided.load/store
4. D134400 [RISCV] Improve support for vector fp_to_sint_sat/uint_sat.
5. D134168 [RISCV] Make preferred alignment of PointerArgs for MemIntrinsic

QEMU/Spike/Sail/ACT进展 (PLCT)

- QEMU
  - Zce版本更新
    - https://github.com/plctlab/plct-qemu/tree/plct-zce-upstream
  - RVV 反汇编支持更新
    - https://lists.gnu.org/archive/html/qemu-riscv/2022-09/msg00211.html
- Spike
  - Zce版本更新
    - https://github.com/plctlab/plct-spike/tree/plct-zce-upstream
- Sail/ACT
  - CMO扩展支持更新
    - https://github.com/riscv/sail-riscv/pull/137
    - https://github.com/riscv-non-isa/riscv-arch-test/pull/226
    - https://github.com/riscv-software-src/riscof/pull/46
    - https://github.com/riscv-software-src/riscv-ctg/pull/22
    - https://github.com/riscv-software-src/riscv-isac/pull/43

GEM5进展 (PLCT)

- V拓展新增指令
  - index访存指令(vluxei8.v, vsuxei8.v等)
  - 浮点扩位规约指令(vfwredosum.vs等)
  - 单操作数指令(vfirst.m等)
  - 饱和位移指令(vssra.v等)
- 离V标准拓展全部实现的TODO
  - 向量访存Fault only first 指令(vle8ff.v等)
  - 向量元素移位指令(vslideup.vx等)
  - 向量压缩指令(vcompress.vm等)
- 近期PR
  - https://github.com/plctlab/plct-gem5/pull/11
  - https://github.com/plctlab/plct-gem5/pull/8

V8 for RISC-V 更新（邱吉、陆亚涵）

PLCT贡献：

- 修复没有正确插入 vsetvli指令的问题

  3917324: [riscv] Fix not calling vsetvli to set vtype correctly after branch | https://chromium-review.googlesource.com/c/v8/v8/+/3917324

- 修复在rv32平台当移位量小于-32时结果不正确

  3912629: [riscv] Fix shift error when the shift amount is less than or equal to -32 | https://chromium-review.googlesource.com/c/v8/v8/+/3912629

- 修复rv64平台遇到uint32 compare时，source location不准确的问题

  3903733: [riscv] Don't cover when node is Trap and uint32 compare | https://chromium-review.googlesource.com/c/v8/v8/+/3903733

- Port上游更新

  3905856: [riscv] Port 3904233: Remove unused RelocInfo::Mode::RUNTIME_ENTRY | https://chromium-review.googlesource.com/c/v8/v8/+/3905856

社区人员贡献：

Ting Chou

- 3878448: [riscv] Fix cctest/test-assembler-riscv*/RISCV_UTEST_FLOAT_WIDENING_vfwmacc_vf. | https://chromium-review.googlesource.com/c/v8/v8/+/3878448

Spidermonkey for RISC-V更新（邱吉、陆亚涵）

- **Jittests Status**
  - 9096个通过 715个失败 26个超时 通过率92.4%

- **更新的Patch**
  - 3312c423c71d3 Implement some func (#40)
  - e55c9aa55a3b1 fix block (#39)
  - 76d629b36f056 fix float reg alloc (#38)
  - 295c061e92a98 fix-osi (#37)
  - 272b49b480c08 fix asmjs (#36)
  - 3826c654a3e6f fix WriteLoad64Instructions (#35)
  - 9c0c93b5e5421 fix ror/rol (#34)
  - ef8c23b7402e7 [wasm] add ptr patch call (#33)
  - cd4090eac5d48 Fix unbox (#32)

OpenJDK for RISC-V 更新（RV64及upstream）杨飞

Merged JDK-mainline PRs:
- -- https://github.com/openjdk/jdk/pull/10368 (8294083: RISC-V: Minimal build failed with --disable-precompiled-headers)
- -- https://github.com/openjdk/jdk/pull/10382 (8294183: AArch64: Wrong macro check in SharedRuntime::generate_deopt_blob)
- -- https://github.com/openjdk/jdk/pull/10439 (8294430: RISC-V: Small refactoring for movptr_with_offset)

Reviewed JDK-mainline PRs:
- -- https://github.com/openjdk/jdk/pull/10311 (8293781: RISC-V: Clarify types of calls)
- -- https://github.com/openjdk/jdk/pull/10344 (8294012: RISC-V: get/put_native_u8 missing the case when address&7 is 6)
- -- https://github.com/openjdk/jdk/pull/10369 (8294086: RISC-V: Cleanup InstructionMark usages in the backend)
- -- https://github.com/openjdk/jdk/pull/10370 (8294087: RISC-V: Refactor instruction alignment assertions)
- -- https://github.com/openjdk/jdk/pull/10375 (8294100: RISC-V: Move rt_call and xxx_move from SharedRuntime to MacroAssembler)
- -- https://github.com/openjdk/jdk/pull/10384 (8294187: RISC-V: Unify all relocations for the backend into MacroAssembler::relocate())
- -- https://github.com/openjdk/jdk/pull/10391 (8294198: Implement isFinite intrinsic for RISC-V)
- -- https://github.com/openjdk/jdk/pull/10462 (8294492: RISC-V: Use li instead of patchable movptr at non-patchable callsites)

Support for Foreign-API & RISCV-RVC:
- -- Foreign-API RISC-V Port:
  - -- https://github.com/feilongjiang/jdk/pull/3 (basic porting work)
  - -- https://github.com/feilongjiang/jdk/pull/6 (code refactoring)
- -- New RISCV-RVC proposal: upstreaming in progress

Loom RISCV Port:
- -- New branch at: https://github.com/RealFYang/jdk/tree/JDK-8286301
- -- Template Interpreter & C1 JIT compiler: can run skynet test
- -- Enable C2 JIT compiler

OpenJDK for RISC-V 更新（RV32/PLCT 史宁宁）

一、PR

1、Fix the reg params of string_compareXXX

2、Fix the get_and_addLXXX

3、Fix the get_and_addLXXXAcq

4、Fix the ALU_COST of get_and_addLXXX_ALU_COST

5、Fix the loadConL

6、Fix the addL_reg_imm

7、Fix the subL_reg_imm

8、Fix the L2F/F2L

9、Fix the D2L/L2D using the call_vm

10、Remove the get_and_setL/addL

11、Remove the get_and_addLAcq instructs

OpenJDK for RISC-V 更新（RV32/PLCT 史宁宁）

12、add long cmp framework in the MacroAssembler

13、Add the insns of long compare funs in C2

14、Add ulong compare funcs

15、Add is_far param for some long compare funcs

16、Use the long_cmp_branch to instead of the cmp_branch

17、Remove the error comment

二、文章

1、OpenJDK RISC-V架构的宏汇编器和汇编器的实现

https://zhuanlan.zhihu.com/p/567690611

OpenJDK for RISC-V 更新（RV64及upstream）张定立

Vector-API support:

- RISC-V: Add VectorLoadConst node for Vector API
- Enable vector and/or/xor node for RISC-V
- RISC-V: Add VectorLoadMask node for Vector API
- RISC-V: Add Widening/Narrowing Floating-Point/Integer Type-Convert Instructions
- RISC-V: Add VectorLoadShuffle node for Vector API

hsdis:

- Add --with-binutils-src support for cross-compile
- Remove useless code related to hsdis-demo.c in Makefile

OpenJDK for RISC-V 更新（RV64及upstream）曹贵

Discuss the implementation and testing of the Vector API with the community

Vector-API support:

- RISCV: Add VectorCastB2X/VectorCastI2X/VectorCastL2X/VectorCastS2X vector node for riscv
- RISCV: Add VectorCastD2X/VectorCastF2X vector node for riscv

OpenJDK8 backporting（章翔）

1、Add sa-jdi.jar on rv64

2、The problem of aarch64

openEuler RISC-V

- 软件包编译构建进度：
  - 核心包：4130 / 4240 97.10%
  - 扩展包：2355 / 4269 55.17%
  - 三方包：未开始
- Tarsier-OBS 构建：
  i. firefox97 rebuild
  ii. vlc removed
  iii. add LibreOffice
- PR：+103（中间仓：14 src-oe：89）
  - https://github.com/isrc-cas/tarsier-oerv/blob/main/biweekly/2022-09-22.md
- 工具：Tarsier-OBS软件包版本获取工具
- 镜像：增加镜像wifi支持、修复镜像问题
- 测试：2209发版测试（WIP）

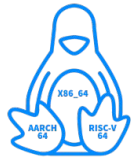
- 软件包版本
  - Toolchain gcc-10.3.1-10 / glibc-2.34-80
  - binutils 2.37-6
  - libmpc 1.2.0-1
  - gmp 6.2.1-1
  - rust 1.57.0-2 → 1.60.0-5 (updating)
  - java-latest-openjdk-18.0.1.9-0
  - llvm/clang 12.0.1-2
  - python 3.10.2-4
  - perl 5.28.0-435
  - golang 1.17.3-3
  - nodejs 16.14.2-1

Gentoo for RISC-V 的情况更新（Gentoo小队）

- A total of 61 keywording commits: https://whale.plctlab.org/riscv/RISC-V-双周会/20220929/commits.txt
  - dev-perl/Starlet: Keyword 0.310.0-r1 riscv
    - PR: https://github.com/gentoo/gentoo/pull/27396
    - Keyword: https://github.com/gentoo/gentoo/commit/6acc84059b08ba58be67d912118ec11f174ee924
- GHC 9.0.2: RISC-V support
  - PR: https://github.com/gentoo/gentoo/pull/27397
- Libvirt: add basic RISC-V support
  - PR: https://listman.redhat.com/archives/libvir-list/2022-September/234530.html
- LuaJIT: DynASM works
  - Forked tree: https://github.com/infiWang/LuaJIT/tree/riscv-dynasm
  - https://gist.github.com/infiWang/f01c00db9285d1190c07c6fc4080274a
- media-sound/helm: add sse2 and atomic build flags
  - PR: https://github.com/mtytel/helm/pull/307
- sys-process/psinfo: fix 'unsigned char' issue
  - Bug: https://bugs.gentoo.org/872821
  - Fixed commit: https://github.com/gentoo/gentoo/commit/8d87286759fdff1a4ed2b9a36f7a1818e031e841

Arch Linux RISC-V（东东）

1. 移植进度
   [core] 251 / 259 (96.91%)
   [extra] 2677 / 3034 (88.23%)
   [community] 8484 / 9545 (88.88%)
2. archboot: add support for riscv64
3. Built distinct package count: 1372
   Highlight packages:
   - linux - 5.19.2.arch1-1 -> 5.19.9.arch1-1
   - firefox - 104.0.1-1 -> 105.0-2
   - qt5-wayland - 5.15.6+kde+r43-2 -> 5.15.6+kde+r49-1
   - rust-analyzer - 20220912-1 -> 20220926-1
   - glib2 - 2.72.3-3 -> 2.74.0-2
   - gtk3 - 1:3.24.34-1 -> 1:3.24.34+r156+g812b3930d0-1
   - gtk4 - 1:4.6.6-1 -> 1:4.8.1-1
   - pandoc - never been built -> 2.19.1-4
   - ffmpeg - 2:5.1.1-3 -> 2:5.1.2-1
   - archiso - never been built -> 67-1
   - imagemagick - 7.1.0.48-1 -> 7.1.0.49-1
   - nodejs - 18.9.0-1 -> 18.9.1-1
   - telegram-desktop - 4.1.1-1 -> 4.2.0-1
   - redis - 7.0.4-1 -> 7.0.5-1
   - docker-compose - 2.10.2-1 -> 2.11.1-1
   - mariadb - 10.9.2-1 -> 10.9.3-1
   - elixir - 1.13.4-1 -> 1.14.0-1
   - jre-openjdk 17.0.1.u12-1 -> 18.0.2.1.u0-1



ARCHBOOT - Arch Linux
Kernel 5.19.x
Secure Boot & Console
Gnome & Plasma & Xfce
https://bit.ly/archboot

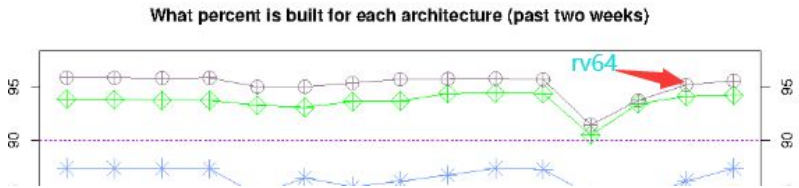
Fedora for RISC-V（傅炜）

- SRPM打包编译进度
  - [fc36] 144000+ / 22832 (70%) [https://openkoji.iscas.ac.cn/repos/fc36dev/] 作为编译环境仓库使用
  - [rawhide]【On Going】
- 以 server 和 desktop 的功能包为目标:
  - firefox and Chromium are blocked by ffmpeg, building dependencies
    - scala【On Going】
    - Mingw-w64-tools（呼唤勇士, 先尝试绕过）
    - ceph、Qemu 和 libvirt 相关的包已补齐，可移除最后几个F33旧包依赖。
- 软件版本:
  - Toolchain gcc-12.2.1-2 / glibc-2.36-4 (up-to-date)
  - Binutils 2.39-3 (up-to-date)
  - Rust 1.63.0-1 [need qemu fix from Felix](up-to-date)
  - java-latest-openjdk-19.0.0.0.36-2(up-to-date)
  - LLVM/Clang 14.0.0-1→ 14.0.5-3[rawhide](updating)
  - Python 3.10.4 → 3.11[rawhide] (updating)【文宇】
  - Perl 5.34.2→ 5.36.0-490[rawhide](updating)【海滨】
  - Go 1.18-1→ 1.19-1[rawhide](updating)
- Images:
  - QEMU/D1/Icicle/Unmatched/JH7110 Images
  - Workstation (GNOME&KDE) Image: will be tested on JH7110

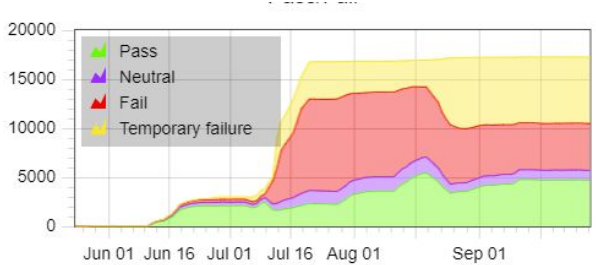
Debian for RISC-V I（于波）

- Buildd status&news

  1. Installed: 15250+
  2. No news for official port
  3. Thanks Zhang BoYang



- Debci update



- Some work

1. https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1020002 [fix ftbfs]
2. https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1009052#15 [libunwind upgrade]
3. https://github.com/git-multimail/git-multimail/pull/224 [PR merged]
4. https://github.com/google/leveldb/issues/1058 [report bug]

FW相关更新（王翔）

- opensb
  - 文档修正一些拼写错误
  - 之前一些补丁的讨论和更新
  - SBI Debug Trigger Extension 扩展的讨论 https://lists.riscv.org/g/tech-debug/topic/92375492
- openocd
  - riscv断点设置添加不支持match napot和match range时的回退；并把trigger类型的检测前移到trigger的枚举中，减少查找空闲trigger对tselect和tdata1的读写

固件相关更新(洛佳)

- embedded-hal发布1.0.0-alpha.9版本，主要是由于Rust的GAT稳定，后续讨论async/await in embedded更方便了
  - 对此我有一个绝妙的想法，只可惜这里页边太小，写不下
  - @Berrysoft：执行器是可与具体计算硬件高度优化的软件领域，甚至可以为每个核专门编写
- Visionfive v1 Oreboot：主要是丹尼尔在负责，现在已经能启动下一阶段
- 其它平台：HPM6750、？？（未发布的芯片）
  - OSFW社区：没有SBI接口的固件也是有用的，因为嵌入式领域也需要初始化主板电源等等
- salus：Rust RISC-V TEE Hypervisor（https://github.com/rivosinc/salus）
  - 虚拟化软件若直接提供Supervisor环境，可以直接用RustSBI作为依赖，这是竞争产品做不到的
  - 可以发布一个实例（而非单例）模型的RustSBI特性，然后包含到RustSBI 0.3版本里
- 与Penglai TEE整合：暂时还没有人兴趣领域接近
- 有哪些内核应当被固件启动？只考虑Linux可能不太够……
- RustSBI Github stars：585（+6），仍然超过所有竞争对手的总和

香山开源RISC-V处理器 - ICT / PCL

- 南湖流片进展
  - 继续优化 BPU 和访存单元的时序
  - 决定采用 1P11M 工艺流片，目前后端频率评估为 1.85GHz@0.9V
  - 根据 riscv-test 加强香山 CSR 单元的 ISA 兼容性
  -
- 昆明湖进展
  - 乱序流水线：推进发射后读设计，完成 FMA 模块设计和时序评估
  - 访存单元：调研讨论 store-load 违例检查机制优化
  - 缓存单元：CoupledL2 构建 Acquire Miss 和 Release 通路

MLIR RISC-V Vector (RVV) Dialect Proposal - 张洪滨

相关链接

- RFC Patch - https://reviews.llvm.org/D108536
- RFC Post - https://discourse.llvm.org/t/rfc-add-risc-v-vector-extension-rvv-dialect/4146/32
- MLIR + RVV 集成测试环境搭建文档 - https://gist.github.com/zhanghb97/ad44407e169de298911b8a4235e68497
- MLIR + RVV 环境搭建 - https://github.com/buddy-compiler/buddy-mlir/blob/main/thirdparty/build-rvv-env.sh
- MLIR + RVV 相关实验 - https://github.com/buddy-compiler/buddy-mlir/tree/main/examples/RVVExperiment

WIP

- Load/Store Scalable Vector Issue
  - VP Intrinsic Load/Store Scalable Vector 报错 Calling a function with a bad signature!
  - RVV Dialect 目前只支持 1D Load/Store Scalable Vector
- 一些解法
  - Add vl support based on Vector Dialect + Mask Region RFC（https://discourse.llvm.org/t/rfc-vector-masking-representation-in-mlir/64964）
  - 等待 VP Intrinsic 支持 Scalable Vector Type / RVV Dialect 支持 nD Load/Store Scalable Vector

面向 RISC-V 的 OpenCV 情况更新 - 韩柳彤

Universal Intrinsic 的 RISC-V Vector 后端：

PR #22558 (Merged): Fix v_signmask for RISC-V Vector

PR #22520 (Under review): Modify the SIMD loop in color_hsv.

PR #22463 (RFC): Redesign the SIMD macro.

Chisel and Additional Technology / Sequencer

- RVV 第一版Bug在push --force的情况下完成！ KUDO 李秦君
  - Checkout https://github.com/sequencer/vector/tree/lane
- RSA MMM 加速器实例完成！ KUDO 郑鉉壬/叶泽文
  - SW Checkout https://github.com/OpenRigil/openrigil-firmware
  - HW Checkout https://github.com/OpenRigil/rocket-chip-blocks
- RocketChip 开始由 sequencer 主导拆分 TileLink/Rocket 出 Mono Repo（庆祝 sequencer manic 期的到来）
  - https://github.com/sequencer/tilelink
  - https://github.com/sequencer/rocket
- RocketChip 正在迁移到 Chisel3
  - 感谢 陈春昀 的卓越贡献们
    - https://github.com/chipsalliance/rocket-chip/pull/3063
    - https://github.com/chipsalliance/rocket-chip/pull/3062
    - https://github.com/chipsalliance/rocket-chip/pull/3061
    - https://github.com/chipsalliance/rocket-chip/pull/3060
    - https://github.com/chipsalliance/rocket-chip/pull/3054
    - https://github.com/chipsalliance/rocket-chip/pull/3053
    - https://github.com/chipsalliance/rocket-chip/pull/3052
    - https://github.com/chipsalliance/rocket-chip/pull/3051
    - https://github.com/chipsalliance/rocket-chip/pull/3049
    - https://github.com/chipsalliance/rocket-chip/pull/3042
    - https://github.com/chipsalliance/rocket-chip/pull/3041
    - https://github.com/chipsalliance/rocket-chip/pull/3040
    - https://github.com/chipsalliance/rocket-chip/pull/3039
    - https://github.com/chipsalliance/rocket-chip/pull/3038
- 其他人或有或无 贡献但无外部 产出望再接再 厉

自由讨论 / AOB

- 国庆有什么计划？
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