欢迎第一次加入的伙伴(开会时请从下一页开始展示)

- 开放编辑，直接点击 request for edit 然后在东亚时区群里at吴伟
- 如果没有找到自己的内容分类，可以添加1-2页在最开始或中间
- 欢迎在开始的前5分钟进行自我介绍
- 日常八卦在东亚时区RISC-V双周同步微信群中，欢迎加入

东亚时区RISC-V双周会

2022年11月10日·第047次

https://github.com/cnrv/RISCV-East-Asia-Biweekly-Sync

Host: 陈嘉炜

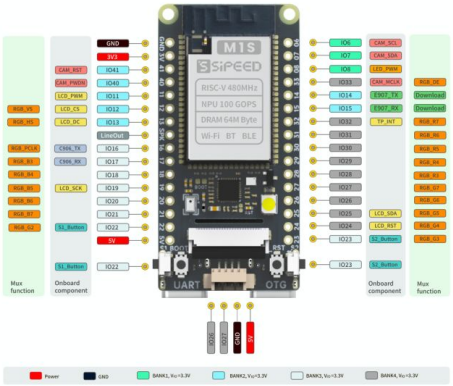
Organizer: PLCT Lab plct-oss@iscas.ac.cn

会议议程（15:00 - 16:00）

- 自我介绍、等待参会者接入、非技术话题八卦（没有的话就直接跳过）
- RVI 的更新和八卦（基本上跟东亚双周会群内消息同步）
- Unratified Specs 的参考实现进展
- 东亚地区小伙伴的项目更新
- 自由讨论

RISC-V International 同步、全球开源社区八卦

- 日本的 RISC-V Day
- 北美的 RISC-V Summit
- SC2022 里面的 RISC-V 厂商和活动
- https://riscv.org/blog/2022/11/xuantie-c908-high-performance-risc-v-processor-catered-to-aiot-industry-chang-liu-alibaba-cloud/
- Andes Technology Unveils The AndesCore AX60 Series, An Out-Of-Order Superscalar Multicore RISC-V Processor Family
- PLCT许愿池计划2023启动啦！
- 新的RISC-V小设备



RISC-V 韩语社区的同步与八卦

- 韩国ZARAM Technology （主要做低功耗嵌入式、通信半导体）
  - 把自家设计的RISC-V CPU和韩国电子技术研究院进行知识产权共有
  - 上个月新闻说IPO，估值一亿美元左右
  - 未来方向与边缘计算、低功耗、riscv相关
- 关于SK海力士和三星收购arm新闻的follow up，海力士明确表示不参与收购。三星没有正式的回应，但是一直增加现金性资产，很多媒体都推测不会进行arm的收购。

RISC-V 日语社区的同步与八卦

- 本月16日~17日三天是日本RISC-V Days，可以网上参加
  RISC-V Days Tokyo 2022 AutumnRISC-V 協会 | RISC-V Alliance Japan (riscv.or.jp)
  - 参会单位包括谷歌，RISC-V Alliance Japan, Redhat 以及庆应大学、清华大学
- 日本的RISCV Alliance 社群有关于llvm和riscv的读书会，内容偏基础一些各位有兴趣可以参加或者看过去的录像。
  https://kobe-processor-architecture.connpass.com/event/262150

RISC-V 俄语社区的同步与八卦

- 本周暂无动静

AOSP for RISC-V - 汪辰、陆旭凡

- Google AOSP upstream PR
  Android (RISC-V) Review，Issue 20221110（in Chinese）：https://zhuanlan.zhihu.com/p/581900441

- RVI Android SIG upstream:
  - support GKI kernel/modules building for android emulator:
    - https://github.com/riscv-android-src/kernel-manifest/pull/1
    - https://github.com/riscv-android-src/kernel-common/pull/2
    - https://github.com/riscv-android-src/kernel-common-modules-virtual-device/pull/1
    - https://github.com/riscv-android-src/kernel-prebuilts-common-modules-virtual-device-5.10-riscv64/pull/1
    - https://github.com/riscv-android-src/manifest/pull/9
    - https://github.com/riscv-android-src/kernel-prebuilts-5.10-riscv64/pull/2
    - https://github.com/riscv-android-src/riscv-android/pull/11
    - https://github.com/riscv-android-src/riscv-android/pull/15

  - initial changes about supporting Android apk for chromium
    - https://github.com/aosp-riscv/chromium/pull/1
    - https://github.com/aosp-riscv/working-group/pull/52

- Articles update（in Chinese）:
  - Linux driver modules: kobject & kset: https://zhuanlan.zhihu.com/p/578581653
  - Notes: How to write a Linux kernel module: https://zhuanlan.zhihu.com/p/579301578
  - Linux sysfs: https://zhuanlan.zhihu.com/p/579434022

RISC-V GCC进展

提交了profiles在gcc上的patch, 在gnu toolchain双周会上讨论了遇到的一些开发问题, 正在整理意见更新实现中:

profile gcc patch: https://gcc.gnu.org/pipermail/gcc-patches/2022-November/604869.html

issues record: sig-toolchains@lists.riscv.org | Profile implement progress and problems

-march string proposal: sig-toolchains@lists.riscv.org | Toolchain conventions: the -march string

psABI requirement: https://github.com/riscv-non-isa/riscv-elf-psabi-doc/pull/351

钟居哲与Kito正在继续推进RVV gcc实现, 目前intrinsic framework已合入gcc上游, RVV C intrinsic API 1.0将在近期release,将成立TG讨论有关问题, gcc会遵循该版本的intrinsic实现

RVV patches: https://gcc.gnu.org/git/?p=gcc.git&a=search&h=HEAD&st=author&s=juzhe

RVV C intrinsic API: riscv-admin/rvv-intrinsics

下周一psABI会议上继续讨论Zc扩展的问题:

tech-code-size@lists.riscv.org | zcmt requires new linker relaxation

欢迎陈逸轩同学加入GNU小队参与有关工作

RISC-V GNU Toolchain双周会slides链接:
https://docs.google.com/presentation/d/1WgZrLwTQI_oySdlR7ugAT-KGvf9xMvKSLgz9EAHxkWg/edit#slide=id.g182888ba841_0_0

Clang/LLVM 进展 (PLCT)

1. **[RISCV] Add support for static chain** https://reviews.llvm.org/D129106
2. **[RISCV] Support for mapping symbol in RISCV.** https://reviews.llvm.org/D137417
   https://github.com/riscv-non-isa/riscv-elf-psabi-doc/pull/196

3. **[LLDB] Optimize lldb build time and memory consumption.**
   https://reviews.llvm.org/D137041
4. **[LLDB][RISCV] Allow accessing registers through ABI names.**
   https://reviews.llvm.org/D137508
5. **[LLDB][RISCV] Allow accessing FPR registers through ABI names**
   https://reviews.llvm.org/D137761

Clang / LLVM 社区的更新（廖春玉、陆旭凡）

1. [IndVars] Forget the SCEV when the instruction has been sunk.
   https://reviews.llvm.org/D137060
2. [MemorySSA] Delete dead MemoryUseOrDef for CallInst when clone loop basicblock
   https://reviews.llvm.org/D137553
3. [LoopFlatten] Forget all block and loop dispositions after flatten
   https://reviews.llvm.org/D137651
4. [RFC] Unify memory effect attributes
   https://discourse.llvm.org/t/rfc-unify-memory-effect-attributes/65579

QEMU/Spike/Sail/ACT进展 (PLCT)

- Spike
  - Zc*扩展支持
    - https://github.com/riscv-software-src/riscv-isa-sim/pull/1141
    - https://github.com/riscv/riscv-opcodes/pull/107
- QEMU
  - 完善可变XLEN支持
    - https://github.com/plctlab/plct-qemu/tree/plct-rv32u-dev

gem5 进展 (PLCT)

- V拓展
  - 对V拓展指令重新分类，添加类别信息
    https://github.com/plctlab/plct-gem5/pull/16
  - 在指令分类基础上完成向量寄存器对齐(align)和重叠(overlap)检查
    https://github.com/plctlab/plct-gem5/pull/18
  - 新增vslideup.vi 和 vslidedown.vi指令
    https://github.com/plctlab/plct-gem5/pull/19

V8 for RISC-V 更新（邱吉、陆亚涵）

- Port Upstream

  3971517: [riscv][wasm] Allocate feedback vectors on demand |
  https://chromium-review.googlesource.com/c/v8/v8/+/3971517

Spidermonkey for RISC-V更新（邱吉、陆亚涵）

- Test status
  - Jit-test 通过率99.38% 9751 Pass 60 Failure 0 timeout
  - Jstests 通过率99.9% 44259 Pass 3 Failure 1 timeout
- Patch
  - 7b126a1ecc3e Implement func (#52)
  - 78ce02b344973 Fix jump long (#51)
  - ab7ee829337b8 Implement riscv branchandlink (#50)
  - 6d2729dd14fbf Fix compareD (#49)
  - 0c86149c7827c Implement copy sign bit (#48)
  - 64d6cd88b4191 Fix wasm load/store error (#47)
  - 356638fcddeff fix wasm conversion error (#46)
  - 70e8c5de2e18c fix cmp set (#45)
  - ba48fda2d4b2e Fix NotSigned (#44)

OpenJDK for RISC-V 更新(RV64及upstream)杨飞

1. Merged jdk-mainline PRs:
- https://github.com/openjdk/jdk/pull/10917 (8286301: Port JEP 425 to RISC-V)
- https://github.com/openjdk/jdk/pull/10965 (8296285: test/hotspot/jtreg/compiler/intrinsics/TestFloatIsFinite.java fails after JDK-8280378)

2. Reviewed jdk-mainline PRs:
- https://github.com/openjdk/jdk/pull/10921 (8296136: Use correct register in aarch64_enc_fast_unlock())
- https://github.com/openjdk/jdk/pull/10884 (8295948: Support for Zicbop/prefetch instructions on RISC-V)
- https://github.com/openjdk/jdk/pull/10878 (8295968: RISC-V: Rename some assembler intrinsic functions for RVV 1.0)
- https://github.com/openjdk/jdk/pull/10880 (8295967: RISC-V: Support negVI/negVL instructions for Vector API)
- https://github.com/openjdk/jdk/pull/10691 (8295261: RISC-V: Support ReductionV instructions for Vector API)
- https://github.com/openjdk/jdk/pull/11005 (8296435: RISC-V: Small refactoring for increment/decrement)
- https://github.com/openjdk/jdk/pull/11009 (8296447: RISC-V: Make the operands order of vrsub_vx/vrsub_vi consistent with RVV 1.0 spec)
- https://github.com/openjdk/jdk/pull/11036 (8296515: RISC-V: Small refactoring for MaxReductionV/MinReductionV/AddReductionV node implementation)

3. Loom RISCV Port:
- Upstreamed: https://github.com/openjdk/jdk/commit/91292d56a9c2b8010466d105520e6e898ae53679
- Will be delivered with JDK 20 (General Availability - 2023/03/21)
- TODO: Postcall NOP optimization

4. Foreign-API RISCV Port:
- New development branch at: https://github.com/feilongjiang/jdk/tree/riscv-foreign-api
- Need rebasing with: https://git.openjdk.org/jdk/pull/10872 (8295044: Implementation of Foreign Function and Memory API (Second Preview))
- Need further rebasing with: https://git.openjdk.org/jdk/pull/11019 (8296477: Foreign linker implementation update following JEP 434)

OpenJDK for RISC-V 更新(RV32/PLCT 史宁宁)

1. Fix the cmovI_cmpL https://github.com/openjdk-riscv/jdk11u/pull/552
2. Fix the cmpUEqNeLeGt_imm0_XXX instructs in riscv32.ad https://github.com/openjdk-riscv/jdk11u/pull/553
3. Fix the loadB2L/loadUB2L https://github.com/openjdk-riscv/jdk11u/pull/554
4. Update the loadUI2L in riscv32.ad https://github.com/openjdk-riscv/jdk11u/pull/555
5. Fix the storeLConditional https://github.com/openjdk-riscv/jdk11u/pull/556
6. Improve the compareAndSwapL/compareAndSwapLAcq https://github.com/openjdk-riscv/jdk11u/pull/557
7. Fix the compareAndExchangeL/compareAndExchangeLAcq https://github.com/openjdk-riscv/jdk11u/pull/558
8. Fix the weakCompareAndSwapL/weakCompareAndSwapLAcq https://github.com/openjdk-riscv/jdk11u/pull/559
9. Add the lShiftL_regI_immGE32 in riscv32.ad https://github.com/openjdk-riscv/jdk11u/pull/560
10. Fix the cmp_l2i in cmpL3_reg_reg https://github.com/openjdk-riscv/jdk11u/pull/561
11. Fix the fp_args of double in calling_convention https://github.com/openjdk-riscv/jdk11u/pull/562
12. Fix the count num of double and array in generate_native_wrapper https://github.com/openjdk-riscv/jdk11u/pull/563
13. Fix the bugs in long cmp of macroAssembler_riscv32.cpp https://github.com/openjdk-riscv/jdk11u/pull/564

OpenJDK for RISC-V 更新（RV64及upstream）张定立

Merged & New JDK-mainline PRs:

- https://github.com/openjdk/jdk/pull/11009 | (8296447: RISC-V: Make the operands order of vrsub_vx/vrsub_vi consistent with RVV 1.0 spec)
- https://github.com/openjdk/jdk/pull/11074 | (8296638: RISC-V: NegVI node emits wrong code when vector element basic type is T_BYTE/T_SHORT)

Reviewed JDK-mainline PRs:

- https://github.com/openjdk/jdk/pull/10691 | (8295261: RISC-V: Support ReductionV instructions for Vector API)
- https://github.com/openjdk/jdk/pull/11036 | (8296515: RISC-V: Small refactoring for MaxReductionV/MinReductionV/AddReductionV node implementation)

Vector-API support:

- Add emit_data64 for loadcon
- Fix typo and instruct format of loadcon/vcompress/vexpand
- RISC-V: Add PopulateIndex node for Vector API

OpenJDK for RISC-V 更新（RV64及upstream）曹贵

Merged & New JDK-mainline PRs:

- https://github.com/openjdk/jdk/pull/11036 | (8296515: RISC-V: Small refactoring for MaxReductionV/MinReductionV/AddReductionV node implementation)

Reviewed JDK-mainline PRs:

- https://github.com/openjdk/jdk/pull/11074 | (8296638: RISC-V: NegVI node emits wrong code when vector element basic type is T_BYTE/T_SHORT)
- https://github.com/openjdk/jdk/pull/11009 | (8296447: RISC-V: Make the operands order of vrsub_vx/vrsub_vi consistent with RVV 1.0 spec)

Vector-API support:

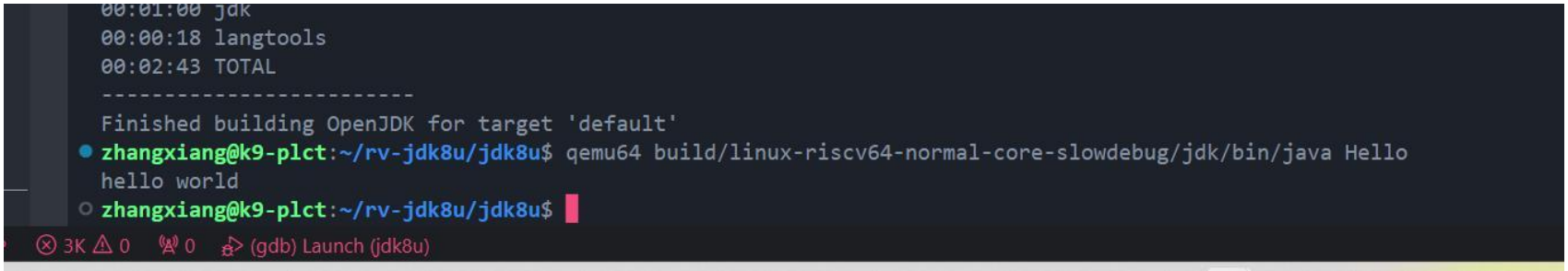
- RISC-V: Support vector api AddVI/AddVL mask node
- RISC-V: Support vector api AndV/OrV/XorV mask node

OpenJDK8 backporting（章翔）

1、修复一些小的问题

- https://github.com/zhangxiang-plct/jdk8u/pull/125
- https://github.com/zhangxiang-plct/jdk8u/pull/126
- https://github.com/zhangxiang-plct/jdk8u/pull/127
- https://github.com/zhangxiang-plct/jdk8u/pull/128
- https://github.com/zhangxiang-plct/jdk8u/pull/129
- https://github.com/zhangxiang-plct/jdk8u/pull/130
- https://github.com/zhangxiang-plct/jdk8u/pull/131
- https://github.com/zhangxiang-plct/jdk8u/pull/132
- Fix lookup_interface_method by replacing Klass with InstanceKlass
- Fix InstanceKlass::vtable_length_offset
- Fix typo on putfield_or_static

2、解释器移植成功，能跑通“Hello World”



openEuler RISC-V

1. PR:+96(中间仓:17 src-oe:79)
   - Init: scim、signon-plugin-oauth2、polkit-kde、kcalc、hyfetch、babeld、accounts-qml-module
   - Fix: hadoop-3.1、etcd、dump等
   - Upgrade: >62
2. Other
   - openeuler riscv衍生版eulaceura发布：qemu镜像　　使用说明
   - qBittorrent(及其引擎 libtorrent)、KeepassXC 、Remmina、botan2：详情
   - Electron（共20；succeeded: 19;failed:1）
   - llvm15 build succeeded
   - qt6及相关软件包（共49；succeeded: 7;unresolvable:40;failed:1）
3. Upgrade package
   - [redacted]RISC-V软件包版本，3版本不低于oe master
     - [redacted] 15.0.3(√)
     - [redacted] 5.34.0(√)

Gentoo for RISC-V 的情况更新（Gentoo 小队）

- Support statistics `(7935/19585, 40.25%)`：https://whale.plctlab.org/riscv/support-statistics/
- A total of 108 keywording commits: https://whale.plctlab.org/riscv/RISC-V-双周会/20221110/commits.txt
  - net-vpn/strongswan: Keyword 5.9.8 riscv gentoo/gentoo@6d5b5b3
  - net-proxy/ziproxy: Keyword 3.3.1-r2 riscv gentoo/gentoo@1c5718a
  - www-servers/fnord: Keyword 1.11-r2 riscv gentoo/gentoo@c07ad17
- Solve some new dependencies in GNOME 43 to keyword it
  - Bug: https://bugs.gentoo.org/880237
  - 6 commits:
    - gentoo/gentoo@9814756 gentoo/gentoo@561fc3d gentoo/gentoo@5c27452
    - gentoo/gentoo@1b10926 gentoo/gentoo@5e21ab0 gentoo/gentoo@6df5edd

Arch Linux RISC-V（东东、潘瑞哲）

```
[ Arch Linux RISC-V Bi-Week Package
Update Stats Report ]

Report generated on: 20221110
Package update count: 2378 updates
Distinct package update count: 1965

[core] 253 / 261 (96.93%)
[extra] 2705 / 3078 (87.88%)
[community] 8721 / 9756 (89.39%)
```

```
Highlight packages:
    linux - 6.0.2.arch1-1 --> 6.0.7.arch1-1
    rust - 1:1.64.0-1 --> 1:1.65.0-1
    rust-analyzer - 20221024-1 --> 20221031-1
    docker - 1:20.10.20-1 --> 1:20.10.21-1
    glib2 - 2.74.0-2 --> 2.74.1-1
    gtk4 - 1:4.8.1-1 --> 1:4.8.2-1
    qt5-wayland - 5.15.6+kde+r50-1 --> 5.15.7+kde+r49-1
    archiso - 67-1 --> 68-1
    imagemagick - 7.1.0.51-1 --> 7.1.0.52-1
    telegram-desktop - 4.2.4-1 --> 4.3.1-1
    graphviz - 6.0.1-1 --> 7.0.0-1.1
```

Arch Linux RISC-V（东东、潘瑞哲）Cont.

- Rust 1.65.0
  - https://github.com/felixonmars/archriscv-packages/pull/1925
  - Backported:
    - https://github.com/rust-lang/cc-rs/pull/676 Use specified compiler in is_flag_supported
    - The last hunk of https://github.com/tikv/jemallocator/pull/40 Fix build on riscv64gc-unknown-linux-gnu
  - Regenerate checksums and replace with sed after patching vendors

- GCC libitm upstreamed [PATCH v4] RISC-V: Libitm add RISC-V support.
  - https://gcc.gnu.org/pipermail/gcc-patches/2022-October/604620.html
  - Ready for bpo & manual tests, will have a PATCH v5 for clarifying error messages

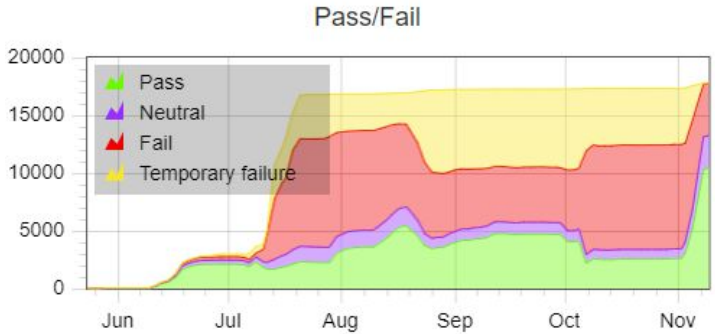
Fedora for RISC-V（傅炜）

- RPM packaging
  - [rawhide/F38]【On Going】[https://openkoji.iscas.ac.cn/repos/fc36dev/] as build repo
  - Libffi (updating)
  - Rpm-list-builder
- 软件版本:
  - Toolchain gcc-12.2.1-2 / glibc-2.36-4 (up-to-date)/Binutils 2.39-3 (up-to-date)
  - java-latest-openjdk-19.0.0.0.36-2(up-to-date)
  - perl-5.36.0-492[rawhide](up-to-date) need testing and merging，文档化中 [perl-bootstrap koji][文宇]
  - Python 3.11(up-to-date) need testing and merging，文档化中 [rpmlb + yaml, mock]
  - Rust 1.63.0-1→Rust 1.64 [need qemu fix from Felix] (updating)
  - LLVM/Clang 14.0.0-1→ 14.0.5-3[rawhide](updating) [赵佳盛]
  - Go 1.18-1→ 1.19-1[rawhide](updating)【海滨】
  - firefox and Chromium are blocked dependencies
    - scala【On Going】
    - Mingw-w64-tools【On Going】working on dependencies for Fedora 37/38
  - libvirt-8.8.0-1【On Going, depends on Mingw】
- Images:
  - QEMU/D1/JH7110 Images , waiting for VisionFive V2
  - Sophgo Server
- Team document: https://github.com/fedora-riscv/Fedora_riscv_devel_docs

Debian for RISC-V（于波）

- Buildd status&news

  1. Installed: ~15000 (blocked by atomic&cargo issues)
  2. Udd FTBFS packages ~278
  3. Official port news (porterbox available)



- Debci update

  1.Britney’s Job Hostory

- Some works

  1. https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=922579#42 [freetrue issue confirmed]
  2. https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1023128 [freetrue RM done]

Debian for RISC-V II

3*. https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1023551 [morse-simulator NMU RC done]

4. https://github.com/yuzibo/talks/blob/main/debian/2022-11-04-Debian-QA-overview.pdf

5*. https://salsa.debian.org/python-team/packages/tkcalendar [new queue]

6*. https://sourceforge.net/p/codeblocks/code/13001/ [upstream support riscv done]

7. https://salsa.debian.org/sunmin/86Box [ITP package]

Deepin for RISCV

- deepin-riscv-stage1 deepin-stage1 源码包 打包数量：6518
  - 添加了 firefox/libreoffice 等应用包
  - 修复部分包编译不通过的问题
- deepin-riscv-board deepin-riscv 板子每日CI构建
  - 支持 D1 三块板子(Nezha/MQ-pro/lichee-rv-dock)
  - 支持 JH7100 两块板子(visionfive-v1/BeagleV_Starlight)
  - 支持 JH7110 一块板子(Star64)
  - 刷写镜像下载地址
- th1520 支持镜像 支持平头哥曳影1520
- deepin-riscv-stage2 deepin-stage2 构建状态：
  - succeeded: 4326
  - failed: 460
  - unresolvable: 1734
- deepin-rv-packages-monitor 监控页面

FW相关更新（王翔）

- opensbi
  - 添加对RZ/Five的支持
  - 简化直接调用fdt_parse_uart_node_common的fdt_parse_xxx_uart_node的函数的代码
  - uart->reg_shift和uart->reg_io_width只在8520中使用，移除多余的代码
  - 添加对debug triggers支持。（存在的问题：只支持type6不支持type2，查找trigger没考虑chained，当前的install没有考虑chained）
  - 修正semihosting的llvm编译问题，llvm的char默认无符号和-1比较报错

固件相关更新(洛佳)

- RustSBI 发布 0.3.0 正式版(docs.rs/rustsbi、github.com/rustsbi/rustsbi)
  - 支持开发虚拟化环境和模拟器，这是O开头的SBI做不到的
  - 平台支持分为两种开发模式:独立包和原型系 统
- RustSBI Prototyping System 正在开发中
  - 预期将解决适配难度过大的问题，即使无Rust基础，一个下午就能适配新的硬件平台
  - 免费获得Penglai TEE、Dram's Emulated Hypervisor和Raven the Firmware Debugger
  - 可与C语言生态配合使用，但是O开头的SBI不能和Rust生态配合使用
- 平台支持独立包的进展
  - rustsbi-qemu预计合并入QEMU项目上游，rustsbi-d1提供成熟的开 发工具和单元测试工具
  - 快速陷入支持包fast-trap发布0.0.0版本
- SBI环境的单元测试和跑分用内核
  - 选择marchid get、ipi delay作为测试指标，RustSBI在真实单核芯片上性能达到 竞品的1.6倍，在多核模拟器上最高达到竞品的20~30倍，核越多性能越好

香山开源RISC-V处理器 - ICT / PCL

- 南湖流片进展
  - DMA 基础功能在 FPGA 上调试通过，成功联通 GMAC 和 PCIe，实现了 NFS 和 SSD 的访问
  - 推进双核、FLASH 和 JTAG 在 FPGA 上的调试工作
  - 对近期的代码修改进行 SPEC 性能分析
- 昆明湖开发进展
  - 前端：开始实现 Loop Buffer，继续调优 Loop Predictor 和预取
  - 后端：浮点加法规约模块的流水线划分完毕；继续重构后端流水线
  - 访存：细化新版 LSQ 的设计方案（新的违例检查框架、LQ 不存数据）
  - 缓存：对 Coupled L2 的进行主流水线各流水级功能划分，撰写设计文档

MLIR RISC-V Vector (RVV) Dialect Proposal - 张洪滨

提交人不在线 hongbin2019@iscas.ac.cn

相关链接

- RFC Patch - https://reviews.llvm.org/D108536
- RFC Post - https://discourse.llvm.org/t/rfc-add-risc-v-vector-extension-rvv-dialect/4146/32
- MLIR + RVV 集成测试环境搭建文档 - https://gist.github.com/zhanghb97/ad44407e169de298911b8a4235e68497
- MLIR + RVV 环境搭建 - https://github.com/buddy-compiler/buddy-mlir/blob/main/thirdparty/build-rvv-env.sh
- MLIR + RVV 相关实验 - https://github.com/buddy-compiler/buddy-mlir/tree/main/examples/RVVExperiment

WIP

- MLIR VP Ops on RVV Backend Integration Test and Issues Report - https://discourse.llvm.org/t/mlir-vp-ops-on-rvv-backend-integration-test-and-issues-report/66343/1
- VP Intrinsic 测试用例相关链接：
  - 集成测试汇总表：https://www.notion.so/MLIR-VP-Op-RVV-Integration-Test-df0b5470a4824b2cb101df4dd4205ea2
  - 集成测试 Web 服务：https://buddy.isrc.ac.cn/rvv/rvv-vp-intrinsic-add-scalable.mlir?line=1&column=1
- [VP] Add support for vp.inttoptr & vp.ptrtoint - https://reviews.llvm.org/D137169

Chisel and Additional Technology / Sequencer

- 向量单元设计进展
  - Load/Store 调试通过
  - verilator单元测试框架完成，VCS正在TODO
  - 正在用力修bug中
- RocketChip Working Group CI
  - Already on sequencer/rocket and sequencer/vector
- Rocket Standalone
  - 开始cosim
- 不小心做了个 PLL in TSMC28

（提交人不在 线）

OpenHW & OpenHW Aisa Working Group

- AWG
  - 欢迎更多会员和参与者
- COREV LLVM项目
  - 代码rebase，欢迎review（https://github.com/openhwgroup/corev-llvm-project/pull/21）
  - 待讨论：多指令集版本支持方案（CV32E40PV1、CV32E40PV2）
- COREV GCC项目
  - 讨论了CV32E40P的测试用例问题
  - 待讨论：多指令集版本支持方案（CV32E40PV1、CV32E40PV2）

自由讨论 / AOB

-

BACKUP

准备加入更多的国际开源组织进行同步观测

欢迎追加或提议

CHIPS Alliance

ISCAS将提供CI资源到chipsalliance，负责未来RocketChip的CI工作