

## 欢迎第一次加入的伙伴(开会时请从下一页开始展示)

- 开放编辑, 直接点击 request for edit 然后在东亚时区群里at吴伟
- 如果没有找到自己的内容分类, 可以添加1-2页在最开始或中间
- 欢迎在开始的前5分钟进行自我介绍
- 日常八卦在东亚时区RISC-V双周同步微信群中, 欢迎加入

# 东亚时区RISC-V双周会

2024年10月31日·第 90 次

<https://github.com/cnrv/RISCV-East-Asia-Biweekly-Sync>

Host: 陈逸轩

Organizer: PLCT Lab [plct-oss@iscas.ac.cn](mailto:plct-oss@iscas.ac.cn)

## 会议议程(15:00 - 16:00)

- 自我介绍、等待参会者接入、非技术话题八卦(没有的话就直接跳过)
- RVI 的更新和八卦(基本上跟东亚双周会群内消息同步)
- Unratified Specs 的参考实现进展
- 东亚地区小伙伴的项目更新
- 自由讨论

# RISC-V International 同步、全球开源社区八卦(陈逸轩)

SEGGER 推出了一款 RISC-V 调试器。点击[此处](#)跳转购买。

[SiFive P550](#) 开始发货了。

[ASHLING 和 Embecosm 合作为 Akeana 的RISC-V处理器提供工具链。](#)

RVA23 Profile spec 相关文章两则：

<https://www.edn.com/rva23-profile-ratification-bolsters-risc-v-software-ecosystem/>

[https://www.theregister.com/2024/10/23/rva23\\_profile\\_ratified/](https://www.theregister.com/2024/10/23/rva23_profile_ratified/)

David Patterson 写的50年记

<https://cacm.acm.org/opinion/life-lessons-from-the-first-half-century-of-my-career/>

# RISC-V 中文社区的同步与八卦(聂雨婷)

## 生态相关

- [英伟达、高通等芯片四巨头联手, 以新CPU架构对抗英特尔、AMD](#)
- [联通发布RISC-V智算3.1亿大单, 内蒙古华鑫超算科技有限公司中标](#)
- [国产编程语言MoonBit发布原生后端, 比Java快15倍, 拥抱 RISC-V](#)
- [傅炜先生获RISC-V国际基金会颁发2024年度社区领导力奖](#)
- [中国移动智能水表方案发布:RISC-V 架构国产自研芯片 CM6620](#)

## 一些好消息

- 无锡亚科鸿禹电子有限公司 & 跃昉科技加入甲辰计划

# RISC-V 韩语社区的同步与八卦

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# RISC-V 日语社区的同步与八卦

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# RISC-V 俄语社区的同步与八卦

无更新



# RISC-V 德语社区的同步与八卦(罗云翔)

RISC-V summit north america 2024

<https://events.linuxfoundation.org/riscv-summit/program/schedule/>



## Codasip

- Member Day Session: CHERI 101 and Standardization Session - Tariq Kurd, Codasip
- Member Day Session: Verifying a CPU with Sail - Tim Hutt, Codasip
- Say Goodbye to Fear, Uncertainty, and Doubt: Innovate with Codasip Studio Fusion - Keith Graham, Codasip(AI/ML)
- Demo: Securely Booting CHERI on a Full OS to Prevent Buffer Overflow Attacks - Carl Shaw, Codasip
- Software Engineers Are Tomorrow's Processor Engineers - Keith Graham, Codasip (Security)
- Hardening Linux and FreeBSD on RISC-V with CHERI - Carl Shaw, Codasip (Security)

## 西门子

- Demo: Accelerate RISC-V Development with Tessent UltraSight-V - Francisca Tan, Siemens EDA
- Understanding the Unformatted Trace & Diagnostic Data Packet Encapsulation for RISC-V Specification - Iain Robertson, Siemens EDA (Security)

# RISC-V 中国峰会进展(吴伟)

- 2024已经结束、2025尚未开始

# RISC-V 学习资源汇总整理计划(汪辰)

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# GCC 进展

- Support new option `-m(no-)autovec-segment`.

<https://gcc.gnu.org/git/?p=gcc.git;a=commit;h=f2989316139c3e7a99b1babe2606833c05b8a12f>

- Add intrinsic support for CMO extensions

<https://gcc.gnu.org/git/?p=gcc.git;a=commit;h=d2c8548e0ce51dac6bc51d37236c50f98fca82f0>

- Continue to improve SAT (Saturated arithmetic) template

<https://gcc.gnu.org/git/?p=gcc.git;a=search&h=HEAD&st=commit&s=SAT>

- Add `target_version` support

[https://patchwork.sourware.org/project/gcc/list/?series=39863&state=\\*](https://patchwork.sourware.org/project/gcc/list/?series=39863&state=*)

# Clang/LLVM 进展 (PLCT)

- [RISCV] Implement Clang Builtins for XCVmac Extension in CV32E40P

<https://github.com/llvm/llvm-project/pull/110623>

- [RISCV] Add svvptc extension

<https://github.com/llvm/llvm-project/pull/113882>

- [RISCV] Add Smdbltrp and Ssdbltrp extension

<https://github.com/llvm/llvm-project/pull/111837>

- RVP [in-progress]

<https://github.com/realqhc/llvm-project/tree/p-mc>

# QEMU/Spike 进展(呼唤志愿者)

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# Sail/ACT进展 (PLCT)

## Sail

- Add Smepmp extension  
(PMP Enhancement for memory access and execution prevention on M mode)  
<https://github.com/riscv/sail-riscv/pull/601>
- Remove N extension  
(N extension was never ratified, has been removed from the ISA manual )  
<https://github.com/riscv/sail-riscv/pull/584>
  - remove function sys\_enable\_next  
<https://github.com/riscv/sail-riscv/pull/606>
- Fix/Optimize V extension
  - Remove vlenb register  
<https://github.com/riscv/sail-riscv/pull/607>
  - Make calculate new vl configurable  
<https://github.com/riscv/sail-riscv/pull/608>

## ACT

- Add ruff check[submit]  
<https://github.com/riscv-non-isa/riscv-arch-test/pull/538>
- Add cli param env\_dir[submit]  
<https://github.com/riscv-non-isa/riscv-arch-test/pull/539>
- Bug Fix
  - Fix brackets not closed  
<https://github.com/riscv-non-isa/riscv-arch-test/pull/528>
  - fix ext\_specific\_vars bug  
<https://github.com/riscv-non-isa/riscv-arch-test/pull/517>
  - fix isac string bug[submit]  
<https://github.com/riscv-non-isa/riscv-arch-test/pull/544>

# V8 for RISC-V 更新(邱吉、陆亚涵)

1. 5977487: [riscv] Fix TruncateInt64ToInt32 | <https://chromium-review.googlesource.com/c/v8/v8/+5977487>
2. 5977673: [riscv][wasm][jspi][sandbox] Verify stack state on stack switch | <https://chromium-review.googlesource.com/c/v8/v8/+5977673>
3. 5971174: [riscv][codegen] Use a zone to track unresolved branches | <https://chromium-review.googlesource.com/c/v8/v8/+5971174>
4. 5971173: [riscv] Fix check failed in debug mode. | <https://chromium-review.googlesource.com/c/v8/v8/+5971173>
5. 5960218: [riscv] Reland "[CFI] Use WritableJitAllocation for relocation writes" | <https://chromium-review.googlesource.com/c/v8/v8/+5960218>
6. 5960217: [riscv]Reland "[wasm][jspi] Add JSPI stress mode" | <https://chromium-review.googlesource.com/c/v8/v8/+5960217>

(Yuri Gaevsky) [yuri.gaevsky@syntacore.com](mailto:yuri.gaevsky@syntacore.com):

1. 5899523: [riscv] Add 3rd scratch reg for Maglev compiler | <https://chromium-review.googlesource.com/c/v8/v8/+5899523>
2. 5953144: [riscv][wasm] Fix Load/Store trapping in LiftoffAssembler | <https://chromium-review.googlesource.com/c/v8/v8/+5953144>



Spidermonkey for RISC-V更新（邱吉、陆亚涵）

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# OpenJDK for RISC-V 杨飞

## 1. Authored/Co-authored JDK-mainline PRs:

- <https://github.com/openjdk/jdk/pull/21565> (8338383: Implement JEP 491: Synchronize Virtual Threads without Pinning)
- <https://github.com/openjdk/jdk/pull/21273> (8337511: Implement JEP 404: Generational Shenandoah (Experimental))
- <https://github.com/openjdk/jdk/pull/20677> (8305895: Implement JEP 450: Compact Object Headers (Experimental))

## 2. Reviewed JDK-mainline PRs:

- <https://github.com/openjdk/jdk/pull/19960> (8334999: RISC-V: implement AES single block encryption/decryption intrinsics)
- <https://github.com/openjdk/jdk/pull/21083> (8320500: [vectorapi] RISC-V: Optimize vector math operations with SLEEP)

## 3. Proposed/Reviewed JDK-21u / JDK-17u mainline PRs:

- <https://github.com/openjdk/jdk21u-dev/pull/953> (8339248: RISC-V: Remove li64 macro assembler routine and related code)
- <https://github.com/openjdk/jdk21u-dev/pull/962> (8339548: GHA: RISC-V: Use Debian snapshot archive for bootstrap)
- <https://github.com/openjdk/jdk17u-dev/pull/2842> (8339248: RISC-V: Remove li64 macro assembler routine and related code)
- <https://github.com/openjdk/jdk17u-dev/pull/2860> (8339548: GHA: RISC-V: Use Debian snapshot archive for bootstrap)

## 4. Reviewed riscv-port-jdk11u PRs:

- <https://github.com/openjdk/riscv-port-jdk11u/pull/28> (8339548: GHA: RISC-V: Use Debian snapshot archive for bootstrap)
- <https://github.com/openjdk/riscv-port-jdk11u/pull/29> (8287552: riscv: Fix comment typo in li64)
- <https://github.com/openjdk/riscv-port-jdk11u/pull/30> (8290137: riscv: small refactoring for add\_memory\_int32/64)
- <https://github.com/openjdk/riscv-port-jdk11u/pull/31> (8292867: RISC-V: Simplify weak CAS return value handling)
- <https://github.com/openjdk/riscv-port-jdk11u/pull/32> (8293050: RISC-V: Remove redundant non-null assertions about macro-assembler)



## JDK 24

This release will be the Reference Implementation of version 24 of the Java SE Platform, as specified by JSR 399 in the Java Community Process.

### Status

The main line is open for bug fixes, small enhancements, and JEPs as proposed and tracked via the JEP Process.

### Schedule

2024/12/05	Rampdown Phase One (branch from main line)
2025/01/16	Rampdown Phase Two
2025/02/06	Initial Release Candidate
2025/02/20	Final Release Candidate
2025/03/18	General Availability

## Test

test/jdk/jdk/incubator/vector

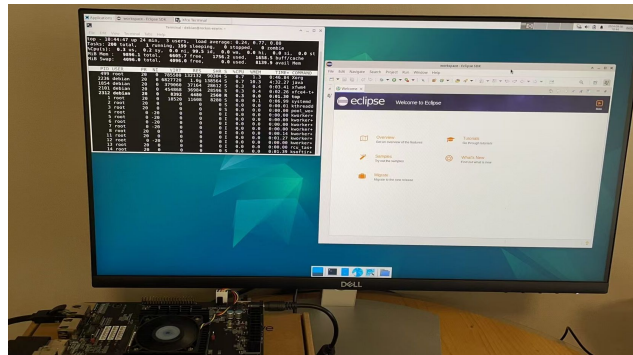
## Performance

data on bananapi

Benchmark - bananapi	(size)	Mode	Cnt	Score +intrinsic	Error +intrinsic	Score -intrinsic	Error -intrinsic	Units	Improvement
Double128Vector.ACOS	1024	avgt	10	112444.388	655.761	208554.742	1508.709	ns/op	1.855
Double128Vector.ASIN	1024	avgt	10	104121.259	243.167	208314.499	2833.61	ns/op	2.001
Double128Vector.ATAN	1024	avgt	10	136941.263	243.486	284024.53	2204.224	ns/op	2.074
Double128Vector.ATAN2	1024	avgt	10	163228.681	435.455	427589.587	3045.192	ns/op	2.62
Double128Vector.CBRT	1024	avgt	10	146395.753	239.355	317136.654	1330.869	ns/op	2.166
Double128Vector.COS	1024	avgt	10	154865.298	235.697	305721.518	1319.313	ns/op	1.974
Double128Vector.COSH	1024	avgt	10	189212.943	262.399	220756.27	61324.863	ns/op	1.167
Double128Vector.EXP	1024	avgt	10	113941.594	219.647	252853.07	891.272	ns/op	2.219
Double128Vector.EXPM1	1024	avgt	10	184552.939	513.715	254087.184	2144.997	ns/op	1.377
Double128Vector.HYPOT	1024	avgt	10	111580.194	423.282	374537.338	2091.811	ns/op	3.357
Double128Vector.LOG	1024	avgt	10	110680.548	192.731	265391.129	2653.519	ns/op	2.398
Double128Vector.LOG10	1024	avgt	10	116708.105	167.095	285764.405	2489.08	ns/op	2.449
Double128Vector.LOG1P	1024	avgt	10	115633.302	567.7	317235.967	1062.848	ns/op	2.743
Double128Vector.POW	1024	avgt	10	321655.14	36.55	560765.066	2669.33	ns/op	1.743
Double128Vector.SIN	1024	avgt	10	166240.988	512.253	287741.373	2089.286	ns/op	1.731
Double128Vector.SINH	1024	avgt	10	196233.614	225.88	221493.573	60941.438	ns/op	1.129
Double128Vector.TAN	1024	avgt	10	203347.384	267.385	372912.183	2093.675	ns/op	1.834

Eclipse IDE on linux-riscv64 (OpenJDK 24):

<https://download.eclipse.org/eclipse/downloads/index.html>



# Go community work update (2024/10/30)

1. Plugin support
  - a. no merge symbol #435015 [submit]
  - b. GOT\_PCREL\_ITYPE\_RELOC support #612635 [submit]
  - c. implement plugin mode #420114 [submit]
2. Vector instructions
  - a. opcode#595403 [merged]
  - b. register#595404 [merged]
  - c. codegen/runtime [plan]
3. Go runtime syscall with ABI internal
  - a. prerequisites: tools #620056 [merged]
  - b. runtime: #620755 [ready]
4. objdump
  - a. support disasm #622257 [merged]



# RuyiSDK (Xi Jing, PLCT)

- RuyiSDK [V0.20](#)
  - `ruyi self uninstall --purge` 不会遗留遥测数据了。
  - 修复了 `ruyi admin` 子命令无法被调用的问题。
  - 修复了 Ruyi 虚拟环境中, 向无 `target tuple` 前缀的命令 (如一系列 LLVM 工具) 的转发。
  - 移除了插件机制的 Starlark 沙箱。这有助于简化打包与降低开发门槛: 按照 RuyiSDK 当前的威胁模型 (threat model), 沙箱机制不会带来额外的安全性。
- 《从零开始开发VSCode插件与Ruyi IDE插件》[第2课](#)已经上线B站。
- [操作系统支持矩阵](#)
  - 新增:
    - VisionFive 2 / NetBSD
    - Duo 256M / Alpine, Arch Linux
    - Mango MQ Pro / NetBSD
    - Duo S / Arch Linux
    - Huashan Pi / buildroot
    - Milk-V Jupiter / Bianbu 1.0
    - CI 生成首页表格 SVG
  - 更新:
    - VisionFive 2 / Ubuntu: 24.04 LTS -> 24.04.1 LTS, 24.10
    - BPI-F3: typo fix
    - VisionFive 2 / openKylin: 2.0
    - PIC64GX / Ubuntu: 24.10
  - 此外, 我们为所有测试报告都添加了元数据, 方便后续与 `packages-index` 同步更新。

# openEuler RISC-V (周嘉诚)

Status / 20241031

- 🎉 openEuler 24.09 available now [[Dnld](#)]
- 🎉 24.09 Preview Release of oE LLVM Parallel Universe Project available now [[Dnld](#)]
- Following releases in 2H'24
  - Late Q4 - 24.03 follow-up community release for supporting more devices w/ vendor kernels, proprietary drivers, etc.
  - Late Q4. - 24.03 LTS Service Pack 1
- Fundamental packages in 24.03 LTS [[Full List](#)]
  - glibc 2.38, binutils 2.41, gcc 12.3.1, llvm 17.0.6
  - openjdk 8u402-b08 / 11.0.23 / 17.0.11 / 21.0.3
  - python 3.11.6, perl 5.38.0
  - golang 1.21.4, rust 1.77.0
- Features:
  - 6.6-based [common kernel](#) for Qemu, SG2042 (Pioneer) & TH1520 (LPi4A)
  - UEFI-supported Hardware & QEMU images
  - [Penglai TEE](#)-enabled firmware variants
- Images:
  - UEFI Install ISO for SG2042 (Pioneer)
    - Standard & Netinst variants available
  - UEFI qcow2 Image w/ [Penglai TEE](#)
  - Legacy-boot Images for Pioneer & LPi4A
  - *Other images coming in the next community release*

# Gentoo for RISC-V 的情况更新（Gentoo 小队）

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# Arch Linux RISC-V (Felix & PRZ)

- linux (regression): submit a new patch for the a0/ENOSYS issue  
<https://lore.kernel.org/linux-riscv/59505464-c84a-403d-972f-d4b2055eeaac@gmail.com/T/>
  - Follow up: after heated discussions with kernel devs, we realized that we have to make changes to UAPI
  - <https://github.com/torvalds/linux/blob/c1e939a21eb111a6d6067b38e8e04b8809b64c4e/arch/riscv/include/uapi/asm/ptrace.h#L24>
  - Palmer didn't add orig\_a0 into struct user\_regs\_struct at the very beginning. So, ptrace syscall that requires modifying a0 never worked, even prior to 4.x, where RISC-V still uses the old entry instead of the latest generic entry.
  - The only fix is to modify UAPI and add orig\_a0 into the user\_regs\_struct.
  - No need to bpo to 4.x because they will be EOL on Nov. 2024.
    - Downstream might need to fix this manually or just leave ptrace broken for some special corner cases

# Arch Linux RISC-V (Felix & PRZ) - Electron

- Electron 33 for riscv64 release:  
<https://github.com/riscv-forks/electron-riscv-releases/releases/tag/v33.0.0.riscv1>
  - <https://github.com/riscv-forks/electron/commit/34f1d404a9e25f2353e2c43d55e9657b5c817a1f>
  - Update the patches for chromium 130
  - Notably, pull latest chromium sandbox patch from gerrit
  - Upstreamed patches and not applicable patches are dropped.
- VSCodeium for RISC-V
  - Extension host throws exception "Named export 'rgPath' not found." on RISC-V64 (installed by Open Remote - SSH) [VSCodeium/vscodeium#2060](https://github.com/riscv-forks/vscodeium/issues/2060)
  - It turns out to be some kind of bug specifically in node.js 18 for RISC-V
  - Fixed by updating node.js to v20.16.0



# Fedora for RISC-V status update (20241030)

- **RPM packaging**

- Koji Status: Rawhide(F41), GA on Nov 12
- **F39: 98.59% srpm [stop]**
- **Rawhide/41: 23460/24320[96.46%] srpm**
- <https://www.fedoravforce.com>
- <https://images.fedoravforce.org>
- <https://upstream.fedoravforce.org>

- **main package version:**

- Toolchain: gcc-14.0.1-0.15.3, [glibc-2.40-4](#),  
binutils-2.43.1-3[up-to-date]
- [libffi-3.4.6-2\(up-to-date\)](#)
- [java-1.8.0-openjdk](#)
- [java-11-openjdk](#), [java-17-openjdk](#), [java-21-openjdk](#)
- [java-latest-openjdk](#)
- [perl-5.40.0-511\(up-to-date\)](#)
- [python3.13-3.13.0~rc1-3\(up-to-date\)](#)
- [llvm-19.1.0-1\(up-to-date\)](#)
- [golang-1.23.2-2\(up-to-date\)](#)
- [rust-1.81.0-6\(up-to-date\)](#)

- **Desktop support Fedora Rawhide:**

- **DONE:** XFCE/LXDE/LXQT/Cinnamon/Sway/Budgie  
/Sugar/GNOME/Mate
- **Testing:** KDE/Deepin
- **Key Desktop App**
  - **firefox-131.0-2[upstreamed]**
  - **libreoffice-24.8.2.1-1[upstreamed]**
  - **Thunderbird-115.11.1-1[DONE]**
  - **chromium-126.0.6478.182-2[DONE]**

- **Image :**

- <https://images.fedoravforce.com>
- <https://openkoji.iscas.ac.cn/pub/dist-repos/dl>
- <https://mirrors.iscas.ac.cn/fedora-riscv>
- [https://dl.fedoraproject.org/pub/alt/risc-v/fedora-r  
emix](https://dl.fedoraproject.org/pub/alt/risc-v/fedora-r<br/>emix)

- **ROS/ROS2 upgraded to F41**

- **[Sail](#) for rawhide[UPSTREAMING]**

- **function testing for F41:**

- **Podman[pass], Image: [fedora-rv64](#) (f41)**
- **Ceph[ONGOING]**
- **K8s[ONGOING]**

# Fedora 41 ON TH1520 WITH NEW KERNEL

```
Warning: skipped PGP checks for 125 packages from repository: fedora-riscv-koji
[root@fedora-riscv ~]#
[root@fedora-riscv ~]#
[root@fedora-riscv ~]# fastfetch

      .',;:::,,'.
    .':;cccccccccccccc;,,.
      .;cccccccccccccccccccccc;,.
    .:cccccccccccccccccccccccccc:.
      .;cccccccccccccc;.:dddl.:;cccccc;,.
    .:cccccccccccccc;OWMKOOXMWd;ccccccc:.
      .:cccccccccccccc;KMMc;cc;xMMc;ccccccc:.
    ,cccccccccccccc;MMM.;cc;;WW:;cccccccc,
      :cccccccccccccc;MMM.;cccccccccccccccc:
    :ccccccc;oxOOOo;MMM000k.;cccccccccccccc:
    ccccc;0MMKxdd;:MMmkddc.;cccccccccccccc;
    ccccc;XMO';cccc;MMM.;ccccccccccccccccccc'
    ccccc;MMo;cccc;MMW.;cccccccccccccccccc;
    ccccc;0MNC.ccc.xMMd;cccccccccccccccccc;
    ccccc;dnMWXXXWM0:;cccccccccccccccccc;,.
    ccccccc;.:odl.:;cccccccccccccccccc;,.
    ccccccccccccccccccccccccccccccccccc;'.
      :cccccccccccccccccccccccccc;,.
    ':cccccccccccccccccccccc;::,.
[root@fedora-riscv ~]#
```

# Debian for RISC-V(干波)

- Official port update

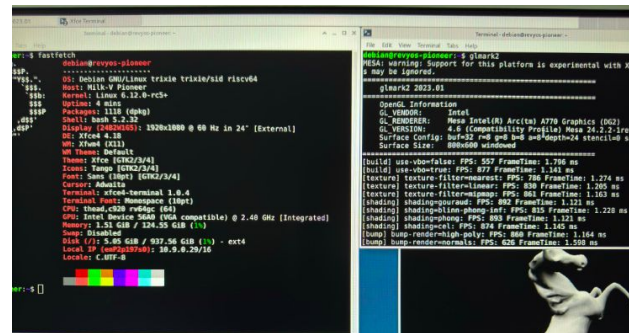
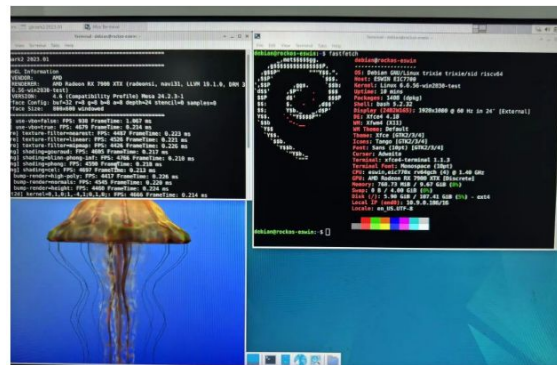
1. AMD 7900XTX running on Milk-v [Megrez](#)
2. Intel A770 running on milk-v [pioneer](#) with 6.12+rc5
3. [crossqa](#) support riscv64 on Debian

- debci

1. Replacing new licheepi cluster for riscv64 workers

- Some works

1. [pcr2](#) [backport commit], [eclipse](#) [testing package]
2. [zlog](#) [issue 1 2 3], strace[[repack](#) it]
- 3.chromium [130 [WIP](#)]



# RevyOS (程龙灿)

- New image (20241025)

- <https://mirror.iscas.ac.cn/revyos/extra/images/sg2042/20241025/>
- Kernel version: 6.6.46
- supported devices: Milk-V Pioneer / sg2042 evb / sg2042 evb2
- <https://mirror.iscas.ac.cn/revyos/extra/images/lpi4amain/test/>
- LicheePi4A6.6内核镜像正在测试中, 目前有测试版可用

- ROS2

- RevyOS 目前维护着两个ros发行版: Humble and Jazzy
- jazzy build 1109/1185 > 1200/1401 (93%)
- humble build 1384/1577 > 1138/1608 (88%)
- 仓库更新后 humble 的包有些库版本不对导致编译失败, 目前在重新编译
- <https://mirror.iscas.ac.cn/revyos/revyos-ros2/>
- ci测试情况:

pass: (39428/39496) > (39,312/39,568)

failed 146, skip 102 > 110

总计6.3h

# RevyOS supported devices

## [Image download directory](#)

- 1、LicheePi 4A
- 2、LicheePi Cluster 4A
- 3、beaglev-ahead
- 4、Milk-V Pioneer
- 5、Milk-V Meles
- 6、LicheeConsole4A
- 7、RISC-V Book
- 8、LicheeBook

## SD card support

- 1、LicheePi 4A
- 2、beaglev-ahead
- 3、Milk-V Meles
- 4、LicheeConsole4A

## Mainline support

- 1、LicheePi 4A
- 2、Milk-V Pioneer

# FW相关更新（王翔）

## ❖ opensbi

- platform添加香山，但并没有特别的驱动，可以通过devicetree和generic platform实现
- 修复sbi\_scratch.h中的一个typo

# RustSBI团队进展(洛佳)

- HAL 组(朱俊星)

- 为bouffalo-hal(BL808, etc)添加PSRAM支持:将读写错误率降低至0
- 为allwinner-hal添加SD/MMC支持:已完成
- 添加了SMHC外设和更新了其他外设
- 举办社区活动:两场RustSBI线上宣讲会 and Rust & RustSBI线下沙龙活动;组织参观Linux中国大会

- 发行版组(邢志昂)

- 解耦rustsbi原型系统实现与驱动,提高原型系统的可扩展性
- 加入了RISCV扩展探测机制,支持在无SSTC扩展环境下的timer实现
- 为香山nemu提供支持,实现以payload固件形式在香山nemu上引导
- 修复了若干错误

# RustSBI团队进展(洛佳)

- 大模型组(马铭芮)
  - 指定专业领域知识问答大模型实施方案, 分为L1阶段和L2阶段;同时落实了算力资源问题 / 洛佳、马铭芮
  - 针对RAG数据解析相关任务进行调研分析, 撰写阅读笔记与调研报告 / 张子涵、罗传杰
  - RAG demo实现并撰写论文阅读报告 / 任潇
  - 开源大模型能力调研, 分析与总结;大模型结核性调研(重点工作) / 邝嘉诺
- 受GOSIM大会邀请, 参加10月18日的嵌入式Rust分享, 演讲主题为《让我们试试RustSBI!》, 演讲人: 洛佳&董庆
- RustSBI 0.4.0版本发布





# 香山开源RISC-V处理器 - ICT / PCL

香山开源技术讨论群：  
879550595 (QQ)

- 功能

- 前端
  - 修复 ECC 到 Bus Error Unit 路径上的 Mux1H (#3784)
- 后端
  - 修复 H 拓展 gpa 获取不一致的问题以及修复 Mismatch 访问相关 TLB 的问题 (#3681, #3679)
  - 修复向量访问异常在写回时, 如果有更老的异常时, isEnqExcp 应置零的问题 (#3778)
  - 修复 ebreak 指令触发 breakpoint 异常时, 以及压缩指令发生非法指令异常时, xtval 更新错误的问题 (#3769, #3762), NEMU 也完成了对应修改 (#599)
  - 修复向量访问 trigger 相关问题 (#3772, #3745)
  - 修复 CSR 异常分开存储导致的错误拉高问题 (#3771)
  - 修复 xcause 的中断选择策略与 xtopi 不一致的问题 (#3753)
  - 修复 NEMU 在部分指令设置 xstatus.FS 为 Dirty 时的行为与 RTL 不一致的问题 (#606, #605, #598, #595, #591, #588)
  - 计数溢出和基于特权级的过滤拓展 (Sscofpmf): 添加 RTL 指导 NEMU overflow 更新, RTL 支持基于特权级的过滤 (#3771), NEMU 完成 mhpmevent 实现以及相应修改 (#574)
  - VS/S/M 模式双重陷入拓展 (Ss/mdltrp) 正在合入主线 (#3789)
  - NEMU 实现 A 拓展的 trigger 支持 (#592)
- 访存与缓存
  - CHI-L3: OpenLLC + OpenNCB 合入主线 (配置: KunminghuV2Config) (#3672)
  - 修复连续的两条 MMIO 访存, 均发生 non-data error 异常时导致的卡死问题 (#3728)
  - 修复对非对齐的 HLV(hypervisor load)指令进行拆分后, 丢失虚拟化相关信息的 Bug (#3759)
  - 修复未执行完毕一条非对齐指令前, StoreQueue 误提交该指令的 Bug (#3758)
  - 修复向量异常相关的 Bug, 保证向量访问指令在乱序执行后, 能够保留按顺序最早的一项异常 (#3733)
  - 修复由向量访存单元无法接收 uop 发射导致的卡死问题 (#3741)

- 时序

- 前端
  - FTQ -> FDIP 预取的时序优化 (#3499)
  - 将 io.flush 从预取的关键路径上移除 (#3542)
  - s2\_finish 到预取的时序优化 (#3545)
- 后端
  - 优化唤醒, 取消以及访存依赖时序 (#3737)
- 访存与缓存
  - MemBlock 内部和端口时序持续优化, 目前内部违例优化至 -45ps, 近期优化包括: 去除 Dcache s2tag 到 dataArray 之间的关键路径、优化 MemBlock 向 L2 Cache 发送 CMO 请求的时序、优化 LoadUnit 写回端口的选择逻辑, 以及非对齐访存的异常写回逻辑等 (#3748)

- 时序

- 对 DCache SRAM 添加 clock gating, memory 的内部功耗降低 51%



# Chisel and Additional Technology / Sequencer

- 提交人不在线
- 
- T1
  - 重构Mask Unit单元
  - 初始化FPGA仿真
  - 进一步后端评估
- Chisel
  - Scala3的初步支持
  - rocket-uncore 提供axi版本的统一-debug module plic aclint的支持

OpenHW & OpenHW Aisa Working Group

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# 甲辰计划进展(吴伟)

- **甲辰计划月度进展上线！**

- <https://github.com/rv2036/jiachen-monthly>
- 欢迎直接PR分享自己的 RISC-V工作进展！

- RISC-V开发板漂流继续欢乐地漂着

- 过去两周漂流了8次, 包括2次个人捐赠和6次申领

- 有1家企业新加入甲辰计划

- 在CNCC2024上宣传布道了甲辰计划(效果还没体现)

- 攻击型论文阅读小组无活动

- 「RISC-V芯片安全挑战赛」转由甲辰计划组织, ISCAS不再作为主办方

- 承办单位(拟): 中科微澜、苦芽科技

- 人才互认计划: 本次无新增

自由讨论 / AOB

BACKUP

# 准备加入更多的国际开源组织进行同步观测

欢迎追加或提议