

# 欢迎第一次加入的伙伴(开会时请从下一页开始展示)

- 开放编辑, 直接点击 request for edit 然后在东亚时区群里at吴伟
- 如果没有找到自己的内容分类, 可以添加1-2页在最开始或中间
- 欢迎在开始的前5分钟进行自我介绍
- 日常八卦在东亚时区RISC-V双周同步微信群中, 欢迎加入

# 东亚时区RISC-V双周会

2023年02月16日·第052次

<https://github.com/cnrv/RISCV-East-Asia-Biweekly-Sync>

Host: 史宁宁

Organizer: PLCT Lab [plct-oss@iscas.ac.cn](mailto:plct-oss@iscas.ac.cn)

## 会议议程(15:00 - 16:00)

- 自我介绍、等待参会者接入、非技术话题八卦(没有的话就直接跳过)
- RVI 的更新和八卦(基本上跟东亚双周会群内消息同步)
- Unratified Specs 的参考实现进展
- 东亚地区小伙伴的项目更新
- 自由讨论

# RISC-V International 同步、全球开源社区八卦

- 2月17日（明天）先楫半导体[发布新产品并举行线上生态讨论会](#)
- 3月2日，上海，平头哥主办「玄铁RISC-V生态大会」，[议程和报名入口](#)
- [RISC-V双周报（第53期-20230215）发布](#)
- RISC-V Summit Europe 定档6月初，在西班牙巴塞罗那，[演讲征集中](#)
- RISC-V Summit China 定档8月下旬，北京，3月上旬开始官宣
  - 今年线下，预期会有非常宏大的展区和参会规模
- RISC-V Summit North America 有可能提前到11月中旬（待定）
- 第一届 RISC-V HPC 学术workshop征集论文中，5月中旬跟ISC2023一起德国开
- RVA23 Profile 征集意见中（尚未进入 public review，成员可以评论）注意**V强制了**。
- 又一台RISC-V笔记本电脑宣布要制作和销售了，这次是大陆之外的企业
- 



RISC-V Summit Europe Barcelona



Monday-Friday

5-9 June 2023

# RISC-V 韩语社区的同步与八卦

- SiFive High Five Pro P550
  - RISC-V RV64GBC ISA
  - Intel Horse Creek SoC
    - SiFive RISC-V P550 quadcore at 2.2GHz
  - 16GB DDR5
  - 文档现在还没有，预计今年夏天出 [HiFive Pro P550 - SiFive](#)
- “三星电子急于开发Galaxy专用芯片”
  - 成立AP (Application Processor) 解决方案开发组，在MX (移动经验) 事业部下
    - 崔元俊 (高通出身)，李钟硕 (苹果搞cpu设计的)
  - Exynos 2200烂爆了，Galaxy S22发热、性能低下；Galaxy S23搭载骁龙82
    - 据预测Galaxy S23系列出厂价提高15万韩元左右 (八百rmb)
  - 去年第三季度从高通、联发科买AP支出的金额为8.1423万亿韩元，比去年同期(4.1032万亿韩元)增加了98.4%


# RISC-V 日语社区的同步与八卦

- NSITEXE 開発の 64bit RISC-V **Akaria NS72** (Vector 拡張有)
  - Users can quickly estimate execution performance with reasonable accuracy without FPGAs, emulators, etc
  - C and OpenCL interfaces are available
  - Domain Specific Accelerator based on NS72 will be released
  - VPU for vector operation
- RISC-Vの特徴とAArch64との比較
- 这个比较得很细, 可以看slides参考一下
- <https://docs.google.com/presentation/d/1dgPbZd6vYeW6PoKXOp0bHolb7AnJCqf7yxDA2VxYxvI/edit?usp=sharing>

# RISC-V 俄语社区的同步与八卦

Элпитех (Eliptech) компания首款基于48核Baikal-S CPU的产品上市

**Baikal-S. Готов и приятно удивляет**



**Для серверов и СХД**  
**Использованы лучшие ядра**  
**Успешно запущен с 1 раза**

**48 ядер**  
Arm Cortex-A75

**до 2,5 ГГц**  
частота

**от 1 до 4**  
сокетов

**120 Ватт**  
TDP

**Baikal-S: бенчмарки**

	Baikal-S 2,0 ГГц	Intel Xeon Gold 6148 2,4 ГГц	Kunpeng 920 2,6 ГГц
SPEC CPU 2006 int, 1 core	19	n/a	26
Coremark, all cores	650 000+	455 000	945 000
Whetstone, all cores	230 000+	162 500	210 000
7zip, all cores decompress	108 000	97 000	119 000
HPLinpack, GFLOPs	230+	1126	298

**Baikal-S в сравнении с прямыми конкурентами**



**1x Intel Xeon Gold 6148**  
20x Skylake  
2,4 ГГц

**1x AMD EPYC 7351**  
16x Zen 1  
2,9 ГГц

**0,85x Huawei Kunpeng 920**  
48x Armv8.2  
2,6 ГГц

# Zvfhmin extension - 陆旭凡

- The Zvfhmin extension provides minimal support for vectors of IEEE 754-2008 binary16 values
- the **vfwcvt.f.f.v** and **vfncvt.f.f.w** instructions become defined when SEW=16
- The Zvfhmin extension depends on the Zve32f extension.



## Zvfh extension - 陆旭凡

- **Vector Floating-Point Instructions, Vector Single-Width Floating-Point Reduction Instructions, Vector Widening Floating-Point Reduction Instructions, Vector Floating-Point Move Instruction, Vector Floating-Point Slide1up Instruction, and Vector Floating-Point Slide1down Instruction** become defined when SEW=16.
- Additionally, conversions between 8-bit integers and binary16 values are provided. The floating-point-to-integer narrowing conversions (**vfncvt[.rtz].x[u].f.w**) and integer-to-floating-point widening conversions (**fwcvt.f.x[u].v**) become defined when SEW=8.
- The Zvfh extension depends on the Zve32f and Zfhmin extensions.

# AOSP for RISC-V - 汪辰、陆旭凡

- Google AOSP upstream PR
  - Android (RISC-V) Review 双周报 第 10 期 (in Chinese): <https://zhuanlan.zhihu.com/p/606739609>
    - Google 自己新做了一个和 riscv 有关的库: [berberis](#) 这是 Google 新发起的一个小项目, 还不是很成熟, 假如你手上没有合适的 riscv 的开发板硬件, 希望在 x86 的机器上测试你的 app 程序, 可以使用这个库来将 riscv 的机器指令翻译成 x86 的机器指令。具体参考邮件列表: [https://lists.riscv.org/g/sig-android/topic/who\\_know\\_what\\_s\\_this\\_repo\\_in/96978347](https://lists.riscv.org/g/sig-android/topic/who_know_what_s_this_repo_in/96978347)
    - 目前看上去 cuttlefish 的 kernel crash 问题算是解决了, 采用了一个相对临时的方法绕开在 machine mode 下通过 u-boot 启动 kernel (会 crash 但是很难调试), 所以使用 opensbi 在 s-mode 下启动 u-boot 再引导 kernel。采用该方式后不发生 crash。需要找个时间来测试一下。TBD
  - [Add riscv64 support to the linker relocation benchmark.]  
<<https://android-review.googlesource.com/c/platform/bionic/+2302559>> merged
  - 一月份 RVI Android SIG 会议跳过一次
- RVI Android SIG upstream:
  - Chromium for Android apk 从 93/96 升级到 109.0.5414.87: working
- 技术文章
  - 笔记: Clang for Chromium 构建分析: <https://zhuanlan.zhihu.com/p/602554347>

# RISC-V GCC进展

GCC upstream已合入了大量RVV intrinsic支持, 遵循最新的RVV intrinsic doc

<https://gcc.gnu.org/git/?p=gcc.git&a=search&h=HEAD&st=author&s=juzhe>

<https://github.com/riscv-non-isa/rvv-intrinsic-doc>

廖仕华重构了k扩展的gcc实现, 已向gcc upstream重新提交了patch

<https://gcc.gnu.org/pipermail/gcc-patches/2023-February/611871.html>

Binutils 2.40将用.insn替代原有的.byte, 来更清晰的描述反汇编中未识别的指令

Christoph计划成立Intrinsic工作组, 用来讨论RISC-V Intrinsic API的制定

OpenHW申请批准Xcvalu扩展, 用来支持特定的算数 逻辑运算操作

<https://github.com/riscv-non-isa/riscv-toolchain-conventions/pull/29>

RISC-V GNU toolchain双周会slides链接:

[https://docs.google.com/presentation/d/18jhHGE0leG3tsaH8-KtHBFqdySzPpcxYAwVS0Uj6del/edit#slide=id.g207178cced1\\_0\\_0](https://docs.google.com/presentation/d/18jhHGE0leG3tsaH8-KtHBFqdySzPpcxYAwVS0Uj6del/edit#slide=id.g207178cced1_0_0)

<https://docs.google.com/document/d/1JSs-BSIPJ3QYbAb-Add1TlbYx0nOT1ur3jcsITIJ01U/edit#heading=h.c0d80mdpqcl5>

# Clang/LLVM 进展 (PLCT)

- Gollvm 合并了一个patch, 还有两个patch在路上
  - 修改 CallingConvId , <https://go-review.googlesource.com/c/gollvm/+427737>
- Upstream, 大部分时间在解决套娃regression
  - [RISCV] Permit tail call to an externally-defined function with weak linkage  
<https://reviews.llvm.org/D143137>
  - [RISCV] Enable preferZeroCompareBranch to optimize branch on zero in codegenprepare,  
<https://reviews.llvm.org/D142071>
  - [RISCV] Return false from shouldFormOverflowOp <https://reviews.llvm.org/D143646>
  - . . .
  - 小队更多patch没来得及收集, 下次展示

# Clang / LLVM 社区的更新 (廖春玉、陆旭凡)

1. D143641 [MemorySSA] Iteratively check if gep's pointer operand is a guaranteed loop invariant
2. D142687 [Local] Don't keep K's range even if K dominates J
3. D142801 [Local][InstCombine][GVN] Handle !noundef metadata in combineMetadata
4. D142234 [ConstantRange] Handle `Intrinsic::ctlz`

# QEMU/Spike/Sail/ACT进展 (PLCT)

- Qemu
  - Zc\* 更新
    - <https://lists.gnu.org/archive/html/qemu-riscv/2023-02/msg00187.html>
  - 浮点相关fix以及Zve64d, Zvfh{min} 支持
    - <https://lists.gnu.org/archive/html/qemu-riscv/2023-02/msg00375.html>
  - Svadu扩展支持
    - <https://github.com/plctlab/plct-qemu/tree/plct-svadu-dev>
- Spike
  - 可写misa相关fix
    - <https://github.com/riscv-software-src/riscv-isa-sim/pull/1250>
  - Zc\*更新
    - <https://github.com/riscv-software-src/riscv-isa-sim/pull/1251>

## gem5 进展 (PLCT)

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# V8 for RISC-V 更新(邱吉、陆亚涵)

## 常规上游更新Port

1. 4252497: [riscv] Remove duplicate declaration in regexp macro assembler | <https://chromium-review.googlesource.com/c/v8/v8/+4252497>
2. 4204830: [riscv] Fix atomics | <https://chromium-review.googlesource.com/c/v8/v8/+4204830>
3. 4243114: [riscv32]Fix regress-1412940 DCHECK failed. | <https://chromium-review.googlesource.com/c/v8/v8/+4243114>
4. 4237943: [riscv][regexp] Add a frame marker for irregexp frames | <https://chromium-review.googlesource.com/c/v8/v8/+4237943>
5. 4242224: [riscv][regexp] Fix stack iteration when -fomit-frame-pointer is enabled | <https://chromium-review.googlesource.com/c/v8/v8/+4242224>

## 优化指针加载常数的指令数量, 采用LLVM的递归算法

1. 4230306: [riscv] Optimize constant immediate load with a recursive function | <https://chromium-review.googlesource.com/c/v8/v8/+4230306>



# Spidermonkey for RISC-V更新（邱吉、陆亚涵）

1. Port Patch  
<https://phabricator.services.mozilla.com/D167901>
2. 优化常数加载的指令数目  
<https://phabricator.services.mozilla.com/D169770>

# OpenJDK for RISC-V 更新(RV64及upstream) 杨飞

## 1. Authored jdk-mainline PRs:

- <https://github.com/openjdk/jdk/pull/12176> (8301033: RISC-V: Handle special cases for Minl/Maxl nodes for Zbb)
- <https://github.com/openjdk/jdk/pull/12177> (8301036: RISC-V: Factor out functions baseOffset & baseOffset32 from MacroAssembler)

## 2. Reviewed jdk-mainline PRs:

- <https://github.com/openjdk/jdk/pull/12247> (8301067: RISC-V: better error message when reporting unsupported satp modes)
- <https://github.com/openjdk/jdk/pull/12219> (8301153: RISC-V: pipeline class for several instructions is not set correctly)
- <https://github.com/openjdk/jdk/pull/12295> (8301313: RISC-V: C2: assert(false) failed: bad AD file due to missing match rule)
- <https://github.com/openjdk/jdk/pull/12379> (8301628: RISC-V: c2 fix pipeline class for several instructions)
- <https://github.com/openjdk/jdk/pull/12402> (8301743: RISC-V: Add InlineSkippedInstructionsCounter to post-call nops)
- <https://github.com/openjdk/jdk/pull/12401> (8301740: RISC-V: Address::uses() should check address mode)

## 3. Generational-ZGC RISC-V Port:

- Merged to ZGC development repo: <https://github.com/openjdk/zgc/pull/10>
- TODO: Add support for RVV extension
- TODO: Optimize with Bitmanip extension

## 4. 17u/11u/8u backport staging repos are ready:

- <https://github.com/openjdk/riscv-port-jdk17u>
- <https://github.com/openjdk/riscv-port-jdk11u>
- <https://github.com/openjdk/riscv-port-jdk8u>

Seeded with jdk{17, 11, 8}u-dev repos respectively.

# OpenJDK for RISC-V 更新(RV32/PLCT 史宁宁)

1. improve the object code in generate\_call\_stub

<https://github.com/openjdk-riscv/jdk11u/pull/585>

2. Changed the 'java function register(caller-save registers)'

<https://github.com/openjdk-riscv/jdk11u/pull/588>

3. Fix the loadL according the arm 32bit

<https://github.com/openjdk-riscv/jdk11u/pull/589>

4. 将C2分支和解释器分支都做了一次回归测试, 修正了个别问题

测试用例库: <https://github.com/openjdk-riscv/testcase-jdk11u-rv32g>

# OpenJDK for RISC-V 更新(RV64及upstream) 张定立

## Merged & New JDK-mainline PRs:

- <https://github.com/openjdk/jdk/pull/12401> | (8301740: RISC-V: Address::uses() should check address mode)
- <https://github.com/openjdk/jdk/pull/12434> | (8301852: RISC-V: Optimize class atomic when order is memory\_order\_relaxed)
- <https://github.com/openjdk/jdk/pull/12553> | (8302453: RISC-V: Add support for small width vector operations)(as co-author)

## Articles update (in Chinese):

- <https://zhuanlan.zhihu.com/p/604060721> | (在docker中构建meta-riscv并使用特定版本的qemu和linux内核)

# OpenJDK for RISC-V 更新(RV64及upstream) 曹贵

## Merged & New JDK-mainline PRs:

- <https://github.com/openjdk/jdk/pull/12379> | (8301628: RISC-V: c2 fix pipeline class for several instructions)
- <https://github.com/openjdk/jdk/pull/12425> | (8301818: RISC-V: Factor out function mvw from MacroAssembler)
- <https://github.com/openjdk/jdk/pull/12525> | (8302289: RISC-V: Use bgez instruction in arraycopy\_simple\_check when possible)
- <https://github.com/openjdk/jdk/pull/12553> | (8302453: RISCV: Add support for small width vector operations)

# OpenJDK8 backporting (章翔)

## 1、javac调试

- [Fix do\\_oop\\_store by using do\\_oop\\_store\\_rv for includeClassFile error](#)
- [Fix do\\_oop\\_load by using load\\_heap\\_oop\\_rv for MethodHandles adapters](#)
- [Fix additional based on pr262 & pr263](#)
- [Delete some code about lea in assembler\\_riscv64](#)
- [Fix do\\_oop\\_store on fast\\_storefield](#)

## 2、openEuler调试

- [Fix some errors about include](#)
- [Fix errors about include in openEuler](#)
- [Fix sa-jdi.jar for openEuler](#)

3、benchmark测试结果: [SPECjvm2008测试记录](#) · (通过率:68.4%) [dacapo测试通过率](#) (通过率:64.2%)

# openEuler RISC-V

- PR(24个)
  - [bpfttrace : 将riscv64加入支持的架构](#) @laokz
  - [etcd : 在支持的架构中增加 riscv64](#) @laokz
  - [gawk : backport上游补丁修复 riscv上测试错误](#) @laokz
  - [libaio : 修正原有补丁的架构隔离 错误](#) @laokz
  - [libffi : 修复 riscv架构上测试错误](#) @laokz
  - [libffi : 修复测试失败](#) @laokz
  - [mpich : 重新应用中间仓补丁](#) @laokz
  - [node\\_exporter : 增加riscv架构支持](#) @laokz
  - [oneDNN : 将riscv64加入支持的架构](#) @laokz
  - [samba : 将2203Next已合入的 riscv修改提交到 2203sp1](#) @laokz
  - [systemtap : 应用上游补丁修复 gcc12兼容性问题](#) @laokz
  - [clang : Upgrade to 15.0.7](#) @jchzhou
  - [llvm : Upgrade to 15.0.7](#) @jchzhou
  - [compiler-rt : Upgrade to 15.0.7](#) @jchzhou
  - [lldb : Upgrade to 15.0.7](#) @jchzhou
  - [lxc : Add patch to fix RISC-V build errors](#) @misaka00251
  - [NetworkManager-fortisslvpn : Init package](#) @misaka00251
  - [NetworkManager-iodine : Init package](#) @misaka00251
  - [NetworkManager-openconnect : Init package](#) @misaka00251
  - [NetworkManager-openvpn : Init package](#) @misaka00251
  - [NetworkManager-ssh : Init package](#) @misaka00251
  - [NetworkManager-vpnc : Init package](#) @misaka00251
  - [xfce4-appfinder : Revert avoid saving duplicate command changes](#) @misaka00251
  - [x264 : 升级 master 分支, 修复构建 错误](#) @Jingwiw
  - [risc-v-kernel : Backport make mmap\(\) with PROT\\_WRITE implied PROT\\_READ](#) @xingmz

- 镜像:

- [openEuler RISC-V image for VisionFive v2 \(2203v2vf2\)](#)
- [WIP] openEuler 23.03创新版启动:完成构建工程 创建
  - <https://build.tarsier-infra.com/project/show/openEuler:23.03> 4300
  - <https://build.tarsier-infra.com/project/show/openEuler:23.03:Epol> 1234

# Gentoo for RISC-V 的情况更新 (Gentoo 小队)

- Support statistics (8086/19090, 42.36%) : <https://whale.plctlab.org/riscv/support-statistics/>
- A total of 67 keywording commits: <https://whale.plctlab.org/riscv/RISC-V-双周会/20230216/commits.txt>
  - dev-util/pwntools: Keyword 4.10.0\_beta0-r2 riscv
  - sys-cluster/mpich: Keyword 3.4.3 riscv
  - x11-misc/shutter: keyword shutter-0.99.2 riscv
- T-head xuantie-gnu-toolchain as Gentoo native toolchain
  - The V vector extension has been tested on qemu-user mode
  - <https://github.com/peeweep/xuantie-gnu-toolchain-overlay>
  - <https://github.com/peeweep/gentoo/commits/xuantie-gnu-toolchain-V2.6.1>
  - WIP: working on getting T-head kernel (<https://github.com/t-head-Semi/linux/>) working on Lichee RV Dock (XuanTie C906 Chip)
- libreoffice is working, tested on 7.5.0.3 (need to version bump to 7.5.1.1 and test again)
  - <https://bugs.gentoo.org/881389>



# Arch Linux RISC-V (东东、潘瑞哲)

[ Arch Linux RISC-V Bi-Week Package  
Update Stats Report ]

Report generated on: 20230216

Package update count: 1429

Distinct package update count: 1231

[core] 255 / 262 (97.32%)

[extra] 2868 / 3092 (92.75%)

[community] 8943 / 10026 (89.19%)

**stackoverflow can't be correctly caught inside of  
qemu user:**

[https://github.com/felixonmars/archriscv-packages/issues/  
2192](https://github.com/felixonmars/archriscv-packages/issues/2192)

Highlight packages:

glibc - 2.36-7 --> 2.37-2.1

firefox - 108.0.2-1 --> 109.0.1-1

rust - 1:1.66.1-2.1 --> 1:1.67.1-1

rust-analyzer - 20230130-1 --> 20230213-1

racket - 8.7-2 --> 8.8-1

docker - 1:20.10.23-1 --> 1:23.0.1-1

docker-compose - 2.15.1-1.1 --> 2.16.0-1

mariadb - 10.9.4-2 --> 10.10.3-1

harfbuzz - 6.0.0-1 --> 7.0.0-1

mesa - 22.3.3-3 --> 22.3.4-1

qt5-wayland - 5.15.8+kde+r57-1 --> 5.15.8+kde+r58-1

kwayland - 5.102.0-1 --> 5.103.0-1

imagemagick - 7.1.0.60-1 --> 7.1.0.62-1

telegram-desktop - 4.5.3-1 --> 4.6.1-1

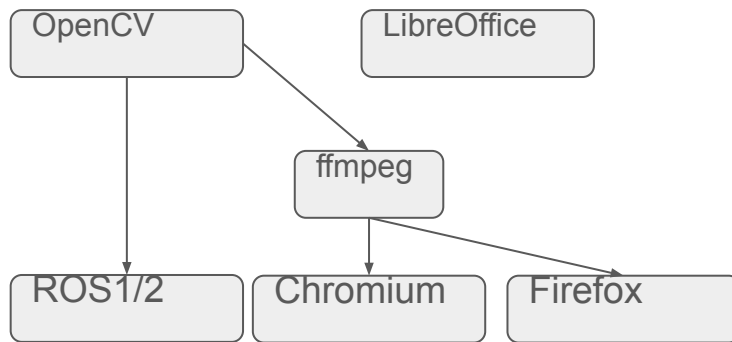
kotlin - 1.8.0-1 --> 1.8.10-1

git - 2.39.1-1 --> 2.39.2-1

[chromium](#) - 104.0.5112.101-1 -> 110.0.5481.77-2

# Fedora for RISC-V (傅炜)

- RPM packaging
  - Status: Fedora 37, then upgrade to Rawhide
  - REPO: 16600+ (72%) srpm have been built.
- main package version:
  - Toolchain(up-to-date)
    - gcc-12.2.1-4 --> gcc-13[on going]
    - glibc-2.36-9
    - Binutils 2.38-25[F37] --> 3 2.39-3[rawhide]
  - libffi-3.4.3-1.1(up-to-date)
  - java-latest-openjdk-19.0.1.0.10-3(up-to-date)
  - perl-5.36.0-492(up-to-date)
  - Python 3.11.1(up-to-date)
  - LLVM/Clang 15.0.7-1(up-to-date)
  - Go 1.19.4-1(up-to-date)
  - Rust 1.66.0-1(up-to-date)
  - [mingw-w64-tools upstream](#)



- Images:
  - [QEMU](#) Builder, XFCE, GNOME
  - Sophgo Server(SG2042)

# Debian for RISC-V(I) (于波)

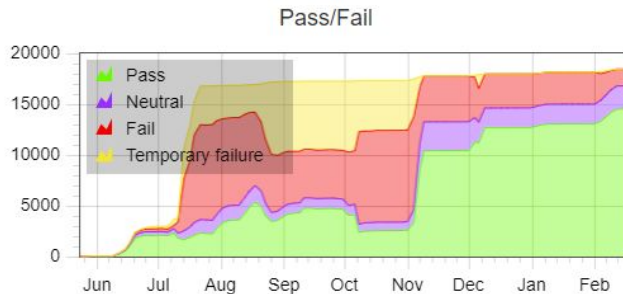
- [Build status&news](#)

1. Installed(sid): [15720+](#)
2. [Udd FTBFS packages](#) ~217 (+20)
3. More Unmatched boards found, but it takes time to happened.

- [Debci update](#)

[Britney's Job Hostory](#)

- Some works



1. <https://github.com/prody/ProDy/issues/1594> [help to test]
2. <https://lists.debian.org/debian-ocaml-maint/2023/02/msg00240.html> [help to fix OCaml-\* ftbfs on build]

# Debian for RISC-V(II)

- 3\*. [https://salsa.debian.org/go-team/compiler/golang/-/merge\\_requests/11](https://salsa.debian.org/go-team/compiler/golang/-/merge_requests/11) [workaround for golang 1.20 on rv64 ] -> [https://gcc.gnu.org/bugzilla/show\\_bug.cgi?id=105870](https://gcc.gnu.org/bugzilla/show_bug.cgi?id=105870) [gcc 12 issue]
- 4. <https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1031203> [fix gawk ftbfs]
- 5. <https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1031225> [a2jmidid RFS team done]
- 7\*. <https://github.com/yuzibo/diff-debian-build> [0.1 release]
- 8\*. <https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1031257> [genparse RFS QA done]

# Deepin for RISCV

stage2:

succeeded: 5331

failed: 140

unresolvable: 1088

<https://build.tarsier-infra.com/project/show/home:revy:deepin-riscv-stage2>

Deepin 发布了alpha2 后续进行软件同步

<https://community-packages.deepin.com/beige/>

其他更新参加tarsier月报deepin部分

<https://github.com/isrc-cas/tarsier-monthly/blob/main/004-20230201.md#deepin>

# FW相关更新（王翔）

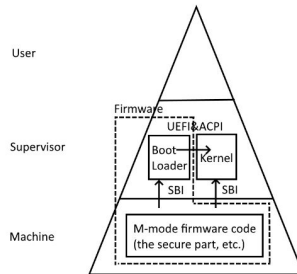
- opensbi
  - AE350的HSM扩展添加深度睡眠支持。
  - 对HSM代码进行整理, 并添加系统休眠扩展。
  - 因为C99支持true/false, 所以替换调代码中的TRUE/FALSE。
  - 把SBI分为RW/RX的两个段。
  - 添加optee支持(当前问题: 缺少规格、使用保留扩展号等)。
  - rzfive的LID/DLM映射的内存, 防止低特区等级访问添加到root domain并设置权限。
  - rzfive添加PMA支持并添加厂商扩展扩展。
  - 在初始化和休眠时, 不能清除整个MIP(意外清除MEIP/SEIP外部中断可能引起中断不被响应), 修改为只清除软件中断MSIP/SSIP。
  - 修复之前把内存权限拆分为M/SU的错误(把保留内存权限设置为SU)。
  - 修复\_fw\_rw\_offset的问题。
  - 合并fdt中的保留内存(地址相同大小不同)防止占用太多MP。
  - 添加大小端转换的支持。
  - 优化tlb和ipi, 尽快把ipi信息传递出去, 消除tlb队列满后的等待。
  - SBI debug console(DBCN)扩展合并到主线
  - DBCN的puts最终可能由sbi\_putc或console\_puts实现, sbi\_putc会在\n之前添加\r, 而console\_puts不会, 添加代码支持。但是会打破原本的非阻塞写, 已经尽可能减少阻塞
- u-boot
  - u-boot有32核心限制, 之前提交的代码在重新review
  - u-boot当前使用的sbi0.1, ipi核心数限制在xlen, 提交代码修正

# 固件相关更新(洛佳)

- RustSBI 0.3.1版本现已发布(<https://github.com/rustsbi/rustsbi>)
  - 修复了若干依赖问题, 包括使用riscv crate的0.10版本。其它的都是一些文档的小修复
- RustSBI开发教程正在编写中
  - 介绍如何从零开发一个使用RustSBI的SBI固件, 期望揭开固件黑盒的面纱, 帮助未来的SBI开发者实现自己的固件。教程是从以前酝酿的“教育版RustSBI”和其它计划中发展出来的
  - 链接: <https://github.com/rustsbi/rustsbi-tutorial/>
- RISC-V PRS小组会讨论SBI、UEFI与ACPI同时实现的特权级模型
  - UEFI、LinuxBoot等位于固件生态的S特权层, 这与操作系统内核的特权层相同
  - 在任何条件下都应当存在SBI
  - 与会成员讨论认为模型与目前实现的一致性较好, 接下来应讨论兼容引导规范等细致问题
- SBI DBCN调试扩展
  - 很精简, 设计思想较好, 通过的概率比较大
- RustSBI原型设计系统的未来发展
  - 提供固件接口或简化的支持接口, 为LinuxBoot、UEFI等引导阶段提供环境准备

## Coexistence of UEFI, ACPI and SBI

- UEFI and ACPI can serve on S-mode, the same mode as the kernel
- We can refer to ARM EL3 for a proper M-mode secure firmware architecture
- LinuxBoot solutions may handle low-power peripheral in kernel driver instead of ACPI, acting as bootloaders
- ACPI can be included in implementation of a S-mode bootloader, other than a M-mode firmware
  - (Should SBI CPPC extension be defined in ACPI standard other than SBI standard?)



\* LinuxBoot solutions not shown in this figure

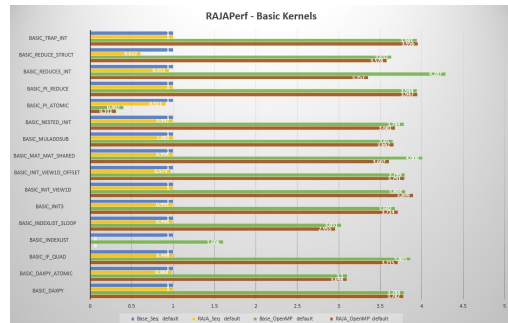
# RISCV性能跟踪小队 - 陈小欧

- Run benchmarks on Visionfive v1. Performance data comparing D1, unleashed, unmatched, visionfive v1 is shown in the table below:

		D1 (1core 1GHz)	Unleashed(4cores 1.5GHz)	Unmatched (4cores 1.4GHz)	Visionfive (2cores 1.0GHz)
INT	Dhrystone	833 DMIPS	706 DMIPS	1176 DMIPS	979 DMIPS
	CoreMark	2237	8506	12363	6495
	Linpack	91.2 MFLOPS	91.0 MFLOPS	99 MFLOPS	99 MFLOPS
FP	Whetstone	909 MIPS	610 MIPS	649 MIPS	645 MIPS
	FPMark(MultiCore)	-	-	4240	2326

(single-core tests: Dhrystone, Linpack, Whetstone. Multi-core tests: Whetstone, FPMark) Unmatched and Visionfive use the same CPU core (U74). The difference is that Unmatched is quad-core, and Visionfive is dual-core. It can also be seen from the multi-core performance measured by CoreMark and FPMark that Unmatched is almost twice that of Visionfive. The single-core integer performance of Visionfive is slightly lower than that of Unmatched, and the single-core floating-point performance is basically the same. (For details, please refer to <https://zhuanlan.zhihu.com/p/599418843>)

- Run HPC Benchmarks on Unmatched: RAJAperf、ExCALIBUR、Sombrero  
<https://zhuanlan.zhihu.com/p/606800441>



```
BabelStream
Version: 4.0
Implementation: OpenMP
Running kernels 100 times
Precision: double
Array size: 268.4 MB (=0.3 GB)
Total size: 805.3 MB (=0.8 GB)
Function  MBytes/sec  Min (sec)  Max  Average
Copy      1126.516    0.47658    0.49552  0.48006
Mul        1000.311    0.53670    0.55211  0.53997
Add        1087.773    0.74033    0.76730  0.74616
Triad      1085.774    0.74169    0.75780  0.74613
Dot        1315.404    0.40814    0.41559  0.41060
```



# 香山开源RISC-V处理器 - ICT / PCL

- 南湖架构修复最后的 SRAM 半频问题和 FPU 的 Bug, 进入后端流程
- 
- 昆明湖进展
  - 前端: FDIP 初步可用; 修复新版设计中 ICACHE multi-hit 问题
  - 后端: 推进乱序流水线的重构工作; 完成向量指令拆分单元对首条指令的支持
  - 访存: 推进 LQ 拆分工作; 设计了 L2 - L1 之间的自定义 Hint Channel, 用于优化 load miss latency
  - 缓存: 成功通过 tl-test 测试框架在双核下的测试; 新缓存接入南湖版香山, 运行 workload 进行测试
- 
- 新增常量注入工具 Constantine, 允许仿真器运行前修改RTL内常数值而无需重新编译

# MLIR 结合 RISC-V 相关工作 - 张洪滨

[Backend] Add gemmini instructions. -

<https://github.com/buddy-compiler/buddy-mlir/commit/c5a7a162abfe9daed034086a226c7ad1f0d78321>

[RVV] Add Rsqrt operation -

<https://github.com/buddy-compiler/buddy-mlir/commit/b3e86a6c19c270a806fe9da313c0de0183ba97e7>

[examples][MLIRVector] improve vector dialect examples for mask creation and casting -

<https://github.com/buddy-compiler/buddy-mlir/commit/8470d9e135d72ae196879047b6b461123bab1f37>

[examples][MLIRVector] improve vector dialect examples for element access -

<https://github.com/buddy-compiler/buddy-mlir/commit/aa5f1ada5e2be19fab172ee4ae6d2033c10a9780>

Restrict vector.type\_cast to only cast to aligned multi-dim vectors - <https://reviews.llvm.org/D142280>

**WIP:**

[examples][DLModel] Add e2e case for ResNet18 on RISC-V - <https://github.com/buddy-compiler/buddy-mlir/pull/118>

[examples][MLIRVector] improve vector dialect examples for memory access -

<https://github.com/buddy-compiler/buddy-mlir/pull/107>

MLIR dialect for gemmini instructions.

# Chisel and Additional Technology / Sequencer

- Vector
  - More tests to pass
  - Pass all in this month
  - Donate to chipsalliance after documentation
- Chips Alliance
  - <https://github.com/chipsalliance/tilelink>
    - The official tilelink implementation repo
    - WIP on BFM and RTL for crossbar
  - <https://github.com/chipsalliance/rocket-chip>
    - Start to actively development (dev branch)
  - Chisel is working on Chisel 5
    - Wait for next master branch.
  - Managements:
    - Congrats to @ZenithalHourlyRate becoming the rocket-chip developer!
    - @sequencer is able to delete chisel3/RC now?(granted to be organization owner)
- ASIC
  - PLL schematic done
    - Simulating!!!
  - Serdes
    - Digital FPGA prototype worked!
    - Linking in ASIC
    - Analog design is stall
      - Pushing
  - Vector core PnR

# OpenHW & OpenHW Aisa Working Group

# 自由讨论 / AOB

- PLCT实验室低调的公布了2023路线图：
  - <https://github.com/plctlab/PLCT-Weekly/blob/master/PLCT-Roadmap-2023.md>
-

BACKUP

# 准备加入更多的国际开源组织进行同步观测

欢迎追加或提议

