# 东亚时区RISC-V双周会

2024年11月28日·第 92 次

https://github.com/cnrv/RISCV-East-Asia-Biweekly-Sync

Host: 邱吉

Organizer: PLCT Lab <u>plct-oss@iscas.ac.cn</u>

## 会议议程(15:00 - 16:00)

- 自我介绍、等待参会者接入、非技术话题八卦(没有的话就直接跳过)
- RVI 的更新和八卦(基本上跟东亚双周会群内消息同步)
- Unratified Specs 的参考实现进展
- 东亚地区小伙伴的项目更新
- 自由讨论

### RISC-V International 同步、全球开源社区八卦(陈逸轩)

- <u>Openchip、NEC 和巴塞罗那超级计算中心</u>研究合作开发下一代基于 RISC-V的 超级计算机
- RISC-V for HPC at SC24
- 一生一芯在 sig-academia-training work group进行<u>交流分享</u>

### RISC-V 中文社区的同步与八卦(张宇溪)

#### 新产品及技术

- 赛昉联合国芯推出高性能AI MCU芯片, 实现RISC-V+AI新应用
- 深度数智DC-ROMA RISC-V Laptop II
- RustVMM 官方支持 RISC-V
- RISC-V 第一次硬件虚拟化, Milk-V Megrez 为您奉上
- 全国产自主可控车规MCU发布!使用RISC-V内核,进入动力安全域应用

#### 生态

- RISC-V软件共建平台——"如意RISC-V社区"重磅发布
- <u>"RISC-V松竹梅计划"在2024 世界互联网大会乌镇峰会开源生态发展论坛正式发</u> <u>布</u>
- RDI生态·成都创新论坛·2024 | 奕斯伟计算携手合作伙伴再拓RDI应用示范场景

### RISC-V 德语社区的同步与八卦(罗云翔)

Future of computing conference 2024 <a href="https://www.future-of-computing.com/conference/">https://www.future-of-computing.com/conference/</a> Munich Urban Colab December 11, 2024, 2 – 9 pm

Keynote by Tenstorrent, on Open vs Close: The Beauty of Open Source and RISC-V as the Next CPU Solution of Choice

#### Codasip

- Cosmic Compute at the RISC-V Summit North America Hackathon
- codasip 开源 Lockstep sail fork

#### IEEE

- Special Session: Software-Based Self-Test Generation for RISC-V Stuck-At Generation, Functional Cell-Aware Untestability, and FPGA Demonstration
  - University of Freiburg, Freiburg, Germany
- An Automated and Effective Approach for SBST Generation Targeting RISC-V CPUs Infineon Technologies AG, Germany
- Special Session: A Mixed Simulation-, Emulation-, and Formal-Based Fault Analysis Methodology for RISC-V Infineon Technologies AG, Germany
- AMPER-X: Adaptive Mixed-Precision RISC-V Core for Embedded Applications Technische Universität Dresden, Germany
- RV-ProViler: Evaluating RISC-V ISA for Application-Specific Requirements
  Technische Universität Dresden, Dresden, Germany
- Automated Intrinsic Support for ISA Extensions: Enhancing Software Generation for RISC-V and Beyond Infineon Technologies AG, Germany

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续上次双周会, 德国RISC-V论文数量相对于10月前(发表7月前)明显增多

#### ☐ Special Session: Software-Base **Functional Cell-Aware Untestal** Tobias Faller; Nikolaos I. Deligiannis; R 2024 IEEE International Symposium or Year: 2024 | Conference Paper | Publ ∨ Abstract HTML 1 (C) An Automated and Effective A Endri Kaia: Nicolas Gerlin: Jad Al Halak 2024 IEEE International Symposium or Year: 2024 | Conference Paper | Publ ✓ Abstract HTML D C Special Session: A Mixed Simul Methodology for RISC-V Endri Kaia: Nicolas Gerlin: Ares Tahirac 2024 IEEE International Symposium or Year: 2024 | Conference Paper | Publ ✓ Abstract HTML 💆 © □ AMPER-X: Adaptive Mixed-Pre Ahmad Othman; Ahmed Kamaleldin; I □ RV-ProViler: Evaluating RISC-V 2024 IEEE Nordic Circuits and Systems Year: 2024 | Conference Paper | Publ ✓ Abstract HTML M © Automated Intrinsic Support for RISC-V and Beyond Mayuri Bhadra; Stephanie Ecker; Danie 2024 IEEE Nordic Circuits and Systems Year: 2024 | Conference Paper | Publ ∨ Abstract HTML M (C) □ Hardware-accelerated Compre Year: 2024 | Conference Paper | Publ ✓ Abstract HTML 1 © Processor Vulnerability Detecti 2024 IEEE Nordic Circuits and Systems Year: 2024 | Conference Paper | Publ ∨ Abstract HTML (C) RISC-V Triplet: Tapeouts for Se Jonas Schupp: Patrick Karl: Jens Nöpel 2024 IEEE Nordic Circuits and Systems Year: 2024 | Conference Paper | Publ ∨ Abstract HTML 💆 ©

 Rapid Prototyping Platform fo Jonas Mair: Sabitha Kusuma: Daniel Li

### GCC 进展

Supports Zicfiss and Zicfilp extension

https://gcc.gnu.org/pipermail/gcc-patches/2024-November/668918.html

Supports RV64ILP32 ABI feature

https://gcc.gnu.org/pipermail/gcc-patches/2024-November/669046.html

Updated the riscv-gnu-toolchain release CI

https://github.com/riscv-collab/riscv-gnu-toolchain/releases/tag/2024.11.22

Supports Xsf vendor extension

https://sourceware.org/git/?p=binutils-gdb.git;a=commit;h=595e49a4b7c6769ef23a2573148db 72872c61935

• Supports Svvptc and Smdbltrp extension

https://gcc.gnu.org/pipermail/gcc-patches/2024-November/669684.html

## Clang/LLVM 进展 (PLCT)

- [RISCV] Inline Assembly Support for GPR Pairs ('R') #112983
   <a href="https://github.com/llvm/llvm-project/pull/112983">https://github.com/llvm/llvm-project/pull/112983</a>
- [RISCV] Support \_\_builtin\_cpu\_is #116231
   <a href="https://github.com/llvm/llvm-project/pull/116231">https://github.com/llvm/llvm-project/pull/116231</a>
- [RISCV] Intrinsic Support for XCVsimd
   https://github.com/realqhc/llvm-project/commit/8fa72399a1cacb24b977c1
   ad0ac184bf34c7f17c
- [flang] Add new intrinsic function backtrace and complete the TODO of abort #117603
   <a href="https://github.com/llvm/llvm-project/pull/117603">https://github.com/llvm/llvm-project/pull/117603</a>

## Sail/ACT进展 (PLCT)

- Remove pc alignment mask
   <a href="https://github.com/riscv/sail-riscv/pull/618">https://github.com/riscv/sail-riscv/pull/618</a>
- Make mstatus[VS] dirty when write to vstart
   <a href="https://github.com/riscv/sail-riscv/pull/623">https://github.com/riscv/sail-riscv/pull/623</a>
- Remove vector of bools in vext
   <a href="https://github.com/riscv/sail-riscv/pull/622">https://github.com/riscv/sail-riscv/pull/622</a>
- (Codasip) Support static compilation of the emulator
  - https://github.com/riscv/sail-riscv/pull/626

- CTG tests are not reproducible
   <a href="https://github.com/riscv-non-isa/riscv-arch-test/pull/570">https://github.com/riscv-non-isa/riscv-arch-test/pull/570</a>
- [CTG] Add new cli param '--filter'
   <a href="https://github.com/riscv-non-isa/riscv-arch-test/pull/571">https://github.com/riscv-non-isa/riscv-arch-test/pull/571</a>
- Update RV64I sra, sraw test cases
   <a href="https://github.com/riscv-non-isa/riscv-arch-test/pull/565">https://github.com/riscv-non-isa/riscv-arch-test/pull/565</a>
- (10x-Engineers)ACTs and coverage points for machine mode software and timer interrupts
   https://github.com/riscv-non-isa/riscv-arch-test/pull/567

### V8 for RISC-V 更新(邱吉、陆亚涵)

- 1. 6047416: [riscv][wasm][cfi] Enable the WasmCodePointerTable by default | <a href="https://chromium-review.googlesource.com/c/v8/v8/+/6047416">https://chromium-review.googlesource.com/c/v8/v8/+/6047416</a>
- 2. 6028869: [riscv][wasm][cfi] Pass WritableJitAllocation into JumpTableAssembler | <a href="https://chromium-review.googlesource.com/c/v8/v8/+/6028869">https://chromium-review.googlesource.com/c/v8/v8/+/6028869</a>
- 3. 6015659: [riscv][wasm] Hardcode jump table instruction bytes on RISCV | https://chromium-review.googlesource.com/c/v8/v8/+/6015659
- 4. 6000166: [riscv] mksnapshot ignores cpu extensions when generating builtins code | https://chromium-review.googlesource.com/c/v8/v8/+/6000166 by yuri.gaevsky@syntacore.com
- 5. 6034521: Reland "[riscv] Enable extension on builtins" | https://chromium-review.googlesource.com/c/v8/v8/+/6034521
- 6. 6027486: [riscv] Fix build failed for native | https://chromium-review.googlesource.com/c/v8/v8/+/6027486

## OpenJDK for RISC-V (PLCT 杨飞)

#### 1 Reviewed JDK-mainline PRs:

- https://github.com/openjdk/jdk/pull/21975 (8343774: Positive list platforms for ir checks of compiler/c2/TestCastX2NotProcessedIGVN.java)
- https://github.com/openjdk/jdk/pull/21957 (8343767: Enumerate StubGen blobs, stubs and entries and generate code from declarations)
- https://github.com/openidk/jdk/pull/21885 (8343555: RISC-V: make some verified (on hardware) extension options diagnostic)
- https://github.com/openjdk/jdk/pull/21922 (8342881: RISC-V: secondary super cache does not scale well: C1 and interpreter)
- https://github.com/openidk/idk/pull/21974 (8343827: RISC-V: set AlignVector as false if applicable to enable SLP)
- https://github.com/openidk/idk/pull/22102 (8334474: RISC-V: verify perf of ExpandBits/CompressBits (rvv))
- https://github.com/openidk/jdk/pull/22130 (8344265: RISC-V: Remove unused function get previous sp entry)
- https://qithub.com/openidk/jdk/pull/22149 (8344010: RISC-V: Zacas do not work with LW locking)
- https://github.com/openidk/idk/pull/22293 (8344382: RISC-V: CASandCAEwithNegExpected fails with Zacas)
- https://github.com/openidk/jdk/pull/22203 (8344387: RISC-V: C2: Improve encoding of LoadNKlass for compact headers)
- https://github.com/openidk/idk/pull/22264 (8344526: RISC-V: implement -XX:+VerifvActivationFrameSize)
- https://github.com/openidk/idk/pull/22363 (8344960: RISC-V: fix TestFloatConversionsVectorNaN for COH and AlignVector)
- https://github.com/openjdk/jdk/pull/22386 (8344306: RISC-V: Add zicond)

#### **JDK 24**

This release will be the Reference Implementation of version 24 of the Java SE Platform, as specified by JSR 399 in the Java Community Process

The main line is open for bug fixes, small enhancements, and JEPs as proposed and tracked via the IEP Process.

#### Schedule

2025/03/18

2024/12/05 Rampdown Phase One (branch from main line) 2025/01/16 Rampdown Phase Two 2025/02/06 Initial Release Candidate 2025/02/20 Final Release Candidate

#### Features

General Availability 404: Generational Shenandoah (Experimental)

450: Compact Object Headers (Experimental) 472: Prepare to Restrict the Use of INI

475: Late Barrier Expansion for G1

478: Key Derivation Function API (Preview)

479: Remove the Windows 32-bit x86 Port

483: Ahead-of-Time Class Loading & Linking

484: Class-File API

486: Permanently Disable the Security Manager

487: Scoped Values (Fourth Preview)

488: Primitive Types in Patterns, instanceof, and switch (Second Preview)

489: Vector API (Ninth Incubator) 490: ZGC: Remove the Non-Generational Mode

491: Synchronize Virtual Threads without Pinning

492: Flexible Constructor Bodies (Third Preview)

493: Linking Run-Time Images without IMODs

494: Module Import Declarations (Second Preview) 495: Simple Source Files and Instance Main Methods (Fourth Preview)

496: Quantum-Resistant Module-Lattice-Based Key Encapsulation Mechanism

497: Quantum-Resistant Module-Lattice-Based Digital Signature Algorithm 498: Warn upon Use of Memory-Access Methods in sun.misc.Unsafe

499: Structured Concurrency (Fourth Preview) 501: Deprecate the 32-bit x86 Port for Removal

#### 4.1. Instruction sequences

Operation	Instruction sequence
Conditional add, if zero rd = (rc == 0) ? (rs1 + rs2) : rs1	czero.nez rd, rs2, rc add rd, rs1, rd
Conditional add, if non-zero rd = (rc != 0) ? (rs1 + rs2) : rs1	czero.eqz rd, rs2, rc add rd, rs1, rd
Conditional subtract, if zero rd = (rc == 0) ? (rs1 - rs2) : rs1	czero.nez rd, rs2, rc sub rd, rs1, rd
Conditional subtract, if non-zero rd = (rc != 0) ? (rs1 - rs2) : rs1	czero.eqz rd, rs2, rc sub rd, rs1, rd
Conditional bitwise-or, if zero rd = (rc == 0) ? (rs1   rs2) : rs1	czero.nez rd, rs2, rc or rd, rs1, rd
Conditional bitwise-or, if non-zero rd = (rc != 0) ? (rs1   rs2) : rs1	czero.eqz rd, rs2, rc or rd, rs1, rd
Conditional bitwise-xor, if zero rd = (rc == 0) ? (rs1 ^ rs2) : rs1	czero.nez rd, rs2, rc xor rd, rs1, rd
Conditional bitwise-xor, if non-zero rd = (rc != 0) ? (rs1 ^ rs2) : rs1	czero.eqz rd, rs2, rc xor rd, rs1, rd
Conditional bitwise-and, if zero rd = (rc == 0) ? (rs1 & rs2) : rs1	and rd, rs1, rs2 czero.eqz rtmp, rs1, rc or rd, rd, rtmp
Conditional bitwise-and, if non-zero rd = (rc != 0) ? (rs1 & rs2) : rs1	and rd, rs1, rs2 czero.nez rtmp, rs1, rc or rd, rd, rtmp
Conditional select, if zero rd = (rc == 0) ? rs1 : rs2	czero.nez rd, rs1, rc czero.eqz rtmp, rs2, rc or rd, rd, rtmp
Conditional select, if non-zero rd = (rc != 0) ? rs1 : rs2	czero.eqz rd, rs1, rc czero.nez rtmp, rs2, rc or rd, rtmp



### Go community work update (2024/11/28)

- Vector instructions
  - cmd/internal/obj/riscv: update references to RISC-V specification #631935 [reviewed]
  - cmd/internal/obj/riscv: rework instruction encoding information #622535 [merged]
  - codegen
    - cmd/internal/obj/riscv: implement vector configuration setting instructions #631936 [reviewed]
    - cmd/internal/obj/riscv: implement vector load/store instructions #631937 [reviewed]
  - runtime [plan]
- Go runtime syscall with ABI internal
  - o prerequisites: tools #620056 [merged]
  - runtime: #620755 [merged]
- Misc
  - internal/bytealg: optimize IndexByte for riscv64 #561275 [merged]



## RuyiSDK (Xi Jing, PLCT)

- Ruy i SDK <u>V0. 22</u>
  - 新增了 RuyiSDK 的平台支持文档, 基于此完善了 RuyiSDK 包管理器的平台兼容性
    - 将 Python 版本的最低要求降至 3.10, 以与 Ubuntu 22.04 LTS 系统默认 Python 版本保持兼容。
    - 降低了各种 Python 依赖关系的版本要求, 以支持与 Ubuntu 22.04 LTS 系统提供软件包配合工作。
    - 按照 Python 打包标准,新增声明 ruyi 入口点,以便发行版打包机制自动识别、处理。
- "探路 Eclipse RISC-V 插件开发"系列<u>学习日志</u>及<u>视频</u> 更新,欢迎更多的人加入到 Eclipse RISC-V 插件的学习和开发。
- 操作系统支持矩阵
  - Duo/Duo 256M Alpine, FreeRTOS, openEuler, Fedora, Ubuntu: <u>ruyisdk/support-matrix#99</u>
  - Duo Fedora: <u>ruyisdk/support-matrix#100</u>
  - Duo OpenWrt/Yocto: <u>ruyisdk/support-matrix#102</u>
  - LPi4A & Pioneer Box Firefox 的可用性观测报告: https://github.com/QA-Team-lo/firefox\_test
  - Milk-V Duo 系列的 RT-Thread / Smart 测试: https://github.com/QA-Team-lo/rttest
- 完成 Milkv Duo 官方SDK 的验证及缺陷总结,为后续SDK优化做准备。
  - Milkv Duo/Duo 256M/DuoS 缺陷更新

详见RuyiSDK双周进展报告: https://github.com/ruyisdk/wechat-articles

## openEuler RISC-V (周嘉诚)

#### Status / 20241128

- oE 24.03 SP1: finishing building on OBS, moving to Eulermaker for rebuilding, testing and release
  - Everything: 4810/4846 (99%)
  - Epol: 1210/1283 (95%)
- oE LLVM Parallel 24.03 SP1:
  - evaluating 'RVA22+V' equiv. march[1] (with oE clang 17.0.6) and linking with mold
- Pkgs & HW
  - Cloud-hypervisor: enabling linux VM on RISC-V
  - VF2: evaluating booting thru 'bootstd' w/ mainline uboot & self-service FW auto-upgrading
- Following releases in 2H'24
  - Late Q4 24.03 follow-up community release for supporting more devices w/ vendor kernels, proprietary drivers, etc.
  - Late Q4. 24.03 LTS Service Pack 1

#### Features:

- 6.6-based <u>common kernel</u> for Qemu, SG2042 (Pioneer) & TH1520 (LPi4A)
- UEFI-supported Hardware & QEMU images
- Penglai TEE-enabled firmware variants

#### mages:

- UEFI Install ISO for SG2042 (Pioneer)
  - Standard & Netinst variants available
- UEFI qcow2 Image w/ Penglai TEE
- Legacy-boot Images for Pioneer & LPi4A
- Other images coming in the next community release
- 1. rv64gcv\_zicbom\_zicbop\_zicboz\_zicsr\_zihintpause\_zihpm\_zmmul\_zfhmin\_zba\_zbb\_zbs\_zkt

## Arch Linux RISC-V (Felix & PRZ)

- Package update count: 1399
- Distinct package update count: 1229
- [core] 259 / 264 (98.11%)
- [extra] 13635 / 14028 (97.2%)
- •
- Highlight packages:
- firefox 132.0.2-1 --> 133.0-1
- mariadb 11.5.2-1 --> 11.6.2-2
- electron32 32.2.2-1 --> 32.2.3-1
- mesa 1:24.2.6-1 --> 1:24.2.7-1
- imagemagick 7.1.1.40-1 --> 7.1.1.41-1
- git 2.47.0-1 --> 2.47.1-1

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Chromium 131.0.6778.69-1

Disabled the download of pgo profiles because we cannot patch gsutils which is downloaded and executed on the fly. The pgo profiles are useless anyway, due to chrome\_pgo\_phase=0.

Replaced std::hardware\_destructive\_interference\_size with 64 because clang18 doesn't support this on riscv64. Can be dropped once clang19 is ready.

Added riscv-chromium-variations-130.patch to fix a crash.

Added a patch for ffmpeg to fix linking problem regarding PIC. See: <a href="https://trac.ffmpeg.org/ticket/11302">https://trac.ffmpeg.org/ticket/11302</a>. This has been fixed on ffmpeg master.

## Fedora for RISC-V status update (20241128)

get\_filename\_component: Fix REALPA
.. after symlink (!10025)

- RPM packaging
  - Koji Status: Rawhide(F41), GA on Nov 12
    - Rawhide/41: 23460/24320[96.46%] srprn
    - 738 rpm will fail to install
  - https://www.fedoravforce.com
  - https://images.fedoravforce.org
  - https://upstream.fedoravforce.org
- main package version:
  - Toolchain: gcc-14.2.1-3, glibc-2.40-4, binutils-2.43.1-3[up-to-date]
  - o libffi-3.4.6-3(up-to-date)
  - java-1.8.0-openjdk
  - o java-11-openjdk,java-17-openjdk,java-21-openjdk
  - java-latest-openjdk(up-to-date)
  - o perl-5.40.0-511(up-to-date)
  - o python3.13-3.13.0-1(up-to-date)
  - Ilvm-19.1.0-1(up-to-date)
  - o golang-1.23.3-1(up-to-date)
  - o rust-1.82.0-1(up-to-date)

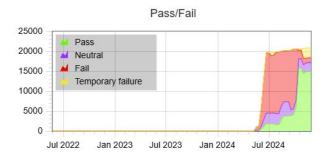
- Desktop support Fedora Rawhide:
  - DONE: XFCE/LXDE/LXQT/Cinnamon/Sway/Budgie /Sugar/GNOME/Mate
  - Testing: KDE/Deepin
  - Key Desktop App
    - o firefox-131.0-2[upstreamed]
      - libreoffice-24.8.3.2-2[upstreamed]
      - Thunderbird-115.11.1-1[DONE]
      - o chromium-126.0.6478.182-2[DONE]
- Image :
  - https://images.fedoravforce.com
  - https://openkoji.iscas.ac.cn/pub/dist-repos/dl
  - https://mirrors.iscas.ac.cn/fedora-riscv
  - https://dl.fedoraproject.org/pub/alt/risc-v/fedora-r emix
- ROS/ROS2 upgraded to F41
- <u>Sail</u> for rawhide[UPSTREAMING]
- function testing for F41:
  - Podman[pass], Image: fedora-rv64(f41)
  - Ceph[ONGOING]
  - K8s[ONGOING]

### Debian for RISC-V(于波)

- Official port update
  - 1. Python 3.13 <u>transition</u> in progress
  - 2. Debian sid image on k1
- Debci
  - 1. Mirrors issue
  - 2. <u>Drop</u> some rv64 workers
- Some works
  - 1. luajit [build on <u>rv64</u>], eclipse [release <u>testing</u>], linksem [<u>done</u>]
  - 2. strace [fix ftbfs], pygalmesh [ftbfs done], python-libais [fix ftbfs]
  - 3. python-softplayer [new <u>release</u>]



testing/riscv64



### RevyOS (程龙灿)

image

- A new image for Lichee Pi 4A is expected to be released next month. th1520-linux-kernel
  - **GPU-related fixes**
- Code synchronization for SDK 2.0.2
- Fixes for HDMI-related issues
- Sq2042-vendor-kernel

  - Optimizations in memory management and I/O performance
  - Updates to hardware-related configurations 0

jazzy build 1239/1401 > 1303/1401 (88%)

humble build 1474/1654 > 1477/1654 (89%)

Resolved some issues related to hardware interactions 0

RevyOS maintains two ROS2 distributions: Humble and Jazzy.

- ROS2
- - 0
  - 0
    - 0

    - 0
    - CI test results:
    - Pass: (39,312/39,568) > (39,323/39,578)

      - ailed: 145, Skipped:110
    - - Total time: 6.3 hours

- 1. LicheePi 4A
- 2, beaglev-ahead

RevyOS supported devices

Image download directory

2, LicheePi Cluster 4A

1. LicheePi 4A

3, beagley-ahead

4, Milk-V Pioneer

5. Milk-V Meles

7. RISC-V Book

SD card support

8. LicheeBook

6. LicheeConsole4A

- 3. Milk-V Meles

- 4. LicheeConsole4A
- Mainline support
- 1, LicheePi 4A

- 2. Milk-V Pioneer

## Sophgo Linux Upstream Status Update(汪辰)

https://github.com/sophgo/linux/wiki [Last updated: Nov/27/2024]

#### CV18XX Series

 DTS part for PinCtrl/SARADC/LicheeRV Nano is now on master for targeting v6.13-rc1

#### SG2042

- Key Poweroff support is now on master for targeting v6.13-rc1
- MSI Controller support patchset v1 was submitted
- PCIe Controller support patchset v1 was submitted

## RT-Thread (RISC-V) Upstream Status Update(汪辰)

- [libcpu]riscv使用call指令解决长跳转问题: <a href="https://github.com/RT-Thread/rt-thread/pull/9652">https://github.com/RT-Thread/rt-thread/pull/9652</a>
- [libcpu][riscv]纠正pv\_offset的对齐检查:
- bsp: qemu-virt64-riscv: Improve README: <a href="https://github.com/RT-Thread/rt-thread/pull/9651">https://github.com/RT-Thread/rt-thread/pull/9651</a>
- [bsp][qemu-virt64-riscv]:remove the redundant UART1 configuration: <a href="https://github.com/RT-Thread/rt-thread/pull/9680">https://github.com/RT-Thread/rt-thread/pull/9680</a>
- <a href="https://github.com/RT-Thread/rt-thread/pull/9679">https://github.com/RT-Thread/rt-thread/pull/9679</a>
- [bsp][cvitek]support milkv-duo rt-smart:
   <a href="https://github.com/RT-Thread/rt-thread/pull/9657">https://github.com/RT-Thread/rt-thread/pull/9657</a>
- bsp: cvitek: support mouting rootfs during bootup for RT-smart.: <a href="https://github.com/RT-Thread/rt-thread/pull/9703">https://github.com/RT-Thread/rt-thread/pull/9703</a>

### Box64 RISC-V 进展

- 用 RVV 和 XTheadVector 实现了 MMX 指令
- SIMD 指令优化
  - PSLL\*, PSRL\*
  - PUNPCK\*
- 改进 TSO 模拟性能
  - 重做 STRONGMEM 机制, 减少栅栏指令数量
- Benchmark
  - 对比扩展指令集对 DBT 性能的影响

### FW相关更新 (王翔)

#### opensbi

- 修正makefile中的grep命令,解决一些平台下的兼容性 问题
- 把carry数组修改成const并以null结尾
- 移除驱动初始化的重复代码,之前的每一个驱动都需要扫描dt调用初始化方法,把 这部分合并 了
- fwft在热启动时清除配置锁定的标志位.
- 实现sbi3.0中的pmu增强功能,添加一个ecall获取event信息,允许更多的比特位用来编码平台raw event
- 修复sse中的一些错误,修正一个编码范围错误,和一个event注入时的参数传递错误

## RustSBI团队进展(洛佳)

- HAL组(朱俊星)
  - 为bouffalo-hal(BL808, etc)添加PSRAM初始化功能
  - 为bouffaloader(BL808, etc)添加TF卡初始化与文件加载功能: 扫描TF卡加载DTB
    和bootargs.txt文件, 以启动TF卡内的Linux内核
  - 提供命令行界面,支持引导程序的基本调试功能,增加reload、read/write、print、 bootargs、boot命令
  - 添加FWFT 扩展支持的 SBI 实现
- 发行版组(邢志昂)
  - 重构prototyper启动逻辑和设备树解析逻辑, 支持使用 PMP 保护 prototyper
  - 为 prototyper 提供可重定向代码支持
  - 增加了 FreeBSD 的支持文档
  - 修复一些 bug

## RustSBI团队进展(洛佳)

- 大模型组(马铭芮)
  - 实现了对 PDF 文档的向量化存储功能和文档的分块与检索,集成了 Qwen 作为 Embedding 模型进行检索和 Gemma2 作为生成模型进行回答的生成,并建立了 用户交互界面/张子涵
  - 调研了系统面向领域的现存文档范围与格式,进行了文档解析部分的优化,实现了对 LaTeX、AsciiDoc 等格式的解析支持/任潇
  - 针对组内建立的 RAG 系统进行了不同开源模型测试和系统故障排查,解决了系统 在解析流程中存在的部分逻辑问题/邝嘉诺

#### others

- 举办社区活动:三场 RustSBI 在线分享会
- 我们将在华中科技大学 (HUST) 举办 WHLUG 线下社区活动, 详情见以下链接 https://mp.weixin.qq.com/s/EzOkwHnDTPH7-Qr10DdBKg

## 香山开源RISC-V处理器 - ICT / PCL(提交人不在线)

香山开源技术讨论群:

879550595 (QQ)

#### 功能

前端

■ BPU s2 fire 赋值修复 (#3850)

- 修复 xstatus.FS 关闭时 C 扩展 fp 指令报异常时 xtval 的值不正确的问题 (#3859)
- 不允许顺序取指跨越 MMIO/非MMIO边界 (#3873)
- 修复 H 扩展取指 Guest Page Fault 时 gpaddr 不正确的问题 (#3795)
- 修复支持 Zcb 后剩余 16b 空间指令异常时 xtval 的值不正确的问题 (#3886)
- L1 ICache 校验出错时从 L2 重新取指 (#3899)

#### ○ 后端

- 修复 dret 返回到机器模式时,未清除虚拟特权级标志位 (#3898)
- 修复 vstval 在访存 trigger 触发 breakpoint 异常时没有正确更新 (#3875)
- 修复 fround/fcvtmod.w.d 指令实现问题 (#3816)
- 修复 vnclip 立即数是无符号数问题 (#3894)
- 修复 vlbusytable 向量浮点与整数混淆的问题 (#3909)
- 修复 critical-error 信号传递过早导致 difftest 比对失败 (#3885)
- 修复 flh/fsh 在 fs 关闭的时候应当报非法指令异常的问题 (#3841)
- 修复 ase64ks1i 保留位未报非法指令异常的问题 (#3845)
- 修复大量 NEMU 模拟器与 RTL 未对齐的问题 (#669, #667, #666, #665, #664)
- 调试模式完成 dcsr 剩余字段 stopcount, stoptime, nmip, certig, extcause 设计
- 支持 critical error 进入 debug 模式 (#3786)
- 完善 spike 对 smrnmi/dbltrp 拓展的支持 (#3870)
- 在 verilog 代码中插入编译所用 RTL 版本的 commitID 信息 (#3818)

#### 功能

访存与缓存

- 修复 NEMU 在虚拟化 G-stage 翻译中 GVPNi 生成逻辑错误, 导致根页表的物理地址计算错误的 Bug(NEMU #673)
- 修复前端取指出现 guest page fault 时, gpaddr 生成逻辑错误的 Bug(#3871)
- 修复 load 指令首次进入 LoadQueueReplay 且需 redirect 时 , engMask 的生成逻辑(#3884)
- 实现完成支持 uncache outstanding 的初版 RTL 代码, 正在完善自测用例并进行测试(#3900)
- 在 RTL 和 NEMU 中为验证 DCache ECC 添加硬件故障注入指令 (#3923), 正在本地 AM 环境中进行测试
- 完成 RTL 和 NEMU 对 pointer masking(Ssnpm + Smnpm + Smmpm)扩展的支持, 正在整理代码准备合入主线(XiangShan #3921, NEMU #677)

#### PPA优化

- 前端
- BPU 动态时钟门控率优化 (#3579, #3670)
  - 增加 SRAM 时钟门控, 前端功耗降低 10% (#3889)
- 后端
  - 完成去除 dispatch queue 的新版分派算法, 正在评估性能
  - 评估裁剪浮点乘加流水线条数后的性能
- ) 访存与缓存
  - MemBlock 优化 ECC 校验相关的关键路径, 优化时序违例 -54ps -> -40ps (#3908)
  - 为 DCache SRAM 添加门控, MemBlock 总功耗降低 23.38% (#3824)
  - 优化 L1 TLB 中寄存器多份复制导致的面积冗余, 优化后 L1 TLB 面积降低约 24% (#3903)
  - DCache 容量不变的同时由 8-way 改为 4-way (#3849)
  - Directory 中合并 tagArray 与 eccArray (#3902)
  - 删除 MemBlock 中冗余的信号/逻辑以优化面积 (#3560)

# Chisel and Additional Technology / Sequencer(提交人不在线)

- Chisel
  - AutoBlackbox (#4495)
  - CIRCTSRAMInterface (<u>#4494</u>) Memory Replacement
- T1
  - Performance benchmark 254x to K1, 0.8x to KP920
  - Benchmark from DLEN128 to DLEN1024

## 自由讨论 / AOB

# **BACKUP**

## 准备加入更多的国际开源组织进行同步观测

欢迎追加或提议