

# 欢迎第一次加入的伙伴(开会时请从下一页开始展示)

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- 欢迎在开始的前5分钟进行自我介绍
- 日常八卦在东亚时区RISC-V双周同步微信群中, 欢迎加入
- 东亚时区Slides会公开到  
: <https://github.com/cnrv/RISCV-East-Asia-Biweekly-Sync/tree/main/biweekly-meetings>仓库, 并且默认了CC协议

# 东亚时区RISC-V双周会

2025年05月15日·第 102 次

<https://github.com/cnrv/RISCV-East-Asia-Biweekly-Sync>

Host: 郑俊杰

Organizer: PLCT Lab [plct-oss@iscas.ac.cn](mailto:plct-oss@iscas.ac.cn)

# 会议议程(15:00 - 17:00)

- 自我介绍、等待参会者接入、非技术话题八卦(没有的话就直接跳过)
- RVI 的更新和八卦(基本上跟东亚双周会群内消息同步)
- 东亚地区小伙伴的项目更新
- 自由讨论

# RVI 的更新和八卦

# RISC-V International 同步、全球开源社区八卦(陈逸轩)

[tech-p-ext] SIMD TG委员会选举结束, Rich Fuhler当选主席, Jiawei Chen当选副主席。

[sig-perf-analysis] 性能分析sig开始举办主席和副主席选举。

[tech-attached-matrix-extension] 中国移动提案[复数矩阵](#)

[sig-fp] Nicolas Brunie当选主席

[sig-hpc] Nick Brown当选主席, Teresa Cervero当选副主席

# RISC-V 中文社区的同步与八卦(聂雨婷)

1. [Vitalik Buterin提议用RISC-V替换EVM\(币圈大事件\)](#)
2. [Ubuntu官方支持OrangePI RV2](#)
3. [进迭时空携手珠海共建RISC-V生态应用中心、苏州市RISC-V开源芯片产业创新中心启动](#)
4. [跃昉科技顺利完成B轮融资，融资总金额超2亿元人民币](#)
5. [乐鑫ESP32-C5全面量产：行业首款双频Wi-Fi 6的RISC-V SoC](#)
6. [太好玩啦！在Excel里面跑一个RISC-V](#)
7. [【第一轮预热】首届RISC-V高水平大赛即将开启！](#)

zkVM	ISA	team
Boojum 2.0	RISC-V	MatterLabs
Ceno	RISC-V	Scroll
Euclid	RISC-V	Scroll
[redacted] NEW	Lean4	[redacted]
Jolt	RISC-V	a16z
Keith	Cairo	Kakarot
Nexus zkVM 3.0	RISC-V	Nexus
o1VM	RISC-V	O(1) Labs
OpenVM	RISC-V	Axiom
Pico	RISC-V	Brevis
powdrVM	RISC-V	powdr
R0VM	RISC-V	RISC Zero
SP1	RISC-V	Succinct
[redacted] NEW	RISC-V	[redacted]
Valida	Valida ISA	Lita
[redacted] NEW	[redacted]	[redacted]
ZisK	RISC-V	Hermez
zkMIPS	MIPS	ZKM
zkWASM	WASM	Delphinus

# RISC-V 韩语社区的同步与八卦

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# RISC-V 德语社区的同步与八卦(罗云翔)

参加2025年 RISC-V 欧洲峰会的德国厂商



The image shows a wide view of the exhibition hall with multiple booths. In the foreground, there is a large display board for Codasip. Behind it, other booths are visible, including one for Siemens with a "RISC-V Core for Edge AI Applications" poster, one for Infineon with a "CVA6 Core for Edge AI Applications" poster, and one for Lauterbach Development Tools. The hall has a modern design with a high ceiling and bright lighting.

**Codasip**

**Customized RISC-V in a simple game console**

**Island Poster Number**  
2.1 08

**Automating RISC-V Custom Instruction leveraging High-Level Synthesis**

**Background**

Performance requirements for system-on-chips (SoCs) have increased significantly over the last years. System-on-chip (SoC) designers are facing challenges in meeting these requirements while maintaining low power consumption and fast time-to-market.

**High-level Synthesis**

→ High-level IP: RISC-V's support of various instruction sets (e.g., RISC-V, VLIW, SIMD, etc.) allows for a wide range of customization options. This can be achieved by using different synthesis tools or by manually defining custom instructions.

→ Verification & Validation: Using a formal verification approach, such as model checking, can help ensure that the synthesized code meets the specified requirements. This can be done by verifying the correctness of the generated code against the original RISC-V verification test cases.

**Coprocessor Generation**

→ Coprocessor Generation: Codasip's HLS tool can automatically generate coprocessors for specific applications. This can be done by specifying the required functionality and constraints, and then letting the tool generate the corresponding hardware description language (HDL) code.

**Hardware Acceleration Flow**

→ Hardware Acceleration Flow: Codasip's HLS tool can automatically generate hardware accelerators for specific applications. This can be done by specifying the required functionality and constraints, and then letting the tool generate the corresponding hardware description language (HDL) code.

**Results and Future Work**

→ Results: Codasip's HLS tool has been used to generate RISC-V cores for various applications, including a game console, a medical imaging system, and a real-time control system. The results show significant performance improvements compared to hand-coded solutions.

→ Future Work: Codasip is currently working on improving the HLS tool's performance and flexibility, and exploring new application domains for RISC-V.

**Island Poster Number**  
2.1 01

**BOSCH CVA6 Core for Edge AI Applications**

**Island Poster Number**  
2.1 01

**Infineon CVA6 Core for Edge AI Applications**

**Island Poster Number**  
2.1 01

**Lauterbach Development Tools**

**RISC-V Summit Europe 2025**

**SIEMENS**

**Codasip**

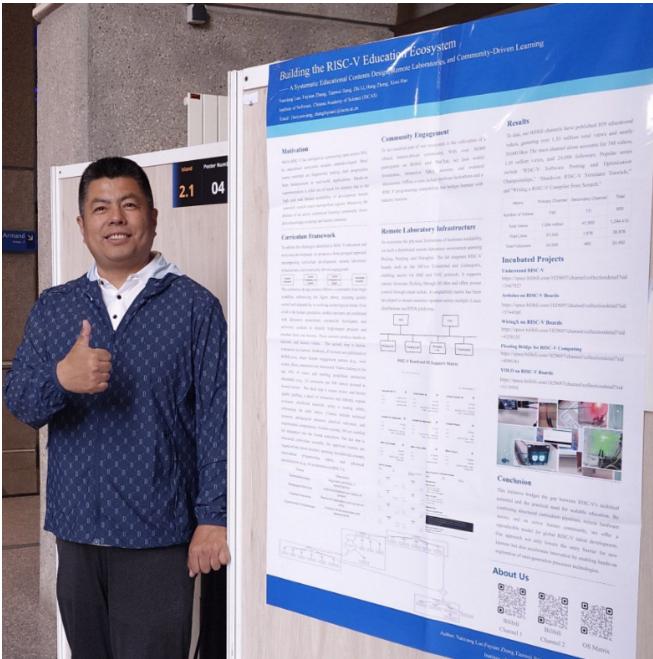
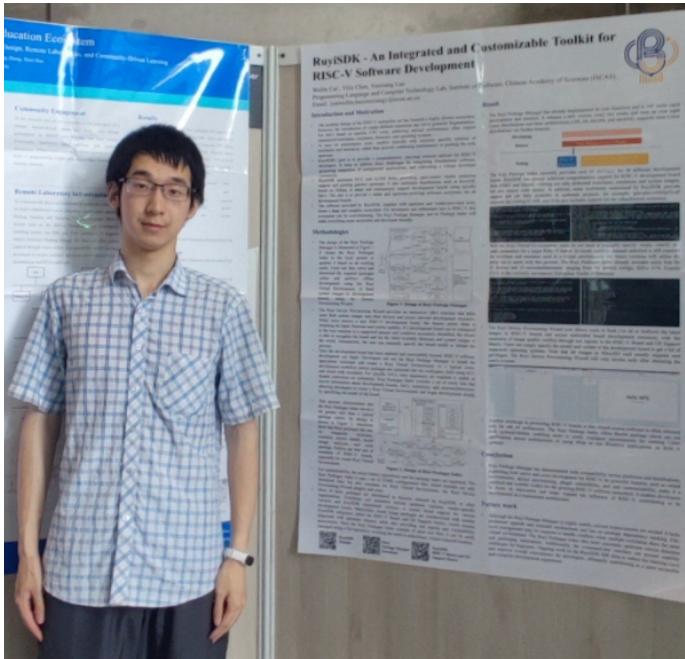
**infineon**

**LAUTERBACH**  
**DEVELOPMENT TOOLS**

# 参加2025年 RISC-V 欧洲峰会的中国厂商



# RuyiSDK 在 RISC-V 欧洲峰会



RuyiSDK  
Website



Ruyi  
Package Manager  
Download



RuyiSDK  
RISC-V Board and OS  
Support Matrix

<https://riscv-europe.org/summit/2025/posters>

# RISC-V 日语社区的同步与八卦

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# RISC-V 中国峰会进展(吴伟)

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# 项目进展

# Clang/LLVM 上游进展

- Assembler support for Q extension ([#139369](#), [#139495](#),[#139508](#))
- An initial scheduler model was added for the SpacemiT-X60 RISC-V CPU ([#137343](#))
- RISC-V SDNodes are now tablegenerated (similar cleanups were made recently to other backends, but I think this is the most in-depth). ([#c60db55](#))
- Initial code generation support was added for the RISC-V Zvqdotq (dot product) extension.([#1ac489c](#)).
- [RISCV][MC] Support Base P non-GPR pair instructions([#137927](#))

# GCC 进展

- GCC 15 is released, <https://gcc.gnu.org/gcc-15/>
- RISC-V Profiles RV20/22/23 supports on gcc upstream

<https://gcc.gnu.org/git/?p=gcc.git;a=commit;h=66d17ba3cb47980455ee9d6b4123dce61aef2fa2>

-march = profiles -march = profiles\_ISA e.g. -march=rva23u64

- Priv1.13 Supports on binutils upstream

<https://sourceware.org/git/?p=binutils-gdb.git;a=commit;h=433372af69804bd134f250e71479860c33a51c39>

- Supports [zilsd](#), [zclsd](#), [j](#), [sha](#) extensions

# QEMU/Spike 进展(呼唤志愿者)

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# Sail/ACT进展 (PLCT)

## Feature

- #752 Add support for Zvkned.
- #777 Add the Zawrs extension

## Configuration

- #932 Make RVFI a runtime option
- #928 Add config option to trap on sfence.vma if virt mem not supported
- #941 Add Lean back to CI for each PR but don't require it to pass

## Other

- #942 Fix vreg write print output
- #946 Add mstatush to csr\_name\_map
- #940 Add missing unit argument to zrvfi\_trap()
- #926 Remove tick\_platform() and htif\_tick()
- #937 Define and use a width type for memory widths.
- #867 Fix macOS compilation and add to CI
- #915 Update CI to run in merge queue

- #650 Update CI to use Latest Sail Config at Run time
- #648 Fix RVTEST\_CASE macro for rv32i bseti-01 test
- #645 Minor change in GOTO\_LOWER\_MODE macro
- #644 Modified B-extension Tests
- #643 Made changes as per discussion in PR#427
- #642 [ACT]add missing rv32zdinx testcases

# V8 for RISC-V 更新(邱吉、陆亚涵)

Add Zfh extension

1. 6530700: [riscv] Add extension zfh assembler | <https://chromium-review.googlesource.com/c/v8/v8/+/6530700>

Port Uptream

2. 6537691: [riscv][maglev] Monomorphise on seq one-byte strings | <https://chromium-review.googlesource.com/c/v8/v8/+/6537691>
3. 6537690: [riscv][wasm][shared] Implement struct.atomic.get for reference fields | <https://chromium-review.googlesource.com/c/v8/v8/+/6537690>
4. 6537692: [riscv][wasm][shared] Implement struct.atomic.get\_[s|u] | <https://chromium-review.googlesource.com/c/v8/v8/+/6537692>
5. 6522585: [riscv][wasm][growable-stacks] Increase stack limit margin | <https://chromium-review.googlesource.com/c/v8/v8/+/6522585>
6. 6515920: [riscv] Load JS dispatch table from isolate. | <https://chromium-review.googlesource.com/c/v8/v8/+/6515920>

# Spidermonkey for RISC-V更新（邱吉、陆亚涵）

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# OpenJDK on RISC-V (PLCT 杨飞)

JDK-24.0.1 is freely available:

<https://adoptium.net/temurin/releases/?version=24>

Use the drop-down boxes below to filter the list of current releases.

Operating System	Architecture	Package Type	Version
Any	Any	Any	24

**24.0.1+9**  
Temurin   
April 23, 2025

Linux riscv64

JDK - 137 MB [Checksum](#) [.tar.gz](#)

JRE - 57 MB [Checksum](#) [.tar.gz](#)

## JDK-24 Timelines

### JDK 24.0.1 timeline

- Feb 3rd RDP2
- Mid Apr 2025 GA

### JDK 24.0.2 timeline

- Apr 22nd RDP2
- Mid Jul 2025 GA

## JDK 25

This release will be the Reference Implementation of version 25 of the Java SE Platform, as specified by JSR 400 in the Java Community Process.

### Schedule

2025/06/05	Rampdown Phase One (branch from main line)
2025/07/17	Rampdown Phase Two
2025/08/07	Initial Release Candidate
2025/08/21	Final Release Candidate
2025/09/16	General Availability

RISC-V JDK mainline development work:

1. Co-authored two JEPs:

- <https://github.com/openjdk/jdk/pull/24296> (8352251: Implement JEP 518: JFR Cooperative Sampling)  
(RISC-V port: <https://github.com/RealFYang/jdk/commit/be8eac493bef865d7825848f0b31a06d95b08efc>)
- <https://github.com/openjdk/jdk/pull/23739> (8342382: Implementation of JEP G1: Improve Application Throughput with a More Efficient Write-Barrier)

2. Reviewed JDK-mainline PRs:

- <https://github.com/openjdk/jdk/pull/25181> (8350960: RISC-V: Add riscv backend for Float16 operations - vectorization)
- <https://github.com/openjdk/jdk/pull/24129> (8329887: RISC-V: C2: Support Zvbb Vector And-Not instruction)
- <https://github.com/openjdk/jdk/pull/24709> (8355074: RISC-V: C2: Support Vector-Scalar version of Zvbb Vector And-Not instruction)
- <https://github.com/openjdk/jdk/pull/24096> (8320997: RISC-V: C2 ReverseV)
- <https://github.com/openjdk/jdk/pull/23614> (8349908: RISC-V: C2 SelectFromTwoVector)
- <https://github.com/openjdk/jdk/pull/23580> (8321003: RISC-V: C2 MulReductionVI)
- <https://github.com/openjdk/jdk/pull/24797> (8355293: [TEST] RISC-V: enable more ir tests)



# Go community work update (PLCT 蒙卓)

## TL;DR Summary:

- race detector upstreaming
- RVV asm support DONE and a lots fixes, runtime optimazation reviewing
- RISC-V ELF attributes support upstreaming
- RV Zk asm support upstreaming, runtime/crypto library TBD

## 1. Authored/Co-authored Go-mainline CLs:

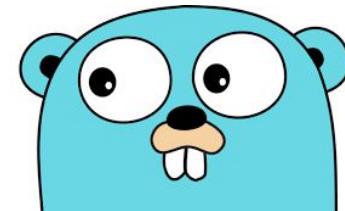
- 647596: runtime: unify C -> Go ABI transitions on riscv64 | <https://go-review.googlesource.com/c/go/+/647596>
- all: add race support for riscv64 | https://github.com/mengzhuo/go/commit/a1b9b0d4faae07a31c599e00ee73aa6b4f882068  
<https://github.com/golang/go/issues/64345>
- 659175: cmd/link: generate proper attributes for riscv profile | <https://go-review.googlesource.com/c/go/+/659175>
- 657036: internal/bytealg: vector implementation of count 1 byte for riscv64 | <https://go-review.googlesource.com/c/go/+/657036>
- 663778: cmd/asm, cmd/internal/obj: add zvbb/zvbc/zvkb for riscv64 | <https://go-review.googlesource.com/c/go/+/663778>
- 664155: cmd/asm, cmd/internal/obj: add crypto algorithm suites for riscv64 | <https://go-review.googlesource.com/c/go/+/664155>
- 664375: cpu: add crypto extensions detection for riscv64 | <https://go-review.googlesource.com/c/sys/+/664375>
- 663675: cmd/internal/obj: add crypto extension for riscv64 | <https://go-review.googlesource.com/c/go/+/663675>

## 2. Reviewed Go-mainline CLs:

- 660856: cmd/compile,internal/cpu,runtime: intrinsify math/bits.OnesCount on riscv64 | <https://go-review.googlesource.com/c/go/+/660856> [MERGED]
- 637317: cmd/internal/obj/riscv: fix the encoding for REV8 and ORCB | <https://go-review.googlesource.com/c/go/+/637317> [MERGED]
- 669675: cmd/link: ignore mapping symbols on riscv64 | <https://go-review.googlesource.com/c/go/+/669675> [MERGED]
- 646777: cmd/internal/obj/riscv: add support for vector floating-point instructions | <https://go-review.googlesource.com/c/go/+/646777> [MERGED]
- [merged] 646776: cmd/internal/obj/riscv: add support for vector fixed-point arithmetic instructions | <https://go-review.googlesource.com/c/go/+/646776> [MERGED]
- 660855: cmd/compile: intrinsify math/bits.Bswap on riscv64 | <https://go-review.googlesource.com/c/go/+/660855> [MERGED]
- 646778: cmd/internal/obj/riscv: add support for vector reduction instructions | <https://go-review.googlesource.com/c/go/+/646778> [MERGED]
- 646779: cmd/internal/obj/riscv: add support for vector mask instructions | <https://go-review.googlesource.com/c/go/+/646779> [MERGED]
- 646780: cmd/internal/obj/riscv: add support for vector permutation instructions | <https://go-review.googlesource.com/c/go/+/646780> [MERGED]
- 669315: cmd/internal/obj/riscv: reject invalid vadc/vsbc encodings | <https://go-review.googlesource.com/c/go/+/669315> [MERGED]
- 670016: cmd/internal/obj/riscv: fix LMUL encoding for MF2 and MF8 | <https://go-review.googlesource.com/c/go/+/670016> [MERGED]
- 652717: doc, cmd/internal/obj/riscv: document the riscv64 assembler | <https://go-review.googlesource.com/c/go/+/652717>
- 646736: internal/bytealg: vector implementation of equal for riscv64 | <https://go-review.googlesource.com/c/go/+/646736>
- 646737: internal/bytealg: vector implementation of compare for riscv64 | <https://go-review.googlesource.com/c/go/+/646737>

## 3. News

- 1.25 will freeze at 29 May



# RuyiSDK (Xi Jing, PLCT)

- RuyiSDK 包管理器发布[v0.33](#)版本：
  - RuyiSDK 包管理器：将设备安装器的数据源迁移到了实体数据库，以降低维护成本、避免频繁更新时潜在的合并冲突等
  - RuyiSDK 软件源：
    - 完善了设备支持：新增支持了 Milk-V Meles 的 16G RAM 型号，支持 RevyOS 系统
    - 实体数据库更新：
      - 设备实体定义更新：设备型号变体现已被拆分为单独实体类型 device-variant 了
      - 新增了“设备适用系统信息”实体 image-combo
  - 服务器组件：
    - 新增了官方软件源的新闻条目阅读 API
    - 新增了按版本号查询 RuyiSDK 版本发行注记的 API
    - 将官方软件源当前目录结构下的所有子目录都纳入了下载量统计范围
    - 改进了服务容器的构建方式。
- RuyiSDK IDE 插件版本 0.0.4 发布：
  - 新增 ruyi 包管理器检测、安装及版本更新向导。
  - 新增 RuyiSDK 配置项 (Windows > Preferences > RuyiSDK)
- 操作系统支持矩阵
  - 新增 OpenWRT/NuttX/Arch Linux 对 Mars 开发板的支持
  - 升级 FreeRTOS、Alpine、RockOS 等系统版本至最新稳定版
  - 修复多平台测试报告中的问题

# openEuler RISC-V (周嘉诚)

Status / 20250515

- openEuler 24.03 SP2:
  - Official (RVA20): [Mass-rebuilding](#)
- openEuler 25.03:
  - Official (RVA20): [Released](#)  [\[DL Link\]](#)
  - Preview (RVA22+V): [Mass-rebuilding](#)
- Updates -
- RVCK (Common 6.6 Kernel)
  - update to 6.6.88, test & adapt numerous tests
- ISA-L: implement RVV support for module `raid`
- golang: update to 1.24.x, plugin mode patch backporting
- openjdk: contribute & backport upstream vector fixes
- openssl: setup RISC-V CI for upstream
- CI: setup a pipeline for building docker image on Gitee Go

Following releases in 1H'25

- [Late Q2](#) - openEuler 24.03 SP2

Features:

- 6.6-based [common kernel](#) for QEMU, SG2042 (Pioneer) & TH1520 (LPi4A)
- UEFI-supported Hardware & QEMU images
- [Penglai TEE](#)-enabled firmware variants

Images:

- [UEFI ISO](#)
- [UEFI](#) qcow2 Image w/ [Penglai TEE](#)
- Legacy-boot Images for Pioneer & LPi4A

# Gentoo for RISC-V 的情况更新 (Gentoo 小队)

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# Arch Linux RISC-V (Felix & PRZ)

- [core] 265 / 266 (99.62%)
- [extra] 13958 / 14294 (97.65%)
- Linux kernel updated to 6.14.3 with Spacemit K1 drivers enabled.
- GCC 15.1.1 toolchain updates in progress.
- Attempting to re-enable valgrind tests and update valgrind to upstream version.
- Electron 35/36 and Chromium 136 patched and compiles on SG2042.
- GHC 9.4.8 updates in progress.
- Working on Icenowy's GLVNDized PowerVR Driver on ROMA 2. (\*Still many problems)
- Disabled xtheadvector and LTO for NCNN, unfortunately.
  - [https://gcc.gnu.org/bugzilla/show\\_bug.cgi?id=110812](https://gcc.gnu.org/bugzilla/show_bug.cgi?id=110812)
  - [https://gcc.gnu.org/bugzilla/show\\_bug.cgi?id=116590](https://gcc.gnu.org/bugzilla/show_bug.cgi?id=116590)

# Arch Linux RISC-V (Felix & PRZ) - Electron

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# Fedora on RISC-V status update (20250417)

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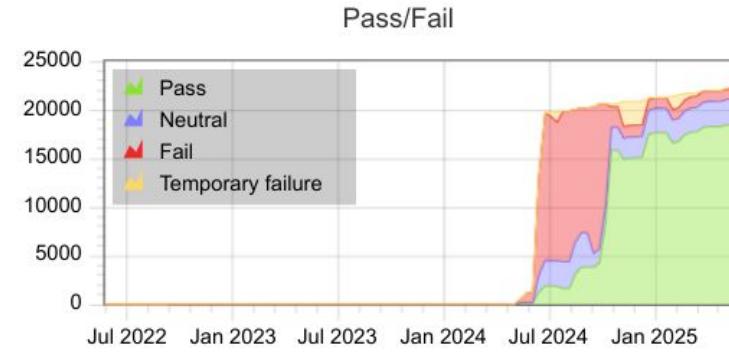


*Fedora-V Force*

# Debian for RISC-V(于波)

- **Official port update**
  0. Debian Trixie [hard](#) freeze 05/15
  1. reproduce build for [riscv64](#) catch up trixie
- **Debci [update](#)**
  1. [piuparts](#) failed on riscv64 unstable
  2. update [riscv64](#) nodes
- **Some works**
  1. opensnith[[MR](#)], ananta [[uploaded](#)], qt6-webengine [6.6.2 [package](#)]
  2. mame[rv64 [ftbfs](#)], haskell-charsetdetect-ae [support rv64 [patch](#)], strace[merge [MR](#)]
  3. eclipse [[test](#) +1], debci [[update](#)] rv64 nodes]

testing/riscv64



RevyOS (本周无更新)



# Guix on RISC-V(郑俊杰)

Migrating repositories, issues, and patches to Codeberg

ci.guix.gnu.org add a visionfive2 builder

python3 3.10 -> 3.11

R 4.43-> 4.5

elogind 252.9 -> 255.17

Add linux-libre 6.14.6

Add valgrind 3.25.0

支持开发板:

visionfive2/mars megrez  
unmatched

	https://ci.guix.gnu.org/		https://bordeaux.guix.gnu.org/	
aarch64-linux	15.4%	☁️	aarch64-linux	90.7%
armhf-linux	9.1%	☁️	armhf-linux	82.0%
i586-gnu	0.6%	☁️	i586-gnu	0.0%
i686-linux	83.6%	☀️	i686-linux	87.0%
powerpc64le-linux	44.2%	☁️	powerpc64le-linux	42.5%
riscv64-linux	4.9%	☁️	riscv64-linux	58.0%
x86_64-linux	91.1%	☀️	x86_64-linux	97.4%

# Sophgo Linux Upstream Status Update(汪辰)

<https://github.com/sophgo/linux/wiki> [Last updated: May/14/2025]

- CV18XX Series
  - Mailbox patch v3: <https://lore.kernel.org/linux-riscv/20250428-cv18xx-mbox-v3-0-ed18dfd836d1@pigmoral.tech>
  - PWM patch v8: [https://lore.kernel.org/linux-pwm/20250509-pwm\\_sophgo-v8-0-cfaebbeb8ee17@bootlin.com](https://lore.kernel.org/linux-pwm/20250509-pwm_sophgo-v8-0-cfaebbeb8ee17@bootlin.com)
  - RTC patches are divided into two part, [1/3] & [2/3] is now for RTCSYS and have been picked by sophgo/soc-for-next.
  - CV18xx DTS rework part1 & part2 are now ready and picked by sophgo/for-next
- SG2042
  - SPI patch v5: <https://lore.kernel.org/linux-riscv/20250422-sfg-spi-v5-0-c7f6554a94a0@gmail.com/>
  - SPI patch v6: <https://lore.kernel.org/linux-riscv/20250425-sfg-spi-v6-0-2dbe7bb46013@gmail.com/>
  - Network patch v1: <https://lore.kernel.org/linux-riscv/20250506093256.1107770-1-inochiama@gmail.com/>
  - SG2042\_EVB\_V1.0 & SG2042\_EVB\_V2.0 patch  
v1:<https://lore.kernel.org/linux-riscv/cover.1746811744.git.rabenda.cn@gmail.com>
  - SG2042 add more isa extension patch v1:<https://lore.kernel.org/linux-riscv/cover.1746828006.git.rabenda.cn@gmail.com>
- SG2044
  - Clock patch v5: <https://lore.kernel.org/linux-clk/20250418020325.421257-1-inochiama@gmail.com>
  - PWM patch v2: <https://lore.kernel.org/linux-riscv/20250418022948.22853-1-looong.bin@gmail.com>
  - PWM patch v3: <https://lore.kernel.org/linux-riscv/20250424012335.6246-1-looong.bin@gmail.com>
  - PWM patch v4:: <https://lore.kernel.org/linux-riscv/20250428013501.6354-1-looong.bin@gmail.com>
  - SRD3-10 board support is now ready and picked by for-next

# Canaan Linux Upstream Status Update(汪辰)

<https://github.com/plctlab/linux/wiki> [Last updated: May/14/2025]

- K230
  - Reset patch v2:  
<https://lore.kernel.org/linux-riscv/20250420-k230-reset-v2-0-f1b4a016e438@pigmoral.tech/>
  - Reset patch v3:  
<https://lore.kernel.org/linux-riscv/20250507-k230-reset-v3-0-c85240782ea5@pigmoral.tech/>

# RT-Thread (RISC-V) Upstream Status Update (汪辰)

PR list:

- bsp: cvitek: riscv: use marco for linker script:  
<https://github.com/RT-Thread/rt-thread/pull/10202>
- bsp: k230: support canmv-k230: <https://github.com/RT-Thread/rt-thread/pull/10221>
- ci: add k230 ci check: <https://github.com/RT-Thread/rt-thread/pull/10229>
- bsp: k210: fix drv\_i2c's include file: <https://github.com/RT-Thread/rt-thread/pull/10234>
- bsp: k230: use rtppkgtool to package kernel:  
<https://github.com/RT-Thread/rt-thread/pull/10236>
- bsp: k230: eliminate warnings for kconfig: <https://github.com/RT-Thread/rt-thread/pull/10245>

RFC discussion

- N/A

# OpenCloudOS RISC-V 进展(孙敏)

1

## OC月度例会 (2025年5月6日)

- ocs riscv 开发进度同步(内核:基于sg2042 6.6.68适配驱动; yum源/镜像已发布到官网; 基础设施:现有3台sg2042, 机箱、显卡、ipkvm)
- 开放探讨:oc riscv sig 的发展目标讨论(**北向繁荣软件生态**, 还是南向适配更多芯片?)
- 开放探讨:在 RVA23 规范的新形势下, 操作系统应该做些什么?(适配RVV gcc 13/14关于rva23的特性 backport gcc12)

2

## 宣发

OC Stream RISC-V 全新架构版本

<https://mp.weixin.qq.com/s/iZAXFivq9pQJybYbgaGA7A>

3

## todo

容器镜像、oc自带套件、办公软件、浏览器视频编解码等图形界面测试优化

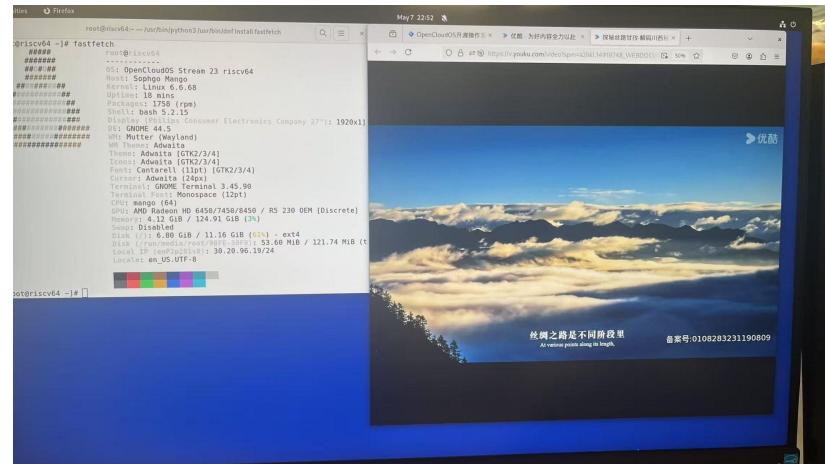
4

## 测试与支持矩阵

<https://matrix.ruyisdk.org/board/Pioneer/openCloudOS-README/>  
[https://matrix.ruyisdk.org/board/Pioneer/openCloudOS-README\\_uefi/](https://matrix.ruyisdk.org/board/Pioneer/openCloudOS-README_uefi/)  
[https://matrix.ruyisdk.org/board/Pioneer/openCloudOS-README\\_linuxboot/](https://matrix.ruyisdk.org/board/Pioneer/openCloudOS-README_linuxboot/)

5

## Gnome桌面展示



# FreeBSD RISC-V 进展(蒙卓)

Queued	Built	Failed	Skipped	Ignored	Fetched	Remaining
36449	11618	280	22538	2013	0	0
Load Averages (23%)	4.07 1.71 1.11	Swapinfo	Elapsed	Pkg/Hour	Impulse	--
52:58:37	225					

Milkv-Megrez KVM (Host RockOS)

14 SMP/net/virtio works

<https://mirror.iscas.ac.cn/FreeBSD-pkgs>

14-quarterly:  $11618/36449 = 32\%$

- python/rubygem/php based pkgs can't be built, **yet**
- latest pkgs is still building
- Linux-based pkg is unavailable



# Box64 RISC-V 进展

- 

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# OpenSBI (王翔)

- 添加工具链的堆栈保护支持  
<https://lists.infradead.org/pipermail/opensbi/2025-May/008429.html>
- 为冻结的RPMI规格更新代码  
<https://lists.infradead.org/pipermail/opensbi/2025-May/008440.html>
- 在pmu代码中通过cbase/cmask标识counter, 添加错误处理代码阻止cmask为0  
<https://lists.infradead.org/pipermail/opensbi/2025-May/008448.html>
- 禁止低特权等级对 CY/IR 的访问以避免侧信道攻击  
<https://lists.infradead.org/pipermail/opensbi/2025-May/008450.html>
- 在sbi\_dbtr.c中优化saddr的mapping操作  
<https://lists.infradead.org/pipermail/opensbi/2025-May/008454.html>

# RustSBI团队进展(洛佳)

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# RustSBI团队进展(洛佳)

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# 香山开源RISC-V处理器 - ICT / PCL

- 后端
  - 修复 LCOFI (本地计数器溢出中断) 位在 xvip/xvien 寄存器中的可读写性问题 (#4648)
  - 修复 xstateen 对 sireg/vsireg 寄存器控制出错的问题 (#4649)
  - 修复虚拟中断注入没有被 mnstatus.nmie 控制的问题 (#4645)
  - 修复 wfi 未能被非屏蔽中断唤醒的问题 (#4645)
  - 修复 tval 寄存器在中断, CSR 相关异常, 重定向同时发生的综合场景下更新出错的问题 (#4671)
  - 修复 mcause 在中断的双重陷入时更新出错的问题 (#4671)
  - 修复部分发生 EX\_I/EX\_VI 异常指令同时发生中断, 且在中断处理函数再次发生上述异常时, tval 寄存器无法正常更新的错误 (#4671)
  - 在仿真输出中添加版本信息 (#4626)
- 访存与缓存
  - 修复 StoreQueue 中, 一条 uncache store 发生异常时的出队逻辑 (#4641)
  - UncacheBuffer 的 store 和 load 改为按照 robIdx 仲裁入队, 防止依赖卡死 (#4628)
  - 修复非对齐访存跨页且新页产生异常时, 写入 \*tval 的值依然为前一页地址的 bug (#4673)
  - 对于非对齐访存指令, 当 RAW queue 满时需要 rollback 以避免阻塞 (#4674)
  - 修复在 StoreQueue 中 cbo 指令出现异常时的 bug (#4663)
  - 修复 genVpn 函数未考虑虚拟化不同阶段、以及未考虑大页的 vpn 拼接等 bug (#4647)
  - 修复虚拟化 allStage 且两阶段均为大页时的部分场景下, 生成 ppn 有误的 bug (#4658)
  - 修复 MMU 在 napot 场景下的部分命中匹配逻辑 (#4659)
  - 修复 StoreQueue 中向量异常的 flag 误发生超时 assert 的问题 (#4660)

# banshanjdk-8 让你的 java8 程序在 RISC-V 平台极限加速

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# Chisel and Additional Technology / Sequencer

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# OpenHW & OpenHW Aisa Working Group

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# 甲辰计划进展(吴伟)

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# 自由讨论 / AOB

## RVP现状介绍

<https://docs.google.com/presentation/d/1Klw0VB0z4iLfh8x4NchWj5PcX5TfDU7qSBzuRAp6Nh8/edit?slide=id.p#slide=id.p>

# BACKUP

准备加入更多的国际开源组织进行同步观测

欢迎追加或提议