欢迎第一次加入的伙伴(开会时请从下一页开始展示)

- 开放编辑，直接点击 request for edit 然后在东亚时区群里at吴伟
- 如果没有找到自己的内容分类，可以添加1-2页在最开始或中间
- 欢迎在开始的前5分钟进行自我介绍
- 日常八卦在东亚时区RISC-V双周同步微信群中，欢迎加入

东亚时区RISC-V双周会

2022年12月08日·第049次

https://github.com/cnrv/RISCV-East-Asia-Biweekly-Sync

Host: 邱吉

Organizer: PLCT Lab plct-oss@iscas.ac.cn

会议议程（15:00 - 16:00）

- 自我介绍、等待参会者接入、非技术话题八卦（没有的话就直接跳过）
- RVI 的更新和八卦（基本上跟东亚双周会群内消息同步）
- Unratified Specs 的参考实现进展
- 东亚地区小伙伴的项目更新
- 自由讨论

RISC-V International 同步、全球开源社区八卦

1. 下周就是 RISC-V Global Summit 2022 了！作为观众还可以进行注册，机会不要错过
2. 中科院软件所加入了 KernelCI 基金会，后续将持续为 RISC-V 的Linux内核测试提供支持
3. 中科院软件所的 Spidermonkey JIT 开始逐步被 Mozilla 社区 review 和接收。
4. 中科院软件所12月9日将举办 PLCT OpenDay 2022，新的 RuyiSDK 计划将会公布。
5. 今天上午举行了2022年最后一次 RISC-V Open hours 活动，RISC-V大使傅炜主持
6. 有人在收集支持H的RISC-V核 https://lists.riscv.org/g/sig-hypervisors/message/196
7. 12月15日：开源芯片系列讲座第07期：基于RISC-V的Linux发行版及软件生态
8. RISC-V: An Open-Source Churn In Computational Hardware Electronics – Part 2
9. Imperas and Andes collaborate to support RISC-V innovations
10. UniHiker education platform teaches STEM with Mind+ and Jupyter (in China)
11. CEVA joins Intel Pathfinder for RISC-V programme
12. Sipeed M1s DOCK is a tiny RISC-V dev board for $11
13. $10.80 RISC-V AIoT module supports Linux
14. Codasip and Intel bring RISC-V development to higher-education

RISC-V 韩语社区的同步与八卦

- Zaram Technology 明年推出基于RISC-V的wearable device和edge computing 解决方案
  - 今年IPO，现在有RISC-V SoC叫做XGSPON ZX300
  - 明年出一个安在CCTV上的带NPU的RISCV板子，以及基于wearable devices
  - 主要在低功耗方面

- 三星电子代工生态系统"SAFE"，代工全家桶提供EDA和DM(design methodology)
  - EDA, Cloud, IP, design solution partner(DSP), package
  - SemiFive: RISC-V SoC design solution partner
    - Design house -> design platform
    - 确定spec开始，设计并体现架构、开发成套设备、制作系统软件

RISC-V 日语社区的同步与八卦

- RISC-V 轮读会 2022/12/20(Tue)
- 主讲人:神户大学 大原遼太郎 | LinkedIn
- 【輪読会】作って学ぶコンピュータアーキテクチャ 第 4回 - connpass

- Open Source Summit Japan Dec. 5~6
- https://events.linuxfoundation.org/open-source-summit-japan/
- 没有跟riscv相关的新闻

- Tuxera
- LINEOWarp!! 超高速启动的embedded system增加对riscv的support
- 在sifive上u740验证了76%的boot time shortening

RISC-V 俄语社区的同步与八卦

- 没有跟risc-v相关的新闻

AOSP for RISC-V - 汪辰、陆旭凡

- Google AOSP upstream PR
  - Android (RISC-V) Review 双周报 第 5 期(in Chinese):https://zhuanlan.zhihu.com/p/589829148
    - 有关 Bionic 库的修改，也就是 2142912 这个补丁的拆解合并已经基本结束
    - 工具链，2313480: Cherry pick riscv patches for bionic
    - GKI 内核构建现在也开始增加对 riscv64 的支持了，相关的修改可以参考 2310710 / 2310387 / 2308504。
  - Dec/9，RVI Android SIG 月会（Google upstream discusstion 第二次）
    https://lists.riscv.org/g/sig-android/message/131
  - Support GKI kernel/modules building on Google upstream master
    - [Initial support for riscv64 kernel build](2310387): merged
    - [ANDROID: Virtual device modules for RISC-V 64-bit](2308370): co-work with googler and in reviewing.

- RVI Android SIG upstream:
  - updated release history in Nov: https://github.com/riscv-android-src/riscv-android/pull/18

- chrome apk build work
  - initial clang version for chrome building for aosp12: https://github.com/aosp-riscv/platform-manifest/pull/1
  - build clang with latest llvm:https://github.com/aosp-riscv/toolchain-llvm-android/pull/1
  - fixed revisions:https://github.com/aosp-riscv/platform-manifest/pull/2
  - updated doc for how to build Chromium RISCV64:https://github.com/aosp-riscv/working-group/pull/53
  - add marco defines missed in last PR:https://github.com/aosp-riscv/chromium/pull/3

RISC-V GCC进展

Philipp 提交了一系列对Bitmanip指令优化的patch，目前已合并到gcc上游：https://gcc.gnu.org/git/bitmanipopt

钟居哲提交了VSETVL PASS支持，使用LCM进行完美适配，目前上游正在review中：

https://gcc.gnu.org/git/?p=gcc.git;a=commit;h=3b16afeb3f6aacf64b9f9c50b7cb9805a9dfff63

RVV Intrinsic C API会议notes链接：https://github.com/riscv-admin/rvv-intrinsics/blob/main/meeting_minutes/2022_11_28.md

Eswin开始向GNU社区提交RISC-V优化支持：

https://gcc.gnu.org/git/?p=gcc.git;a=commit;h=f7a41b5cfd7406da1f2e5a0f1f813521d3dc2bb2

https://sourceware.org/git?p=binutils-gdb.git;a=commit;h=06f0a892a5260d8fe93550ed96364cc76fef971d

提交了pei-riscv64 target支持：

https://sourceware.org/pipermail/binutils/2022-November/124713.html

Christoph 提交了新的RISC-V Intrinsic命名草案：

https://github.com/riscv-non-isa/riscv-c-api-doc/pull/31

RISC-V GNU Toolchain双周会slides链接：

https://docs.google.com/presentation/d/1IGC7kxMqpaNU2hhTqucYkstINzuwTgrUHnnsY-BaELQ/edit#slide=id.g1a061d7f7e9_0_0

gcc已经进入stage3, RVV intrinsic预计会在gcc13 release中正式支持

Clang/LLVM 进展 (PLCT)

- 最近两周被合并的patch
  1. [flang] Enable RISC-V for x86CompatibleBehavior in floating point flag. https://reviews.llvm.org/D138503
  2. [flang] Add RISCV-64 support to Optimizer/CodeGen/Target.cpp. https://reviews.llvm.org/D136547
  3. [flang] Diagnostic for shape argument in c_f_pointer https://reviews.llvm.org/D138743
  4. [RISCV]Keep (select c, 0/-1, X) during PerformDAGCombine https://reviews.llvm.org/D139272
  5. [OpenMP][LegacyPM] Remove OpenMPOptCGSCCLegacyPass https://reviews.llvm.org/D139004
  6. [LLDB][RISCV] Add RV64F instruction support for EmulateInstructionRISCV https://reviews.llvm.org/D139294
  7. [LLDB][RISCV] Add RV32FC instruction support for EmulateInstructionRISCV https://reviews.llvm.org/D139390

Clang / LLVM 社区的更新（廖春玉、陆旭凡）

1. https://reviews.llvm.org/D137713 [SCCP] Add support for with.overflow intrinsics
2. https://reviews.llvm.org/D139289 [SCCP] Propagate equality of a not-constant
3. https://reviews.llvm.org/D138660 [MachineCombiner][RISCV] Support inverse instructions reassociation
4. https://reviews.llvm.org/D139391 [RISCV] Codegen support for Zfhmin.

QEMU/Spike/Sail/ACT进展 (PLCT)

- Spike
  - Zc*扩展Fix已合并至上游
    - https://github.com/riscv-software-src/riscv-isa-sim/pull/1156
- QEMU
  - Zc*扩展更新到v8版本
    - https://github.com/plctlab/plct-qemu/tree/plct-zce-upstream-v8

gem5 进展 (PLCT)

- V拓展
  - 新增 vector slide 类型的全部指令
    https://github.com/plctlab/plct-gem5/pull/19
  - 修复vl=0时，微指令拆分出错的问题
    https://github.com/plctlab/plct-gem5/pull/25
  - 正在整理向量拓展 patch 提交 gem5 上游

V8 for RISC-V 更新（邱吉、陆亚涵）

- 增加simulator调试ebreak函数，方便在simulator上调试

  4074457: Reland "[riscv] Add tracepoint instructions to help simulator debug" | https://chromium-review.googlesource.com/c/v8/v8/+/4074457

- 减少警告的产生

  4032085: [riscv] Convert Opcode from enum to integer type. | https://chromium-review.googlesource.com/c/v8/v8/+/4032085

优化和修复rv实现问题：

- 4050268: [riscv] Fix vector move | https://chromium-review.googlesource.com/c/v8/v8/+/4050268
- 4032085: [riscv] Convert Opcode from enum to integer type. | https://chromium-review.googlesource.com/c/v8/v8/+/4032085
- 4039240: [riscv] Optimize ComputeCodeStartAddress func | https://chromium-review.googlesource.com/c/v8/v8/+/4039240

Spidermonkey for RISC-V更新（邱吉、陆亚涵）

- 仍在review当中
  https://bugzilla.mozilla.org/show_bug.cgi?id=1800431

OpenJDK for RISC-V 更新(RV64及upstream)杨飞

1. Authored jdk-mainline PRs:
- https://github.com/openjdk/jdk/pull/11310 (8297476: Increase InlineSmallCode default from 1000 to 2500 for RISC-V)
- https://github.com/openjdk/jdk/pull/11406 (8297715: RISC-V: C2: Use single-bit instructions from the Zbs extension)
- https://github.com/openjdk/jdk/pull/11496 (8298055: AArch64: fastdebug build fails after JDK-8247645)

2. Reviewed jdk-mainline PRs:
- https://github.com/openjdk/jdk/pull/11239 (8297238: RISC-V: C2: Use Matcher::vector_element_basic_type when checking for vector element type in predicate)
- https://github.com/openjdk/jdk/pull/11276 (8297359: RISC-V: improve performance of floating Max Min intrinsics)
- https://github.com/openjdk/jdk/pull/11344 (8297549: RISC-V: Support vloadcon instruction for Vector API)
- https://github.com/openjdk/jdk/pull/11370 (8297644: RISC-V: Compilation error when shenandoah is disabled)
- https://github.com/openjdk/jdk/pull/11388 (8297697: RISC-V: Add support for SATP mode detection)
- https://github.com/openjdk/jdk/pull/11414 (8297763: Fix missing stub code expansion before align() in shared trampolines)
- https://github.com/openjdk/jdk/pull/11453 (8297953: Fix several C2 IR matching tests for RISC-V)
- https://github.com/openjdk/jdk/pull/11461 (8297967: Make frame::safe_for_sender safer)
- https://github.com/openjdk/jdk/pull/11188 (8297036: Generalize C2 stub mechanism)

3. Generational-ZGC RISC-V Port:
- Basic support contributed by Huawei: https://github.com/openjdk/zgc/pull/10
- Need rebasing with: https://github.com/openjdk/zgc/tree/zgc_generational
- TODO: Add support for RVV extension

4. Foreign-API RISC-V Port:
- New development branch at: https://github.com/feilongjiang/jdk/tree/riscv-foreign-api
- Need rebasing with: https://git.openjdk.org/jdk/pull/10872 (8295044: Implementation of Foreign Function and Memory API (Second Preview))
  https://git.openjdk.org/jdk/pull/11019 (8296477: Foreign linker implementation update following JEP 434)

OpenJDK for RISC-V 更新（RV32/PLCT 史宁宁）

1. Fix the long data in signExtractL of riscv32.ad

https://github.com/openjdk-riscv/jdk11u/pull/572

2. Fix the immLAdd data type errors in riscv32.ad

https://github.com/openjdk-riscv/jdk11u/pull/573

3. Fix the reg error in MoveL2D_reg_reg

https://github.com/openjdk-riscv/jdk11u/pull/574

4. Fix the lrem/ldiv in macroassembler

https://github.com/openjdk-riscv/jdk11u/pull/575

5. Fix the num errors in zero_words() imm

https://github.com/openjdk-riscv/jdk11u/pull/576

6. Fix the i2c and c2i adapter according arm 32bit

https://github.com/shining1984/jdk11u/commit/4f3c17e17c70b128169718b554264bf07b44637e

OpenJDK for RISC-V 更新（RV64及upstream）张定立

Merged & New JDK-mainline PRs:

- https://github.com/openjdk/jdk/pull/11575 | (8298342: RISC-V: RoundDoubleModeV does not use dynamic rounding mode correctly)

Reviewed JDK-mainline PRs:

- https://github.com/openjdk/jdk/pull/11577 | (8298345: Fix another two C2 IR matching tests for RISC-V)

Vector-API support:

- RISC-V: Enable v0 mask in vaddl_masked
- RISC-V: Fix vloadmask in c2

OpenJDK for RISC-V 更新（RV64及upstream）曹贵

Merged & New JDK-mainline PRs:

- https://github.com/openjdk/jdk/pull/11577 | (8298345: Fix another two C2 IR matching tests for RISC-V)

Reviewed JDK-mainline PRs:

- https://github.com/openjdk/jdk/pull/11344 | (8297549: RISC-V: Support vloadcon instruction for Vector API)

Vector-API support:

- Basic support vector api mask

JAVA 开源工具调研及测试 - async-profiler

- async-profiler 是一款开源的JAVA 性能分析工具，在 JAVA 程序出现性能问题时可以实时分析到性能瓶颈，主线版本还不支持 RISC-V平台。红帽 shipilev 老师 提交的 Basic RISC-V support 在 RISC-V 平台上进行了支持，在测试的时候发现，因为官方主分支有一些功能更新，导致主分支合并到该分支后编译时有报错，参考 ARM64 修复后，在该 PR 下进行相关修复描述，修复内容已被更新到这个 PR 下。当前该PR还在等待合并中，需要 maintainer 解决代码贡献相关问题后才能进行合并。

- 使用最新的 PR 后，在 RISC-V unmatched 平台上，正常通过了 aysnc-profiler 自带的所有官方测试，在 RISC-V unmatched 平台使用 async-profiler 对 SPECjvm2008 derby, compress 进行性能分析，对比该场景在 ARM64 平台下的性能数据，采样的性能热点数据正确，并将测试结果数据在该 PR 下进行了更新。

- 根据红帽 shipilev 老师在PR中提到，当前为基本支持，还有一些特性没有支持，后续我会对其相关功能进行支持，并持续在 RISC-V 平台上跟进 async-profiler 的主线功能。

OpenJDK8 backporting（章翔）

javac调试

- [Fix safepoint] https://github.com/zhangxiang-plct/jdk8u/pull/209
- [Add metaspaceShared_riscv64.cpp and delete is_icholder_call_site in compiledIC.cpp] https://github.com/zhangxiang-plct/jdk8u/pull/212
- [Delete throw_abstract_method_error/throw_AbstractMethodErrorWithMethod] https://github.com/zhangxiang-plct/jdk8u/pull/213

C1调试

- [Fix lir_cmove/lir_branch/LIR_OpBranch::print_instr]https://github.com/zhangxiang-plct/jdk8u/pull/213
- [Add has_common_register] https://github.com/zhangxiang-plct/jdk8u/pull/206
- [Fix __branch] https://github.com/zhangxiang-plct/jdk8u/pull/232
- [Add HAS_FLAGREG_ONLY in LIR_Op2::verify() for rv64 support] https://github.com/zhangxiang-plct/jdk8u/pull/230
- [Fix ideal_reg to add rv64g backend support] https://github.com/zhangxiang-plct/jdk8u/pull/229
- [Fix c1_LIR.hpp to initial rv64g backend support] https://github.com/zhangxiang-plct/jdk8u/pull/228
- [Fix delete_unnecessary_jumps] https://github.com/zhangxiang-plct/jdk8u/pull/226
- [Fix delete_unnecessary_jumps by adding NO_FLAG_REG about lir_cmove/lir_cmp] https://github.com/zhangxiang-plct/jdk8u/pull/217
- [Fix CounterOverflowStub::emit_code] https://github.com/zhangxiang-plct/jdk8u/pull/218

openEuler RISC-V

- PR:+44
  - Init package：21 KDE桌面软件包补充完善;
  - Fix：17
  - Upgrade：3 clang、compiler-rt、llvm 更新;
  - 合规性修复：3
- other
  - Electron（共21；succeeded: 19;failed:1）
  - qt6及相关软件包（共51；succeeded: 36;unresolvable:3;failed:11）
  - KDE：（共205；succeeded: 203;）
  - HPC：（共14；succeeded：11；）openmpi单机部署与集群部署
  - add autoboot for efi:https://build.tarsier-infra.com/package/show/Factory:RISC-V:Kernel/risc-v-uboot-d1s
- 测试
  - [WIP] 测试自动化工具调研:avocado调研、部署及测试用例调试；openQA调研；
  - 更多测试进展:https://github.com/isrc-cas/tarsier-monthly/blob/main/002-20221201.md
- 软件包版本

  Toolchain gcc-12.1.1-3 / glibc-2.36-10
  binutils 2.37-6
  libffi 3.4.2-2
  libmpc 1.2.0-2
  gmp 6.2.1-3
  rust 1.60.0-5 → 1.62.1(√) → **1.65.0**((√)
  java-latest-openjdk-18.0.2.9-0 → 19.0.0.36-1(√)
  llvm/clang 12.0.1-2 → 13.0.1(√) → 14.0.5(√) → 15.0.4(√)
  python 3.10.2-4
  perl 5.28.0-435 → 5.34.0(√)

Gentoo for RISC-V 的情况更新（Gentoo 小队）

- Support statistics `(8026/19575, 41.00%)`：https://whale.plctlab.org/riscv/support-statistics/
- A total of 9 keywording commits: https://whale.plctlab.org/riscv/RISC-V-双周会/20221208/commits.txt
  - dev-ruby/rails: Keyword 6.1.7 riscv, https://github.com/gentoo/gentoo/commit/7851644925db3acfc7443ed2d4392490c542f23c
  - dev-vcs/stgit: Keyword 2.0.3 riscv, https://github.com/gentoo/gentoo/commit/d6bbd5cdd7e93b8c3cd1c19d2c186054cb0b85fd
- sys-cluster/mpich: Keyword 3.4.3 riscv, PR created
  - https://github.com/gentoo/gentoo/pull/28595
- WIP
  - sys-cluster/ceph: fixed atomic issue, build successfully

Arch Linux RISC-V（东东、潘瑞哲）

```
[ Arch Linux RISC-V Bi-Week Package
Update Stats Report ]

Report generated on: 20221208
Package update count: 2793
Distinct package update count: 2296

[core] 254 / 261 (97.31%)
[extra] 2844 / 3079 (92.36%)
[community] 8777 / 9808 (89.48%)
```

```
Highlight packages:
    nodejs - 19.1.0-1 --> 19.2.0-1
    glib2 - 2.74.1-1 --> 2.74.3-1
    libreoffice-fresh - none --> 7.4.3-2
    qt5-wayland - 5.15.7+kde+r53-1 --> 5.15.7+kde+r55-1
    kwayland - 5.99.0-1 --> 5.100.0-1
    imagemagick - 7.1.0.52-1 --> 7.1.0.53-1
    telegram-desktop - 4.3.1-2 --> 4.4.0-1
    kotlin - 1.7.21-1 --> 1.7.22-1
    graphviz - 7.0.1-2 --> 7.0.4-1
```

https://github.com/felixonmars/archriscv-packages/pull/1943

Fedora for RISC-V（傅炜）

- **RPM packaging**
  - **https://openkoji.iscas.ac.cn/koji/ For RISC-V**
  - **[rawhide/F38]【On Going】[https://openkoji.iscas.ac.cn/repos/fc36dev/] as build repo**
  - **Rpm-list-builder with yaml for Python 3.11**
- **Key software:**
  - **Toolchain gcc-12.2.1-2 / glibc-2.36-4 (up-to-date)/Binutils 2.39-3 (up-to-date)**
  - **libffi-3.4.3-1.1(up-to-date)**
  - **java-latest-openjdk-19.0.0.0.36-2(up-to-date)**
  - **perl-5.36.0-492[rawhide](up-to-date) Building modules [perl-bootstrap koji]**
  - **Python 3.11(up-to-date) need testing and merging, [rpmlb + yaml, mock]**
  - **LLVM/Clang 15.0.0-1(up-to-date)**
  - **Rust 1.63.0-1→Rust 1.64 [need qemu fix from Felix] (Hold)**
  - **Go 1.18-1→ 1.19-1[rawhide](updating)**
  - **firefox and Chromium (updating)**
- **Images:**
  - **QEMU/D1/JH7110 Images , waiting for VisionFive V2**
  - **Sophgo Server（SG2042）**
- **Koji with real hardware**

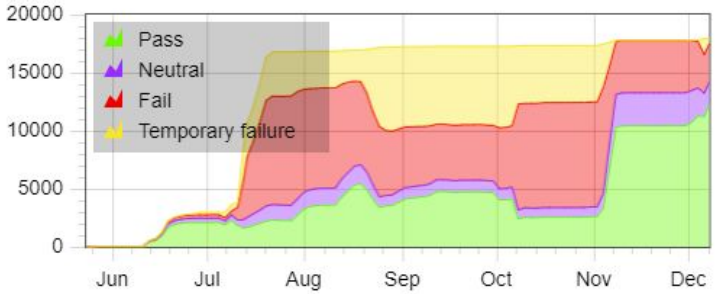
Debian for RISC-V I（于波）

- Buildd status&news

  1. Installed: 15510+ (llvm-toolchain-15)

  2. Udd FTBFS packages ~264

  3. Official porting news (no reply)



- Debci update

  Britney's Job Hostory

- Some works

  1. https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1024801 [dds2tar QA RC done]
  2. https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1024991 [jamulus QA upload done]

Debian for RISC-V II

3. https://salsa.debian.org/mentors.debian.net-team/debexpo/-/merge_requests/198 [MR merged]
4. https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1025228 [clblas upload done]
5. https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1025376 [libcds patch]
6. https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1022526 [python-ssdeep RC done]
7. https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1024877 [python-softlayer RC done]
8. https://bugs.debian.org/cgi-bin/bugreport.cgi?bug=1004547 [binutils-riscv64-linux-gnu issue done]
9. https://sourceware.org/bugzilla/show_bug.cgi?id=29858 [glibc bug]

Deepin for RISCV

Deepin-riscv-stage2:

succeeded: 5266 failed: 179 unresolvable: 1100

升级gcc/binutils/glibc/base-files 重构工具链解决pie相关问题

deepin-riscv-board：增加unmatched支持 升级d1内核

FW相关更新（王翔）

- opensbi
  - 有关fdt的一些修正，主要是移除重复的参数检测和数据类型修正以及错误检查。
  - 根据编译器版本选择使用.word和.insn使反汇编易于查看（作为库时存在问题，编译库的工具链和最终编译目标软件的工具链可能不同）
  - 对AE350添加通用平台支持
  - 修正plic优先级的保存和恢复，因为中断号0被保留
  - 优化重定位（把程序拷贝到正确的位置），移动了一个跳转减少不必要的计算
  - opensbi原本通过原子操作随机选择boot hart，添加宏用于指定boot hart（还在扯皮）。
  - gitignore添加vim swap文件
  - debug trigger更新，添加type2支持，大小端支持（通过构体位域实现csr定义带来的大小端问题，可以通过位操作规避）
  - PMP设置需要与虚拟内存系统同步，sbi_hart_pmp_configure添加同步指令
  - 在fw_platform_lookup_special中使用fdt_match_node替代fdt_find_match使代码更简洁
  - 修正fdt_parse_region，防止移位溢出
  - 修正__fdt_parse_region，修复错误检测的逻辑错误
  - 为__fdt_parse_region函数添加完整的有效性检测，原本的函数只检测region->order

固件相关更新(洛佳)

- opensbi不再是risc-v sbi标准的参考实现
  - https://github.com/riscv-non-isa/riscv-sbi-doc/pull/104

香山开源RISC-V处理器 - ICT / PCL

- 南湖流片进展
  - 修复 ICache prefetch entry 未加入 TL 总线 id 范围带来的事务混淆问题
  - 修复 RISC-V Debug Mode 相关功能实现
  - 修复 MMU 指针位宽问题
  - 修复 HuanCun 在双核场景下的若干 Bug
- 昆明湖开发进展
  - 前端：Loop Cache 接入处理器核进行调试；FDIP 预取器进一步改进
  - 后端：完成向量浮点符号迁移、Merge、Classify 等运算单元的设计；保留站后读寄存器通过基础测试
  - 访存：实现非阻塞的 L1 DCache Mainpipe，推进load指令重发机制的修改和路预测框架的搭建
  - 缓存：Coupled L2完成 TL 个请求的基本数据和控制通路，正在设计处理数据冒险与请求嵌套相关逻辑

MLIR RISC-V Vector (RVV) Dialect Proposal - 张洪滨

相关链接

- RFC Patch - https://reviews.llvm.org/D108536
- RFC Post - https://discourse.llvm.org/t/rfc-add-risc-v-vector-extension-rvv-dialect/4146/32
- MLIR + RVV 集成测试环境搭建文档 - https://gist.github.com/zhanghb97/ad44407e169de298911b8a4235e68497
- MLIR + RVV 环境搭建 - https://github.com/buddy-compiler/buddy-mlir/blob/main/thirdparty/build-rvv-env.sh
- MLIR + RVV 相关实验 - https://github.com/buddy-compiler/buddy-mlir/tree/main/examples/RVVExperiment

WIP

- MLIR Vector Dialect Dynamic Vector Length Support Proposal
- Add more VP intrinsic integration test cases (fixed & scalable vector)
  - Context：[mlir] Initial MLIR VP intrinsic integration test on host and RVV emulator.
    https://reviews.llvm.org/rGee82b864f2086f944f046bd00b03f30697403f8a

Chisel and Additional Technology / Sequencer

- Chisel
  - Chisel 3.6.0-M1 发布
  - SerializableModuleGenerator
    - https://github.com/chipsalliance/chisel3/pull/2857
- chisel-circt-binder
  - https://github.com/llvm/circt/pull/4404
- RocketChip
  - Scala更新到2.13
- Vector
  - vadd测例在vector上仿真通 过

OpenHW & OpenHW Aisa Working Group

- 在TWG介绍了LLVM开发the initial draft of LLVM Plan Approved pull request
-

自由讨论 / AOB

- 终于开放了国内省际自由行！国际出入境自由还远么？
- 下周北美RISC-V峰会
- 下下周圣诞节？
- 下下下周新年？
- 下下下下周春节？

BACKUP

准备加入更多的国际开源组织进行同步观测

欢迎追加或提议

CHIPS Alliance

风平浪静