

程序代写代做 CS 编程辅导

COMP2300/6300

Computer Organisation and Programming



Digital Logic

Dr Charles Martin

Semester 1, 2022



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Week 1: Boolean algebra

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George Boole

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It starts with a thought

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An Investigation of the Laws of Thought, Which Are Founded on the Mathematical Theories of Logic and Probabilities by George Boole



Which are Founded on the Mathematical Theories of

54

You can still buy it from [Amazon](#)

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Boole's big idea: **true & false are all you need**

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What is Boolean algebra? 程序代写代做 CS编程辅导

Algebra is the study of mathematical symbols and the rules for manipulating these symbols; it's about **variables** like a and b and **operators** like \wedge (binary *and*), \vee (binary *or*), \neg (unary *not*, sometimes represented with an overline e.g. \bar{q}).



Boolean means that all variables & expressions can take one of two values. We can call them **true** and **false**, **1** and **0**, or **Mary** and **Mengyuahn**; it doesn't matter.

Boolean algebra builds expressions with these basic building blocks, e.g.

$$\neg(a \wedge b) \vee c$$

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this is all revision from MATH1005, so we're
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gonna speed through

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Truth tables

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Truth tables are just a convenient way of enumerating all the possible values our variables can take. If you've got n variables, you need 2^n rows in your truth table (why?)



Here's an example with 2 variables:

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a	b	$a \wedge b$
T	T	T
T	F	F
F	T	F
F	F	F

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Other handy Boolean operators



a **implies** b

a **equivalent to** b

a **exclusive or/xor** b

a **not and/nand** b

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a **not or/nor** b

$$\neg(a \wedge b) = (\neg a \vee \neg b)$$

$$\neg(a \vee b) = (\neg a \wedge \neg b)$$

You can reduce any Boolean expression to only NAND or only NOR operators (**try it and see!**).

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Logic functions

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You know about functions from

$$f(x, y) = x^2 \sin(y)$$



here's a two-argument function of $x, y \in \mathbf{R}$

We can have functions of Boolean variables a and b as well:

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$$g(a, b) = \dots$$

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$f(x, y) = \dots$

$g(a, b) = \dots$



Can you think of anything we can do with the Boolean function $g(a, b)$ that we can't do with the real-valued function $f(x, y)$? **WeChat: cstutorcs**

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Full binary operator truth table



	Inputs a, b				Function	Name	of products	NAND	Don't cares
a	F	F	T	T					
b	F	T	F	T					
q	F	F	F	F	False	Constant F			a, b
	F	F	F	T	$a \wedge b$	AND	$\overline{a \wedge b} \wedge \overline{a \wedge b}$		
	F	F	T	F	$\overline{a \rightarrow b}$	NOT-IMPLICATION	$(a \wedge \overline{b})$		
	F	F	T	T	a	IDENTITY a			b
	F	T	F	F	$\overline{a} \wedge b$				
	F	T	F	T	b	IDENTITY b			a
	F	T	T	F	$a \oplus b$	EXCLUSIVE-OR, XOR	$(a \wedge \overline{b}) \vee (\overline{a} \wedge b)$		
	F	T	T	T	$a \vee b$	OR	$\overline{a \wedge \overline{a}} \wedge \overline{b \wedge b}$		
	T	F	F	F	$\overline{a \vee b}$	NOT-OR, NOR	$(\overline{a} \wedge \overline{b})$		
	T	F	F	T	$a = b$	EQUALITY, EQ	$(a \wedge b) \vee (\overline{a} \wedge \overline{b})$		
	T	F	T	F	\overline{b}	INVERSE b			a
	T	F	T	T	$a \vee \overline{b}$				
	T	T	F	F	\overline{a}	INVERSE a	$\overline{a \wedge a}$		b
	T	T	F	T	$a \rightarrow b$	IMPLICATION	$\overline{a} \vee b$		
	T	T	T	F	$\overline{a \wedge b}$	NOT-AND, NAND	$\overline{a \vee b}$		
	T	T	T	T	True	Constant True			a, b
Output q									

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What does this have to do with my microbit?

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Logic gates

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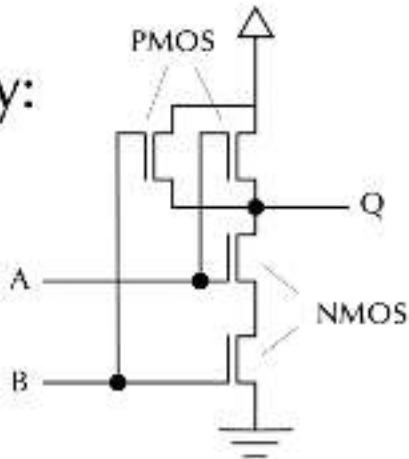
Symbolic: $Q = \overline{A \wedge B}$

Diagram:



\equiv

Technology:



Learn more about logic gate symbols:



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How does your computer add 1+1?

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How would a 5yo do it?

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Number representations

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Remember that an integer can be represented in a different “base” (or “radix”), e.g. binary (base-2), octal (base-8), hexadecimal (base-16) or the familiar decimal (base-10).



Decimal	0
Hex	0x 0000 0000
Binary	0b 0000 0000 0000 0000 0000 0000 0000

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Note: hex & binary padded to 32-bit, negative numbers represented with 32-bit two's complement

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Combinational logic Assignment Project Exam Help

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Let's start simple: 1+1

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Consider the Boolean function $s = a + b$ (the s is short for *sum*). How would we put this in a (pseudo) truth table?



a	b	s
0	0	0
0	1	1
1	0	1
1	1	2

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Not quite...

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This doesn't really work because we have *three* distinct values (0, 1 and 2) in Boolean algebra. But what if we just consider the "carry column" of the addition?



a	b	s
0	0	0
0	1	1
1	0	1
1	1	0

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Add a c (carry) column

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a	b			
0	0			
0	1			
1	0			
1	1			



s	c
0	0
1	0
1	0
0	1

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bit == binary digit
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But what is $s(a, b)$?

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The truth table *is* a complete specification of the function $s(a, b)$ that we're interested in, but it doesn't tell us how to express $s(a, b)$ using the rules we looked at earlier.



a	b	s	c	s minterms
0	0	0	0	
0	1	1	0	$\neg a \wedge b$
1	0	1	0	$a \wedge \neg b$
1	1	0	1	

$$s = (a \wedge \neg b) \vee (\neg a \wedge b) = a \oplus b$$

$$c = a \wedge b$$

c minterms

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So far...

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Combinational Logic:



lets us make a Boolean expressions for any truth-table

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Boolean Algebra:

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lets us simplify Boolean expressions to something manageable

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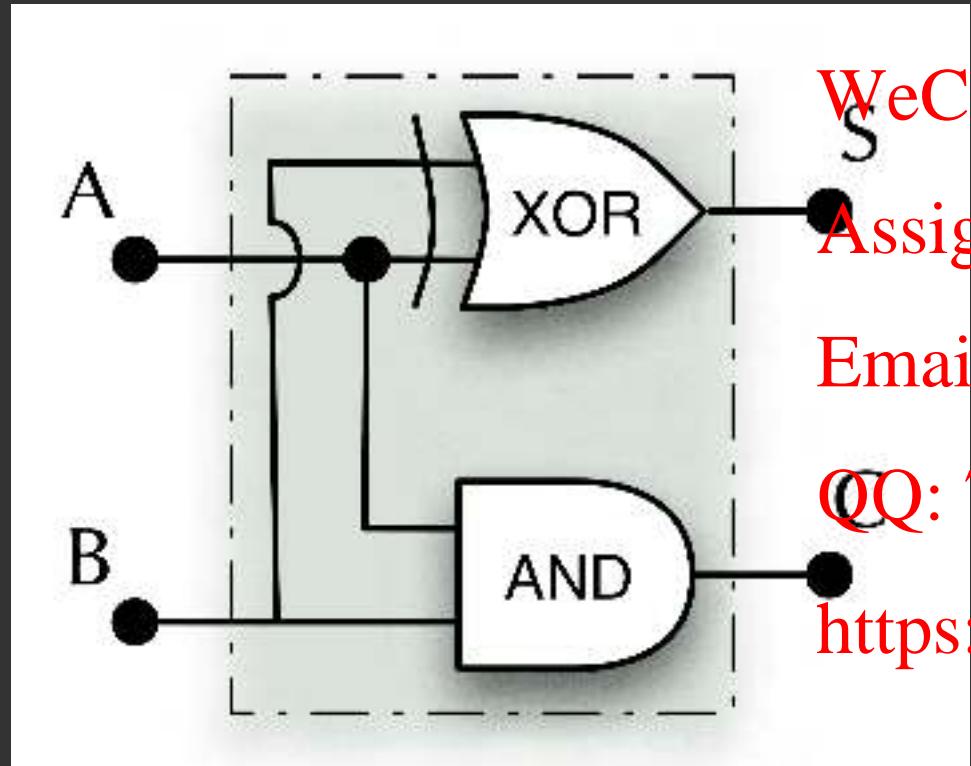
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Half-adder

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$$s = a \oplus b$$

$$c = a \wedge b$$



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DLS: Digital Logic Simulator



DLS is a time-driven event-based Java 3-value digital logic simulator.

There's both **desktop** (cheap) & **mobile** versions.

DLS isn't compulsory for the course, but it's a nice way for me to demo things.

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Demo: Half-adder

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Full-Adder

What about carry in?

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What's missing with the half-adder? The carry in (ci) as well as carry out (co).

a	b	ci	s	co
0	0	0	0	0
0	1	0	WeChat: cstutorcs	0
1	0	0	1	0
1	1	0	Assignment Project Exam Help	1
0	0	1	1	0
0	1	1	Email: tutorcs@163.com	1
1	0	1	0	1
1	1	1	QQ: 749389476	1



$$s = (a \wedge \neg b \wedge \neg ci) \vee (\neg a \wedge b \wedge \neg ci) \vee ((a \wedge b) \wedge ci) \vee ((a \wedge b) \wedge \neg ci)$$

$$= (((a \wedge \neg b) \vee (\neg a \wedge b)) \wedge \neg ci) \vee (((\neg a \wedge \neg b) \vee (a \wedge b)) \wedge ci)$$

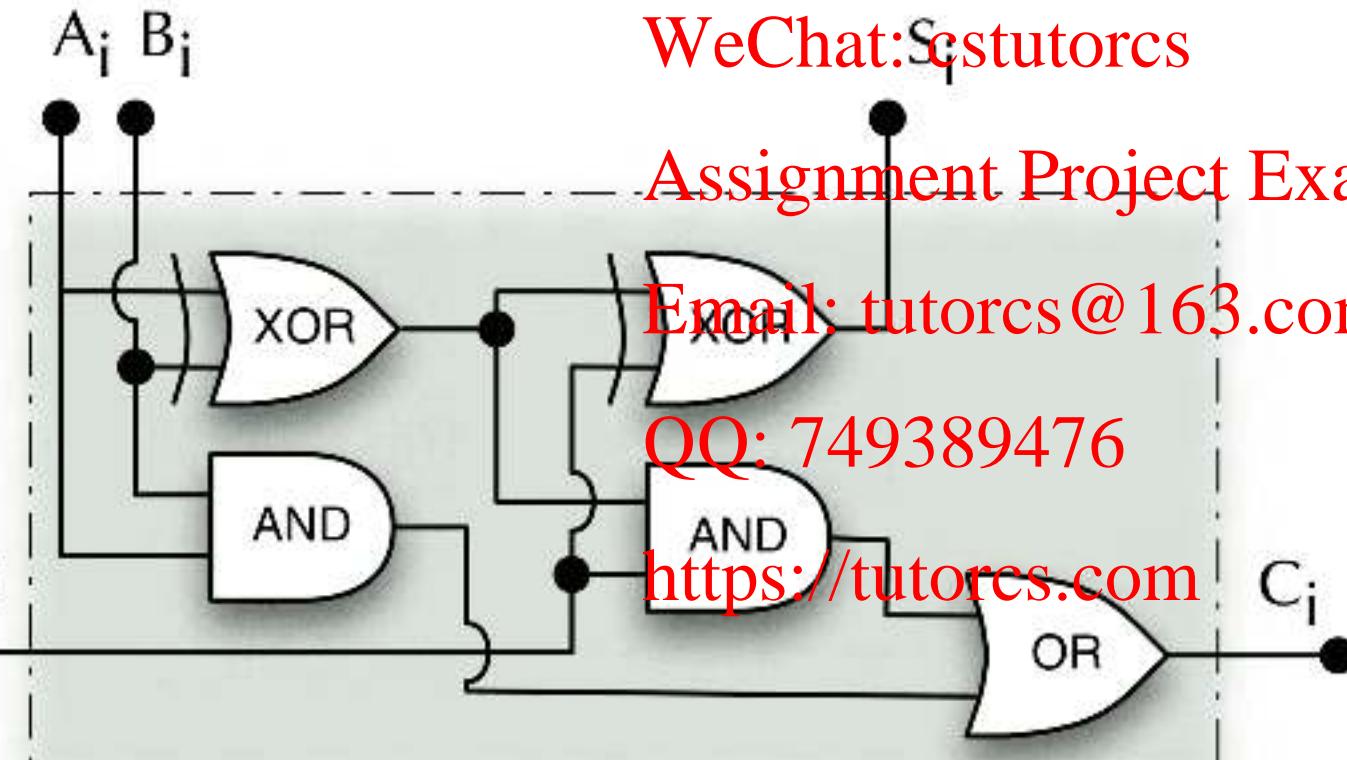
$$= ((a \oplus b) \wedge \neg ci) \vee ((a = b) \wedge ci)$$

Full-adder

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$$\text{cout} = (a \wedge b) \vee ((a \oplus b) \wedge \text{cin})$$

(trust me!)



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Demo: Full-adder

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Ripple-carry adder

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We can join them together like so:



1. how many bits can be added together?
2. how long does it take?



3. where does the final carry bit go?

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What about subtraction?

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We've got two options:

1. do some more minterms stuff



2. trick the full *adder* into subtracting things instead

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show of hands?

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Twos complement representation

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The basic idea: can we define (bi)



tive numbers such that our adder still works?

0	0	1	0	1	0	1	0	0
---	---	---	---	---	---	---	---	---

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?	?	?	?	?	?	?	?
---	---	---	---	---	---	---	---

-42

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1	0	0	0	0	0	0	0	0
---	---	---	---	---	---	---	---	---

256

Twos complement representation



0	0	1	0	1	0	1	0
---	---	---	---	---	---	---	---

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1	1	0	1	0	1	1	0
---	---	---	---	---	---	---	---

-42

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1	0	0	0	0	0	0	0
---	---	---	---	---	---	---	---

256

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The twos complement “circle”



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Quiz: negative or positive?

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0b10



0b011011

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0b011011101110101010010

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0b1011000000000011101111111101010000000001010101

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it's all in your mind
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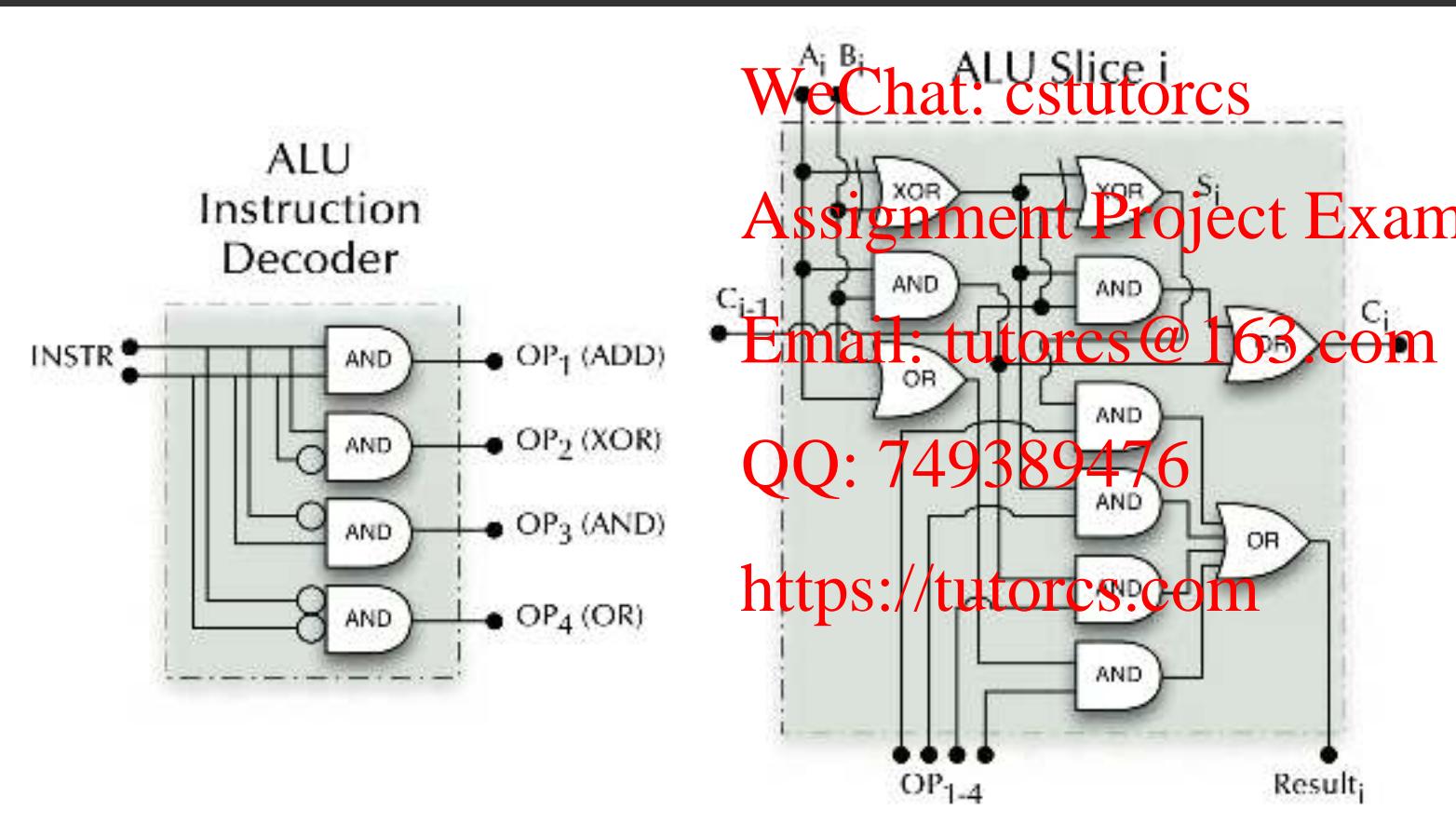
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Simple ALU

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A simple ALU (Arithmetic & Logic Unit) which can ADD, XOR, AND, OR two arguments.



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Sequential logic

What does it mean for a computer to have **memory**? Can the combinational logic functions we've looked at so far *remember*?



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Sequential == state-oriented 程序代写代做 CS 编程辅导

This makes intuitive sense—the feedback loop allows the current output to be fed back in (as input).



Sequential logic circuits can no longer be treated as “pure” input-output black boxes—they carry “state” (i.e. the **sequence** of inputs matters).

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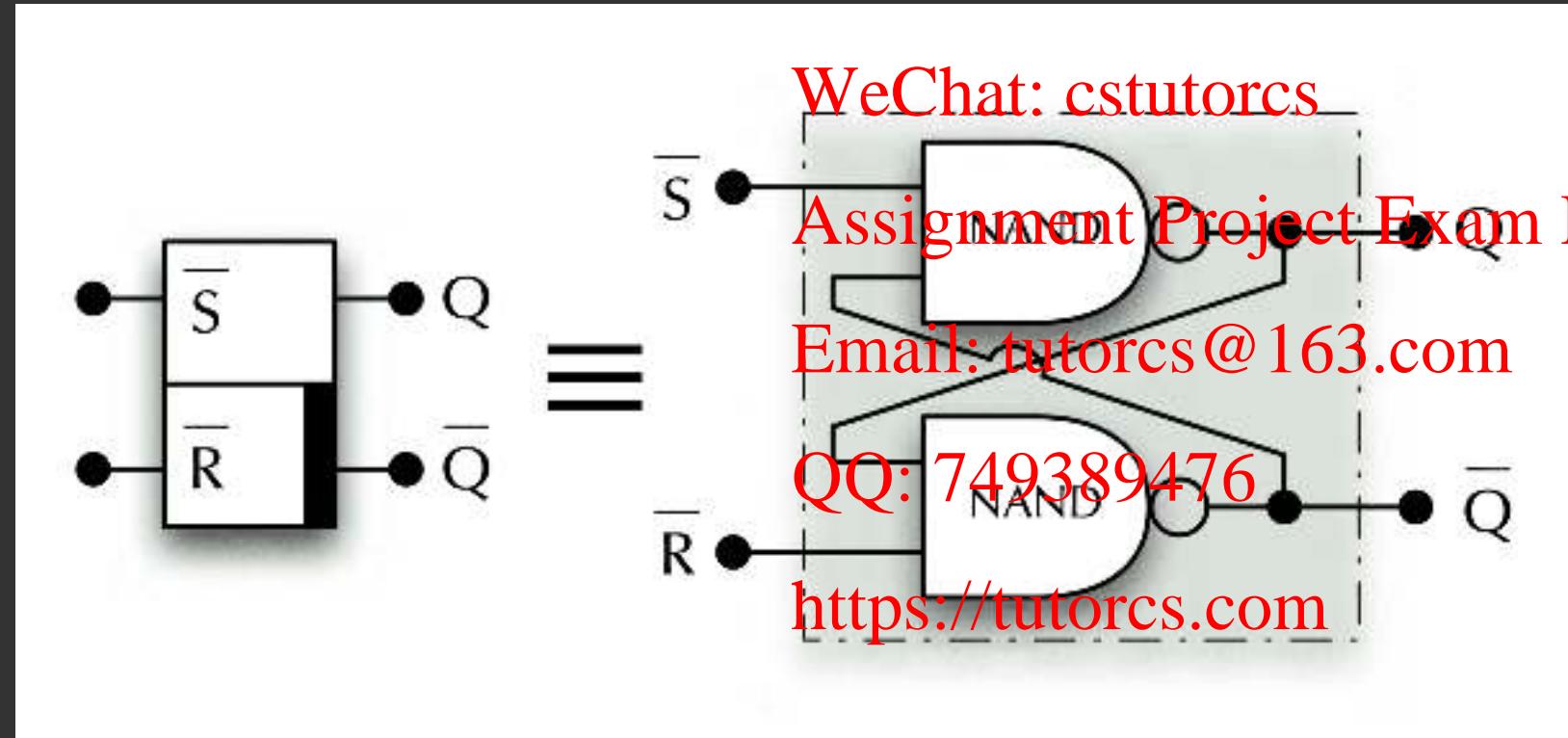
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SR latch

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S (set), R (reset)



stackexchange asks: “Why is the output of stateful elements often named Q?”

SR input

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There are four possible input combinations:

$\neg s \quad \neg r \quad effect$

1 1 keep current state q

0 1 set q (to 1)

1 0 reset q (to 0)

0 0 **forbidden** (q and $\neg q$ both set to 1)



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Demo: SR latch

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Problems with the SR latch



1. the forbidden thing (this is obviously not a problem)
2. there are some tricky timing issues (you have to use physics: remember, there are *real* electrons flying around)
3. have to keep changing inputs...

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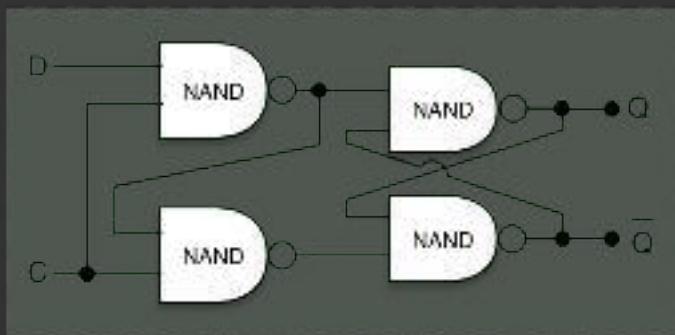
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Gated D latch

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The gated D latch uses an *enable* signal (*C*) so that the latch is set only when you want it to be.



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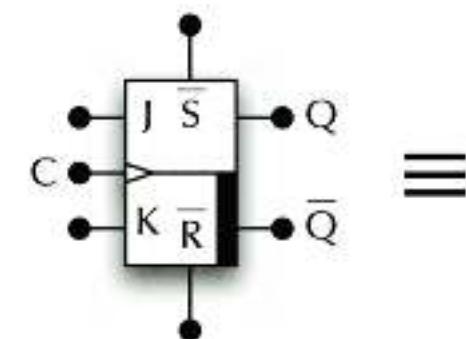
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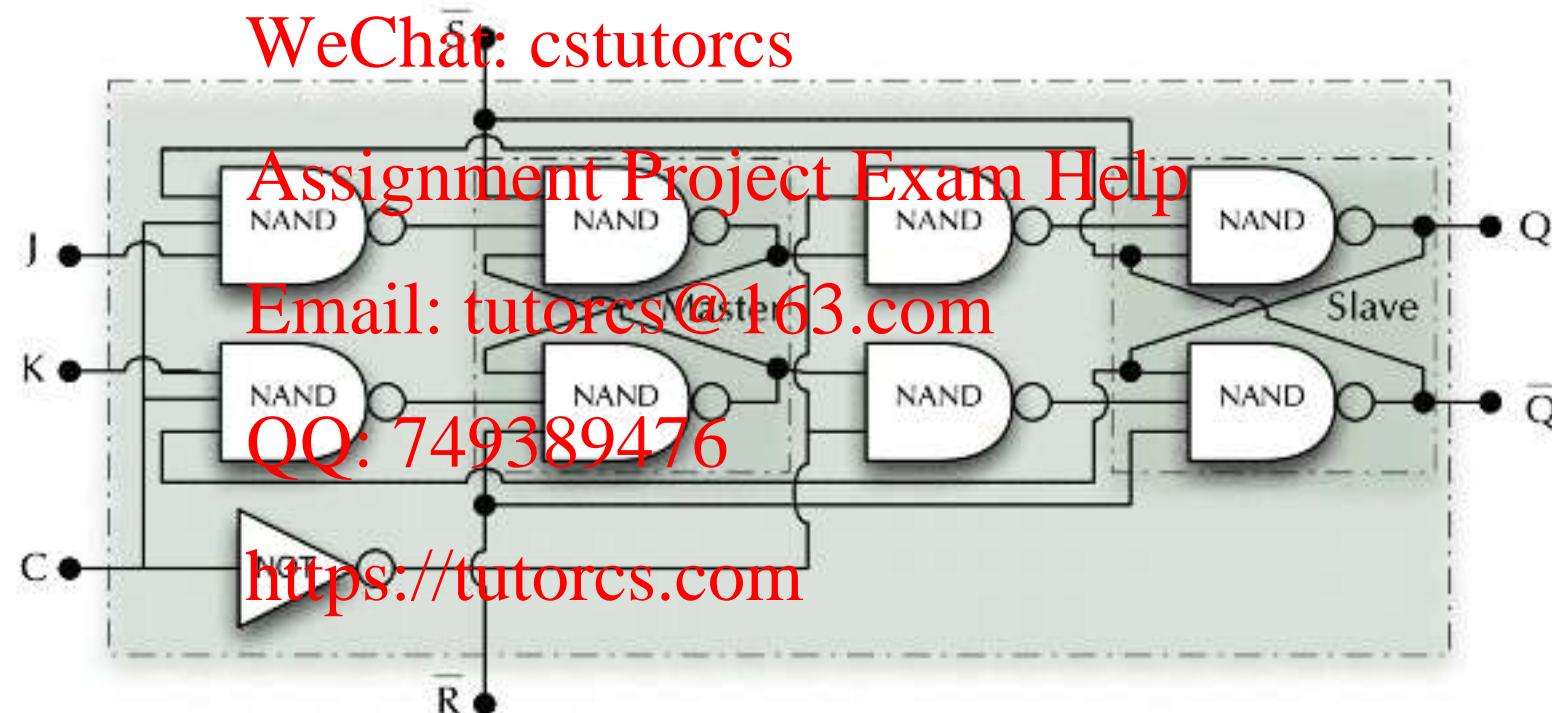
JK master-slave flip-flop

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Better again, set/reset on a *clock* (C). No race problems, no forbidden inputs, toggle operation (although it's a more complex circuit).



=



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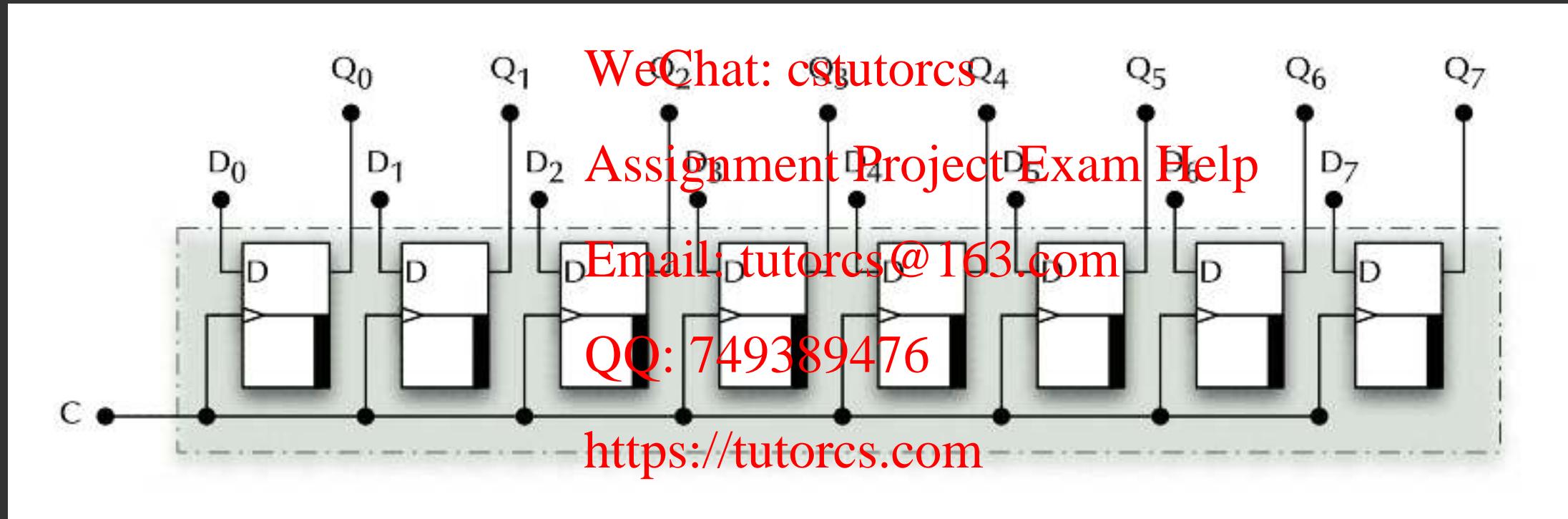
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Register

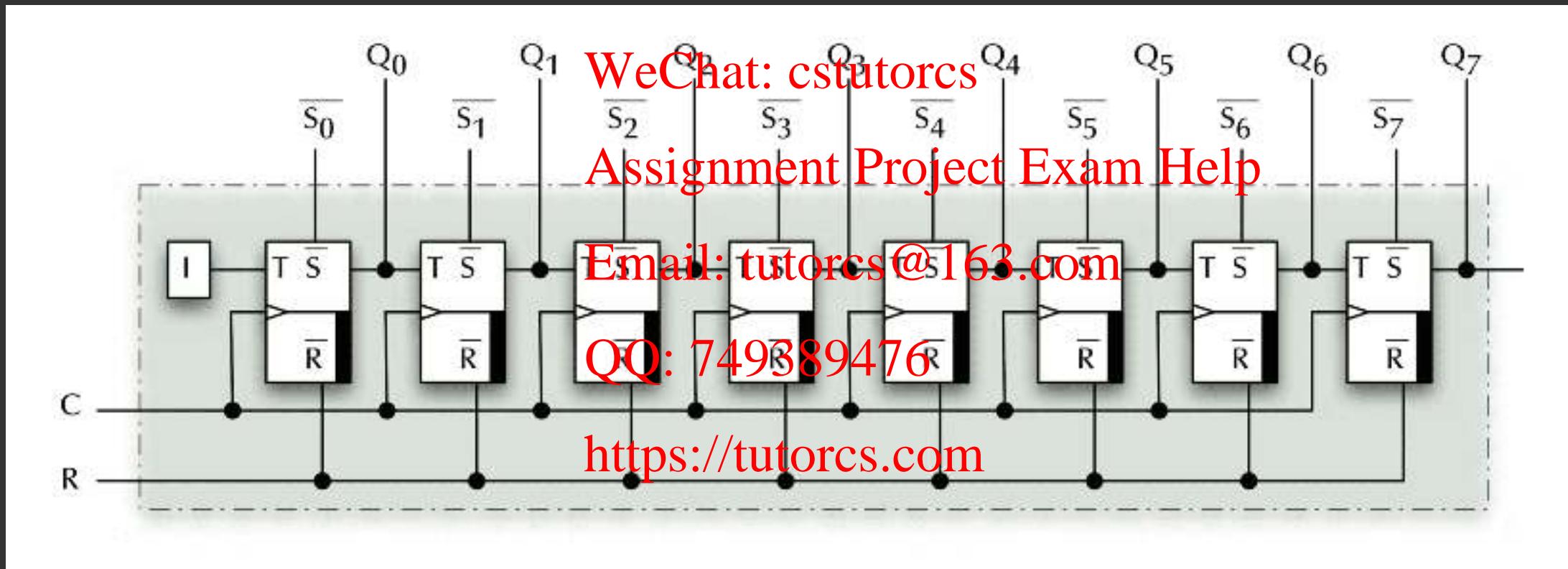
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Store multiple bits, can serve as purpose *fast* on-CPU storage, or hold state for peripherals, etc. Note the shared



Counter

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Feeling lost?

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These are all physical components of a computer.



There's no magic (!), just these **billion** of these little mathematical machines.

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Further reading

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Plantz: Introduction to Computer Organization chapters 5-7



Patterson & Hennessy Appendix A “The Basics of Logic Design”
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EEVblog Intro to Digital Logic (YouTube)
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Ben Eater: Logic Gates, SR Latch, D Latch, T Flip Flop, JK Flip Flop
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Questions

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