NAS-GEM-80 EPROM CARD

Instruction Manual & Functional Description

Contents

1 Introduction

This card has been designed to replace the use of 2708/2716 EPROM's with the more readily available and simpler to program 2732 / 2764 devices. The board support up 5 devices or 4 devices and the original 8K Basic ROM. Both a 2732/2764 EPROM and the Basic ROM may be present on the card simultaneously, with the active device being selected via a switch

Each device may be decoded to any 4K boundary, with a typical configuration being:

- 2732 decoded to D000 for NAS-DOS
- 2732 decoded to C000 for NAS-DIS & NAS-DEBUG
- 2764 decoded to E000 / F000 for 8K BASIC

The card also supports the Nascom Page Mode functionality, with any of the four pages being selectable via a DIL switch. If page 0 is selected then the card will be enabled at power up / reset.

The Page Mode functionality may also be disabled if required via a switch selection

NAS I/O selection is available via a link/switch. This allows I/O on a Nascom to function correctly

M. EXT is supported for Nascom 1 usage. This is selectable via a link

If the original 8K Basic ROM is being used, be aware that no wait states are generated on this card. Some slow devices may not function correctly without the use of wait states.

2 Components

Reference	Quantity	Value
Capacitors		
DC1 DC2 DC3 DC4 DC5 DC7 DC8 DC9 DC10 DC11 DC12 DC13 DC14 DC15 DC16 DC18 DC19	17	10nF
Tant1 Tant2 Tant3 Tant4 Tant5 Tant6 Tant7 Tant8 Tant9 Tant10	10	10uF
Resistors		
R2 R3 R12	3	1K
R13 R18	2	4K7
R1 R4 R15	3	330
R5 R6 R7 R8 R9 R10 R11 R14 R16 R17	10	2K2
IC's		
U1 U3 U5	3	74LS244
U10	1	74LS04
U100 U101 U102 U103 U201	5	2764
U11	1	74LS00
U12	1	74LS30
U200	1	MK36000_8K_ROM
U4	1	74159
U6	1	74LS175
U7	1	74LS32
U8	1	7406
U9	1	74LS20
Sockets		
U10 U11 U12 U7 U8 U9	6	DIP 14 IC socket
U6	1	DIP 16 IC socket
U1 U3 U5	3	DIP 20 IC socket
U2 U200 U4	3	DIP 24 IC socket
U100 U101 U102 U103 U201	5	DIP 28 IC socket
Other Items		
PCB	1	8x8 PCB
D1 D2 D3 D4 D5	5	LED (3mm)
Q1	1	2N3904
SW1	1	6 Way DIP
SW2	1	ERG SCS-2-023
U2	1	Decode Header

3 Construction

3.1 Before you start construction

Inspect the PCB for any damage

Plug the board into an 80-BUS and power it up. Verify no latent shorts exist

Select your components:

- Turned pin sockets are recommended due to robustness and reliability
- The resistors / LED's for power indication are purely optional and may be left out
- Tantalum capacitors can be temperamental. Make sure they are inserted with the correct polarity, are of good quality and are overrated voltage wise.

3.2 Order of construction

The recommended order of construction is:

- Resistors
- Decoupling capacitors
- Sockets
- Tantalum capacitors
- Switches
- LED's
- Transistor
- Wire header
- Insert IC's

4 Functionality

4.1 Page mode

The page mode logic is based around latching 4 data bits into U6 (74LS175- Quad flip flop) whenever a write is made to port FF. The bits represent the page to be selected / deselected. A page 0 select signal is generated from U11A when a reset is performed. This is cleared on the first write to port FF via the latching signal generated from U7D.

4.2 Memory Decode

Memory is decoded into 4K chunks, represented on the U2 decode header. This allows any 4K / 8K chunk to be assigned to any EPROM via links on this header. The top 4 bits of any address presented via U5 are fed to U4, a 74159, a 4-bit decoder / de-mux. Each of the resulting 16output bits represents one 4K block. These are then wired via the header to Bank 1 / 2 /3 / 4 / 8K ROM selects which in turn go to the OE pins on the memory devices.

4.3 Data Read

All data to be read is fed via U1 (Octal buffer). Output enable is controlled by merging BMREQ, BRD, bank select outputs (Via U9A), and the page select via U6 and SW1.

5 Switches

5.1 SW1 – Page Select

This switch selects which page the board is to respond to. This is set via SW1 / 2/ 3/ 4

SW5 selects that page mode functionality is enabled / disabled

SW6 selects that the board ignores page mode operation and is always selected.

Only one of SW5 / SW6 should be selected at once.

5.2 SW2 – BROM / EPROM Select

This switch allows selection between either U200 (Basic ROM) or U201 (2732/2764 EPROM). A wire link may be substituted if only one device is required. (e.g. The Basic ROM is not used)

5.3 JP1 – NASIO Select

This allows the board to generate the NASIO signal if required. Only one board in the system should generate this signal.

Either a switch or wire link may be installed here depending on the requirements to generate NASIO.

6 Notes on Components

All the components used have been selected at time of design to be readily available via eBay and other sources.

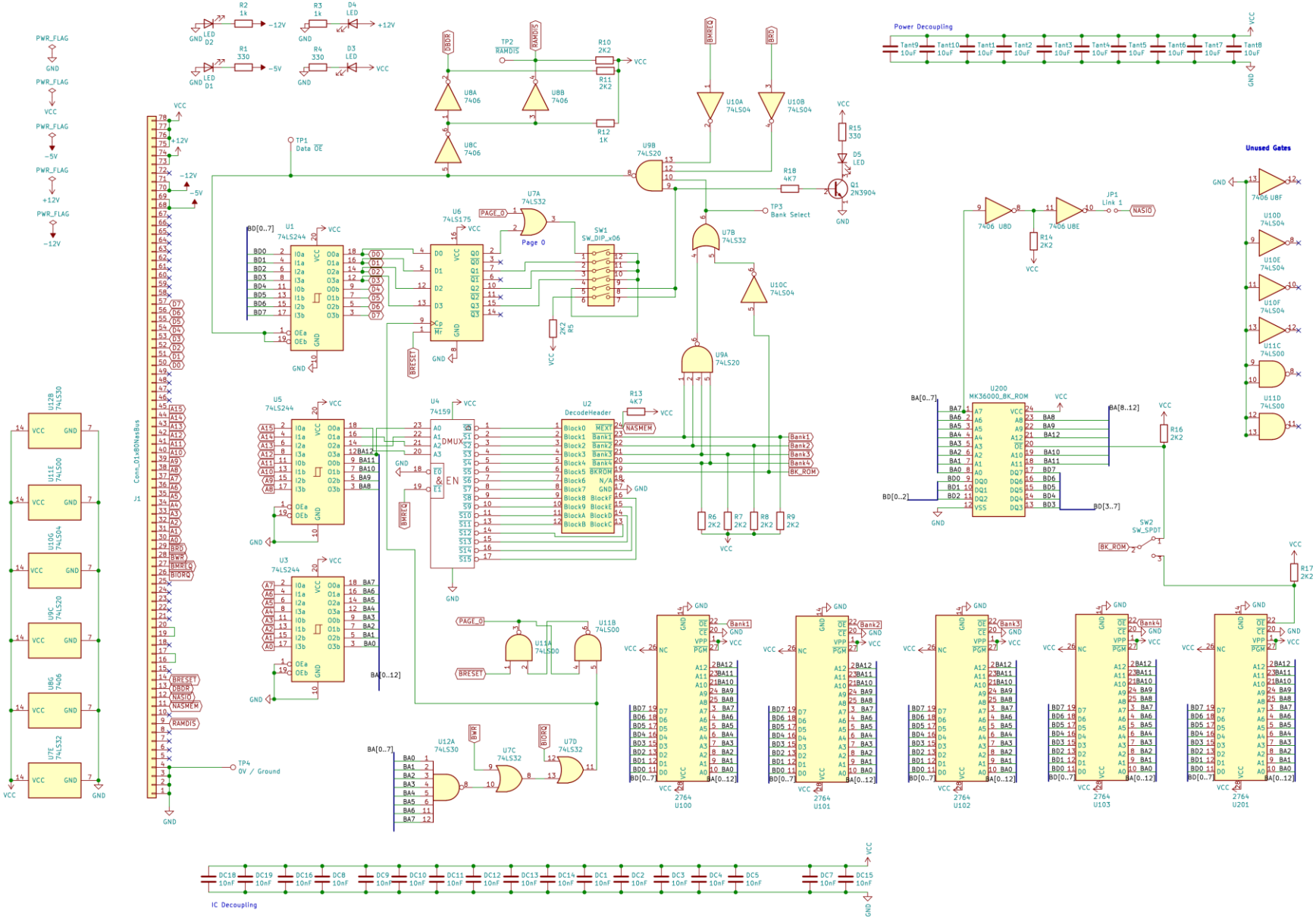
6.1 SW2 – BROM / EPROM Select

This switch is an **ERG SCS-2-023** device. While this can be purchased from various sources, they are not cheap. It is suggested that a wire link is used, and the switch is only considered if the ability to switch between EPROM and Basic ROM is a requirement.

6.2 U2 Decode Header

The socket at U2 should is recommended to be of the turned pin variety so as to allow easier insertion of the header. The default header to fit the 24-way DIL socket is the Cambion 24 Pin DIL IC Type Adapter. While readily available, these are very expensive for what they are and suitable replacement has not been identified.

An alternative is to use Single In Line (SIL) Turned Pin Socket 0.1 Inch Pitch strips which are readily available instead of a header. These are then snipped down to the desired length before being inserted into the socket and the desired wire links being made.


Power Decoupling
Unused Gates
IC Decoupling
Page 0
Bank Select
MK36600_BK_ROM
DecodeHeader
Conn_01x80NexBus
2764
U100
U101
U102
U103
U201

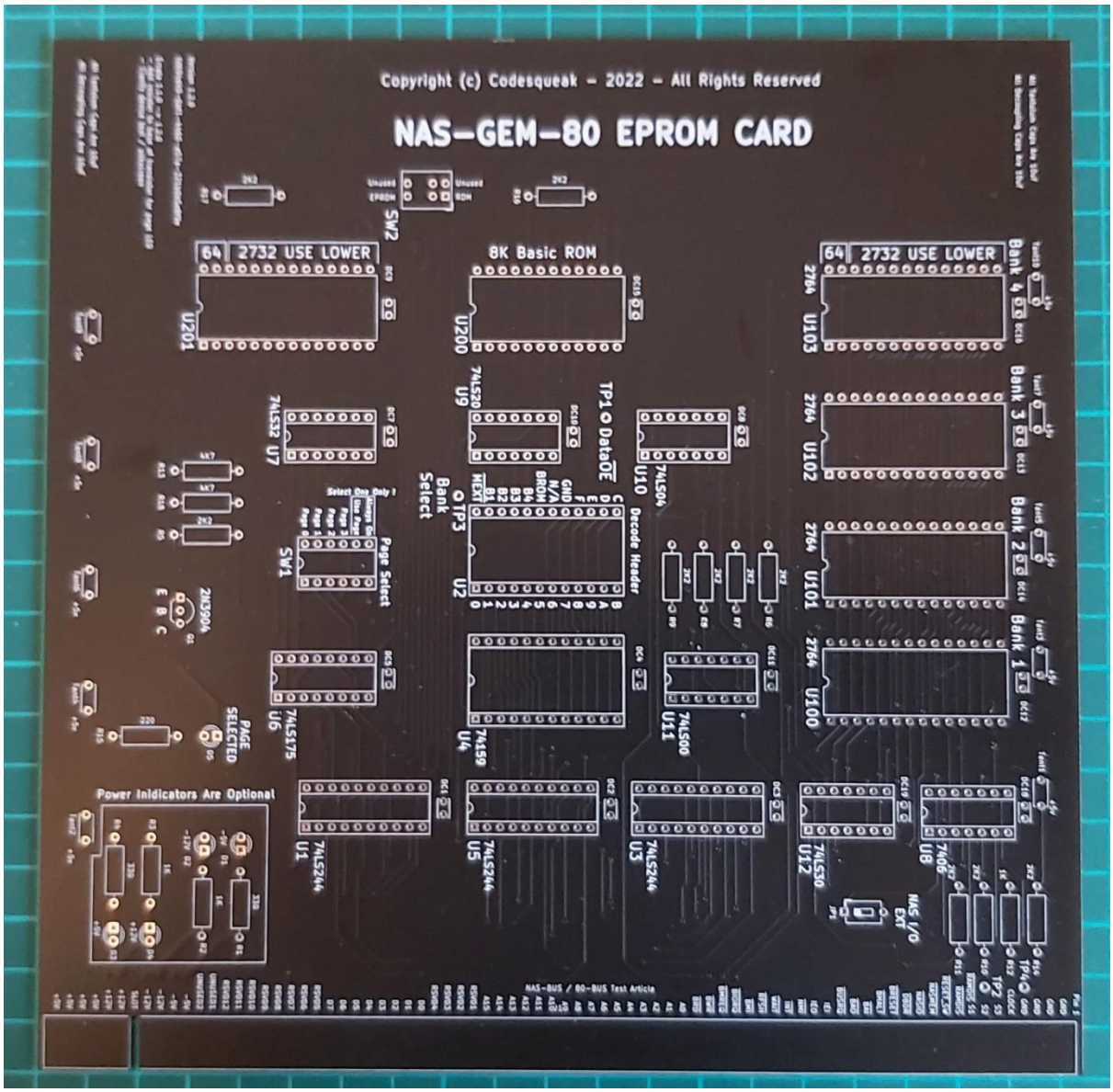
1. Errata

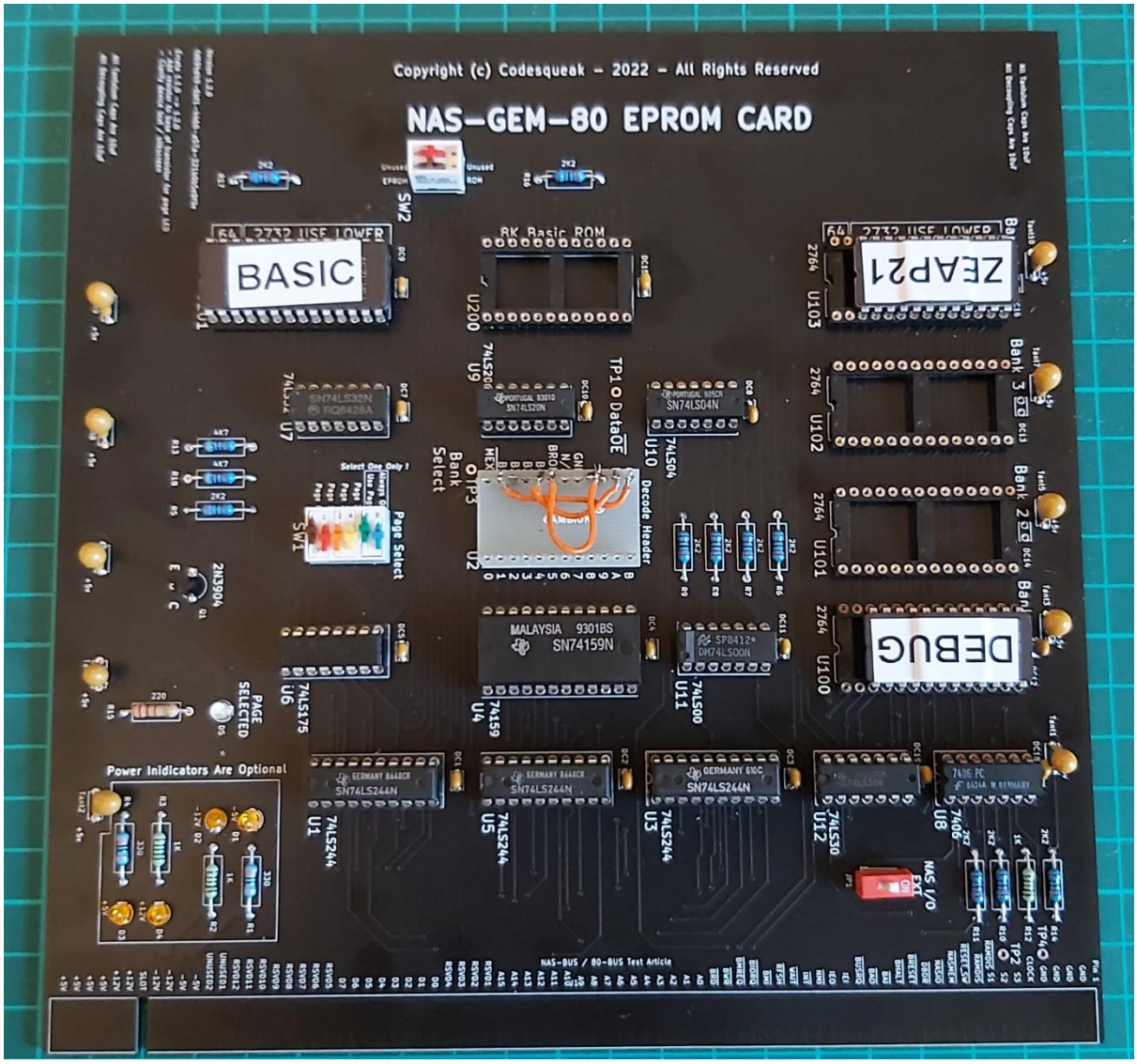
Initial release boards have the decoupling capacitors labelled as 10uF instead of 10nF

R3 is labelled as 220 Ohms. A 330 Ohms resistor may be used if the page select indicator LED is too bright

2. Reference Images

Photo …

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NAS-GEM-80 EPROM CARD
BASIC
ZEAP21
DEBUG
RK Basic ROM
Decode Header
Bank Select
Page Select
PAGE SELECTED
Power Inidicators Are Optional
NAS I/O EXT
NAS-BUS / 80-BUS Test Article