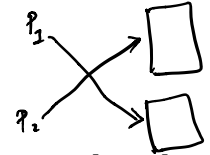


MEMORY PROTECTION IN PAGING



- Protection bits can be associated along with the frame number in the page table
- One protection bit can be defined to check whether the page is read only page or not.
- Another bit called valid-invalid bit can be associated with the page table to check whether a page exists in process logical address space or not

frn | v/i
3 | 0

Assume that the system has 4-bit logical address space.
page size = 4 bit

page 0	a	0
	b	1
	c	2
	d	3
page 1	e	4
	f	5
	g	6
	h	7
page 2	i	8
	j	9
	k	10
	l	11
page 3	m	12
	n	13
	o	14
	p	15

Logical address

→ 0	1	v
→ 1	3	v
→ 2	5	v
→ ③	0	i

page Table

frame 0		0
		4
frame 1	a	page 0
	b	
	c	
	d	
		7
frame 2		11
frame 3	e	page 2
	f	
	g	
	h	
		15
frame 4		19
frame 5	i	page 3
	j	
	k	
	l	
		23

physical address

10 bytes 16 bytes

→ ③ ≥ ③ →

- Any reference to page number 3 in the page table will cause segmentation fault
- The program extends only till logical address 9. What if we try to access memory location 10?

(0-15) (0-9)

● Drawback: Rarely does a program use all its address range. It would be a huge waste of memory if we keep a page table entry for every page in the address range

● Some systems provide hardware support in form of page-table length register (PLTR) to indicate the size of the page table

● If page number \geq PLTR, segmentation fault is raised

OTHER IMPORTANT BITS ASSOCIATED WITH PAGE TABLE

● Referenced bit - whether the page was accessed in the last clock cycle or not

● Dirty or modified bit - whether the page has been modified or not

● Cache enables/disabled bit - whether caching is enabled for the page or not

