OPAL-RT Tutorial

DCES, TU Delft

Back-to-back Modular Multilevel Converters

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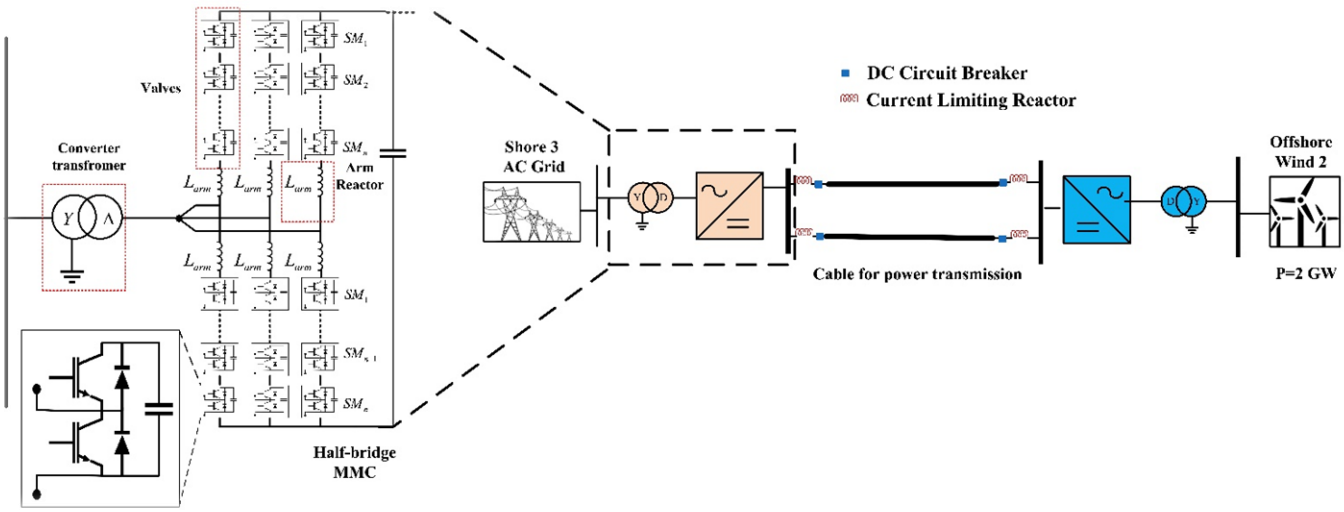
Introduction:

The conventional two-level or three-level VSCs for power conversion result in high switching losses and unimproved AC waveform. These drawbacks were observed and the idea of multilevel converters was developed in 2000 by Professor R. Marquardt. Modular multilevel converters (MMCs) have different attributes like scalability and modularity compared to conventional two or three-level VSCs. The scalability allows the facility to scale up or scale down the voltage levels to any desired level and modularity makes the maintenance easy. Unlike the two-level or three-level VSC, the MMC type converter has:

- low switching losses,
- lower harmonic contents,
- better fault blocking capability
- high reliability
- No need for huge filters at the AC side as a result of good quality waveform



In this tutorial, we will try to understand the basics of control for MMC based grids. The possible configurations using such MMC setup can be medium voltage or high voltage DC power systems. Furthermore, using a back-to-back MMC configurations to form HVDC power grid as the test system, the concept is extrapolated for multiple MMC control. Real-time digital simulations using OPAL-RT (with RT-LAB environment) are used to validate the control schemes. At the end of this tutorial, you should be able to:

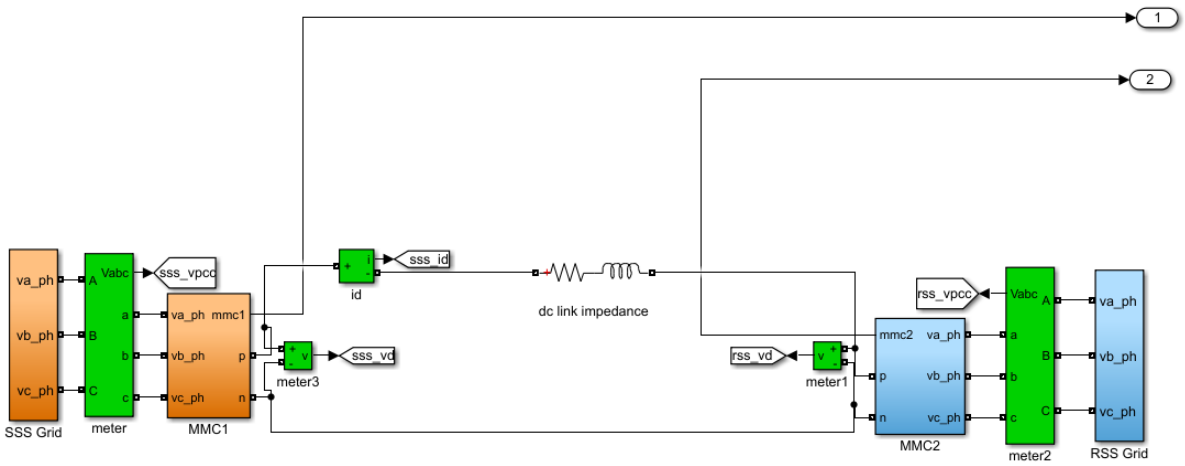
- Develop an understanding of MMC based grids
- Understand the counter-problems with MMC based grids and their solutions

In order to follow the tutorial, you should:

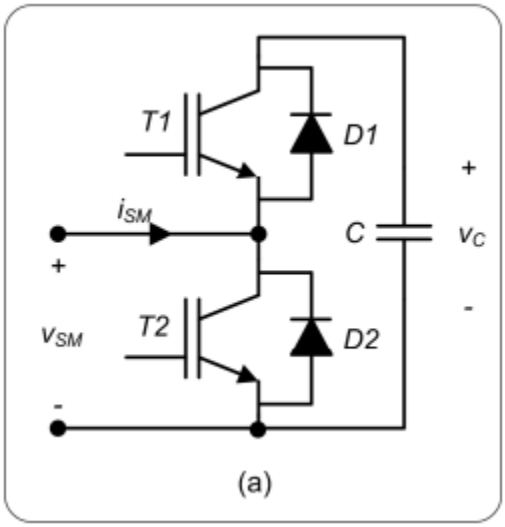
- Be able to do basic real time simulations in OPAL-RT
- Have the basic knowledge of pulse generation to fire the multilevel switches

Overview of Test System:

A back-to-back MMC-HVDC system is considered as the test system. The objective is to operate one of them in volage control mode and one in power control mode. This is because if both are made to operate at voltage control mode, an unnecessary flow of current due to the instantaneous voltage difference would flow between MMCs.



Half-bridge MMCs:



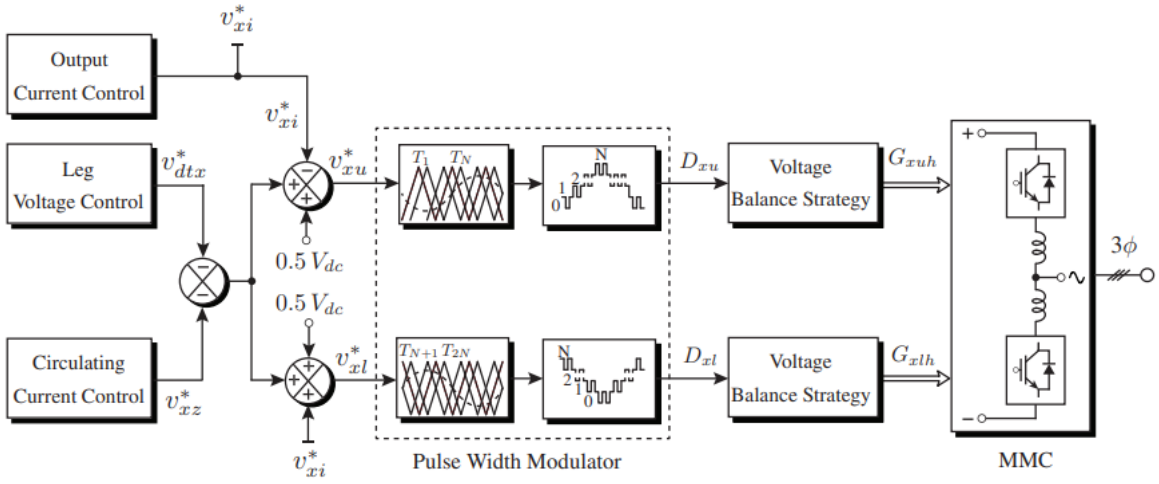
SM State	T_1 State	T_2 State	i_{SM}	Δv_C	i_{SM} Flows Through	v_{SM}
ON	ON	OFF	> 0	$+$	D_1	v_C
ON	ON	OFF	< 0	$-$	T_1	v_C
OFF	OFF	ON	> 0	0	T_2	0
OFF	OFF	ON	< 0	0	D_2	0

[1] Martinez-Rodrigo, F.; Ramirez, D.; Rey-Boue, A.B.; De Pablo, S.; Herrero-de Lucas, L.C. Modular Multilevel Converters: Control and Applications. *Energies* **2017**, *10*, 1709. https://doi.org/10.3390/en10111709
[2] Modular Multilevel Converters: Analysis, Control, and Applications. https://ieeexplore.ieee.org/servlet/opac?bknumber=8292871

Challenges with the use of MMCs:

- **Design of passive components:** Arm inductance and submodule capacitor are external passive components used in the design of MMCs. Arm inductance filters the switching frequency harmonics in the arm current. Its sizing depends on the arm current ripple. The submodule capacitor sizing is based on the tradeoff between the cost and capacitor voltage ripple.
- **Submodule capacitor pre-charging:** From floating state, the submodule capacitances should be charged to its nominal voltage before starting the normal system operation
- **Submodule capacitor voltage control:** The different levels of MMCs should be controlled together with one overall common objective. Individually, they should be regulated at reference voltage to produce a multilevel stepped output. The capacitor voltage control is done in different stages i.e., leg voltage control, voltage balancing between arms, and voltage balancing between the submodules within the arm [2].

1. **Leg voltage control**
2. **Circulating Current control**
3. **Output Current control**



Leg voltage control

The leg voltage control is dual loop with outer voltage control and inner current control. The outer voltage loop regulates the average of 2N submodule capacitor voltages in each leg at a constant value $V_C{}^*$, which is equal to the submodule capacitor voltage v_C. The voltage control loop minimizes the error between the reference and the actual average voltage and gives the DC current component command ($i_{xd}{}^*$). The DC-bus current command is given by

$$i_{xd}^* = k_{pv}(V_c^* - v_{cx}) + k_{iv}\int(V_c^* - v_{cx})dt$$

The measured average voltage of each leg (v_{cx}) is given by,

$$v_{cx} = \frac{1}{2N}\left[\sum v_{Cuh}^x + \sum v_{Clh}^x\right]$$

where $v_{cuh}{}^x$ and $v_{clh}{}^x$ are the submodule capacitor voltages in the upper and lower arm of phase-x. The magnitude of DC current is responsible for the active power flow by the load. It is controlled using the inner control loop. The loop minimizes the error between the reference and the actual DC current component and gives the leg voltage control output signal.

$$\mathrm{v_{dtx}^* = k_{pi}(i_{xd}^* - i_{xd}) + k_{ii}\int(i_{xd}^* - i_{xd})dt}$$

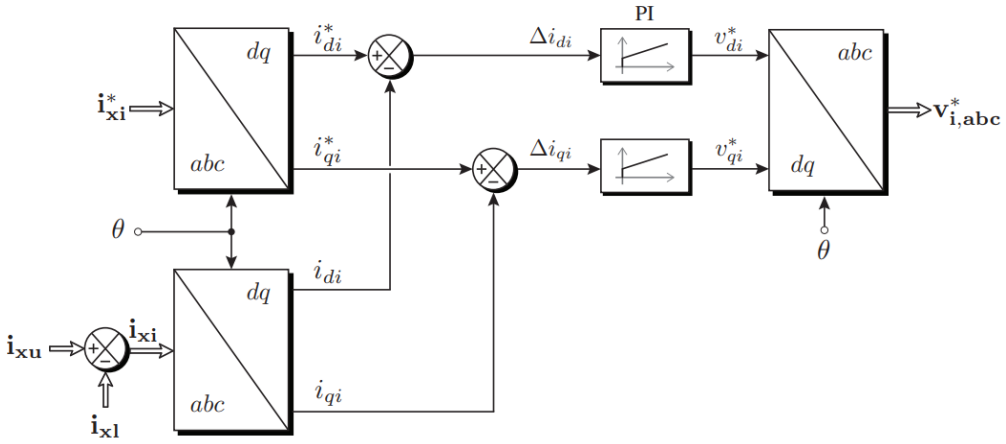
The DC-bus current (i_{xd}) is estimated from the measured arm currents and is given by,

$$i_{xd} = \frac{i_{xu} + i_{xl}}{6}$$

Output Current Control

The output current in terms of the upper and lower arm current is given by,

$$i_{xi} = i_{xu} - i_{xl}$$



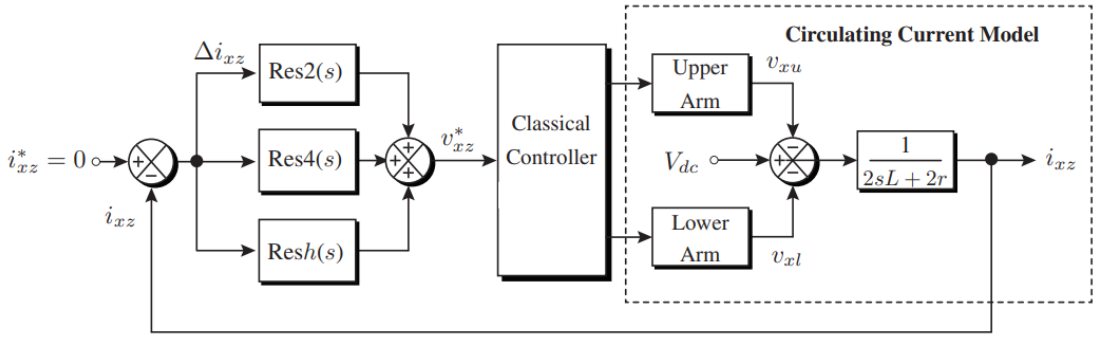
Circulating Current Control

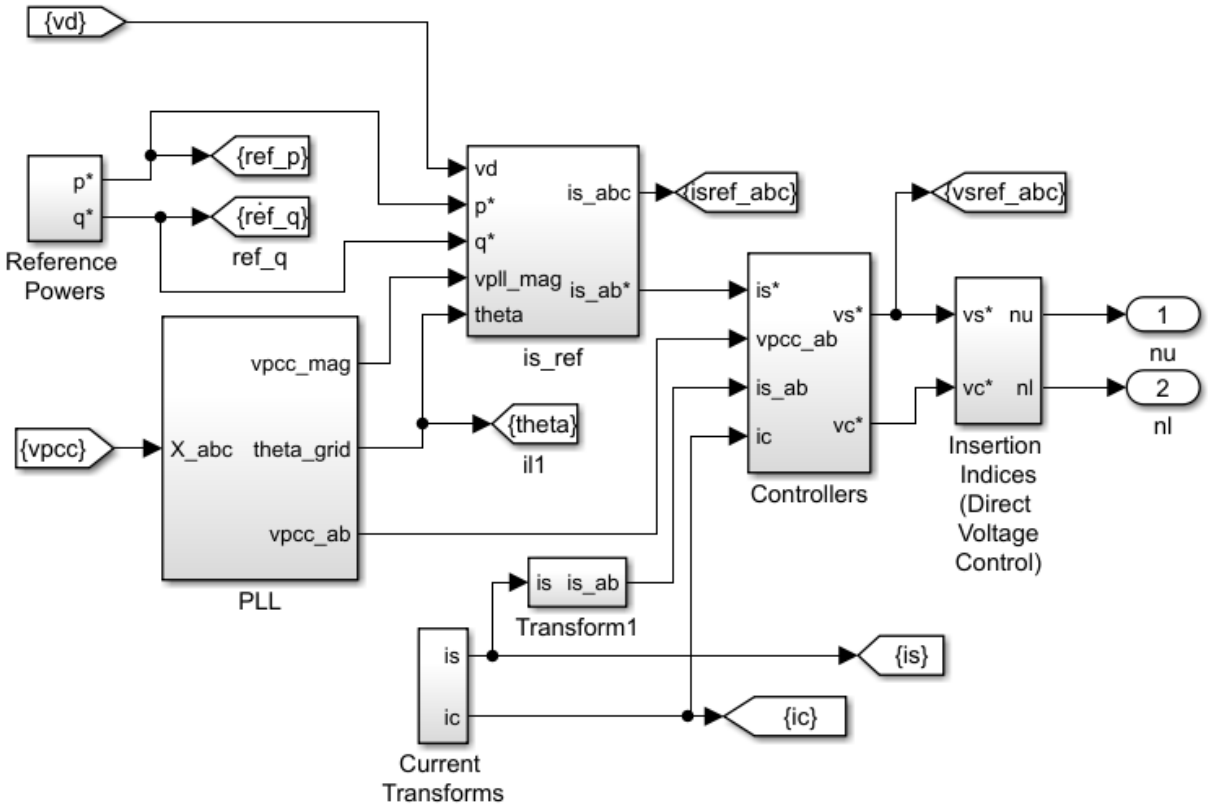
The circulating current, i_{xz} is modelled using differential equations as,

$$\mathrm{L}\frac{di_{xz}}{dt} + \mathrm{r}i_{xz} = \frac{V_{dc}}{2} - \frac{v_{xu} + v_{xl}}{2}$$

Circulating current consists of **even-order harmonics** of frequency $Q\omega_o$, where $Q \in \{2, 4, 6, 8, ...\}$. These harmonic components can be suppressed using multiple resonant current controllers in a stationary-abc frame. Each resonant current controller is specifically designed to eliminate a specific harmonic component. The transfer function of resonant controller is given by,

$$ResQ(s) = \frac{k_Q s}{s^2 + (Q\omega_0)^2}$$





References

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[2] Modular Multilevel Converters: Analysis, Control, and Applications. https://ieeexplore.ieee.org/servlet/opac?bknumber=8292871