

New principles of design and operation for HVDC grids

Aleksandra Lekić, Joris van Doorn, Vaibhav Nougain, Kees Koreman

April 3, 2024

Contents

0.1	Guidelines to use this document	3
0.1.1	Other useful information	3
0.2	Power Electronic Converters	4
0.2.1	Line-Commutated Converter	4
0.2.2	Voltage Source Converter	14
0.3	MMC Control Design	21
0.3.1	Inner controlling loops design:	22
0.3.2	Outer controlling loops design	24
0.3.3	Phase Locked Loop	26
0.4	MTDC Control	27
0.5	HVDC Grids	29
0.5.1	HVDC System Configurations	29
0.6	HVDC Cables	31
0.6.1	Mass-impregnated paper cable	31
0.6.2	Paper-Polypropylene Laminated Paper (PPLP)	31
0.6.3	The extruded insulation HVDC cables	31
0.6.4	Future developments in HVDC cables	32
0.7	Protection	33
0.7.1	HVDC Circuit Breaker	33
0.7.2	Detection of DC faults	37
0.7.3	Locating the DC faults	39
0.8	Overview — RTDS/RSCAD (to be read before the session)	41
0.8.1	RTDS	41
0.8.2	RSCAD	42
0.8.3	RSCAD laboratory preparation	48
0.9	Hands on Session	54
0.9.1	Overview of the Test System	54
Appendix		59
A	Transformations	59

Nomenclature

Constants and functions

\hat{f} averaged signal f over switching frequency

Parameters

f, ω line frequency and angular frequency

v_j phase $j \in \{a, b, c\}$ to neutral voltage

i_j phase current $j \in \{a, b, c\}$

v_{dc} DC voltage

i_{dc} DC current, assumed as constant and equal $i_{dc} = I_{dc}$

The document has the following information:

- Guide readers to the relevant pages in the reference report (Link given below) provided for the topics discussed during class.
- Guide readers to the relevant sections in the reader for detailed insights into some topics discussed during class.
- Give readers a brief overview of converter technologies and their working.
- Guide readers to the lab assignment and tasks.

Note: Please thoroughly read the appendix 0.8 before the lab session.

For more information about MMC read section 0.2 before the hands-on session.

0.1 Guidelines to use this document

This section highlights the guidelines to navigate through the reference report and this reader itself for detailed insights into the topics discussed in the lecture.

- **Converter technologies and control loops** - Sections 0.2 and 0.3 of this reader.
- **DC cable types, materials and future developments** Section 0.6 of this reader.
- **Multi-terminal HVDC networks** Section 0.4 of this reader.
- **HVDC protection** - Section 0.7 of this reader.
- **Preparation for hands-on session** - Section 0.8 of this reader.

0.1.1 Other useful information

- Link for the course "Control and protection of HVDC/AC electrical grids": <https://resourcecenter.ies.ieee.org/education/control-protection-hybrid-grids>.
- RSCAD/RTDS libraries with models: Models for EE4545, and [Models for the MOOC](#).

0.2 Power Electronic Converters

Integration of Renewable Energy Sources (RES) into electrical power system requires extensive application of power electronic converters. Commonly used power electronic converters are Line Commutated Converters (LCCs) and Voltage Source Converters (VSCs).

0.2.1 Line-Commuted Converter

With the rising demand for electricity in the world, the expansion of the power grid is made more feasible with technologies such as the HVDC systems. A HVDC system is mainly in need when transmitting power for long distances or when connecting two AC grids operating at different frequencies. Such systems employ converters to convert the electrical power from AC to DC (rectification: at the sending end) and from DC to AC (inversion: at the receiving end). In general, these types of converters are of two main types - Line Commutated Converter (LCC) and Voltage Source Converter (VSC). The principle of operation of the LCC is covered in this document.

Currently, most of the HVDC systems in operation employ LCC converters [1]. These converter systems use thyristor valves (which can only be controlled to be switched on) as switches to perform rectification or inversion. Commutation can only be performed with the help of the polarity reversal of the AC source line voltage supplying the LCC converter. Hence, this converter is given the name, line-commutated [1]. From the AC source side, the converter can be looked at as a current source which injects both harmonic currents into the AC side. Due to this, the LCC is sometimes referred to as the current-source converter. In such a converter setup, the direction of current cannot be changed. Hence, any change in the power-flow direction can only be made through the reversal of the DC voltage polarity [1]. Furthermore, due to its dependency on the AC source for commutation, it requires a strong AC grid system for proper operation.

One of the major disadvantages of an LCC is the considerable amount of reactive power that is needed for operation [2]. This reactive power demand is caused due to the delay in the current waveforms with reference to the voltage waveforms, during the commutation process. This reactive power consumption can be found to be fairly higher for an LCC inverter, hence making FACTS compensation devices such as STATCOM, Static Var Compensator, large capacitor banks, necessary to be implemented [2]. Also, the harmonics generated by the converters need to be filtered; high pass filters become necessary. Hence the implementation of this converter configuration requires larger space when compared to the VSC counterpart. However, an advantage of such a converter includes lower losses in operation when compared to the VSC converter [2].

Hence, the properties of an LCC converter can be summarized to be:

1. It behaves as a current source from the AC side.
2. Lower costs of implementation.
3. Current direction does not change.
4. Voltage polarity changes according to the power direction.
5. Requires strong AC grids to function.
6. Stores energy inductively.
7. Commutation depends on an external circuit.
8. Only active power control can be performed.
9. It is comparatively a more mature technology.

Line-commutated converters (LCCs) are state-of-the-art since seventies. In Fig. 0.2.1 is depicted 12-pulse LCC for Pole 2 of the HVDC Inter-Island between the North and South Islands of New Zealand.

0.2.1.1 Operation

Line-Commuted Converter is designed using thyristors as switches, as depicted in Fig. 0.2.2 [3]. In Fig. 0.2.2 is depicted 6-pulse Graetz bridge [4, 5]. Thyristors are turned on α radians after the corresponding line-to-neutral voltage becomes maximal/minimal. Angle α is also called a firing angle.

Let us first conduct the analysis considering that the inductors have infinite values, $L \rightarrow \infty$. When we consider $L \rightarrow \infty$, then the inductor represents the short connection. This case presents ideal commutation [6]. During whole analysis, we will consider thyristors as ideal switches, i.e. short connection while conducting and



Figure 0.2.1: Thyristor valve, picture taken from wikipedia.

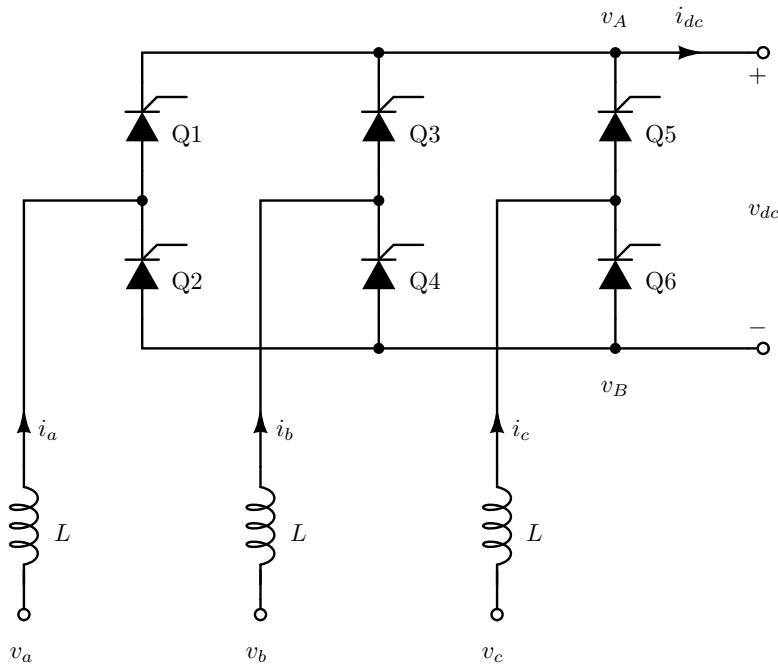


Figure 0.2.2: Line-commutated converter, 6 pulse.

open connection when they do not conduct. In that case, the expected waveforms are given in Fig. 0.2.3, where:

$$v_A(\omega t) = v_j(\omega t) \quad \text{for } j = \arg \max(v_1(\omega t - \alpha), v_2(\omega t - \alpha), v_3(\omega t - \alpha)), \quad (1a)$$

$$v_B(\omega t) = v_j(\omega t) \quad \text{for } j = \arg \min(v_1(\omega t - \alpha), v_2(\omega t - \alpha), v_3(\omega t - \alpha)), \quad (1b)$$

$$v_d(\omega t) = v_A(\omega t) - v_B(\omega t), \quad (1c)$$

$$i_j(\omega t) = \begin{cases} I_{dc} & \text{when } Q_{2j-1} \text{ is turned on,} \\ -I_{dc} & \text{when } Q_{2j} \text{ is turned on,} \\ 0 & \text{otherwise,} \end{cases} \quad (1d)$$

$$i_{dc}(\omega t) = I_{dc}. \quad (1e)$$

In the simulated case (Fig. 0.2.3) is taken that $\alpha = \frac{\pi}{6}$. Similarly can be obtained diagrams for different values for α .

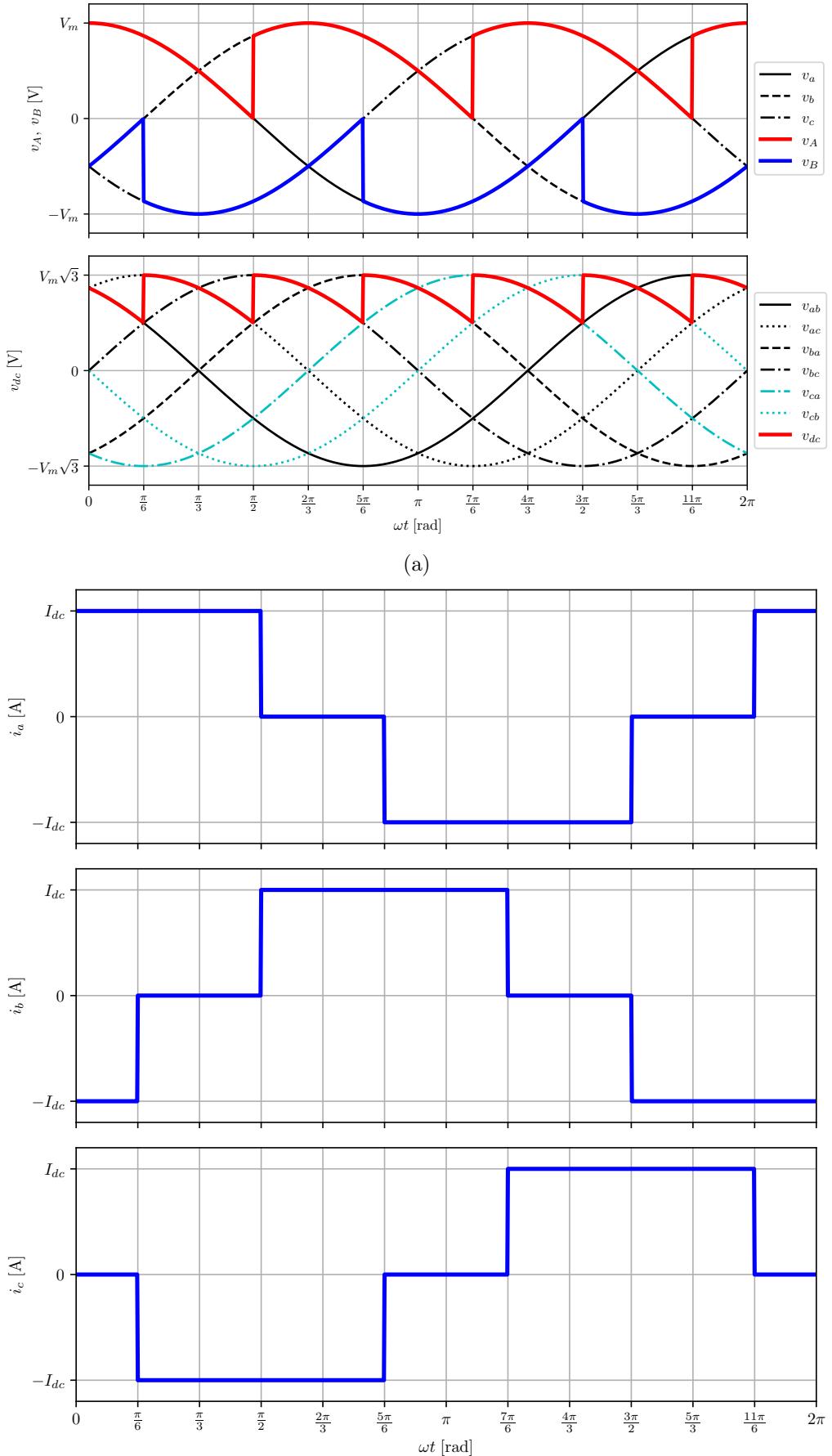


Figure 0.2.3: Waveforms of the LCC with assumption of $L \rightarrow \infty$ for (a) voltages, and (b) currents.

Table 1: Parameters of the 6-pulse LCC

f	50 Hz	V_{dc}	500 kV
I_{dc}	2 kA	V_m	345 kV
L	68.2 mH	α	$\frac{\pi}{6}$

For this case, the DC voltage can be calculated as

$$V_d = \frac{6}{\omega T} \int_{\alpha}^{\alpha + \frac{\pi}{3}} v_{ac}(\omega t) d(\omega t),$$

and the expression is

$$V_d = \frac{3\sqrt{3}V_m}{\pi} \cos \alpha. \quad (2)$$

The estimated output power is

$$P = \frac{3\sqrt{3}I_{dc}V_m}{\pi} \cos \alpha. \quad (3)$$

In this case power factor is

$$PF = \frac{3}{\pi} \cos \alpha. \quad (4)$$

When L has some finite value, then we have commutation between thyristors. That means that when one thyristor turns on, the one that was already turned cannot right away turn off.

Let us observe commutation between thyristors Q1 and Q3 when $\omega t = \frac{\pi}{2}$. Both thyristors are turned on until current of Q3 reaches value of the DC current I_{dc} . This moment can be estimated from the following equations:

$$i_a + i_b = I_{dc}, \quad (5a)$$

$$v_a - L \frac{di_a}{dt} = v_b - L \frac{di_b}{dt}, \quad (5b)$$

which knowing that $\frac{di_a}{dt} = -\frac{di_b}{dt}$, forms differential equation

$$\frac{di_b}{dt} = \frac{v_b - v_a}{2L} = \frac{V_m \sqrt{3}}{2L} \sin \left(\omega t - \frac{\pi}{3} \right). \quad (6)$$

By integrating it in the limits $\frac{\pi}{3} + \alpha$ and $\frac{\pi}{3} + \alpha + \mu$, we get an expression for current i_b :

$$i_b(\omega t) = \frac{V_m \sqrt{3}}{2\omega L} (\cos(\alpha) - \cos(\alpha + \mu)). \quad (7)$$

Finally, the moment when all current is translated into thyristor Q3 is given with:

$$\mu = \arccos \left(\cos(\alpha) - \frac{2\omega L I_{dc}}{V_m \sqrt{3}} \right) - \alpha. \quad (8)$$

During mentioned commutation, voltage at the point A is $v_A = \frac{v_1 + v_2}{2}$.

Waveforms now become as depicted in Fig. 0.2.4. Values used for the simulation are given in table 1. Using the previous calculation, we can estimate DC voltage and power factor as [5]:

$$V_d = \frac{3\sqrt{3}V_m}{\pi} \cos \alpha - \frac{3\omega L I_{dc}}{\pi}, \quad (9a)$$

$$PF = \frac{2V_d I_{dc}}{V_m I_m}, \quad (9b)$$

where $I_m = \frac{2\sqrt{3}I_{dc}}{\pi} \frac{\sin(\mu/2)}{\mu/2}$ represents the first harmonic of the AC current.

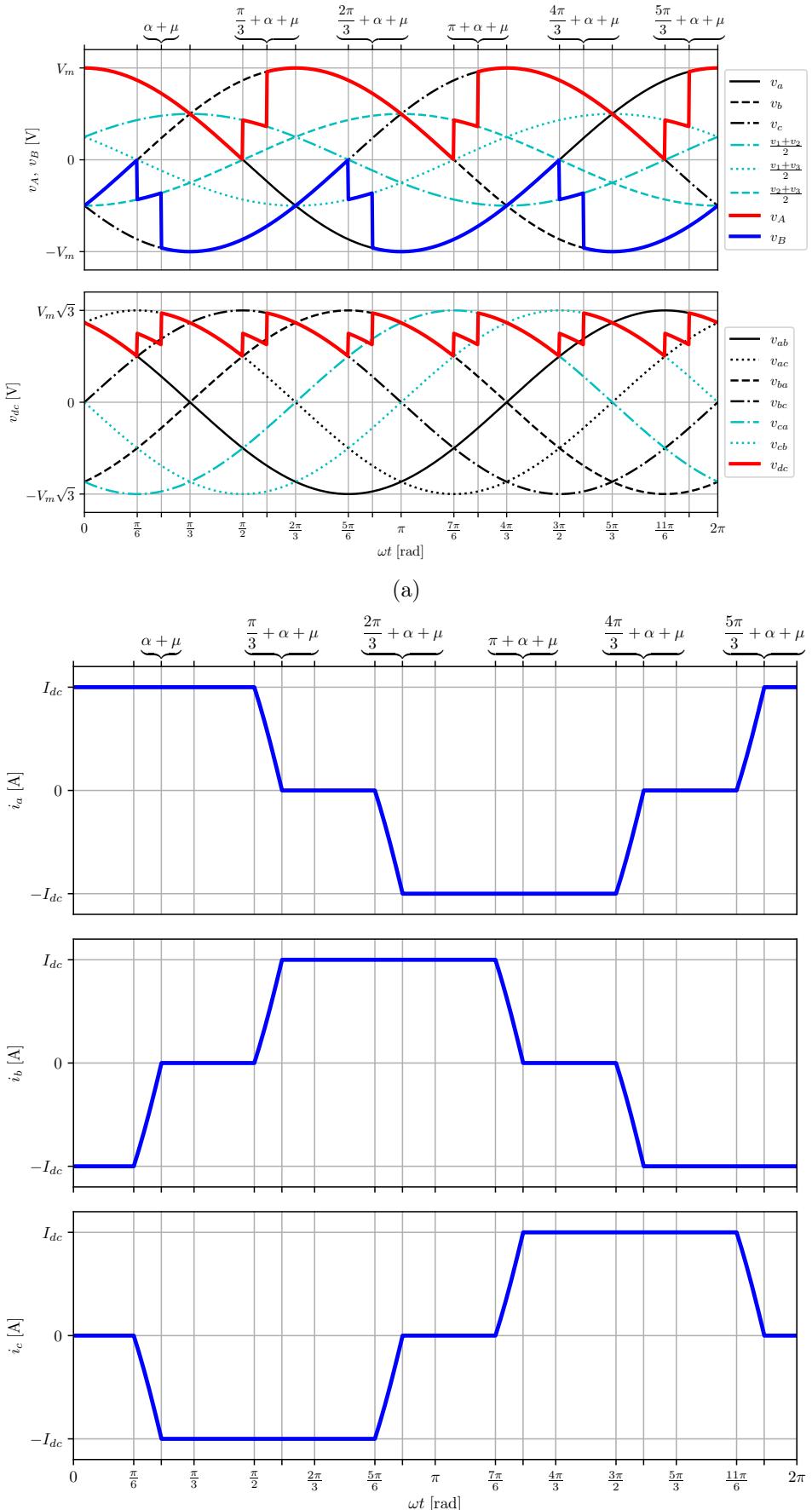


Figure 0.2.4: Waveforms of the LCC with assumption of finite value for L for (a) voltages, and (b) currents.

It should be noted that if the firing angle α is greater than $\frac{\pi}{2}$, the output DC voltage is negative.

One other realisation of the LCC is 12 pulse, as depicted in Fig. 0.2.5. It will not be analyzed in detail in this course. More information about 12 pulse LCC can be found in the course ET4119.

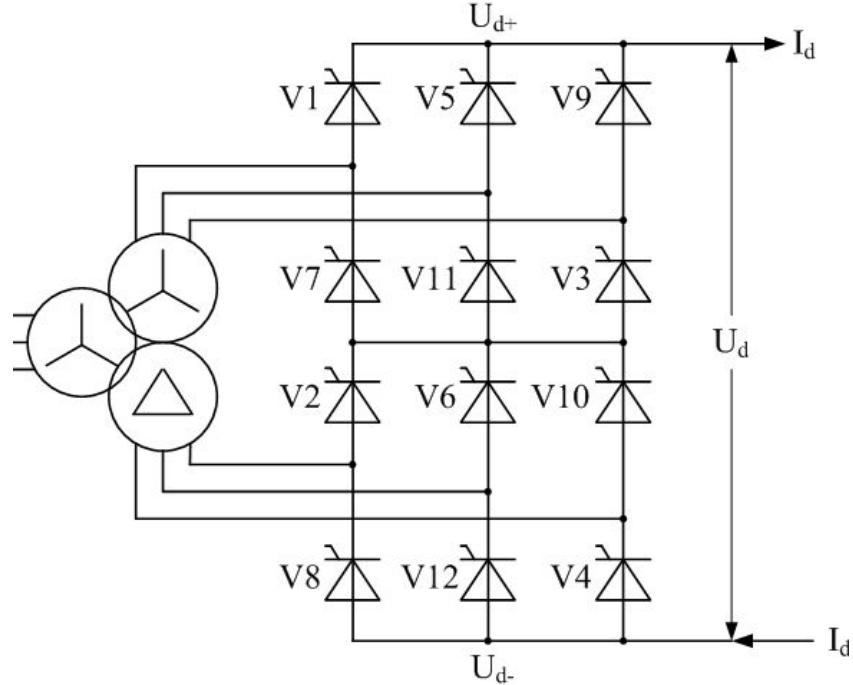


Figure 0.2.5: LCC 12 pulse.

Control Design

For the LCC the control is designed using control layers [6]. It consists of voltage dependent current order limit (VDCOL), a current controller (CC), an extinction angle controller (γ controller), phase locked loop (PLL), and firing pulse generator.

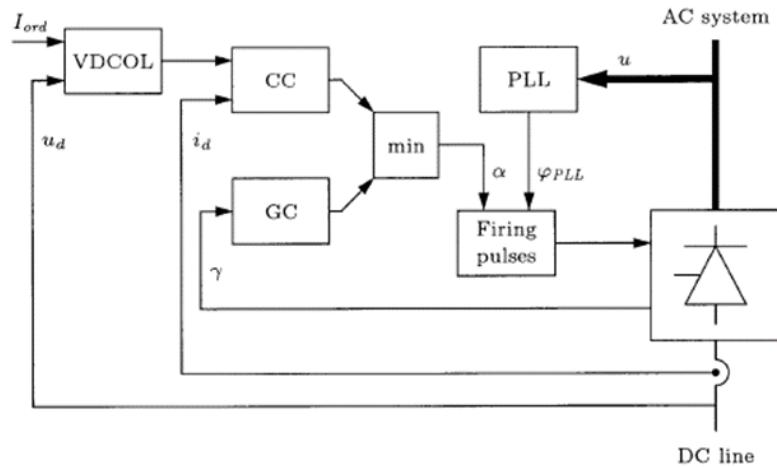


Figure 0.2.6: Classical implementation of LCC controls, picture taken from [5].

Voltage Dependent Current Order Limit (VDCOL): It is considered undesirable to have rated DC current flowing in the system whilst in an under-voltage situation. Hence, the DC voltage is tapped by the VDCOL control circuit as shown in Fig. 0.2.7, where it is filtered by a first-order delay block. Using this filtered voltage

in a look-up table, the lowest permissible voltage limit and the corresponding maximum permissible current I_{ref} is extracted [5]. This I_{ref} is used as a reference for the current controller.

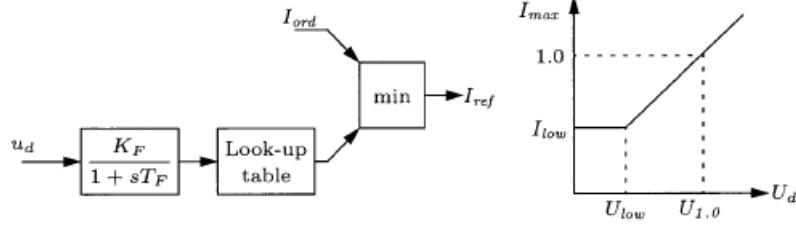


Figure 0.2.7: Overview of VDCOL Control Layer, picture taken from [5].

The look up mechanism used for this example simulation is the Fig. 0.2.8.

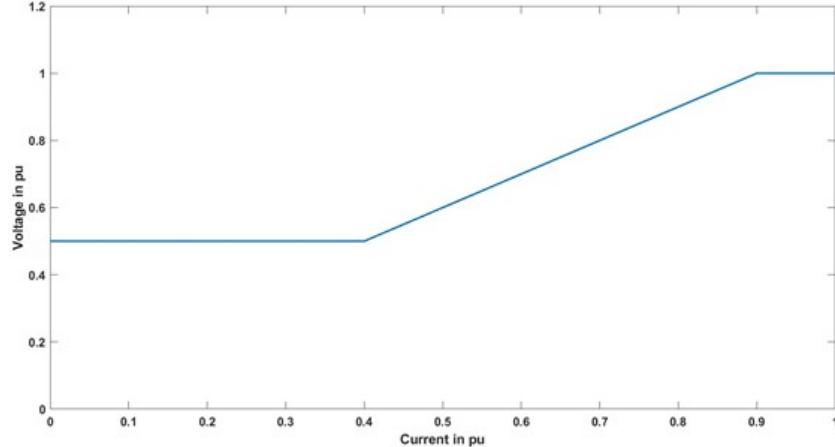


Figure 0.2.8: Graph used for lookup mechanism.

Current Controller (CC): It is depicted in Fig. 0.2.9. The real-time dc current is passed through a first-order delay block for filtering and then summed with some supplementary or reference signals obtained from the VD-COL layer [5]. The resultant signal is then passed to a PI controller so as to obtain the firing angle order. The obtained firing angle order is then limited by a limit block with predefined fixed limits obtained from other layers.

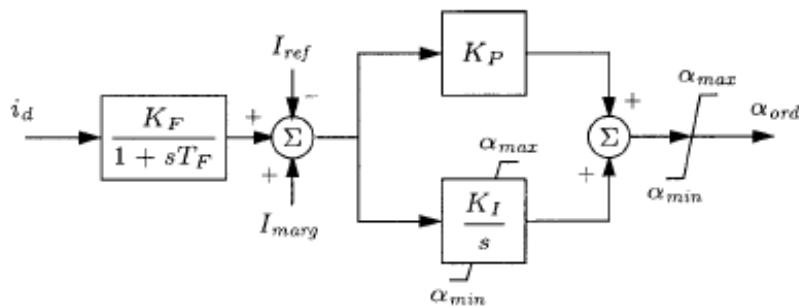


Figure 0.2.9: Overview of Current Control Layer, picture taken from [5].

Gamma Controller: For an LCC inverter operating in an HVDC system, it must be ensured that the commutation process from one set of valves to the other must take place before the voltage of the extinguishing valve is

positive again. This is ensured through a gamma controller as shown in Fig. 0.2.10. The commutation margin γ or “the time delay between the extinction of the valve and the valve voltage becoming positive again” is added to a negative fixed set-point (minimum commutation margin). The resultant difference is filtered through a limit block and then passed to a PI controller. The PI controller is designed in such a way that it saturates at the maximum firing angle order limit if the gamma value is higher than required. If not, the γ value is corrected to the minimal set-point. This, together with the current controller, helps in setting the firing angle order for an LCC inverter.

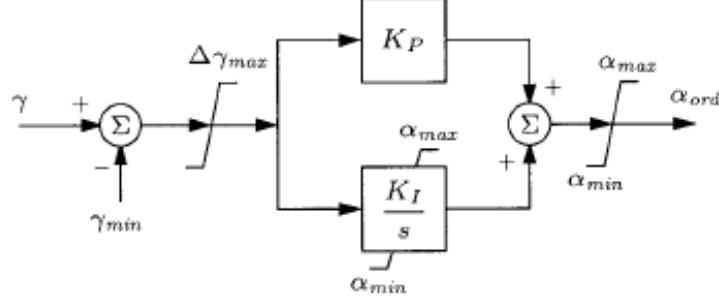


Figure 0.2.10: Overview of Gamma Control Layer, picture taken from [5].

Phase Locked Loop (PLL): Any firing pulse generator requires a reference signal which is in synchronous with the system voltage. To obtain such a reference signal, especially in weak AC systems, a PLL (usually based on the space-vector concept) is required. As shown in Fig. 0.2.11, the PLL takes the system voltages as input in the abc domain and converts it into the space vector domain. This is done to simplify the mathematical integration of the power system and the control system by keeping the analytical equations independent of time. This can be achieved by performing Clark transformation on the abc domain parameters so as to obtain a complex rotating phasor. Subsequently, this rotating phasor can be made non-rotating by applying a bidimensional rotation transformation, which further simplifies the parameters mathematically.

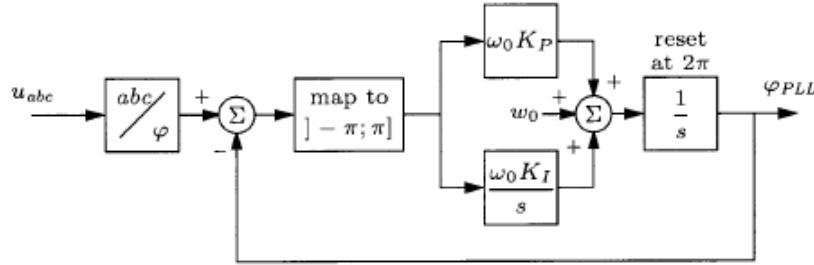


Figure 0.2.11: Overview of the Phase-Locked Loop layer, picture taken from [5].

On obtaining the parameters in the φ domain, the parameters are wrapped in the interval $[-\pi, \pi]$. Now, the real-time angular frequency is integrated and added to the phase angle of the now wrapped, space-vector-domain voltages. With the help of a PI controller, this error is resulted in an increased or decreased angular frequency (output of PLL) to obtain sync with the system voltage. To better understand the space vector theory, check link on Wikipedia SVM, and read chapter 4 from book [7].

Firing Pulse Generator: Now, the reference signal resulting out of the PLL, is compared with the ordered firing angle (output of the gamma and current control) to obtain the firing pulses such that the thyristor valve is switched ON when the carrier signal crosses the ordered firing angle [5]. During steady state, the PLL helps maintain synchronism between the desired system signal and the actual reference signal. However, during network transients the actual and the ordered firing angles are not the same. Therefore, to incorporate the effect of such transients, the firing angle is adjusted to be (mapped to $[-\pi, \pi]$) as in equation:

$$\alpha = \alpha_{ord} = (\varphi_{PLL} - \arg(u)), \quad (10)$$

where α is adjusted firing angle, α_{ord} is firing angle order, φ_{PLL} PLL reference angle, and $\arg(u)$ voltage phasor angle.

As shown above, all the control layers (except for the firing pulse generator) were implemented in RSCAD to achieve LCC control through firing pulses. RSCAD provides its own in-built model block for the firing pulse generator for a specific pulse width (120 degrees).

0.2.1.2 Large Point to point converter system

Fig 0.2.12 shows an LCC-HVDC converter system, with the HVDC cable represented by an equivalent circuit. We can breakdown and differentiate the individual components of an LCC-HVDC converter system as follows:

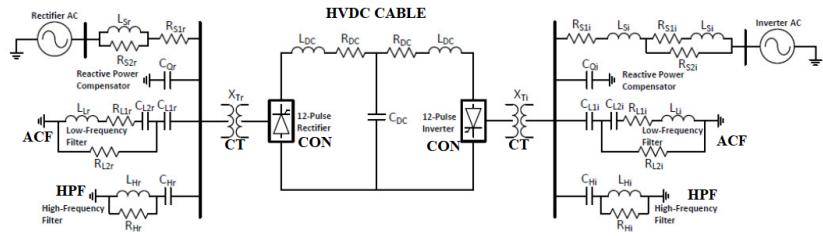


Figure 0.2.12: A HVDC System with LCC converter.

- **AC Harmonic Filter (ACF):** The AC filters are the RLC circuit connected between phase and earth. They offer low impedances to the harmonic frequencies and thus the AC harmonic currents are passed to earth. The AC harmonic filter also provide a reactive power required for the satisfactory operation of converters.
 - **High-Pass Filter (HPF):** The DC converters can produce noises in the range of communication carrier frequencies (20kHz to 490kHz). They can also produce radio interference noise in the megahertz range frequencies. High-frequency filters are used to minimize noise and interference with power line carrier communication. Such filters are placed between the converter transformer and the station AC bus.
 - **DC Harmonic Filter (DCF):** The DC filter is connected between the pole line and the neutral line. It diverts the DC harmonics to the ground and thus prevents them from entering the connected DC system. Such a filter does not require reactive power as the DC line does not require DC power.
 - **Converter Transformer (CT):** An HVDC LCC converter inherently induces current harmonics on the AC side and voltage harmonics on the DC side. In order to reduce or eliminate these current and voltage harmonics, the 12-pulse converter is split into two similar serially-connected 6-pulse bridge converters and are individually fed the AC power input through two converter transformers in the vector group configuration of Yy0 and Yd5 respectively. Such an arrangement causes a phase shift of 30 electrical degrees between the two inputs of the 6-pulse converters affecting the mitigation of the above-mentioned harmonics.
 - **12-pulse Bridge Converter (CON):** As shown in Fig.2, a typical HVDC system incorporates a 12-pulse bridge converter in its layout. The 12-pulse converter is divided into two serially connected 6-pulse converters. Each 6-pulse converter behaves as a typical 3-phase rectifier/inverter (based on the direction of power flow), which converts the AC power input to DC power. This DC power is fed and transmitted through the HVDC line through necessary filters.
To further understand the operation of 6-pulse/12-pulse bridge, use this book or refer the Electronic Power Conversion (ET4119) course on Brightspace.
 - **Valve Hall:** The converter valves of the HVDC station are housed mainly in the Valve Hall. The valve hall provides the necessary infrastructure for the smooth and effective operation of these valves. One such provision is the heating and cooling facilities to regulate the temperature of the hall to the nominal operating temperature of the converter valves. Furthermore, it protects the housed equipment from weather and dust.
 - **Smoothing Reactor (SR):** It is an oil-filled oil-cooled series reactor having a large inductance and forms a part of the 12-pulse converter. It can be located either on the line side or on the neutral side. Its

functions are to (i) smooth the ripples in the direct currents, (ii) limit the fault current in the DC line, (iii) decrease the harmonic voltage and current in the DC lines, (iv) reduce harmonic distortion on the DC line (aiding the DC harmonic filters), (v) reduce the steepness of voltage and current surges from the DC line, and finally (iv) preventing commutation failures in inverters due to collapse of another series-connected voltage by reducing rate of rise in the bridge.

0.2.2 Voltage Source Converter

Through the years, the LCC-HVDC converter has been proven to be a ripe technology. However, recent advances in semiconductor physics has allowed us to explore semiconductor-based controlled switches as an alternative to the semi-controlled thyristor switches [8]. This has led to the eventual replacement of the thyristor by transistor-based switches, mainly IGBTs or Insulated-Gate Bipolar Transistor. IGBTs, are unique from thyristors, in the sense that they can be turned-off without the need of voltage-polarity reversal. Moreover, they possess faster switching times when compared to the thyristors. Hence, when the thyristor of an LCC is replaced by IGBT switches, we obtain the Voltage Source Converter or VSC configuration. When an LCC would require the voltage polarity at the converter stations to be reversed for the reversal of power direction in an HVDC system, a VSC would be able to allow, interrupt, vary and reverse the power direction irrespective of the line voltage [8]. This makes a VSC converter highly flexible, and a more apt choice as an HVDC converter, especially with the recent increase in penetration in renewable generation [8]. With the new IGBT switches, the properties of such a converter in a HVDC setup results to the following [8]:

1. It behaves as a voltage source from the AC side.
2. Higher cost of implementation.
3. Current direction changes based on power direction.
4. Voltage polarity need not change.
5. Doesn't require strong AC grids to function.
6. Stores energy capacitively.
7. Commutation doesn't depend on an external circuit.
8. Both active and reactive power control can be performed.
9. It is comparatively a newer technology.

To speak of some disadvantages of an VSC-HVDC configuration, we can add that the VSC converters are susceptible to short-circuit line faults [8]. Whereas an LCC HVDC configuration could tackle such faults by limiting the fault current with the help of its smoothing reactors. This shortcoming of the VSC has led to the preference of underground cables over overhead lines for this configuration and has also caused the development of HVDC circuit breakers [8]. There are few classes of widely used VSCs: two-level, three-level converters, and modular multilevel converters.

0.2.2.1 Two-level Converter

In Fig. 0.2.13 is depicted two-level converter. Switches in the same arm are operated complementary, e.g. $Q3 = \overline{Q1}$. In Fig. 0.2.14 is depicted one arm operation, where is visible that when $Q1$ is conducting $v_{c,a} = \frac{v_{dc}}{2}$, and when $Q3$ conducts $v_{c,a} = -\frac{v_{dc}}{2}$. VSC can have square-mode operation, where each switch (IGBT) conducts for a half period, with the phase shift of $\frac{2\pi}{3}$ for each phase [9]. This modulation is no longer used because it cannot vary magnitude.

Therefore, VSCs are usually controlled using Pulse Width Modulation (PWM). PWM can be design on various ways, but the goal for it is to ensure that the averaged (over converter's switching frequency) currents and voltages have the desired waveforms (usually sine waveforms).

0.2.2.1.1 Averaged model PWM modulated two-level VSC should have desired voltage/current waveforms. Therefore, for the further analysis is introduced dimensionless parameter denoted as modulation index and represented as m_j for $j \in \{a, b, c\}$ being the phase. For the each switching interval $m_j(t) \in [0, 1]$.

The converter operates in such manner that in the steady-state is $v_A = \frac{v_{dc}}{2}$ and $v_B = -\frac{v_{dc}}{2}$. The following equations can be written

$$\widehat{v_{C,j}} = \widehat{m_j} \frac{v_{dc}}{2}, \quad (11a)$$

$$L \frac{d\widehat{i_j}}{dt} = v_j - \widehat{v_{C,j}}, \quad (11b)$$

$$C_{dc} \frac{dv_{dc}}{dt} = \widehat{i_{cap}}. \quad (11c)$$

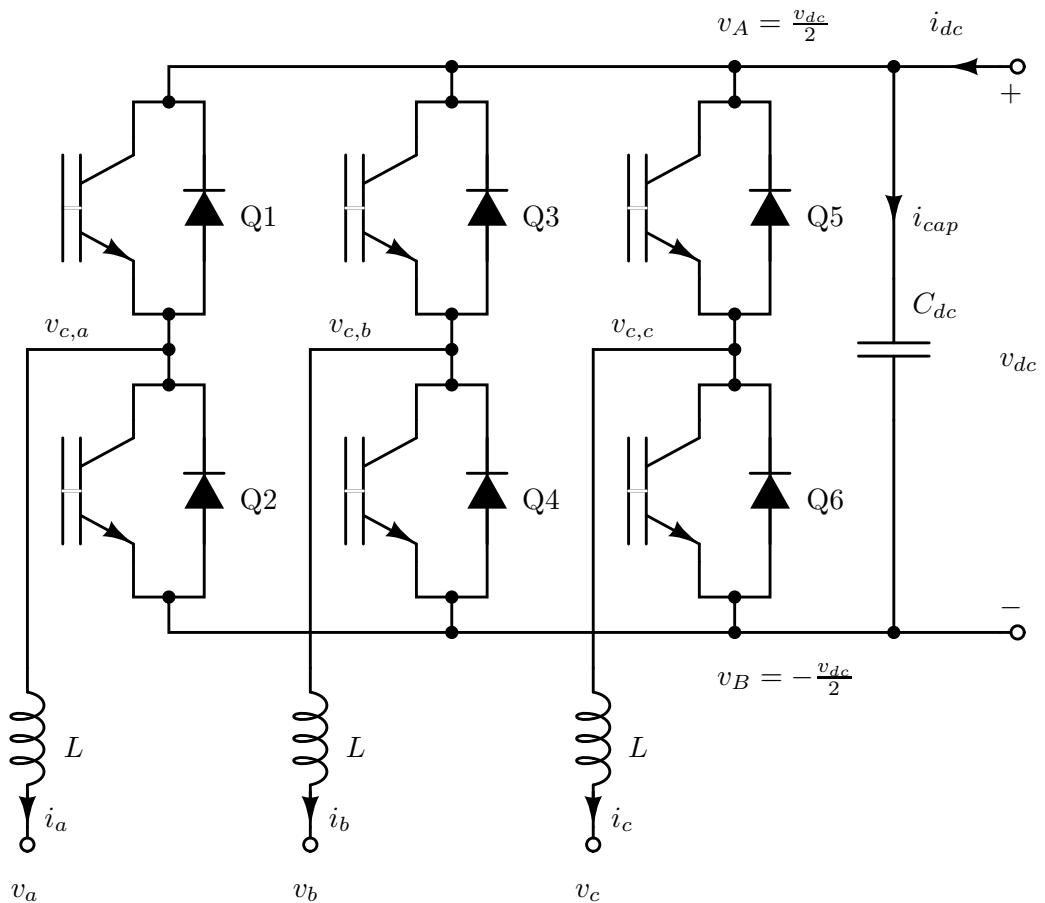


Figure 0.2.13: Two-level VSC.

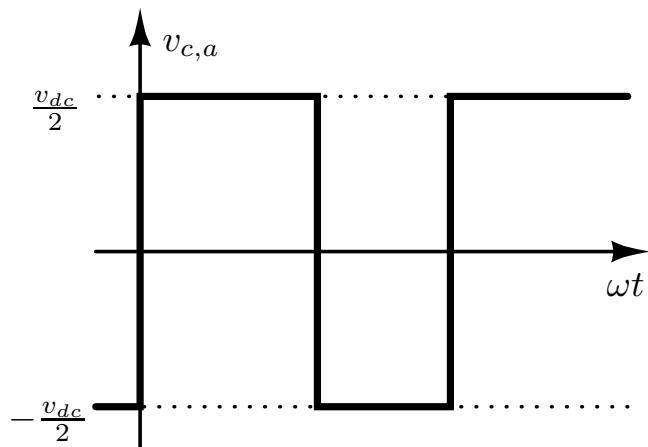


Figure 0.2.14: One arm operation of the VSC.

In addition we can write energy-balance equation as:

$$\widehat{v_{dc}} (\widehat{i_{dc}} - \widehat{i_{cap}}) = \sum_{j \in \{a,b,c\}} \widehat{v_{C,j}} \widehat{i_j},$$

which gives connection

$$\widehat{i_{cap}} = \widehat{i_{dc}} - \frac{1}{2} \sum_{j \in \{a,b,c\}} \widehat{m_j} \widehat{i_j}.$$

Finally, the complete set of differential equations with neglected variations on DC voltage is

$$v_{C,j} = m_j \frac{v_{dc}}{2}, \quad (12a)$$

$$L \frac{di_j}{dt} = v_j - v_{C,j}. \quad (12b)$$

Averaged notation is not used in the previous equations (12) due to simplicity of description.

0.2.2.2 Modular Multilevel Converter

One other way converter topology being researched as a prospect for HVDC transmission is a Multi-level Converter. Typically, these converters help in transforming voltages to a higher level by using multiple VSCs comprising of low-voltage components. Moreover, these converters can be used in a modular arrangement – Modular Multilevel Converter or MMC, to reap the following benefits [10]:

- The output DC voltage can be raised to any level.
- Has superior efficiency with minimal harmonic noise.
- DC-link capacitors are not necessary.

MMC physical appearance is presented in Fig. 0.2.15. In Fig. 0.2.16 is depicted one arm of an MMC. With SMs are denoted submodules which can be: half-bridge (HB), full-bridge (FB), flying-capacitor, cascaded half-bridge, and double clamp [11]. However, HB and FB are usually used.

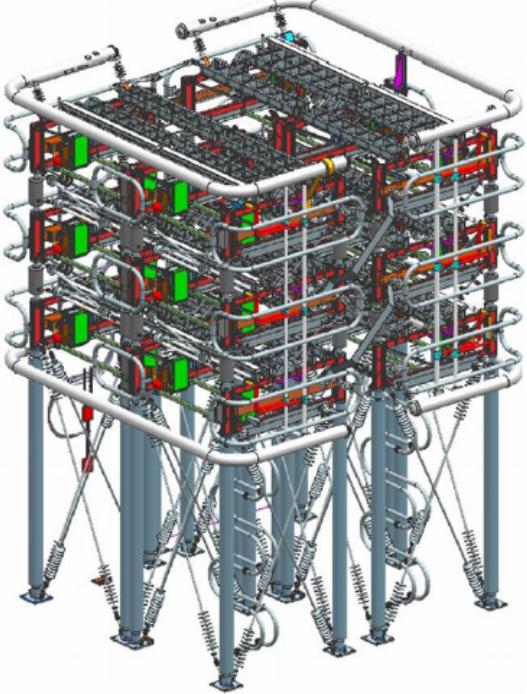


Figure 0.2.15: MMC picture.

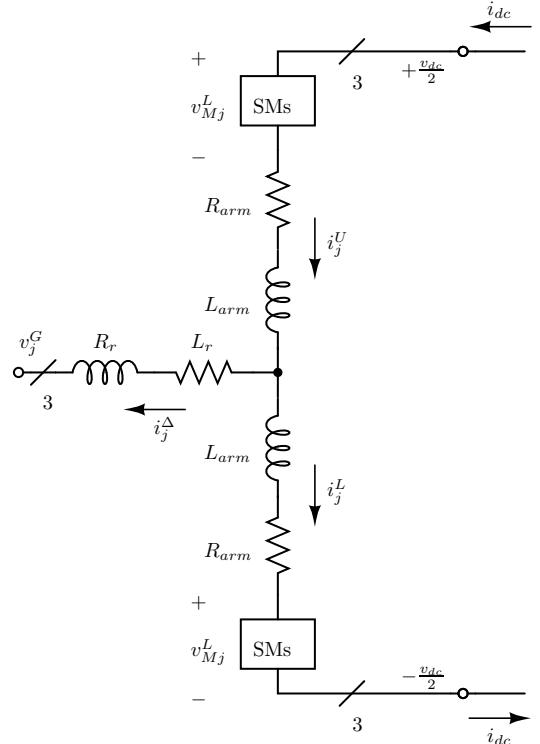


Figure 0.2.16: MMC model.

HB submodule is depicted in Fig. 0.2.17, where is visible that it has two operation modes. Switches have complementary operation, and SM can be conducting (when upper switch S1 conducts) or blocking (when $\bar{S}1$ conducts). The averaged output voltage is $\bar{v}_H = S_1 v_C$.

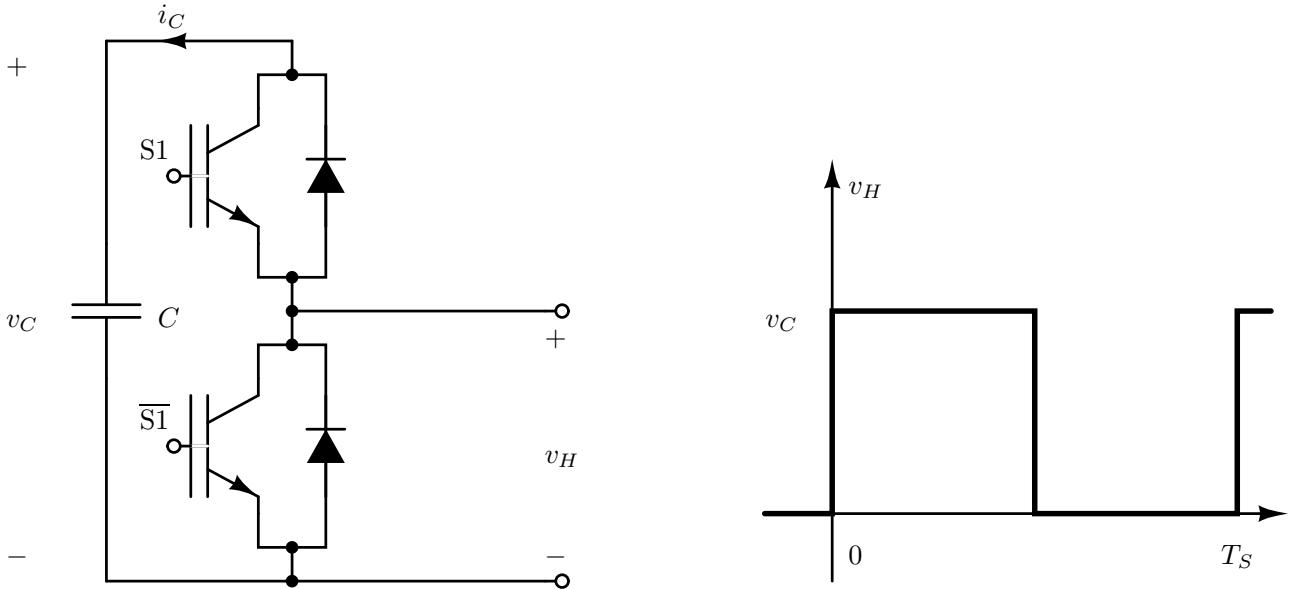


Figure 0.2.17: HB submodule: left – design; and right – principle of operation.

FB submodule is depicted in Fig. 0.2.18. It has three operation modes: when S1 and $\bar{S}2$ conduct – voltage $v_H = v_C$, S1 and S2 (or $\bar{S}1$ and $\bar{S}2$) conduct $-v_H = 0$, and when $\bar{S}1$ and S2 conduct $-v_H = -v_c$. The averaged voltage at the output is then $\bar{v}_H = (S_1\bar{S}_2 - \bar{S}_1S_2)v_C$.

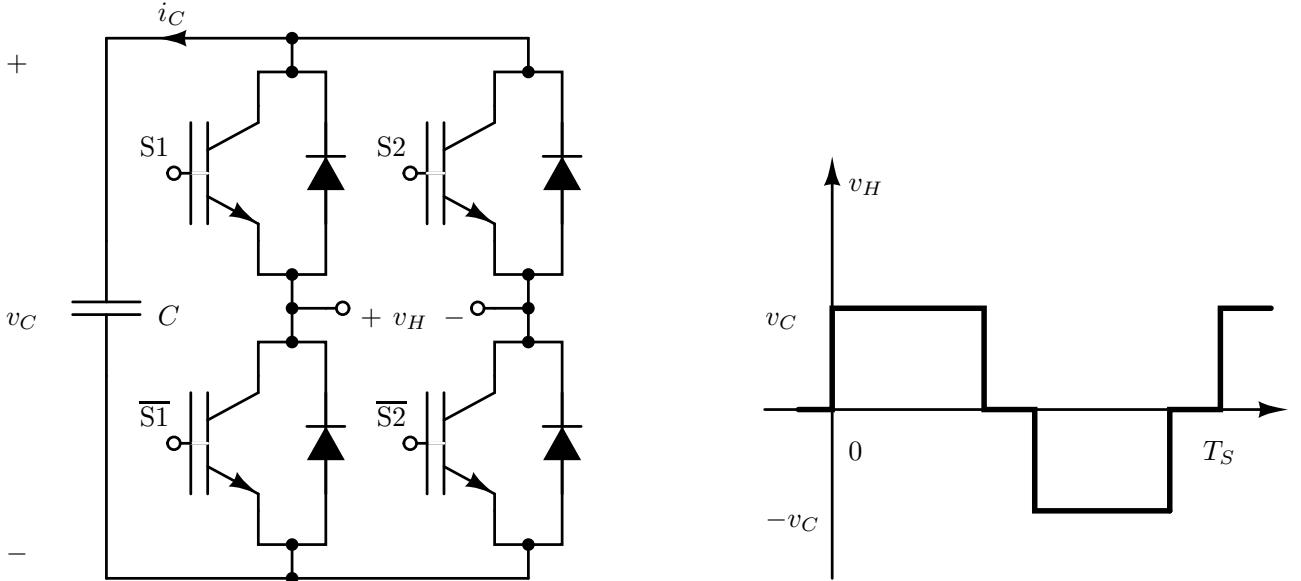


Figure 0.2.18: FB submodule: left – design; and right – principle of operation.

0.2.2.2.1 Averaged model The converter topology is depicted in Fig. 0.2.16, for a single phase of a three-phase MMC. Variables from the Fig. 0.2.16 are defined for all three phases, $j \in \{a, b, c\}$. Submodules are considered with their averaged equivalents, and thus, the following equations for voltage and current can be written for the upper and lower arms:

$$v_{Mj}^{U,L} = m_j^{U,L} v_{Cj}^{U,L}, \quad i_{Mj}^{U,L} = m_j^{U,L} i_j^{U,L}, \quad (13)$$

where $m_j^{U,L}$ are the corresponding upper and lower arm insertion indices, and $v_{Cj}^{U,L}$ is upper and lower are submodules' capacitor voltage.

The converter model is developed by following the $\Sigma - \Delta$ nomenclature, the variables in the upper and lower

converter arms can be represented as:

$$\begin{aligned} i_j^\Delta &= i_j^U - i_j^L, \quad i_j^\Sigma = \frac{i_j^U + i_j^L}{2}, \\ v_{Cj}^\Delta &= \frac{v_{Cj}^U - v_{Cj}^L}{2}, \quad v_{Cj}^\Sigma = \frac{v_{Cj}^U + v_{Cj}^L}{2}, \end{aligned}$$

$$\begin{aligned} m_j^\Delta &= m_j^U - m_j^L, \quad m_j^\Sigma = m_j^U + m_j^L, \\ v_{Mj}^\Delta &= \frac{-v_{Mj}^U + v_{Mj}^L}{2} = -\frac{m_j^\Delta v_{Cj}^\Sigma + m_j^\Sigma v_{Cj}^\Delta}{2}, \\ v_{Mj}^\Sigma &= \frac{v_{Mj}^U + v_{Mj}^L}{2} = \frac{m_j^\Sigma v_{Cj}^\Sigma + m_j^\Delta v_{Cj}^\Delta}{2}. \end{aligned}$$

With the new variables that have Σ and Δ superscripts, the equations of the state variables can be derived. In order to obtain the equations in multiple dqz frames, Park's transformation given in (61) is used with different frequencies.

The parameters are $L_{eq}^{ac} = L_r + \frac{L_{arm}}{2}$, $R_{eq}^{ac} = R_r + \frac{R_{arm}}{2}$, and C represents the submodule capacitor value and N the number of submodules in one converter arm. An equivalent DC-side capacitance $C_{dc} = 6\frac{C}{N}$ is used to model the DC voltage as a state variable. Taking into account previous writing convention, the following equations can be derived:

$$v_{Mj}^\Delta = -\frac{m_j^\Delta v_{Cj}^\Sigma + m_j^\Sigma v_{Cj}^\Delta}{2}, \quad (14a)$$

$$v_{Mj}^\Sigma = \frac{m_j^\Sigma v_{Cj}^\Sigma + m_j^\Delta v_{Cj}^\Delta}{2}, \quad (14b)$$

and differential equations:

$$L_{eq}^{ac} \frac{di_j^\Delta}{dt} = v_{Mj}^\Delta - v_j^G - R_{eq}^{ac} i_j^\Delta, \quad (15a)$$

$$L_{arm} \frac{di_j^\Sigma}{dt} = \frac{v_{dc}}{2} - v_{Mj}^\Sigma - R_{arm} i_j^\Sigma, \quad (15b)$$

$$2C_{arm} \frac{v_{Cj}^\Delta}{dt} = m_j^\Sigma \frac{i_j^\Delta}{2} + m_j^\Delta i_j^\Sigma, \quad (15c)$$

$$2C_{arm} \frac{dv_{Cj}^\Sigma}{dt} = m_j^\Delta \frac{i_j^\Delta}{2} + m_j^\Sigma i_j^\Sigma. \quad (15d)$$

In Fig. 0.2.19 are given diagrams of the all state variables given by differential equations from (15). MMC parameters are chosen as in table x. From diagrams in Fig. 0.2.19 can be seen that the first harmonic (angular frequency ω) is dominant in Δ variables, while in Σ variables dominates second harmonic (angular frequency 2ω). In the diagrams per unit values are calculated with the respect to base values: $S_{base} = 1$ GVA, $V_{base} = \frac{V_m}{\sqrt{3}}$ kV and $I_{base} = \frac{S_{base}}{V_{base}\sqrt{3}}$. Capacitor voltages are represented per unit using DC voltage as base. Modulation indices are set to be $\mathbf{m}_{abc}^\Sigma = [1 \ 1 \ 1]^T$, and $m_a^\Delta = -0.8 \cos(\omega t)$, while b and c components are phase shifted by $\frac{2\pi}{3}$ and $\frac{4\pi}{3}$, respectively.

Table 2: MMC parameters

N	400	C_{arm}	$32.55 \mu\text{F}$	R_{arm}	1.024Ω	L_{arm}	48 mH
R_f	0.521Ω	L_f	58.7 mH	V_m	320 kV	V_{DC}	640 kV

0.2.2.2.2 Model in dqz frame In order to obtain the differential equations in the dqz frame, Park's transformation is used to represent the system in a set of several rotating frames, each of which is related to a different angular frequency. The Park's transformation is as defined in (61). It should be noted that zero sequence of the Σ components corresponds to the DC currents and voltages. On the other hand Z (being Z_d and Z_q) incorporates third harmonic into Δ currents and voltages modeling.

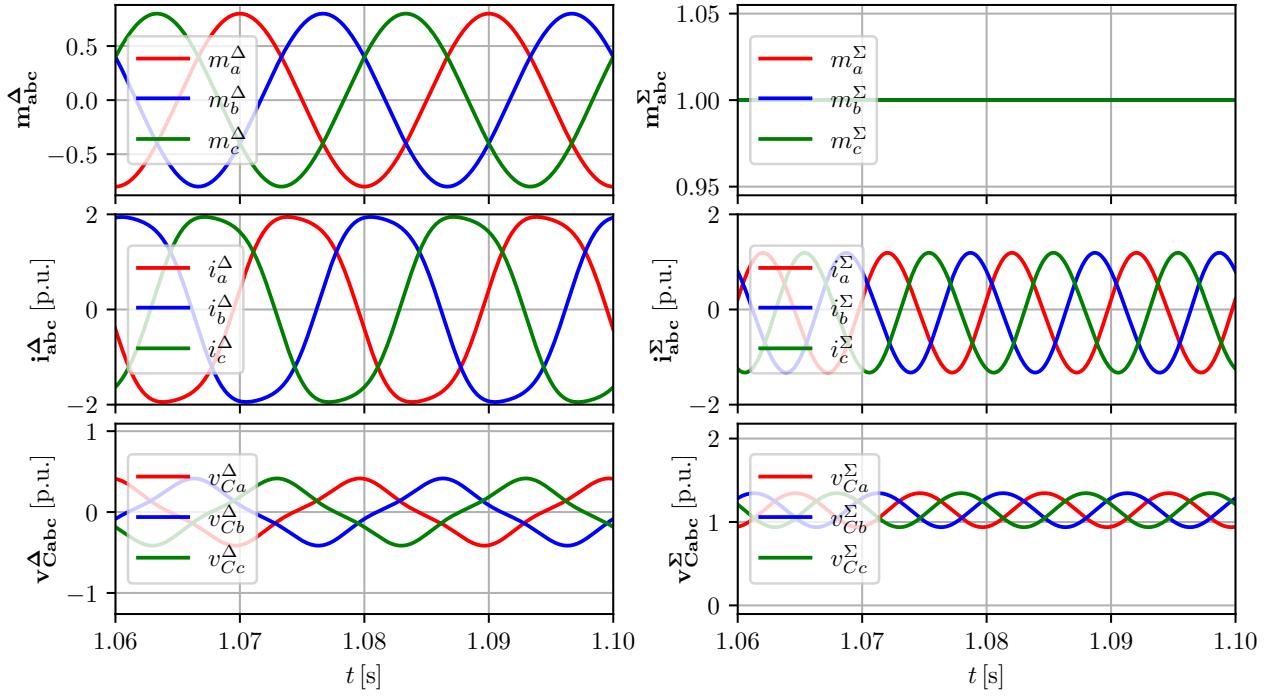


Figure 0.2.19: Diagrams of the open-loop MMC.

For the purpose of the modeling, the MMC converter is represented using 12 differential equations for the state variables [12, 13]:

$$\begin{aligned}
\frac{di_d^\Delta}{dt} &= -\frac{v_d^G - v_{Md}^\Delta + R_{eq}^{ac}i_d^\Delta + \omega L_{eq}^{ac}i_q^\Delta}{L_{eq}^{ac}}, \\
\frac{di_q^\Delta}{dt} &= -\frac{v_q^G - v_{Mq}^\Delta + R_{eq}^{ac}i_q^\Delta - \omega L_{eq}^{ac}i_d^\Delta}{L_{eq}^{ac}}, \\
\frac{di_d^\Sigma}{dt} &= -\frac{v_{Md}^\Sigma + R_{arm}i_d^\Sigma - 2\omega L_{arm}i_q^\Sigma}{L_{arm}}, \\
\frac{di_q^\Sigma}{dt} &= -\frac{v_{Mq}^\Sigma + R_{arm}i_q^\Sigma + 2\omega L_{arm}i_d^\Sigma}{L_{arm}}, \\
\frac{di_z^\Sigma}{dt} &= -\frac{v_{Mz}^\Sigma - \frac{v_{dc}}{2} + R_{arm}i_z^\Sigma}{L_{arm}}, \\
\frac{dv_{Cd}^\Delta}{dt} &= \frac{N}{2C_{arm}} \left(i_z^\Sigma m_d^\Delta - \frac{i_q^\Delta m_q^\Sigma}{4} + i_d^\Sigma \left(\frac{m_d^\Delta}{2} + \frac{m_{Zd}^\Delta}{2} \right) - i_q^\Sigma \left(\frac{m_q^\Delta}{2} + \frac{m_{Zq}^\Delta}{2} \right) \right. \\
&\quad \left. + i_d^\Delta \left(\frac{m_d^\Sigma}{4} + \frac{m_z^\Sigma}{2} \right) - 2\omega C_{arm} v_{Cq}^\Delta \right), \\
\frac{dv_{Cq}^\Delta}{dt} &= -\frac{N}{2C_{arm}} \left(\frac{i_d^\Delta m_q^\Sigma}{4} - i_z^\Sigma m_q^\Delta + i_q^\Sigma \left(\frac{m_d^\Delta}{2} - \frac{m_{Zd}^\Delta}{2} \right) + i_d^\Sigma \left(\frac{m_q^\Delta}{2} - \frac{m_{Zq}^\Delta}{2} \right) \right. \\
&\quad \left. + i_q^\Delta \left(\frac{m_d^\Sigma}{4} - \frac{m_z^\Sigma}{2} \right) - 2\omega C_{arm} v_{Cd}^\Delta \right), \\
\frac{dv_{CZd}^\Delta}{dt} &= -\frac{N}{8C_{arm}} (i_d^\Delta m_d^\Sigma + 2i_d^\Sigma m_d^\Delta + i_q^\Delta m_q^\Sigma + 2i_q^\Sigma m_q^\Delta + 4i_z^\Sigma m_{Zd}^\Delta) - 3\omega v_{CZq}^\Delta, \\
\frac{dv_{CZq}^\Delta}{dt} &= -\frac{N}{8C_{arm}} (i_q^\Delta m_d^\Sigma + 2i_d^\Sigma m_q^\Delta - i_d^\Delta m_q^\Sigma - 2i_q^\Sigma m_d^\Delta + 4i_z^\Sigma m_{Zq}^\Delta) + 3\omega v_{CZd}^\Delta,
\end{aligned} \tag{16}$$

$$\begin{aligned}
\frac{dv_{Cd}^\Sigma}{dt} &= \frac{N}{2C_{arm}} \left(i_d^\Sigma m_z^\Sigma + i_z^\Sigma m_d^\Sigma + i_d^\Delta \left(\frac{m_d^\Delta}{4} + \frac{m_{Zd}^\Delta}{4} \right) - i_q^\Delta \left(\frac{m_q^\Delta}{4} - \frac{m_{Zq}^\Delta}{4} \right) \right) + 2\omega C_{arm} v_{Cq}^\Sigma, \\
\frac{dv_{Cq}^\Sigma}{dt} &= -\frac{N}{2C_{arm}} \left(i_q^\Delta \left(\frac{m_d^\Delta}{4} - \frac{m_{Zd}^\Delta}{4} \right) - i_z^\Sigma m_q^\Sigma + i_d^\Delta \left(\frac{m_q^\Delta}{4} + \frac{m_{Zq}^\Delta}{4} \right) - i_q^\Sigma m_z^\Sigma \right) + 2\omega C_{arm} v_{Cd}^\Sigma, \\
\frac{dv_{Cz}^\Sigma}{dt} &= -\frac{N}{8C_{arm}} (i_d^\Delta m_d^\Delta + i_q^\Delta m_q^\Delta + 2i_d^\Sigma m_d^\Sigma + 2i_q^\Sigma m_q^\Sigma + 4i_z^\Sigma m_z^\Sigma),
\end{aligned} \tag{17}$$

where $L_{eq}^{ac} = L_f + \frac{L_{arm}}{2}$ and $R_{eq}^{ac} = R_f + \frac{R_{arm}}{2}$. The state variables are $\mathbf{x} = [\mathbf{i}_{dq}^\Delta, \mathbf{i}_{dqz}^\Sigma, \mathbf{v}_{CdqZ}^\Delta, \mathbf{v}_{Cdqz}^\Sigma]^T$. The 12 algebraic relations used for determining 7 voltages $[v_{Md}^\Delta, v_{Mq}^\Delta, v_{MZd}^\Delta, v_{MZq}^\Delta, v_{Md}^\Sigma, v_{Mq}^\Sigma, v_{Mz}^\Sigma]$ and insertion indeices $[m_d^\Delta, m_q^\Delta, m_{Zd}^\Delta, m_{Zq}^\Delta, m_d^\Sigma, m_q^\Sigma, m_z^\Sigma]^T$ are given as:

$$\begin{aligned}
v_{Md}^\Delta &= \frac{m_q^\Delta v_{Cq}^\Sigma}{4} - \frac{m_d^\Delta v_{Cz}^\Sigma}{2} - \frac{m_d^\Delta v_{Cd}^\Sigma}{4} - \frac{m_{Zd}^\Delta v_{Cd}^\Sigma}{4} + \frac{m_{Zq}^\Delta v_{Cq}^\Sigma}{4} - \frac{m_d^\Sigma v_{Cd}^\Delta}{4} - \frac{m_z^\Sigma v_{Cd}^\Delta}{2} + \frac{m_q^\Sigma v_{Cq}^\Delta}{4} \\
&\quad - \frac{m_d^\Sigma v_{CZd}^\Delta}{4} + \frac{m_q^\Sigma v_{CZq}^\Delta}{4}, \\
v_{Mq}^\Delta &= \frac{m_d^\Delta v_{Cq}^\Sigma}{4} + \frac{m_q^\Delta v_{Cd}^\Sigma}{4} - \frac{m_q^\Delta v_{Cz}^\Sigma}{2} - \frac{m_{Zd}^\Delta v_{Cq}^\Sigma}{4} - \frac{m_{Zq}^\Delta v_{Cd}^\Sigma}{4} + \frac{m_d^\Sigma v_{Cq}^\Delta}{4} + \frac{m_q^\Sigma v_{Cd}^\Delta}{4} - \frac{m_z^\Sigma v_{Cq}^\Delta}{2} \\
&\quad - \frac{m_d^\Sigma v_{CZq}^\Delta}{4} - \frac{m_q^\Sigma v_{CZd}^\Delta}{4}, \\
v_{MZd}^\Delta &= -\frac{m_d^\Delta v_{Cd}^\Sigma}{4} - \frac{m_q^\Delta v_{Cq}^\Sigma}{4} - \frac{m_{Zd}^\Delta v_{Cz}^\Sigma}{2} - \frac{m_d^\Sigma v_{Cd}^\Delta}{4} - \frac{m_q^\Sigma v_{Cq}^\Delta}{4} - \frac{m_z^\Sigma v_{Zd}^\Delta}{2}, \\
v_{MZq}^\Delta &= -\frac{m_d^\Delta v_{Cq}^\Sigma}{4} - \frac{m_q^\Delta v_{Cd}^\Sigma}{4} - \frac{m_{Zq}^\Delta v_{Cz}^\Sigma}{2} - \frac{m_d^\Sigma v_{Cq}^\Delta}{4} + \frac{m_q^\Sigma v_{Cd}^\Delta}{4} - \frac{m_z^\Sigma v_{Zq}^\Delta}{2}, \\
v_{Md}^\Sigma &= \frac{m_d^\Delta v_{Cd}^\Delta}{4} - \frac{m_q^\Delta v_{Cq}^\Delta}{4} + \frac{m_d^\Delta v_{CZd}^\Delta}{4} + \frac{m_{Zd}^\Delta v_{Cd}^\Delta}{4} + \frac{m_q^\Delta v_{Zq}^\Delta}{4} + \frac{m_{Zq}^\Delta v_{Cq}^\Delta}{4} + \frac{m_d^\Sigma v_{Cz}^\Sigma}{2} + \frac{m_z^\Sigma v_{Cd}^\Sigma}{2}, \\
v_{Mq}^\Sigma &= \frac{m_q^\Delta v_{Zd}^\Delta}{4} - \frac{m_q^\Delta v_{Cd}^\Delta}{4} - \frac{m_d^\Delta v_{Zq}^\Delta}{4} - \frac{m_d^\Delta v_{Cq}^\Delta}{4} + \frac{m_{CZd}^\Delta v_{Cq}^\Delta}{4} - \frac{m_{Zq}^\Delta v_{Cd}^\Delta}{4} + \frac{m_q^\Sigma v_{Cz}^\Sigma}{2} + \frac{m_z^\Sigma v_{Cq}^\Sigma}{2}, \\
v_{Mz}^\Sigma &= \frac{m_d^\Delta v_{Cd}^\Delta}{4} + \frac{m_q^\Delta v_{Cq}^\Delta}{4} + \frac{m_{Zd}^\Delta v_{CZd}^\Delta}{4} + \frac{m_{Zq}^\Delta v_{CZq}^\Delta}{4} + \frac{m_d^\Sigma v_{Cd}^\Sigma}{4} + \frac{m_q^\Sigma v_{Cq}^\Sigma}{4} + \frac{m_z^\Sigma v_{Cz}^\Sigma}{2},
\end{aligned} \tag{18}$$

$$\begin{bmatrix} m_d^\Delta \\ m_q^\Delta \\ m_{Zd}^\Delta \\ m_{Zq}^\Delta \\ m_d^\Sigma \\ m_q^\Sigma \\ m_z^\Sigma \end{bmatrix} = \frac{2}{v_{dc}} \begin{bmatrix} -v_{Md,ref}^\Delta \\ -v_{Mq,ref}^\Delta \\ -v_{MZd,ref}^\Delta \\ -v_{MZq,ref}^\Delta \\ v_{Md,ref}^\Sigma \\ v_{Mq,ref}^\Sigma \\ v_{Mz,ref}^\Sigma \end{bmatrix}. \tag{19}$$

The set of the previous 12 differential equations and the set of algebraic equations are accompanied with the 7 equations for the reference values of the voltages $[\mathbf{v}_{MdqZ,ref}^\Delta, \mathbf{v}_{Mdqz,ref}^\Sigma]$. The reference voltages are given as zero by default, except for the value of $v_{Cz,ref}^\Sigma = \frac{v_{dc}}{2}$.

0.2.2.3 Operating point

The converter's operating point can be defined manually or derived as a result of solving the power flow equations of the interconnected power system (including the converter's steady-state characteristics). In both situations, the following fields should be present:

P_{min}, P_{max}	minimum and maximum active AC power of the converter
P	power flow estimated or predefined active AC power
Q_{min}, Q_{max}	minimum and maximum reactive power
Q	power flow estimated or predefined reactive power
P_{dc}	power flow estimated or predefined DC power
V_{DC}	DC voltage
V_m, θ	amplitude and phase of the AC voltage

Using previous fields, the converter's operating point is estimated by solving a set of linear differential equations to obtain converter's steady-state. As a reference for the MMC's initial operating point using values obtained using power flow, we define:

$$\begin{aligned}
i_{d,ref}^{\Delta C} &= \frac{2}{3} \frac{(v_d^{GC}P + v_q^{GC}Q)}{v_d^{GC2} + v_q^{GC2}}, \\
i_{q,ref}^{\Delta C} &= \frac{2}{3} \frac{(v_q^{GC}P - v_d^{GC}Q)}{v_d^{GC2} + v_q^{GC2}}, \\
i_{z,ref}^{\Sigma} &= \frac{P_{dc}}{3V_{DC}}, \\
P_{ac,ref} &= P, \\
Q_{ar,ref} &= Q, \\
v_{dc,ref} &= V_{DC}, \\
W_{z,ref}^{\Sigma} &= \frac{3C_{arm}V_{DC}^2}{N}.
\end{aligned} \tag{20}$$

0.3 MMC Control Design

The MMC is controlled using high and low level controls. Control hierarchy is depicted in Fig. 0.3.1. Low level controls or inner controlling loops are usually manufactured with the converter itself. They have smaller time constants, usually around 10 ms. High level controls or outer controlling loops can be user configured. Outer controlling loops are used for controlling frequency, energy, power, and DC voltage. They have longer time constants, around 100 ms.

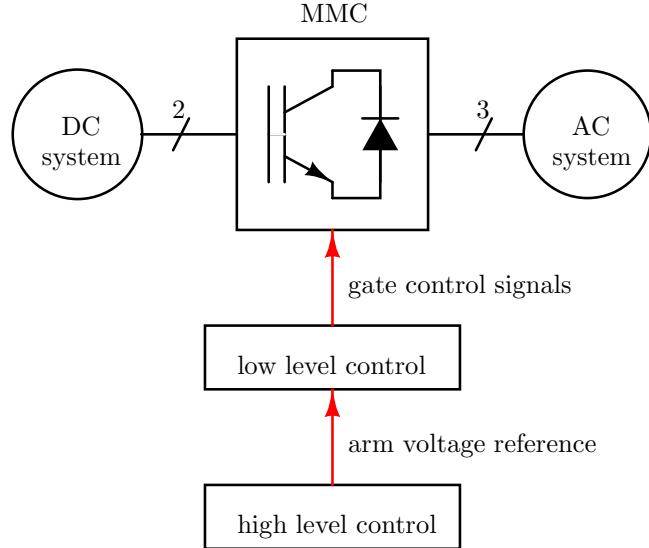


Figure 0.3.1: MMC control hierarchy.

The most common controls in dqz-frame for an MMC are depicted in Fig. 0.3.2. There are presented voltage balancing control for SMs' capacitor voltages, output current control and circulating current control. The SMs' control includes leg voltage control and capacitor voltage balancing control [11]. Since we are considering the MMC with its averaged model, in this course will be not given detailed descriptions about SM control, but they can be found in [11].

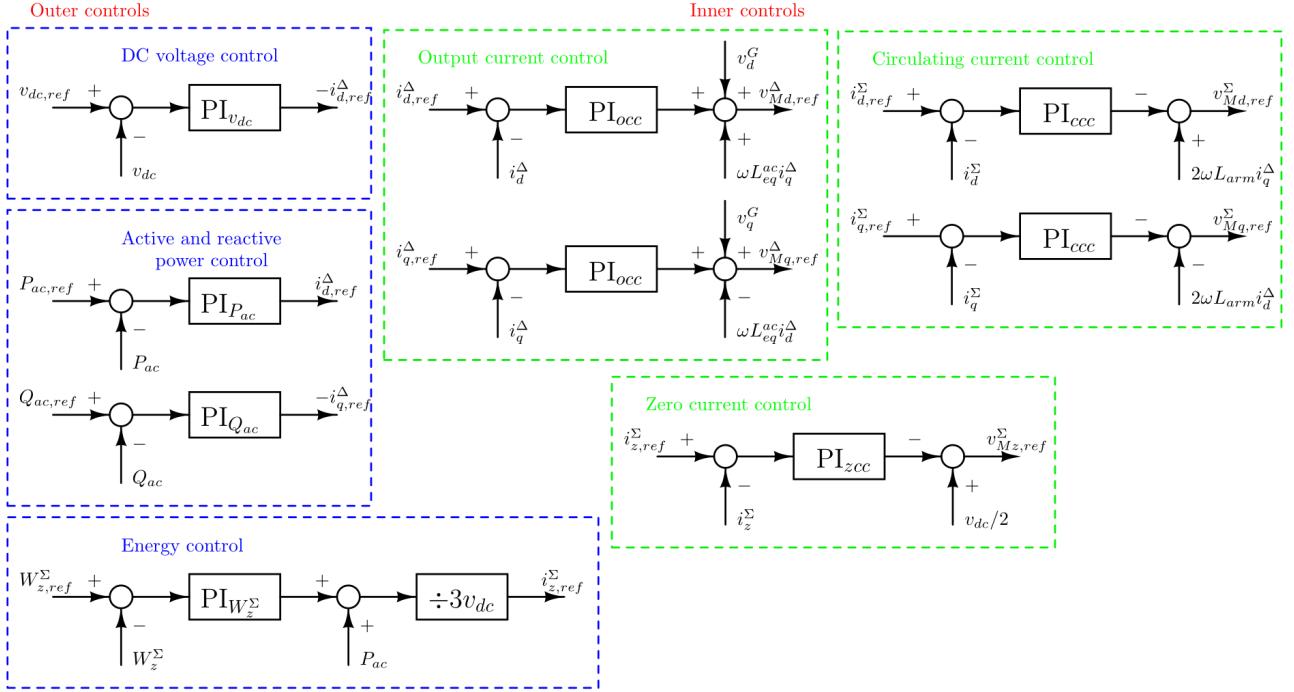


Figure 0.3.2: Inner and outer controls of the MMC.

For the PI controls in the dqz frame additional equations have been developed [12, 13, 14]. The different controllers are considered to be tuned using a pole placement method. Additionally, the PLL can be implemented using a PI controller structure as in [15].

0.3.1 Inner controlling loops design:

Inner controlling loops are capacitor voltage balancing, output current control, circulating current control, and zero current control. In this paragraph we are giving an example how to design output current control and circulating current control.

Output current control can be constructed in abc, $\alpha\beta$ and dq-frames. In this course we will design control using dq-frame formulation. Therefore, we will reformulate equations in abc-frame (15) using Park's transformation on the following matter:

$$\mathbf{T}_{abc \rightarrow dq} \times L_{eq} \frac{d}{dt} (\underbrace{\mathbf{T}_{dq \rightarrow abc} \times \mathbf{i}_{dq}^\Delta}_{\mathbf{i}_{abc}^\Delta}) = L_{eq} (\underbrace{\mathbf{T}_{abc \rightarrow dq} \dot{\mathbf{T}}_{dq \rightarrow abc}}_{\mathbf{J}} \mathbf{i}_{dq}^\Delta + \underbrace{\mathbf{T}_{abc \rightarrow dq} \mathbf{T}_{dq \rightarrow abc}}_{\mathbf{I}} \dot{\mathbf{i}}_{dq}^\Delta),$$

where can be calculated that $\mathbf{J}_\omega = \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix}$ and \mathbf{I} is an identity matrix. Therefore, in dq-frame the output current is given as:

$$L_{eq} \mathbf{i}_{dq}^\Delta = \mathbf{v}_{Mdq}^\Delta - \mathbf{v}_{dq}^G - (R_{eq} \mathbf{I} + L_{eq} \mathbf{J}_\omega) \mathbf{i}_{dq}^\Delta. \quad (21)$$

Similarly, equation for the common circulating current is developed as:

$$L_{arm} \dot{\mathbf{i}}_{dq}^\Sigma = \frac{v_{dc}}{2} \begin{bmatrix} 1 \\ 1 \end{bmatrix} - \mathbf{v}_{Mdq}^\Sigma - (R_{arm} \mathbf{I} + L_{arm} \mathbf{J}_{-2\omega}) \mathbf{i}_{dq}^\Sigma. \quad (22)$$

0.3.1.1 Output current control (OCC)

OCC defines the reference values for the output currents $i_{d,ref}^\Delta$ and $i_{q,ref}^\Delta$ given in the grid reference frame. This control method adds several equations:

$$\frac{d\xi_d^\Delta}{dt} = i_{d,ref}^\Delta - i_d^\Delta, \quad (23)$$

$$\frac{d\xi_q^\Delta}{dt} = i_{q,ref}^\Delta - i_q^\Delta, \quad (24)$$

$$v_{Md,ref}^\Delta = K_{i,occ}\xi_d^\Delta + K_{p,occ}(i_{d,ref}^\Delta - i_d^\Delta) + \omega_0 L_{eq}^{ac} i_q^\Delta + v_d^{G,C}, \quad (25)$$

$$v_{Mq,ref}^\Delta = K_{i,occ}\xi_q^\Delta + K_{p,occ}(i_{q,ref}^\Delta - i_q^\Delta) - \omega_0 L_{eq}^{ac} i_d^\Delta + v_q^{G,C}. \quad (26)$$

If the controller is defined only using bandwidth ω_n and ζ (instead of K_p and K_i), the proportional and integral gains are tuned as:

$$K_{i,occ} = L_{eq}^{ac} \omega_n^2, \quad (27)$$

$$K_{p,occ} = 2\zeta\omega_n L_{eq}^{ac} - R_{eq}^{ac}. \quad (28)$$

This loop is used to control the AC output current in the d and q axes, providing AC current control. The loop is used in cascaded form with the active power or DC voltage for the d-axis current and reactive power or AC voltage for the q-axis current. Further, current saturators or limiters are digitally used to compare the output current reference values with the maximum and minimum allowable current values.

0.3.1.2 Circulating current control (CCC)

The CCC is constructed to set the circulating current to its reference, which is considered to be $i_{d,ref}^\Sigma = 0$, $i_{q,ref}^\Sigma = 0$. The equations added by the CCC are:

$$\frac{d\xi_d^\Sigma}{dt} = i_{d,ref}^\Sigma - i_d^\Sigma, \quad (29)$$

$$\frac{di_q^\Sigma}{dt} = i_{q,ref}^\Sigma - i_q^\Sigma, \quad (30)$$

$$v_{Md,ref}^\Sigma = -K_{i,ccc}\xi_d^\Sigma - K_{p,ccc}(i_{d,ref}^\Sigma - i_d^\Sigma) + 2\omega L_{arm} i_q^{\Sigma C}, \quad (31)$$

$$v_{Mq,ref}^\Sigma = -K_{i,ccc}\xi_q^\Sigma - K_{p,ccc}(i_{q,ref}^\Sigma - i_q^\Sigma) - 2\omega L_{arm} i_d^\Sigma. \quad (32)$$

The proportional and integral gains are tuned as:

$$K_i = L_{arm} \omega_n^2, \quad (33)$$

$$K_p = 2\zeta\omega_n L_{arm} - R_{arm}. \quad (34)$$

This loop is used to control the d and q components of the average current components. It works toward eliminating the circulating current by following a zero reference for the circulating current.

0.3.1.3 Zero current control (ZCC)

Additionally, the zero current control (ZCC) sets the zero current to the desired value. The implementation of this control is depicted in Fig. 0.3.2. It can work without the energy controller.

$$\frac{d\xi_z^\Sigma}{dt} = i_{z,ref}^\Sigma - i_z^\Sigma, \quad (35)$$

$$v_{Mz,ref}^\Sigma = \frac{v_{dc}}{2} - K_{p,zcc}(i_{z,ref}^\Sigma - i_z^\Sigma) - K_{i,zcc}\xi_z^\Sigma. \quad (36)$$

The tuning of the ZCC employs the same principles as for CCC.

Zero sequence current arises in an unbalanced circuit, only if there is a path for it to flow. This can overheat the neutral connection wire and can result in losses. As a result, it is essential to control the value of zero sequence current.

Before applying these controllers, we must first transform relevant currents from abc to dq frame. Also, after getting expected voltage references, we must apply dq to abc transformation on these variables.

0.3.2 Outer controlling loops design

Outer controlling loops are power controllers, energy controllers, DC voltage controllers, and frequency controllers.

Power controllers are used on the offshore converter side for the HVDC link to ensure satisfactory active power transfer. On the offshore side is usually an active power controller together with an AC voltage controller and PLL (phase locked loop) controller. DC voltage control in PI or droop form is used on the onshore side to maintain the DC voltage level of the HVDC transmission line. In addition to the DC voltage controller, the energy controller ensures faster DC voltage and DC current convergence.

Active and reactive power controller design is depicted in Fig. 0.3.2, as well as DC voltage PI controller. In addition to DC voltage PI control, DC droop voltage controller is often used. Droop controller is depicted in Fig. 0.3.3, which is used to provide active power reference to the converter.

0.3.2.1 Energy control

The energy control is built around the “zero” energy and as a result, it provides a reference value for the ‘zero’ current $i_{z,ref}^\Sigma$. The energy controller involves the following equations, as visible from Fig. 0.3.2.

$$W_z^\Sigma = \frac{3C_{arm}}{2N} (v_{Cd}^\Delta{}^2 + v_{Cq}^\Delta{}^2 + v_{CZd}^\Delta{}^2 + v_{CZq}^\Delta{}^2 + v_{Cd}^\Sigma{}^2 + v_{Cq}^\Sigma{}^2 + 2v_{Cz}^\Sigma{}^2), \quad (37)$$

$$\frac{d\xi_{W_z^\Sigma}}{dt} = W_{z,ref}^\Sigma - W_z^\Sigma, \quad (38)$$

$$P_{ac} = \frac{3}{2} (v_d^{G,C} i_d^{\Delta C} + v_q^{G,C} i_q^{\Delta C}), \quad (39)$$

$$i_{z,ref}^\Sigma = \frac{K_{p,ec} (W_{z,ref}^\Sigma - W_z^\Sigma) + K_{i,ec} \xi_{W_z^\Sigma} + P_{ac}}{3v_{dc}}. \quad (40)$$

0.3.2.2 Active and reactive power control

An outer control loop for the control of the active and reactive power can be added, see Fig. 0.3.2. These control loops are used to successfully estimate the AC currents $i_{dq,ref}^\Delta$. The control loops operate according to the following equations:

$$P_{ac} = \frac{3}{2} (v_d^{G,C} i_d^{\Delta C} + v_q^{G,C} i_q^{\Delta C}), \quad (41)$$

$$Q_{ac} = \frac{3}{2} (-v_d^{G,C} i_q^{\Delta C} + v_q^{G,C} i_d^{\Delta C}), \quad (42)$$

$$\frac{d\xi_{P_{ac}}}{dt} = P_{ac,ref} - P_{ac}, \quad (43)$$

$$\frac{d\xi_{Q_{ac}}}{dt} = Q_{ac,ref} - Q_{ac}, \quad (44)$$

$$i_{d,ref}^{\Delta C} = K_p^{P_{ac}} (P_{ac,ref} - P_{ac}) + K_i^{P_{ac}} \xi_{P_{ac}}, \quad (45)$$

$$i_{q,ref}^{\Delta C} = -K_p^{Q_{ac}} (Q_{ac,ref} - Q_{ac}) - K_i^{Q_{ac}} \xi_{Q_{ac}}. \quad (46)$$

0.3.2.3 DC voltage control

DC voltage control (DCC) provides the reference value for $i_{d,ref}^\Delta$, depending of the variation of v_{dc} . The control law provides the following equations

$$\frac{dv_{dc}}{dt} = \frac{N}{6C_{arm}} (i_{dc} - 3i_z^\Sigma), \quad (47)$$

$$\frac{d\xi_{v_{dc}}}{dt} = v_{dc,ref} - v_{dc}, \quad (48)$$

$$i_{d,ref}^\Delta = -K_{p,dc} (v_{dc,ref} - v_{dc}) - K_{i,dc} \xi_{v_{dc}}. \quad (49)$$

The HVDC system needs control of voltage throughout the system. This is essential to ensure that the generated wind power is evacuated even with transient disruptions experienced by the system with countless practical challenges.

0.3.2.4 Droop control

The droop controller, see Fig. 0.3.3, combines DC voltage and active power control. It creates a reference for the d-component of the AC current.

In the DC voltage droop control, all converter stations can participate in the power-sharing after a converter outage. This method is better than the master-slave scheme because it allows for the substations to participate in the power balancing and also to reduce the mismatch in power, which a master station needs to compensate for.

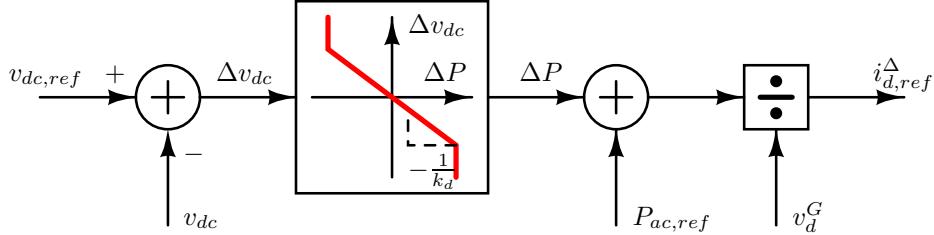


Figure 0.3.3: MMC DC droop controller.

Fig. 0.3.5 shows the comparison between the DC voltage control, active power control, and DC droop control. You can see that the droop control provides a slope that allows re-adjustment of DC voltage and active power references in case of disturbances in the HVDC electrical grid. These diagrams represent the straight lines in the DC voltage and active power control. MMC has one of these three controlling strategies implemented, each of which gives the d component of the AC current as an output. Which control strategy will be used depends on the role of the MMC inside the HVDC electrical grid.

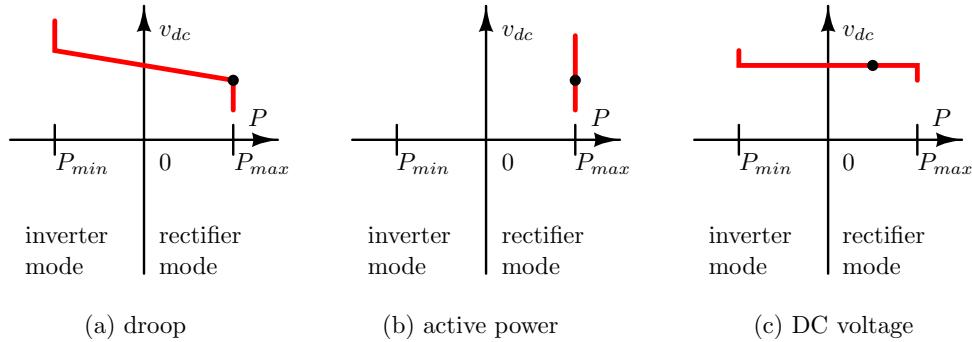


Figure 0.3.4: Comparison of active power, DC voltage and droop control.

0.3.2.5 AC voltage control

To extract the maximum power from the instantaneously changing wind speed in the wind energy systems, it is important to form a suitable grid on the AC side. This ensures stable AC voltage value through an independent frequency source. The AC voltage control creates a reference for the q component of the AC current: $i_{q,ref}^\Delta$. This type of control is suitable for grid-forming converters operating at an independent frequency.

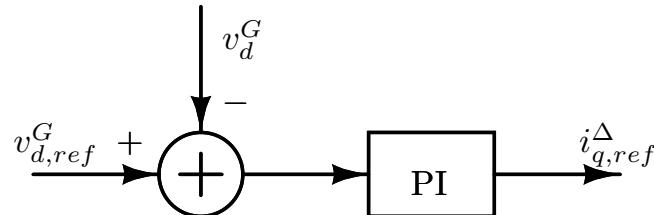


Figure 0.3.5: AC voltage control.

0.3.3 Phase Locked Loop

The phase locked loop, or PLL, is used to synchronize the converter's internal controller frequency, used to control the currents in a rotating frame, to the grid frequency. All converter variables are mapped to the dqz frame using the same Park's transformation without a phase shift.

According to Fig. 0.3.6 the following equations for PLL can be written.

$$\begin{aligned}\frac{d\xi_{pll}}{dt} &= -v_q^{G,C}, \\ \frac{d\theta}{dt} &= \Delta\omega, \\ \Delta\omega &= -K_{p,pll} v_q^{G,C} + K_{i,pll} \xi_{pll}, \\ \omega_C &= \Delta\omega + \omega_0.\end{aligned}\tag{50}$$

It should be noted that the output current control and circulating current control are implemented in the converter's reference frame. Thus, the rotation should be applied to the corresponding variables before the control law is applied. However, since the converter's internal dynamics is analyzed in the grid's reference frame, the output of the mentioned controls should be restored to the grid's reference frame using the inverse of the rotation matrix, given by T_θ matrix given as:

$$T(\theta) = \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \sin(\theta) & \cos(\theta) \end{bmatrix},\tag{51}$$

while its inverse is:

$$T^{-1}(\theta) = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix}.\tag{52}$$

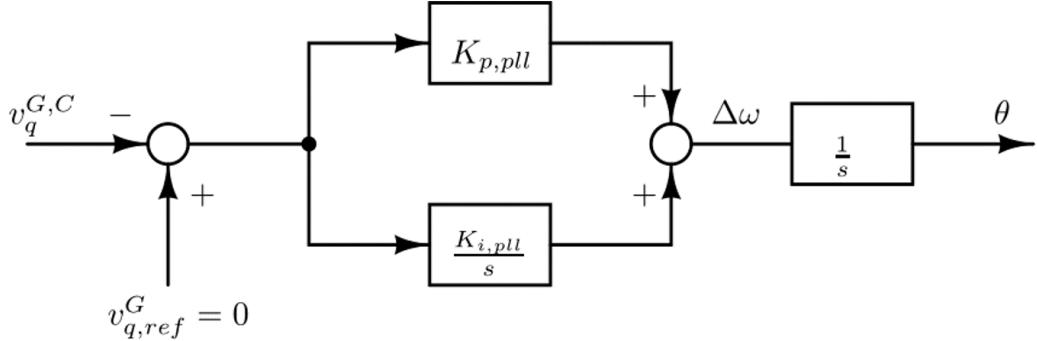


Figure 0.3.6: Phase locked loop design.

0.4 MTDC Control

Multi terminal DC system consists of an HVDC transmission system which is through multiple power converters connected to the AC grids. AC grids can be mutually decoupled. As mentioned earlier, in the MTDC system power converters are usually controlled in a master-slave manner.

Offshore converters should ensure stable AC voltage of the wind farm, together with stable frequency. For that matter offshore converters have AC voltage controllers, frequency controllers, and PLLs (see Fig. 0.4.1) [16]. Offshore converters are denoted to work in islanded mode.

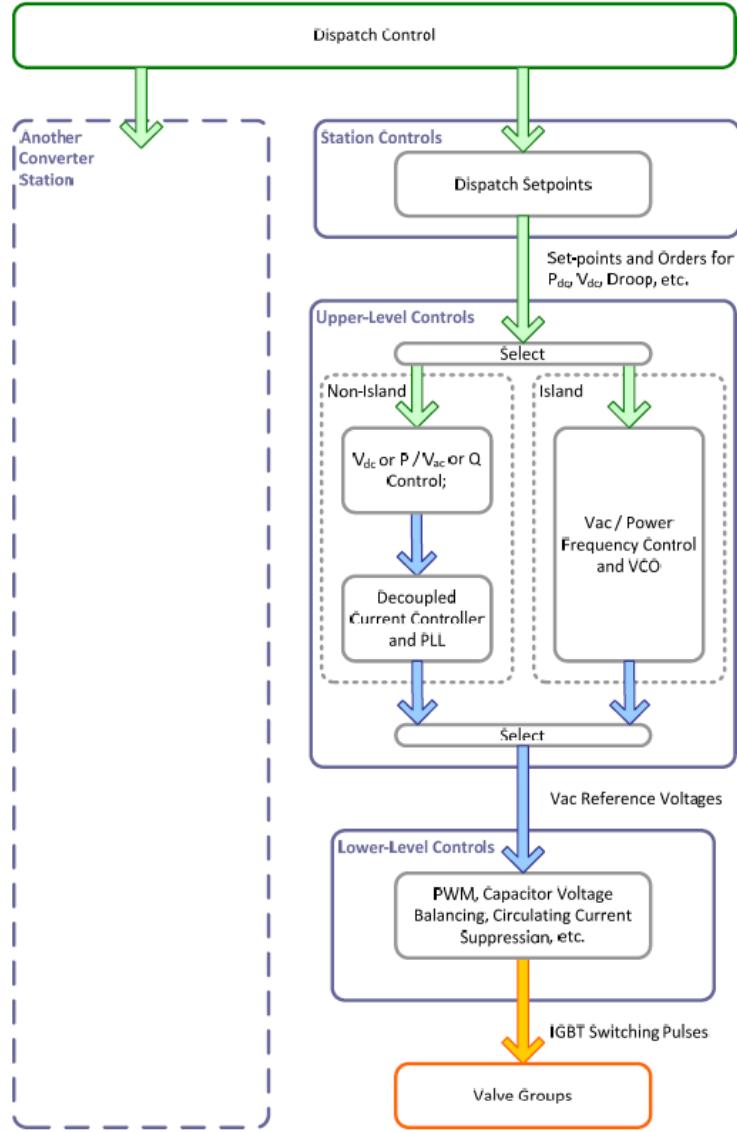


Figure 0.4.1: MTDC controls, picture taken from [16].

Onshore power converters should be controlled with two controllers:

1. DC voltage or active power controller;
2. AC voltage or reactive power controller.

The mentioned two controllers produce reference for output current, and zero current.

To properly control the HVDC electrical grid, three layers are observed as seen in Fig. 0.4.2. Dispatch level is the transmission system operator level, and this control provides the reference values for the AC, and DC voltage and active and reactive powers. Dispatch level control is centralized control. The lowest layer is the system-level design with physical components. The level in between is the control level of each MMC. MMCs are

individually controlled in a decentralized manner. Proper control of MMC is crucial for the control of the whole HVDC power system. MMC control is not an easy task. Due to its modularity, high number of submodules, and even higher number of switches, the MMC is controlled in four levels.

Namely, each MMC inside this system is designed the same way as described in section 0.2.2.2. Then, each MMC is controlled with four cascaded control loops. The control loop is the outer control loop which is responsible for the proper AC active and reactive power control, DC and AC voltage, depending on the role of the converter in the HVDC connection. The outer control loops receive the reference values from the dispatch level or shortly from TSO. The second layer control loops are the inner control loops responsible for DC and AC current controls and the circulating current control. The third control layer is the capacitor voltage balancing control, and the last fourth is the submodule firing control. All control loops are necessary for the proper estimation of the submodule firing signal, as given in this slide.

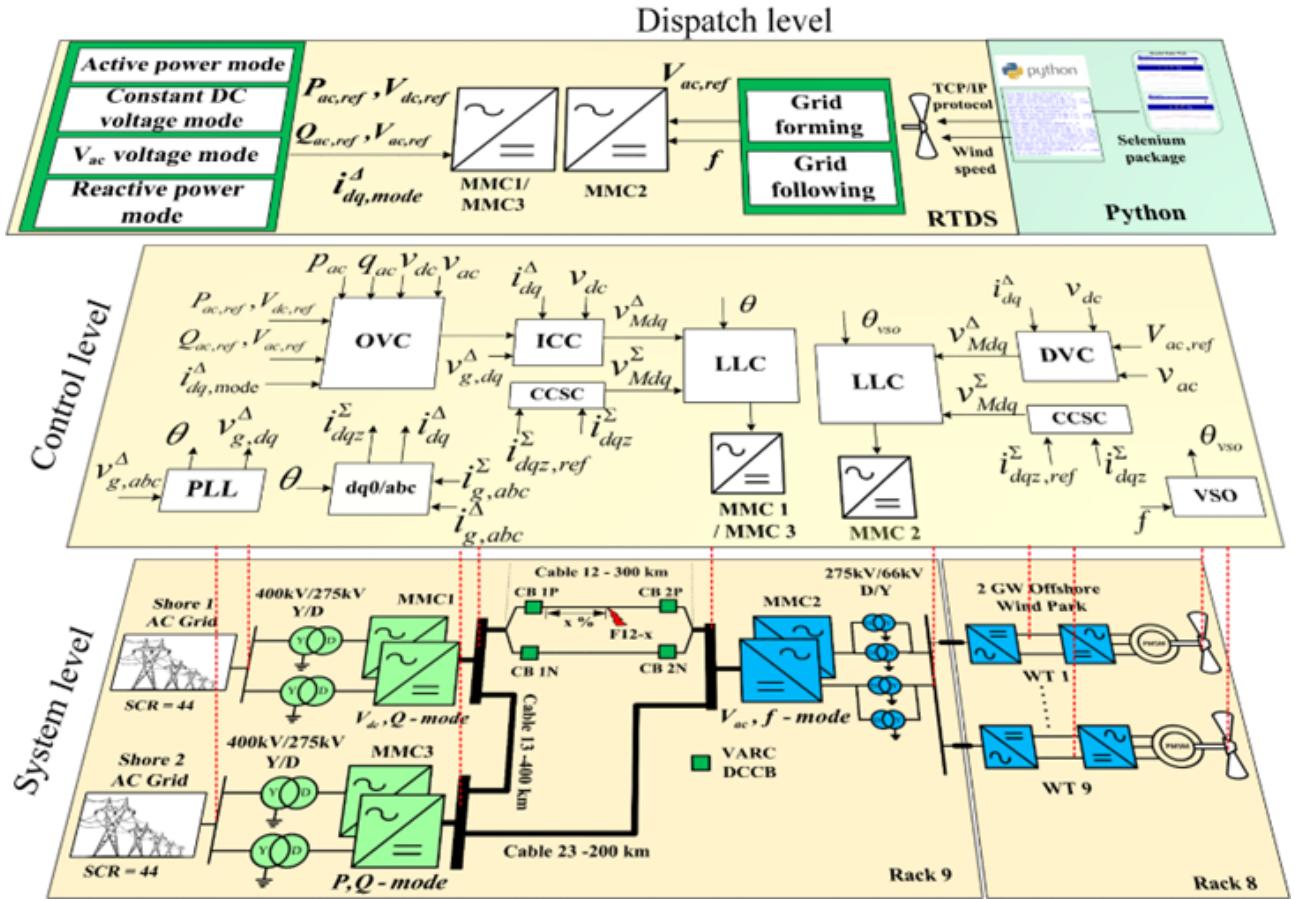


Figure 0.4.2: MTDC control structure.

Each power electronic converter needs to be designed and controlled in such a way that the whole HVDC system operates stable and at a desired operating point. Ideally, AC-DC offshore converters operate in grid-forming mode or islanded mode, and they ensure stable AC voltage and frequency of the wind turbines. Onshore DC-AC converters should provide stable DC voltage for the whole HVDC and also provide power sharing between converter stations.

0.5 HVDC Grids

The inclusion of large wind energy generation and its transmission using HVDC connection requires drastic developments of the power system. This stems from the fact that the current traditional power system is based on AC transmission and distribution. The use of HVDC connections requires devices used for the transfer between AC and DC voltages and currents, known as Power Electronic converters. So, the inclusion of PE requires the complete re-development of the traditional power system.

To function, high voltage DC (HVDC) systems need control strategies to manage the evacuation of generated wind energy to the main grid using modular multi-level converters (MMC) as power electronic interfaces. Underground cables (UGC) and overhead transmission lines (OHL) are used to transmit the generated power. The idea is that the control should be able to operate the MMC-HVDC systems for different operational transients such as power flow changes, wind speed variations, DC/AC grid faults, etc. A good controller should be able to show faster settling time and minimum voltage and power variations for any transient occurring in the system.

0.5.1 HVDC System Configurations

HVDC systems, in general, can be found in various arrangements based on necessity and feasibility. Such configurations are not limited to a VSC system; they can also be used for an LCC or an MMC-based system. Typically, there are three main arrangements – Monopolar, Bipolar, and Symmetric Monopolar arrangements.

0.5.1.1 Monopolar Configuration

In such a system, as shown in Fig. 0.5.1, the VSC stations are interlinked through a single pole line [8] operating at a positive or negative DC voltage. The ground or earth is used as the return path for the current.

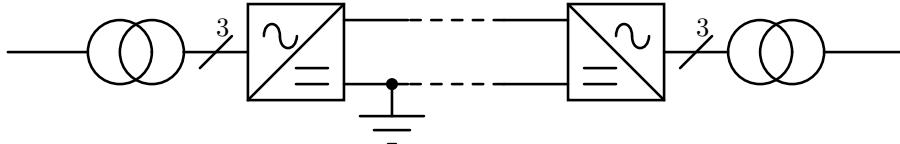


Figure 0.5.1: Monopolar HVDC power system.

The positive converter DC terminal equals the complete capacity of the DC voltage, while the negative terminal is ground. This configuration uses only one cable for the converter connection, and it has low costs. There is no DC ground current due to metallic return. Cons are the complete loss of one terminal in case of malfunctioning, ground return issues, and higher power losses due to the metallic return cable.

0.5.1.2 Symmetric Monopolar

In such a system as shown in Fig. 0.5.2, the symmetric monopole is similar to the monopole with the difference of DC voltage on the converters' terminals. Here the converter's positive and negative terminal voltages have the same absolute value of $V_{DC}/2$, but with opposite polarities. Therefore, the cables or conductors required for this configuration are smaller. There is also no need for the metallic ground return. However, similar to the monopole, the loss of one converter means a total terminal loss. The power losses are higher than in the monopole configuration and the costs are higher due to the existence of two cables. ther.

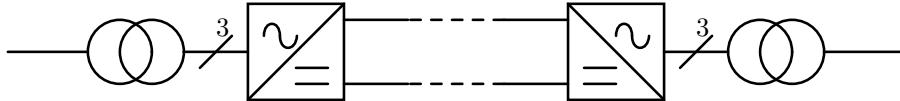


Figure 0.5.2: Symmetric monopolar HVDC power system.

0.5.1.3 Bipolar Configuration

Such a system, as shown in Fig. 0.5.3, involves the combination of two monopolar systems for positive and negative DC voltages [8]. The ground is still used as the return path for the current. In some cases, a metallic return path is used. By incorporating two monopolar arrangements, this configuration helps in providing $N - 1$

redundancy. In other words, a failure of one of the HVDC cables does not lead to the complete failure of the HVDC transmission. Typically, such a configuration is implemented more in overhead HVDC lines.

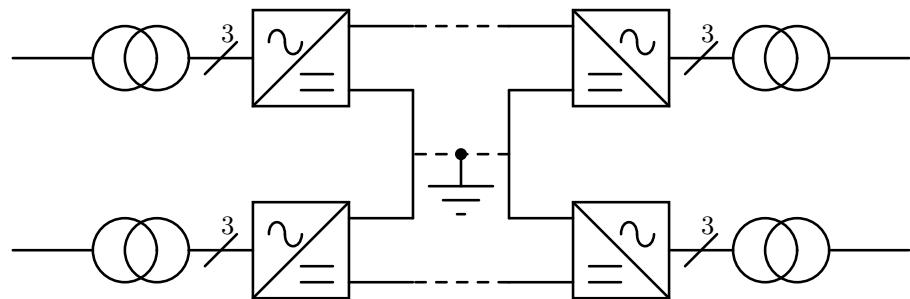


Figure 0.5.3: Bipolar HVDC power system.

0.6 HVDC Cables

The HVDC cables have been through a development of increasing high voltages and power, but also with new technology the HVDC VSC, where the dimensioning polarity reversal can be avoided, have driven the development of cables. The cables for HVDC can be divided into oil filled cables, mass-impregnated paper cables, Paper-Polypropylene Laminated-paper and extruded cables. These types are briefly described.

0.6.1 Mass-impregnated paper cable

This type is widely used in the world. The Mass-impregnated (MI) cable is paper wrapped around the conductor and filled with heavy thick oil. The MI cable do not need oil feeding from the ends and have therefore been the preferred solution for long-distance submarine transmission. The cable type is in service for a large number of power transmission links and is proven with excellent service reliability at voltage levels up to 600 kV and power ratings exceeding 1100 MW per pole, giving a bipole of 2200 MW. The conductor sizes are typically up to 2500 mm². The maximum water depth is 1650 m for the cable Italia-Sardinia 1000 MW and 500 kVdc while the 250 kVdc, 400 MW Spain-Mallorca cable has a maximum laying depth of 1485 m.

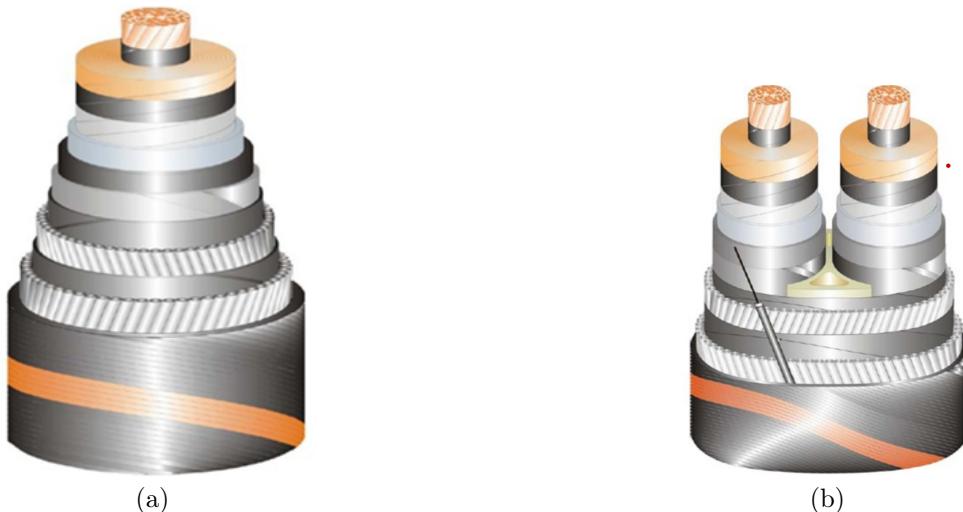


Figure 0.6.1: MI cable: (a) NorNed, NEXANS and ABB 700 mm²; (b) NorNed, 2 × 158 km NEXANS and 2 × 150 km ABB 700 mm².

The MI cables are composed by a very high viscosity impregnating compound which will not leak out of the cable in case of cable damage or failure. Compared to oil-filled cables, the compact design is also an advantage for deep water applications.

The MI cable is mainly used for HVDC, and there is no limitation in maximum length for the MI cable. This type of cable is less suitable for AC applications. The cables can be used for both LCC HVDC and HVDC VSC.

0.6.2 Paper-Polypropylene Laminated Paper (PPLP)

This type of cable uses a special low permittivity – low loss insulation type. Compared to conventional MI cables, it allows for increased transmitted power or reduced conductor size and cable dimensions. The use of PPL is in general considered for large sizes and voltages above 275 kV. The cable is also used for HVDC power transmissions. Currently, there is only one HVDC link in operation that uses this cable type. The Western link, connecting Scotland and UK, operates at a HVDC Voltage of 600 kV. The transmission capacity is 2,2 GW.

0.6.3 The extruded insulation HVDC cables

With the introduction of VSC HVDC introduced in 1997 with a 10 kV, 3 MW demonstration project at Hellsjön in Sweden, the extruded insulation cables were introduced. The insulation material as used is cross-linked polyethylene insulation (XLPE). The cable insulation consists of an inner semi-conducting screen layer, the insulation compound, and an outer semi-conducting insulation screen, extruded simultaneously.

The extruded HVDC cable systems have today the following “standard” levels at 80 kV, 150 kV, 200 kV and 320 kV which currently are in operation, also cables at 525 kV and 640 kV is available. All these systems are based on the same technological platform VSC HVDC.

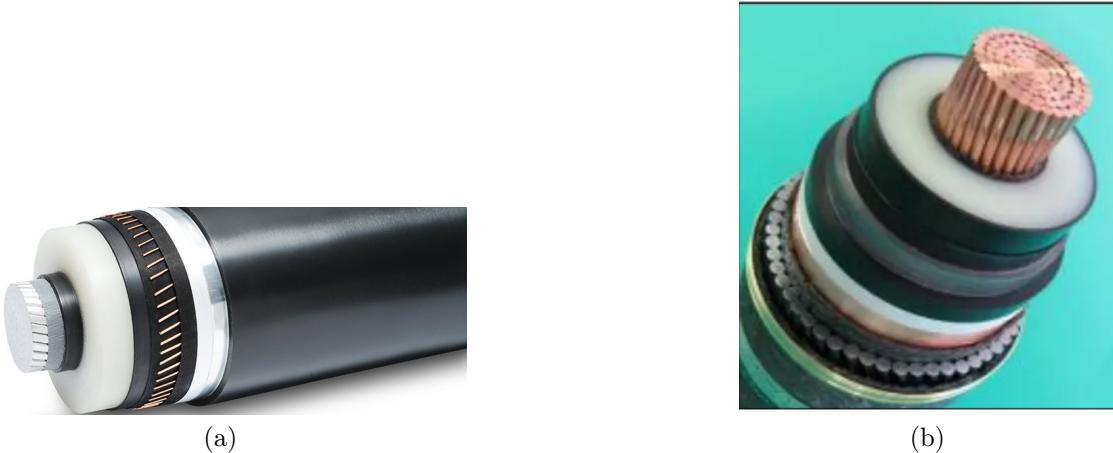


Figure 0.6.2: Extruded cable.

Suppliers claim these cables can be dimensioned for 640 kV cables with a transmission capacity of 3000 MW with a $2500 - 3000 \text{ mm}^2$ Cu conductor. The largest connections in operation today operate at 320 kV and 900 MW. These are all applied in various projects in Germany. The following figure demonstrates the use of cables as a function of the year of application.

0.6.4 Future developments in HVDC cables

The cable industry is heavily involved in innovation. The given fact that much more cables will be needed in the coming decades has led to innovative research on production technologies and installation techniques.

The cable design itself is focusing on a number of areas:

- Reduction of cable losses. In particular high temperature super conduction has gained much interest. Several test and trial projects are in progress around the world.
- Increasing the performance of insulating material. New materials such as High-Performance Thermoplastic Elastomer (HPTE) and materials doped with nano particles offer a lot of benefits.

The future of these developments looks promising. However, given the fact that the NSWPH needs to be developed in the coming years leads to the conclusion that these innovations are not incorporated in the upcoming activities.

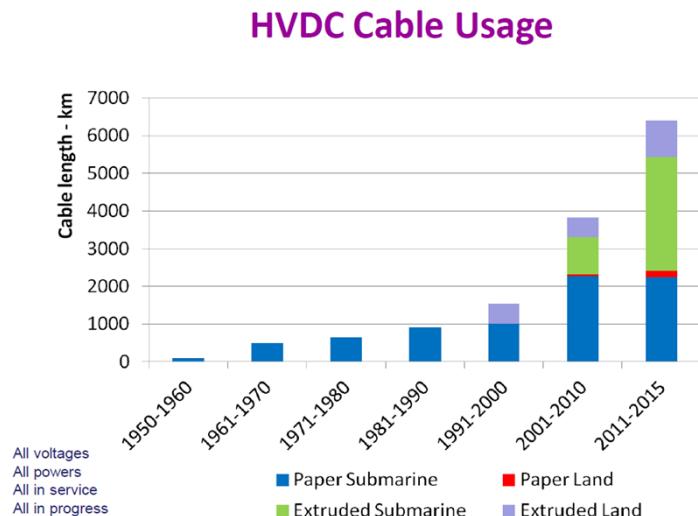


Figure 0.6.3: Cable utilization in the world.

0.7 Protection

The grid protection philosophies are classified into 3 major categories depending on the type of fault-clearing strategy employed:

- Non-selective fault clearing strategy;
- Partial selective fault clearing strategy;
- Full selective fault clearing strategy.

Non-selective Fault Clearing Strategy In this type of grid philosophy, the entire HVDC grid is seen as a single protection zone. So in case of fault, the entire zone is switched off by:

- The AC breakers in all converter bays;
- Current control in full bridge converters;
- HVDC circuit breakers in the converter connection points.

The faulted section is identified and disconnected after fault clearance with mechanical or high-speed switches.

Partial Selective Fault Clearing Strategy In this network, the entire HVDC grid is divided into several protection zones. In case of a fault in a particular zone, it is isolated from other zones by:

- HVDC circuit breakers in the connection points;
- DC-DC converters between the zones;
- Current limiters (SFCL) between the zones.

The faulted section is identified and disconnected after fault clearance with mechanical or high-speed switches.

Full Selective Fault Clearing Strategy In this network, each branch in the HVDC grid is a separate protection zone. The faulted branch is isolated from the other zones by HVDC circuit breakers in the faulted branch. In this case, the faulted branch is immediately identified.

0.7.1 HVDC Circuit Breaker

The same basic idea underlies all DC circuit breakers (DCCBs): creating a counter voltage that is higher than the system voltage for a significant amount of time. The (fault) current is suppressed to zero (really to leakage levels) within the fault-current suppression time while the counter voltage is present.

All phases of DC fault current interruption (from fault inception to current zero) should be defined, however the terminologies used should be independent of the HVDC circuit breaker's technology (arc, semiconductor, or a combination of both) (HVDC CB). This brochure only considers high-voltage topologies; it ignores topologies like low-voltage DC CBs, where the counter-voltage and energy dissipation are accomplished via an arc. The emphasis is on system topologies that allow for the disregard of propagation effects brought on by transmission conductor length. The voltage and current traces change from what is described below and grow more complex as propagation effects become more significant. Furthermore, it is believed that local measurements will be used in the protection plan. Several examples for this are provided in a subsequent section after the definitions because the duration of the various intervals varies and can even overlap depending on the individual topology.

A schematic representation of an interruption process is shown in Fig. 0.7.1. It is presented here in a topology-independent manner. The duration of the time intervals may differ significantly depending on the particular breaker topology. The voltage across the HVDC CB terminals and the fault current flowing through the HVDC CB are plotted (dashed lines). The following provides an explanation of the steps using a fault current as an example:

1. The first vertical dash-dotted line (fault inception) indicates the instant at which the fault occurs, as seen locally at the breaker site.
2. The protection system needs to detect the fault, select the faulted line, and give a trip order to the respective circuit breakers. Depending on the protection system, this may take a certain time (relay time) in the order of tens of microseconds to a few milliseconds. If the protection system contains relays using local and non-local information, also intermediate orders may be given; these may be of help for some kind of circuit breakers with preactivation functions.

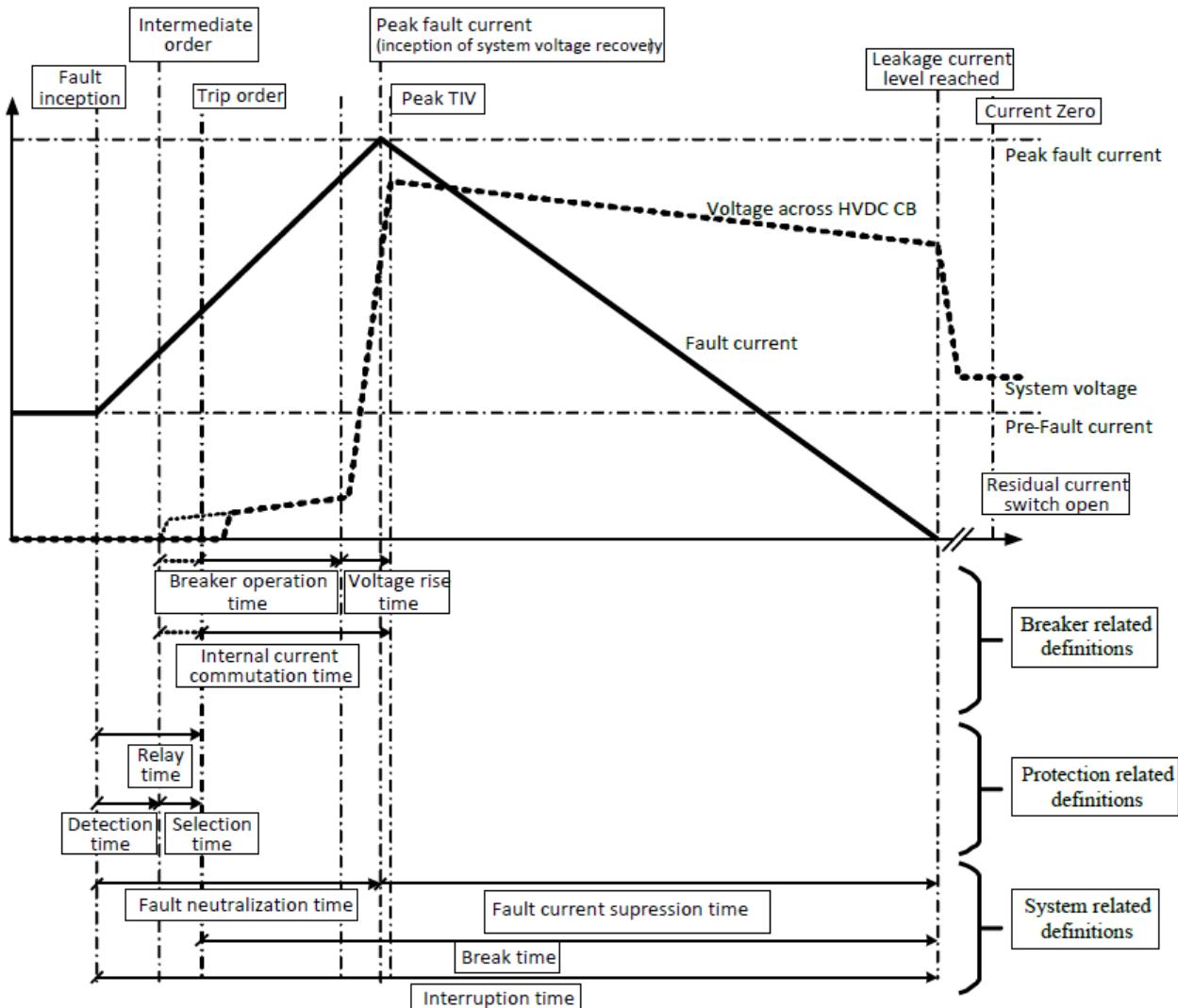


Figure 0.7.1: Schematic of a fault interruption process with current through (solid thick line) and the voltage across the HVDC CB (dashed lines) as a function of time.. Image inspired from [17].

- After the trip order is received by the breaker, it will start to commute the current from the nominal current path into the energy absorption path. This can be in one step or as indicated in Fig. 0.7.1 in several steps, using additional internal commutation path(s). For some HVDC CB topologies, a small voltage increase may be noticeable, either directly at or after the intermediate order or the trip order. This is indicated in Fig. 0.7.1 by the small voltage increase after the trip order and the dashed line at the beginning of the “internal current commutation time” interval.
- During the internal commutation phase, the voltage rises to the peak Transient Interruption Voltage (TIV). In a network this has a particular importance: as soon as the voltage across the HVDC CB has built up enough such that locally the total counter-voltage is larger than the system driving electromagnetic force³, the fault current through the HVDC CB starts to decrease. It is this instant in time when the fault is neutralized so that the system voltage for the remaining healthy system can start to recover, even though the fault current is not yet interrupted. This definition is chosen independently on the circuit breaker topology and can involve steps like turning off power electronic branches, active injection of current pulses, and others.
- When the inductive energy from the faulted system is dissipated, the current through the breaker is reduced to zero. Strictly speaking, the current is reduced to the residual current level that results from the voltage difference across the breaker terminals.

6. An additional residual current breaker may need to open to interrupt the leakage current through the MOSA and to limit the thermal stress on them.

The timing definitions partially overlap, but this is necessary since many experts working with a focus on the circuit breaker, the protection system, or the configuration of the HVDC system will use the definitions. Curly brackets are used to denote the various locations on the right side of Fig. 0.7.1.

Transient Interruption Voltage (TIV): It is the voltage across the HVDC CB terminals as a function of time during the DC current interruption process (see Fig. 0.7.1).

NOTE 1: to decrease the fault current, the TIV must exceed the system-driving electromagnetic force.

NOTE 2: the wording for TIV was deliberate to avoid misunderstanding with TRV as used in AC current interruption. In DC systems, the TIV is the voltage created by the breaker during the entire current interruption process.

Transient Interruption Voltage Peak (Peak TIV): The peak value of voltage across the two terminals of the HVDC CB during the interruption process (see Fig. 0.7.1).

A counter voltage can be created and maintained using a variety of technologies. By lengthening, cooling, and splitting the arc, a counter arc voltage can be attained for voltages up to around 10 kV. The counter voltage in the case of HVDC CBs is produced by directing the current through a high-impedance route, charging the commutation branch or by increasing the resistance (high-impedance route) in the commutation branch. HVDC CBs are classified into four topology groups:

1. **Passive Oscillation HVDC CB (PO HVDC CB):** This kind of CB causes an oscillating current to start when an interrupter in the main current branch of the CB is opened. This type of CB does not match the technical requirements for HVDC applications in terms of fault-clearing time and current turn-off capability because it is typically utilized as a current commutation switch.
 2. **Power Electronic HVDC CB (PE HVDC CB):** According to Fig. 0.7.2, this type of CB contains two parallel branches. The main current branch, which normally consists of numerous power semiconductors coupled both in series and parallel, carries the continuous current during normal operation. All power semiconductors are disabled in the event of an intentional turn-off, and the current is then commutated into the parallel-connected high-impedance energy absorption device. This kind of circuit breaker may swiftly commutate current, often in microseconds because no mechanical switches are required. However, because the load current passes through power semiconductors, a PE HVDC CB's electrical losses are typically deemed to be too large for usage in transmission systems.

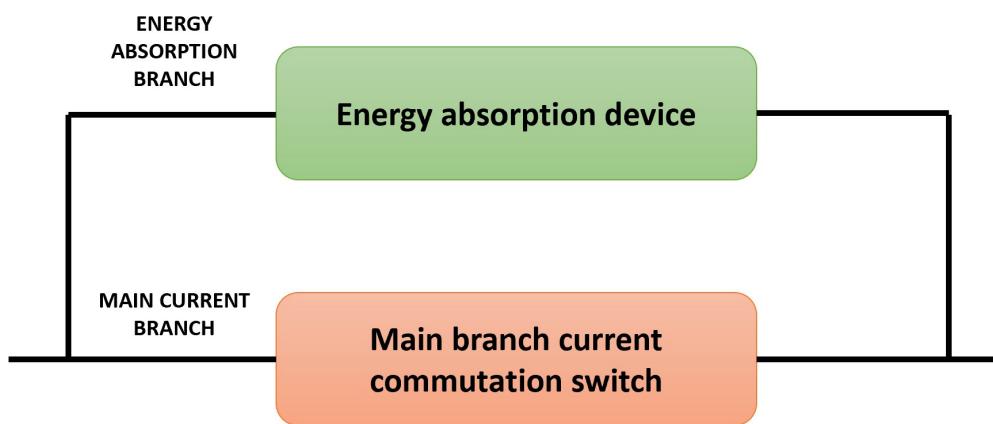


Figure 0.7.2: PE HVDC CB – basic layout. Image inspired from [18].

- 3. Active Current Injection HVDC CB (ACI HVDC CB):** According to Fig. 0.7.3, this type of CB contains three parallel branches. The main branch breaker normally allows current to pass through it, however, to stop current flow, this main branch breaker needs a current-zero. The main branch breaker of the ACI CB is instructed to open as the initial stage in ACI HVDC CB operation. The main branch

breaker is then activated by the current injection branch, which creates an opposite direction, stronger current than the DC current that has to be interrupted. This injected current causes an interruption in the main current branch and zero crossings of the current in the main branch breaker. The current flowing through the main branch breaker is first commutated into (the capacitor of) the current injection branch and then into the energy absorption device when it is opened. Studies and trials have demonstrated that the capabilities of this CB type can satisfy the needs of standard HVDC systems.

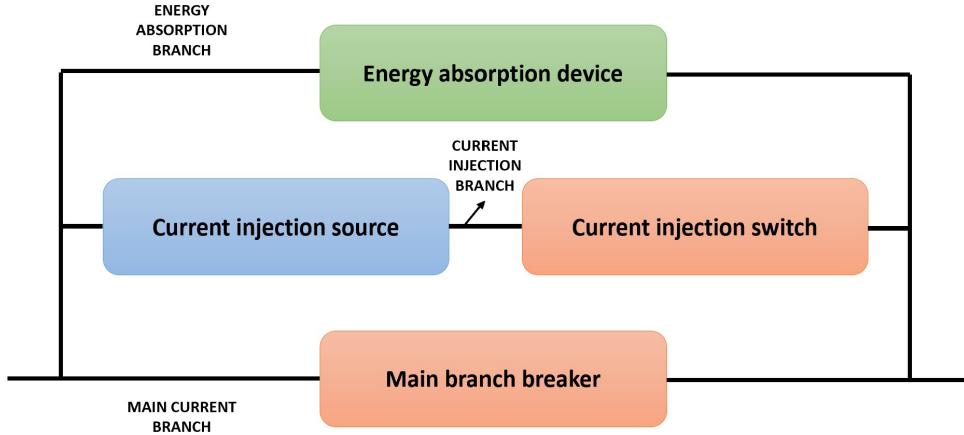


Figure 0.7.3: ACI HVDC CB – basic layout. Image inspired from [18].

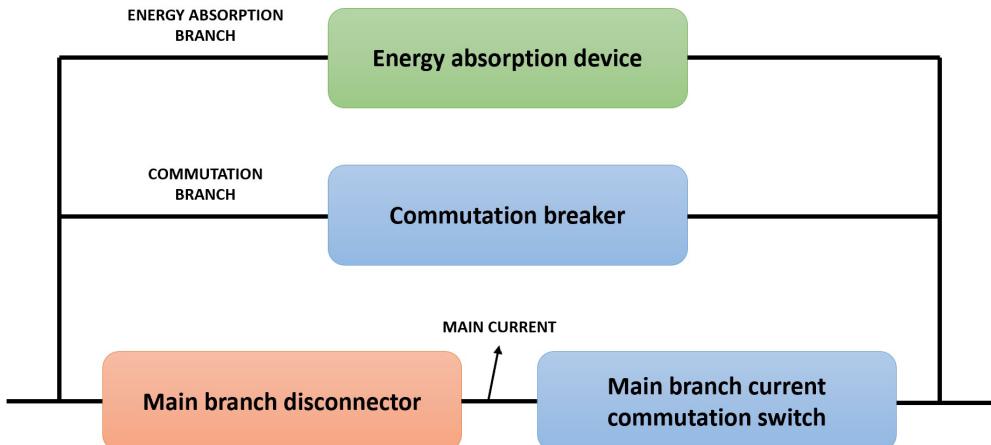


Figure 0.7.4: MPE HVDC CB – basic layout. Image inspired from [18].

4. Mechanical and Power Electronic (Hybrid) HVDC CB (MPE HVDC CB): In some literary works, this HVDC CB type is sometimes referred to as a “hybrid” HVDC CB. According to Fig. 0.7.4, the main current branch is made up of one or more main branch mechanical disconnectors and a main branch current commutation switch that is realized by connecting power semiconductors in series and parallel.

- In the first step, the main branch current commutation switch opens to commutate the DC current to the parallel-connected commutation branch.
- After the voltage withstand capability of the main branch disconnectors is established, the commutation breaker (typically a large number of series connected power semiconductors) is opened.
- The current flowing in the commutation branch is commutated to the parallel connected high-impedance energy absorption device.

Experiments and applications have shown that the capabilities of this breaker type could fulfill HVDC system requirements.

Table 3: Summary of technical features of ACI HVDC CBs and MPE HVDC CBs

	ACI HVDC CB	MPE HVDC CB
Basic layout	see Fig. 0.7.3	see Fig. 0.7.4
Main Components	Main current branch: – Fast mechanical circuit breakers. Current injection branch: – Reactors and capacitors; – Power semiconductor valve or mechanical switch dependent on the topology to initiate the injected current. Energy absorption branch: – MOSA.	Main current branch: – Very fast disconnectors; – Current commutation switch, typically power semiconductors with turn-off capability. Commutation branch: – Power semiconductor valve. Energy absorption branch: – MOSA.
Typical Properties	– Very low (conduction) losses. Requires insulated power supply with sufficient power and voltage for charging of capacitors. – Requires fast circuit breaker in the main current branch with breaking and TIV withstand capability. – Small number of subcomponents.	– Low (conduction) losses. Main branch current commutations which needs continuous cooling. – Requires fast disconnector in main current branch with TIV-withstand capability. – O-C-O and FCL operation mainly limited by MOSA energy capability and auxiliary power capability.

0.7.2 Detection of DC faults

For the process of fault isolation using HVDC CBs, it is important to identify the occurrence of a DC fault in the complex HVDC system. If the faulty line is identified, a trip order can be triggered to the respective CBs. For DC systems, the allowable time to identify and isolate the fault is limited to a few milliseconds as compared to some hundred milliseconds for AC faults. This means that a delay of a few milliseconds to identify and isolate the fault can lead to system collapse in DC grids as shown in Fig. 0.7.5. Here, if the fault is cleared after around 4ms of fault inception, the DC link voltages of the MMC converter settle to a new steady state operating point. However, if the fault clearing time is delayed by 6ms which means that fault is cleared after 10ms, the DC link voltages of the MMC converter collapse leading to system collapse. A DC fault contingency

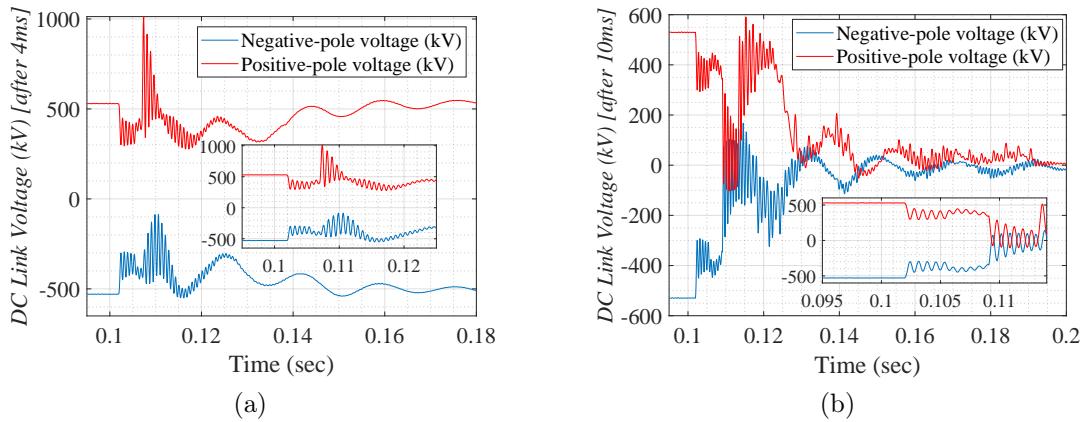


Figure 0.7.5: DC link voltage when DC fault is cleared after (a) 4ms, (b) 10ms of fault inception

shows a peculiar fault behaviour due to the following reasons:

- Capacitance discharge of the converters (CSA1-CSA5 as shown in Fig. 0.7.6) upon the fault inception leads to a very high rate of rise of current. Additionally, DC faults are low-frequency transients which means that a low impedance is offered by the DC cables which increases the equivalent rise of current.
- Practically implemented half-bridge MMCs are defenseless against DC faults as the freewheeling diodes of the converter act as uncontrolled rectifier bridges upon fault inception.

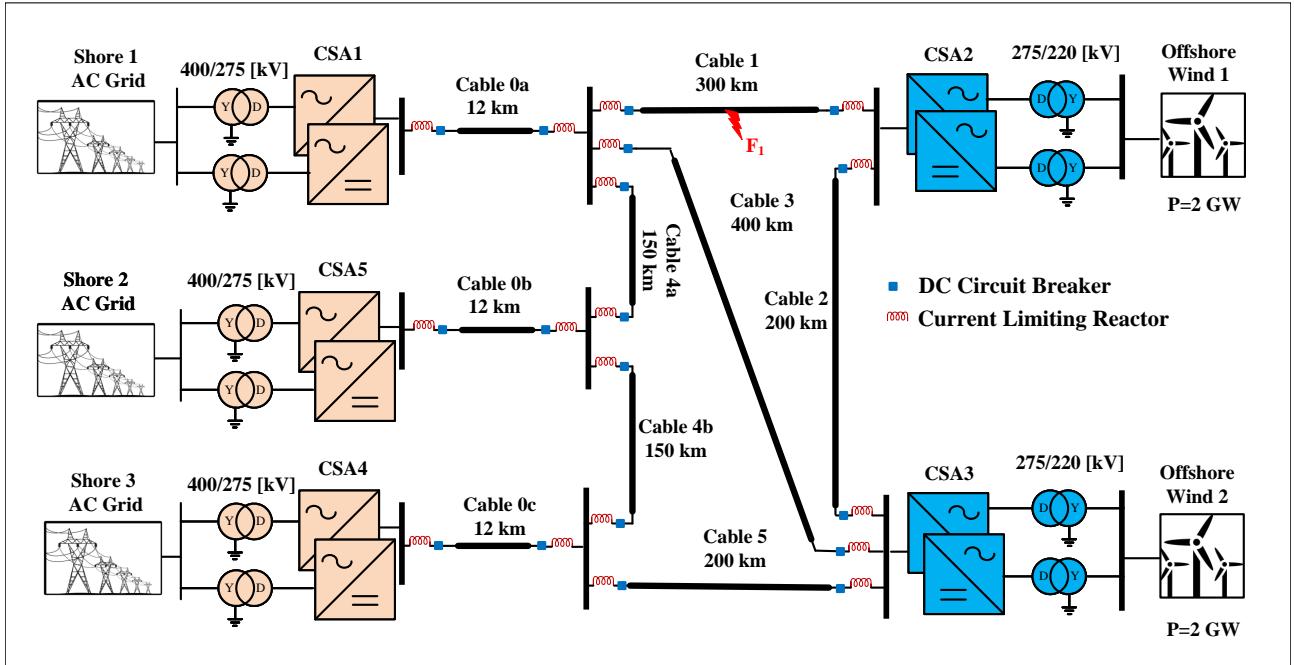


Figure 0.7.6: Multi-terminal $\pm 525\text{kV}$ MMC-HVDC system

As a result, literature on the protection of DC power systems use physical current limiting reactors (CLRs) with each transmission line as shown in Fig. 0.7.6. The externally placed CLRs not only help in limiting the rate of rise of fault current (as shown in Fig. 0.7.7) but also act as unique fault differentiators. The presence of CLRs prevents the instantaneous rise of current, where CLRs accumulate very high energy during the initial fault transients. Therefore, if the voltage across CLRs is measured, the fault shows a peculiar behavior and can be detected in less than 1 ms effectively. Measuring pole-voltages across CLRs and comparing them to a static

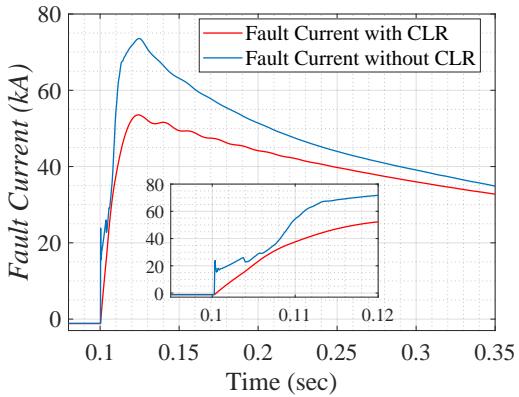


Figure 0.7.7: Fault current in the presence (red line) and absence (blue line) of current limiting reactors

threshold (decided based on the voltage level and system parameters) can be used to detect the occurrence of a DC fault. This approach differentiates between a normal operational power transient and a DC fault transient which means that the approach is secure. Further, everytime there is a DC fault (no matter the type, severity or fault distance), the given approach indicates the presence of the fault without a miss. This means that the approach is dependable. Finally, the approach clearly differentiates the fault zones as internal or external which means that the approach focuses on the occurrence of internal faults only which makes the method selective. The occurrence of the fault is identified almost instantaneously following the inception of the fault. For a bipolar line configuration, the fault can be of different types: pole-to-pole (PTP), positive pole-to-ground (P-PTG), negative pole-to-ground (N-PTG). Based on the voltage across CLRs at each pole, the fault can be detected and further, classified to its type. This helps in narrowing down the affected area due to the fault contingency. For a pole-to-pole (PTP) contingency, it is observed that both the positive and negative pole voltages across the current limiting reactor show instantaneous variations as shown in Fig. 0.7.8(a). For

a positive pole-to-ground (P-PTG) contingency, it is observed that only the positive pole voltage across the current limiting reactor shows an instantaneous variation whereas the negative pole voltage across the current limiting reactor does not violate the fault static threshold as shown in Fig. 0.7.8(b). For a negative pole-to-ground (N-PTG) contingency, it is observed that only the negative pole voltage across the current limiting reactor shows an instantaneous variation whereas the positive pole voltage across the current limiting reactor does not violate the fault threshold as shown in Fig. 0.7.8(c).

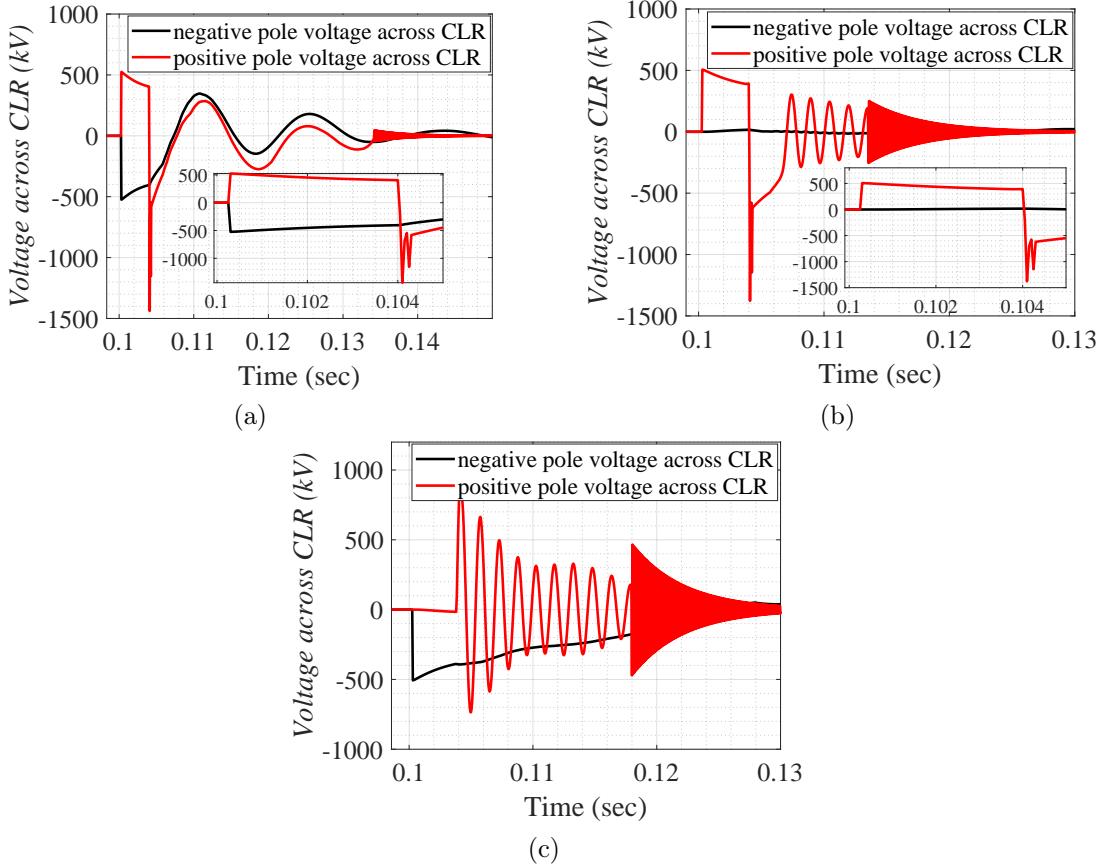


Figure 0.7.8: Voltage across CLRs for (a) PTP fault, (b) P-PTG fault, (c) N-PTG fault

0.7.3 Locating the DC faults

Once the fault is identified, accurately locating the fault (or evaluating the distance of the fault) helps in the rapid restoration of the isolated line back into the system. Generally, HVDC systems have long lines for the transmission of power. Using double-terminal methods is suitable for fault location for systems with long transmission lines. The double-terminal method uses the voltage and current measurements at both terminals which are related to the DC fault. The idea is to use simple R-L representation for long transmission lines or underground cables along with measured terminal currents and voltages related together by Kirchhoff's Voltage Law (KVL). If the fault is identified as PTP, Fig. 0.7.9(a) shows the equivalent 2-terminal circuit. Here $i_1(t)$ and $i_2(t)$ are the current through CLRs at each terminal while $v_{dc1}(t)$ and $v_{dc2}(t)$ are voltage after CLRs, L_{m1} and L_{m2} as indicated in Fig. 0.7.9. Additionally, $v_1(t)$ and $v_2(t)$ are the terminal DC bus voltage whereas x_0 is the defined fault location and D_0 is the total line or cable length. Using simplified R-L representation for the line or cable, r_o is the resistance per unit length whereas l_o is the inductance per unit length of the line or cable. Applying KVL using the two terminal related to the fault as shown in Fig. 0.7.9(a), equation (53)-(54) are obtained.

$$2r_o x_o i_1(t) + 2l_o x_o \frac{di_1(t)}{dt} + R_f [i_1(t) + i_2(t)] = v_{dc1}(t) \quad (53)$$

$$2r_o (D_o - x_o) i_2(t) + 2l_o (D_o - x_o) \frac{di_2(t)}{dt} + R_f [i_1(t) + i_2(t)] = v_{dc2}(t) \quad (54)$$

Using differential term in the application of the location algorithm can lead to erroneous distance calculations in the presence of noise in measurement. These current derivative terms can be replaced by the drop in

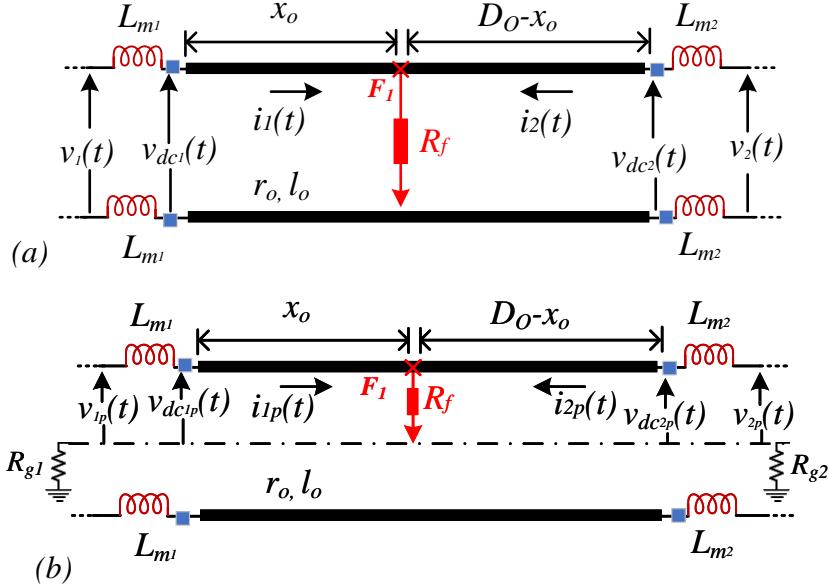


Figure 0.7.9: Equivalent 2T circuit for (a) PTP, (b) P-PTG fault

voltage across the CLR avoiding additional WGN due to differential calculations. These terms are $\frac{di_1(t)}{dt} = \frac{v_1(t) - v_{dc1}(t)}{2L_{m1}} = \frac{u_1(t)}{2L_{m1}}$; $\frac{di_2(t)}{dt} = \frac{v_2(t) - v_{dc2}(t)}{2L_{m2}} = \frac{u_2(t)}{2L_{m2}}$. Subtracting equations (53) and (54) negates the dependence of fault location on fault resistance. Further, substituting the current differential terms with the voltage across CLR and rearranging give x_0 as equation (55) which is defined as the fault location for a PTP fault contingency.

$$x_0 = \frac{[v_{dc1}(t) - v_{dc2}(t)] + 2r_o D_o i_2(t) + \frac{l_o D_o}{L_{m2}} u_2(t)}{2r_o [i_1(t) + i_2(t)] + \frac{l_o u_1(t)}{L_{m1}} + \frac{l_o u_2(t)}{L_{m2}}} \quad (55)$$

If the fault is identified as either P-PTG (category of PTG faults), Fig. 0.7.9(b) shows the equivalent 2-terminal circuit. Here $v_{dc1p}(t)$, $v_{dc2p}(t)$ are the positive pole voltages after CLRs, $i_{1p}(t)$, $i_{2p}(t)$ are the positive pole currents and $u_{1p}(t)$, $u_{2p}(t)$ are positive pole voltages across CLRs. R_{g1} and R_{g2} are the grounding resistances of respective terminal. For a P-PTG fault, the expression for x_0 is given as equation (56).

$$x_0 = \frac{[v_{dc1p}(t) - v_{dc2p}(t)] + r_o D_o i_{2p}(t) + [R_{g2} i_{2p}(t) - R_{g1} i_{1p}(t)] + \frac{l_o D_o}{L_{m2}} u_{2p}(t)}{r_o [i_{1p}(t) + i_{2p}(t)] + \frac{l_o u_{1p}(t)}{L_{m1}} + \frac{l_o u_{2p}(t)}{L_{m2}}} \quad (56)$$

Similar expression can be derived for a N-PTG fault. Further, if the terminals are solidly grounded i.e., $R_{g1}=R_{g2}=0\Omega$, the fault location (x_0) for PTG fault category is same as that for PTP fault contingency and is given by equation (55). The implementation of the discussed time-domain fault location method is simple, accurate and fast. The method gives valuable fault location time-domain plots for nearly 1ms right after the fault detection. The process of fault isolation and fault location can be carried out in parallel for timely system restoration once the fault is identified.

0.8 Overview — RTDS/RSCAD (to be read before the session)

This appendix section is a must to be read before the hands on session. For the preparation of the tutorial, material is used from [19].

This section contains a brief description of converter technologies and their modelling in RSCAD. An overview of RTDS hardware and RSCAD software is also given. Finally, guidelines are given to help students install RSCAD and OpenVpn, navigate through the software and learn more.

0.8.1 RTDS

RTDS simulator, see Fig. 0.8.1, is used for real time power system simulation. The simulator is designed to conduct Electro Magnetic Transient Simulations (EMT). The simulator can work over a frequency range of DC to 3 kHz. The RSCAD software is also designed by RTDS Technologies. It is a power system simulation software designed for interfacing to the RTDS Simulator hardware. The RSCAD software acts an interface which intends to create a working environment familiar to the power system engineer. It allows the user to perform all of the necessary steps to prepare and run simulations, and to analyze simulation results.

RTDS simulator hardware can simulate complex power systems with a typical time step of $25 - 50\mu\text{s}$. The hardware also allows for small time-step in the range of $1 - 4\mu\text{s}$. The hardware is composed of modular chassis which contains multicore processor. The first generations of processor cards were called 3PC. The next generation of processor cards are called PB5 cards, which is currently widely used around the world. The newest generation of simulation hardware is called NovaCor. RTDS facility in TU Delft has 2 NovaCor cards while others are with PB5 processor cards. Figs. 0.8.1, 0.8.2, and 0.8.3, show the different RTDS type of installations in TU Delft.



Figure 0.8.1: A typical RTDS hardware setup.

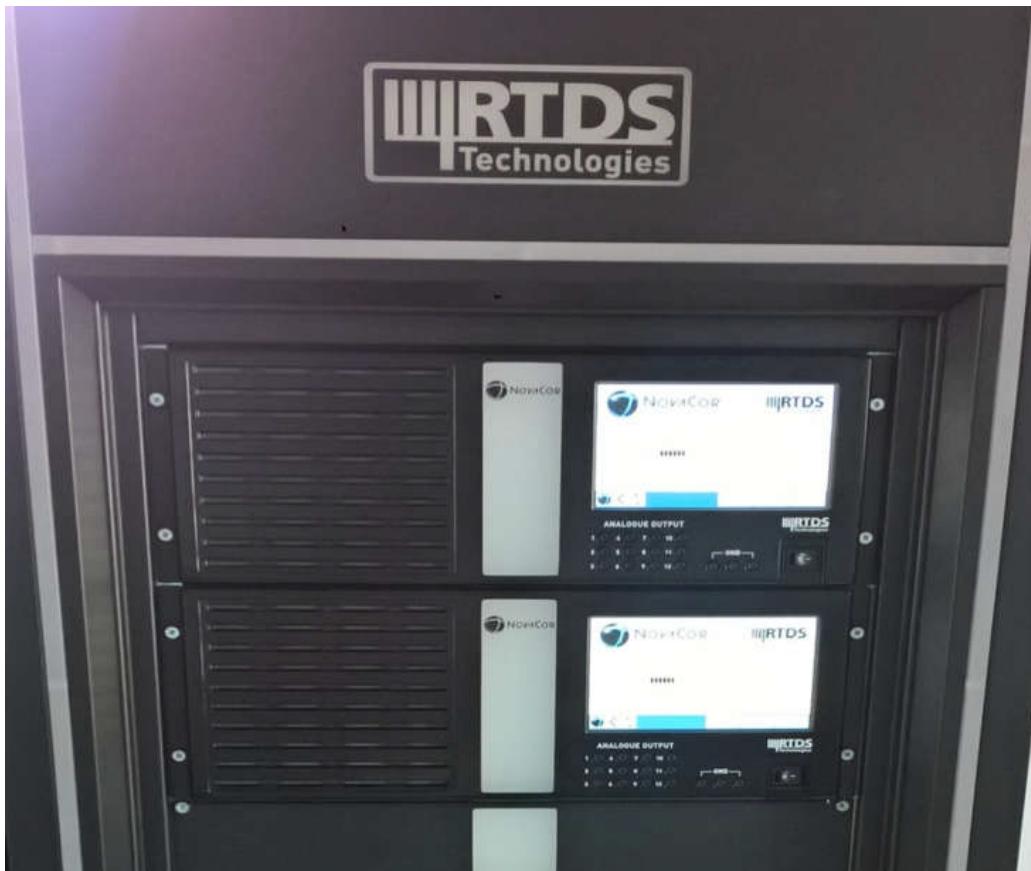


Figure 0.8.2: RTDS hardware setup with the latest NovaCor processor card.

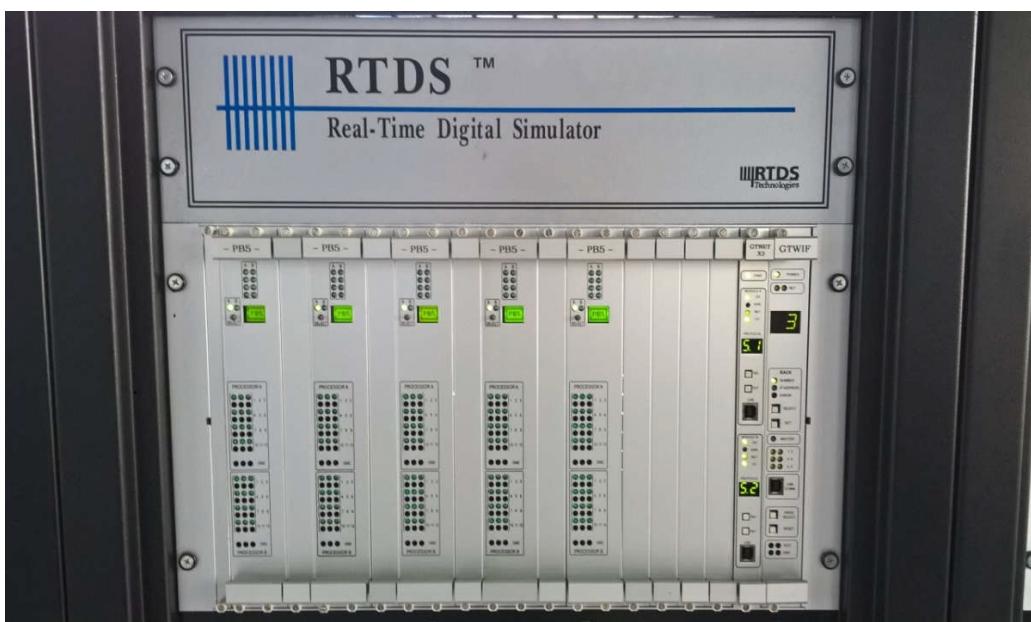


Figure 0.8.3: RTDS hardware setup with the PB5 processor card.

0.8.2 RSCAD

RTDS has its own software support system called RSCAD. RSCAD is used for modelling any power system, compiling it to see if it fits all RTDS requirements and finally executing it in the RTDS hardware. RSCAD is organized into a hierarchy containing three separate levels: high level graphical user interface, mid-level compiler and communications and the low level WIF multi-tasking operating system. The RTDS user is exposed only to

the high level software with the lower levels being automatically accessed through higher level software.

0.8.2.1 RSCAD Graphical User Interface

The high level RTDS software comprises the RSCAD family of tools. RSCAD is a software package developed to provide a fully graphical interface to the RTDS. Prior to the development of RSCAD, another software suite: PSCAD served as the graphical user interface to the RTDS hardware.

0.8.2.2 RSCAD/File Manager

As seen in the below screenshot, Fig. 0.8.4 represents the entry point to the RSCAD interface software. Fileman is used for project and case management and facilitates information exchange between RTDS users. All other RSCAD programs are launched from the Fileman module. Different RSCAD modules can be seen in Fig. 0.8.5.

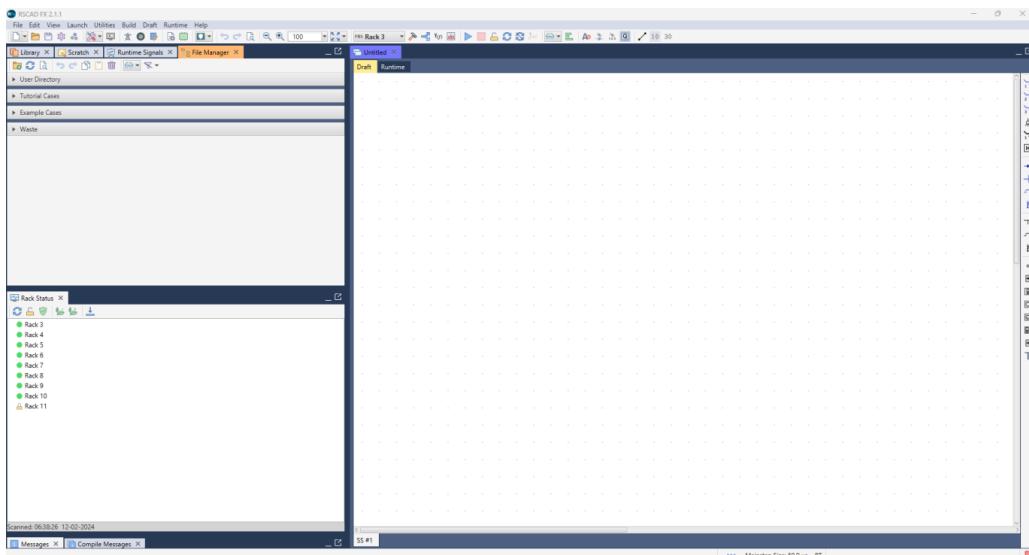


Figure 0.8.4: RSCAD Fileman.

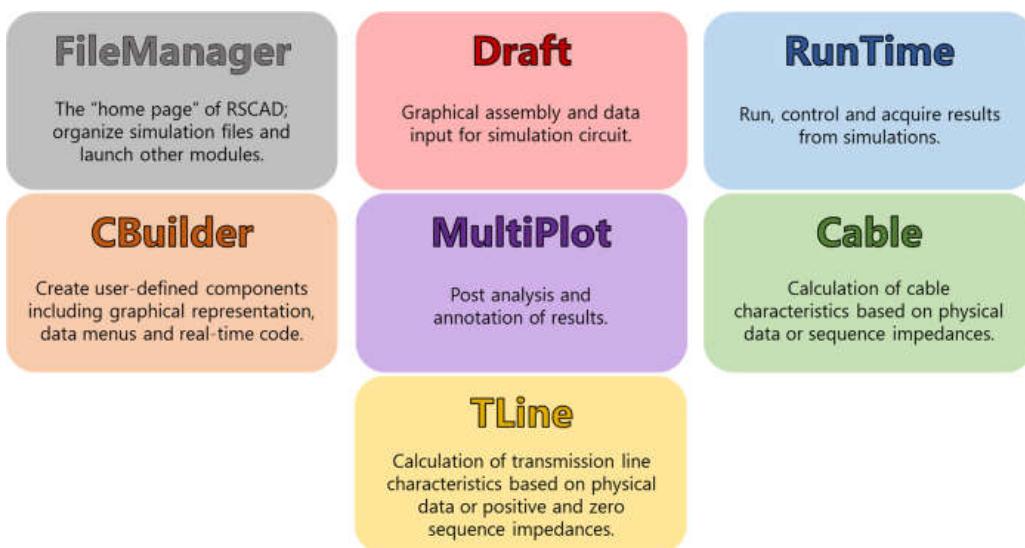


Figure 0.8.5: Different RSCAD modules.

In RSCAD fileman, a circuit is first designed in the draft file and saved. Compiling of the draft file is done to check if it meets all design requirements of RSCAD modelling. Any warning/error is indicated by the software at this stage so that it can be rectified. A draft file cannot be executed on the RTDS hardware unless successfully compiled in the RSCAD software.

RSCAD file manager has 4 sub-sections.

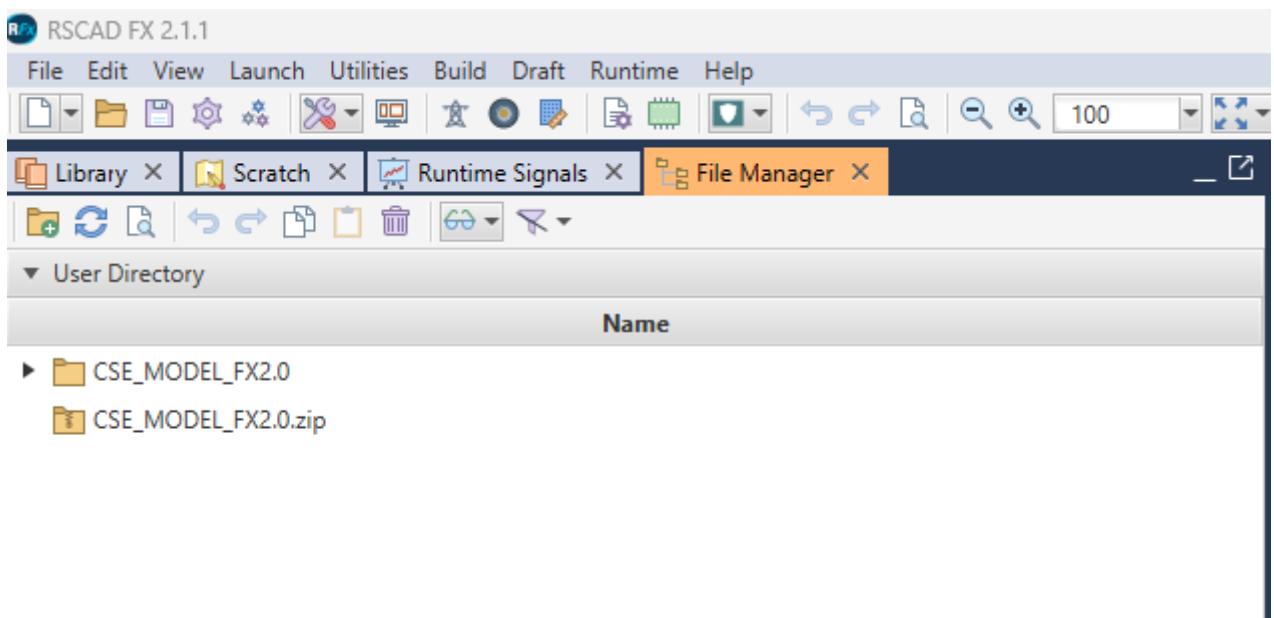


Figure 0.8.6: User Directory in RSCAD.

- User Directory;
- Tutorial cases;
- Example cases;
- Waste.

USER DIRECTORY: It is the path of the all files RSCAD can access in your system. For example, if the RSCAD is installed in the C directory, then to access the user directory of RSCAD use this path C:\RSCAD\RTDS_USER_FX\fileman\.

Where as Tutorials and Example cases have files to sample files to learn and get started with RSCAD.

0.8.2.3 RSCAD Draft

In RSCAD fileman, a circuit is first designed in the draft file and saved. **Compiling** of the draft file is done to check if it meets all design requirements of RSCAD modeling. Any warning/error is indicated by the software at the bottom right corner of the software at this stage so that it can be rectified. A draft file cannot be executed on the RTDS hardware unless successfully compiled in the RSCAD software.

In the RSCAD a new draft file is created or opened as shown in Fig. 0.8.7.

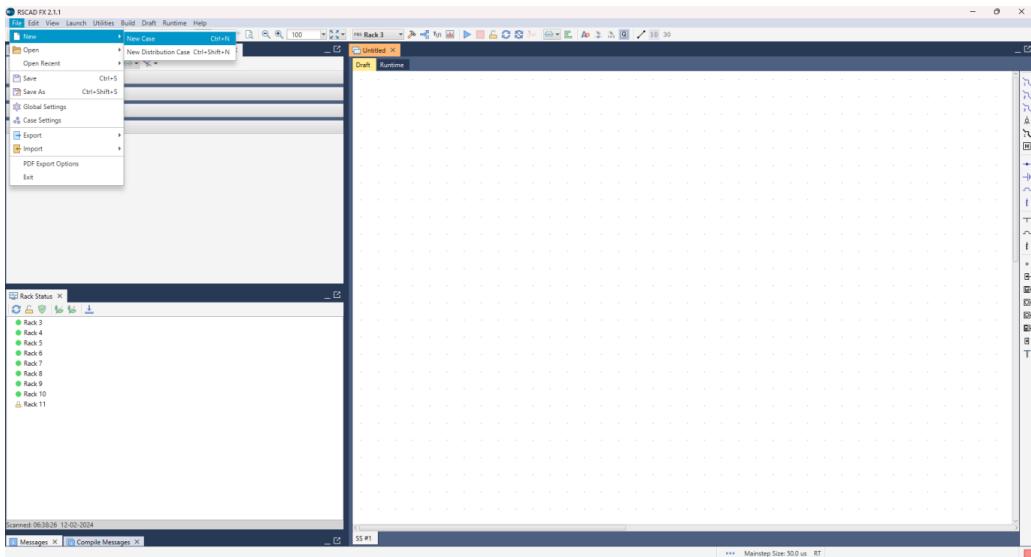


Figure 0.8.7: RSCAD DRAFT create.

RSCAD draft is used for circuit assembly and parameter entry. The draft file screen (see Fig. 0.8.8) is divided into two sections: the library section (left side) and the circuit assembly section (right side). Individual component icons are selected from the library and placed (drag & drop) in the circuit assembly section. Interconnection of individual component icons and parameter entry follows through a series of menus.

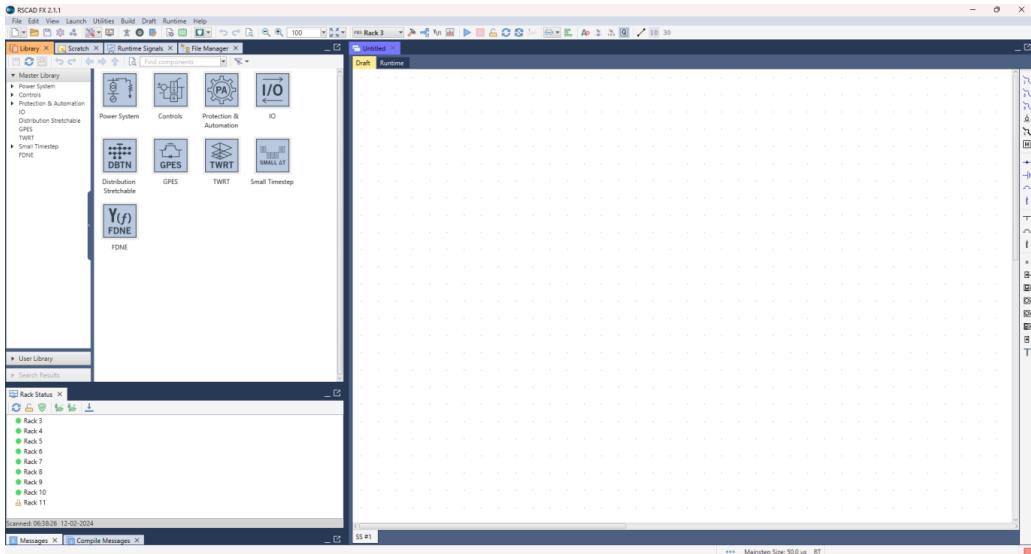


Figure 0.8.8: RSCAD DRAFT module.

The Circuit can be constructed in the draft on the left side of the screen. Various components and libraries for circuit building are available on the left side in the library section. RSCAD has various component libraries which can be used for designing the different circuits. There are 2 libraries named Master library and User library. There are four main components in the master library:

1. Power System Component Library.
2. Control System Component Library.
3. Small Time Step Component Library.
4. Protection & Automation Library.

In the draft file, the above power circuit and the control logic were built using the “Power System” and “Controls” libraries respectively, available in RSCAD as in Fig. 0.8.9. The power circuit is connected using buses, and the control logic is built using wire labels.

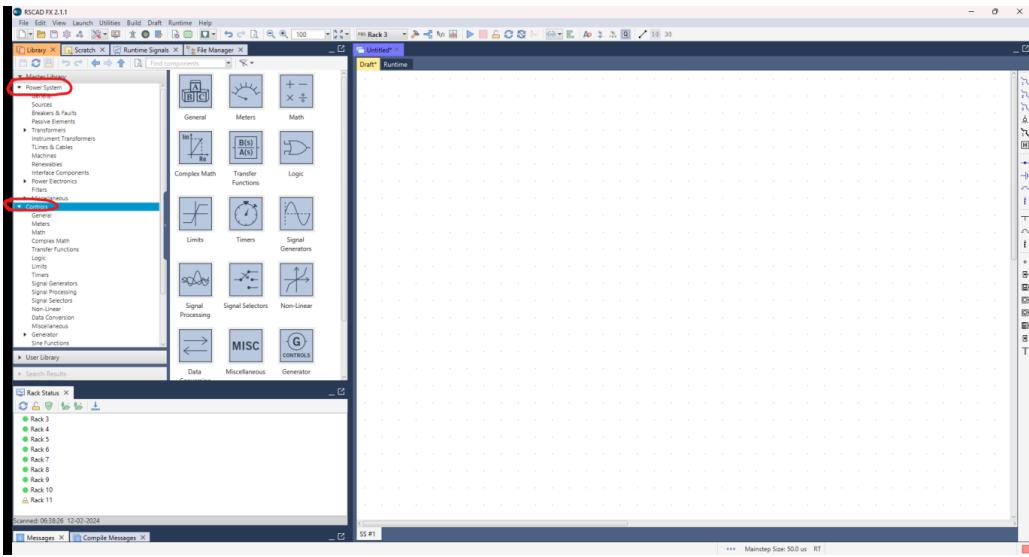


Figure 0.8.9: Accessing the Power System and Control System Libraries.

Once the circuits are made, by clicking on each model block, the respective parameters/simulation settings are entered as shown in Fig. 0.8.10. On completion, the draft file is compiled on one of the RTDS racks. The RTDS racks availability can be checked at the bottom left corner as shown in Fig. 0.8.11 and then one of the available Rack can be selected and then compiled .

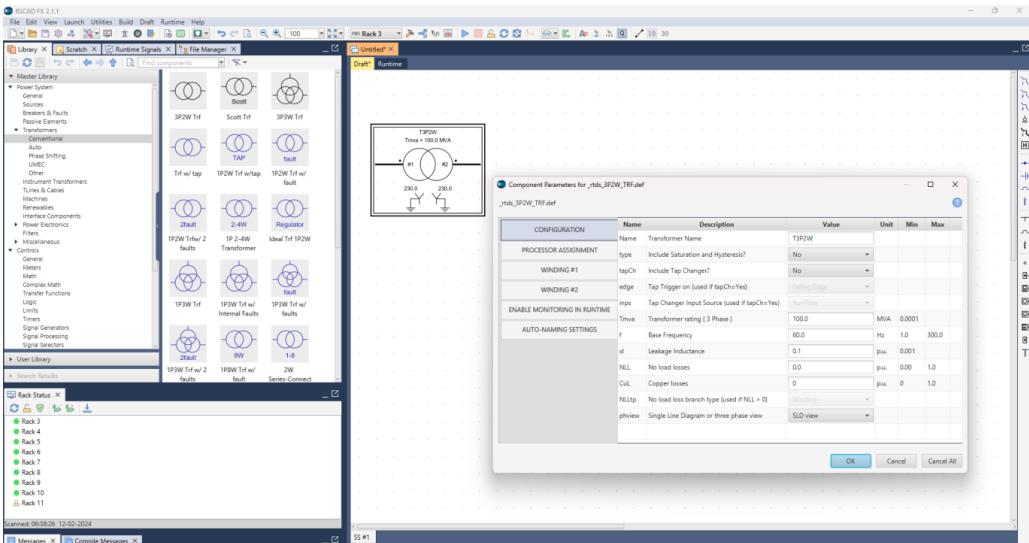


Figure 0.8.10: Change of block parameters.

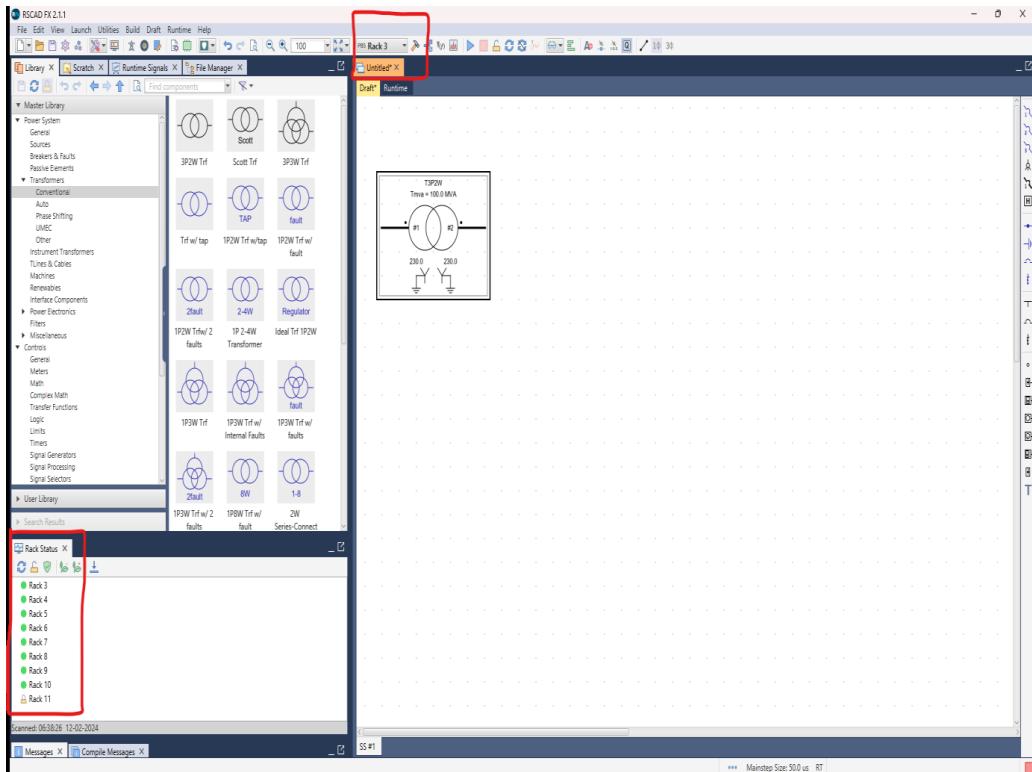


Figure 0.8.11: Check rack availability.

0.8.2.4 RSCAD RunTime

Used to control the simulation case(s) being performed on the RTDS hardware. Simulation control, including start/stop commands, sequence initiation, set point adjustment, fault application, breaker operation, etc. are performed through the RunTime Operator's Console. Additionally, online metering and data acquisition/disturbance recording functions are available in RunTime. The Draft module and the circuit construction modes can be seen in Fig. 0.8.12.

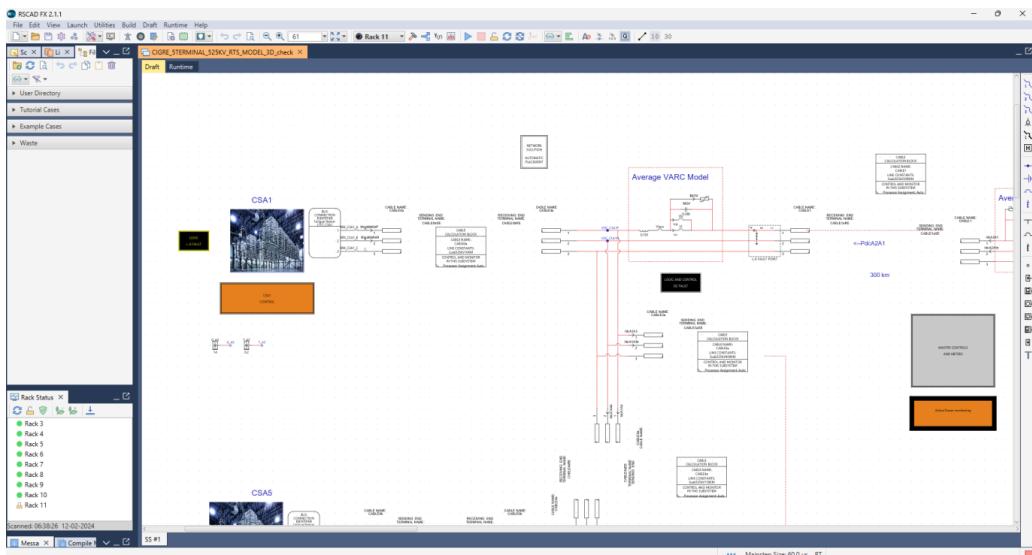


Figure 0.8.12: RSCAD RunTime module.

Creating new runtime module is presented in Fig. 0.8.13.

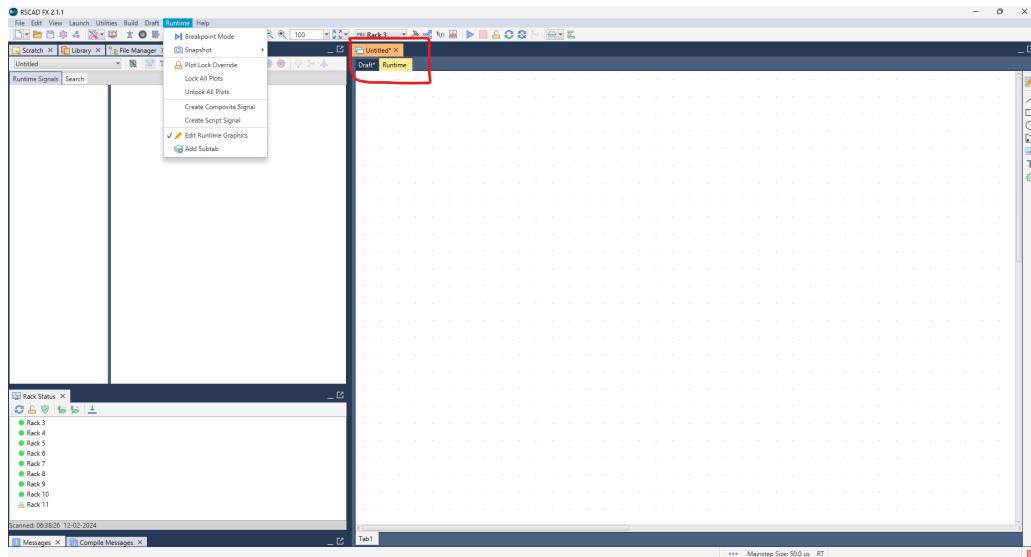


Figure 0.8.13: RSCAD RunTime create.

On the left side panel of the screen, many other utility tabs can be enabled in the view section as shown in Fig. 0.8.14. One of the important tab is runtime scripting, which will allow running script files.

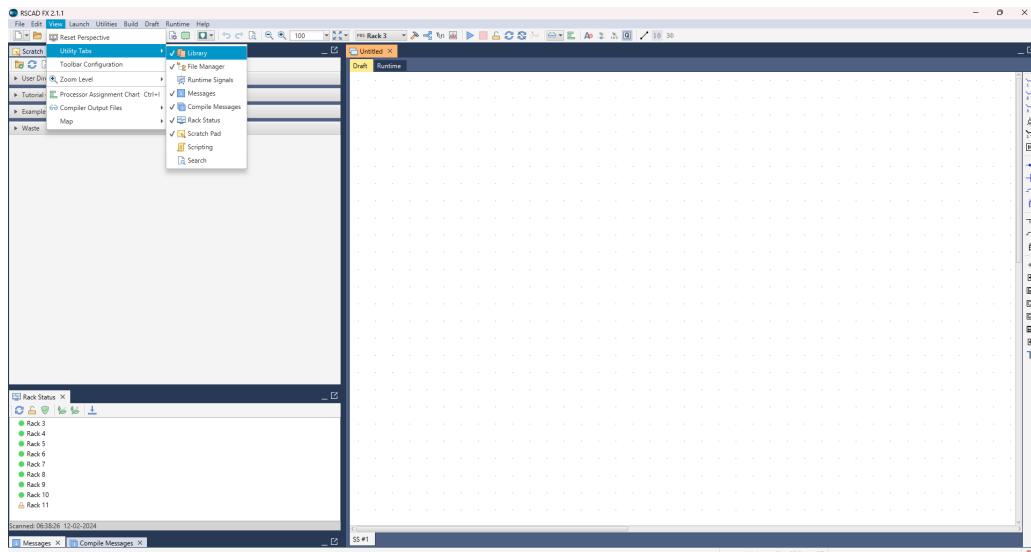


Figure 0.8.14: RSCAD scripts.

0.8.3 RSCAD laboratory preparation

To begin with it's important to understand what RTDS and RSCAD is. Please refer to section C.2 of this document to get a general idea of what RTDS is and how does it integrate with RSCAD along with various modules in the RSCAD software. Once you have a clear overview of the software, you can dive right in.

0.8.3.1 Navigating through RSCAD

Once you understand what the software consists of and its use, you can start with learning more about it.

Navigating through the software is pretty easy:

- At first connect to OpenVPN using your granted credentials.
- Double-click the RSCAD icon on your desktop. The below window will open as shown in Fig. 0.8.4.
- On the top you have a panel with several modules. For the hands-on exercise this year only the ‘Draft’ and ‘Runtime’ modules will be used as shown in Fig 0.8.15.

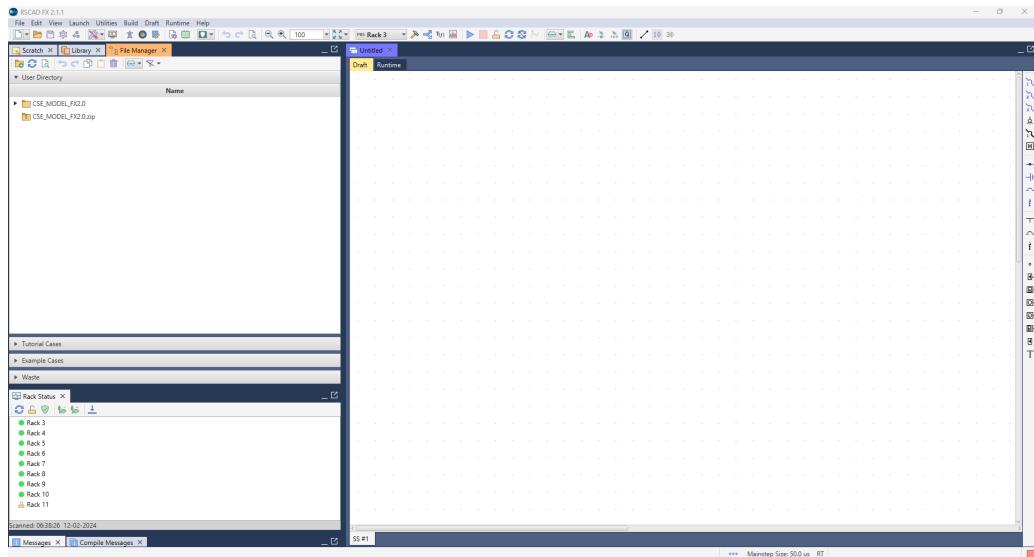


Figure 0.8.15: RSCAD navigate.

- The following steps need to be followed to run the files:

Step 1: Download the files from the [GitHub](#) directory or Brightspace.

Step 2: Extract the zip “**HVDC-RTDS-Models.zip**” in a temporary folder.

Step 3: From the extracted folder, copy the **CSE_MODEL_FX2.0** folder, and paste it to your RSCAD user directory (example: **C:\RSCAD\RTDS_USER_FX\fileman**).

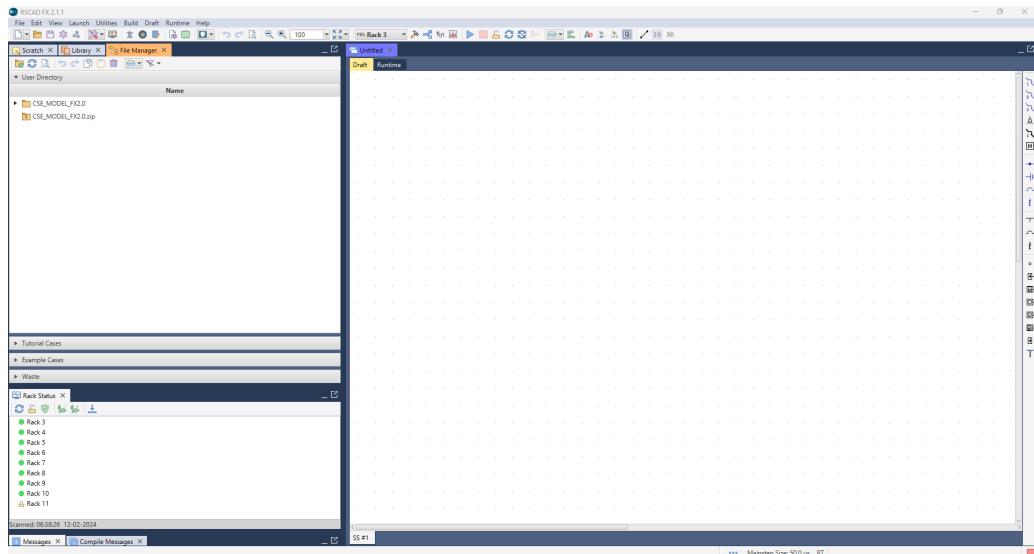


Figure 0.8.16: RSCAD CSE directory [20].

Step 4: Now open the RSCAD FX2.0, and load the desired models from the **CSE_MODEL_FX2.0** folder from your directory. For this explanation, I am considering the **CIGRE_5TERMINAL_525KV_RTS_MODEL_3D_check.rtfx** test case.

Step 5: Upon loading the above file, you will see the following Draft tab as shown in Fig. 0.8.18.

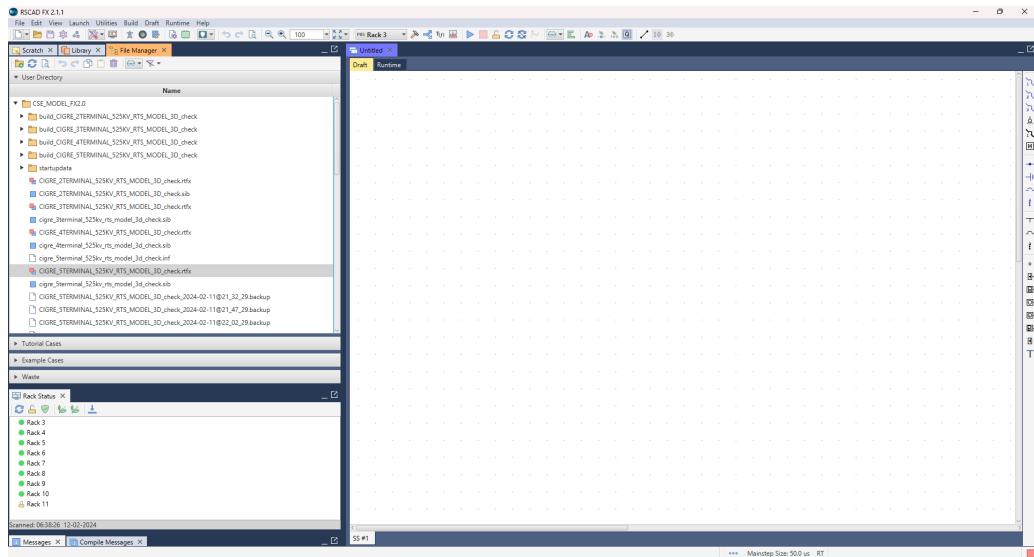


Figure 0.8.17: RSCAD working file.

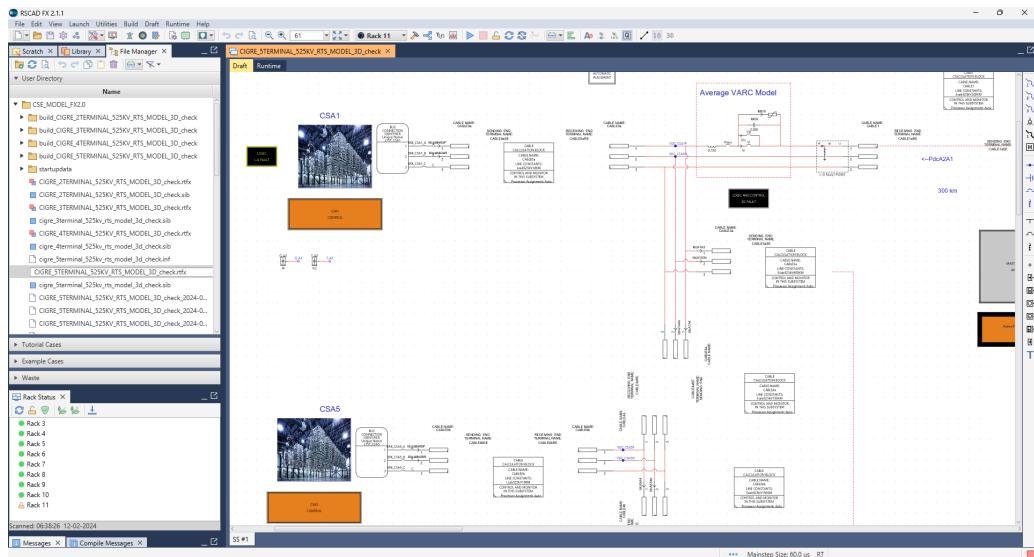


Figure 0.8.18: RSCAD Working file draft module.

Take a good look at the draft file and try to understand the model with its connections.

Step 6: Compile the file based on the availabilities of rack as shown in Fig. 0.8.11, e.g. rack 10 with suitable cores. The red circle indicates that the rack is available. A lock symbol indicates that the rack is locked up and restricted by a user, which can be unlocked from the RTDS hardware at the university. Hopefully, your allotted rack won't be locked up.

After successful compiling the messages will appear in the messages tab in the bottom left section of the software as shown in Fig. 0.8.19 below. The message will state: 'The RSCADFX compile completed successfully'.

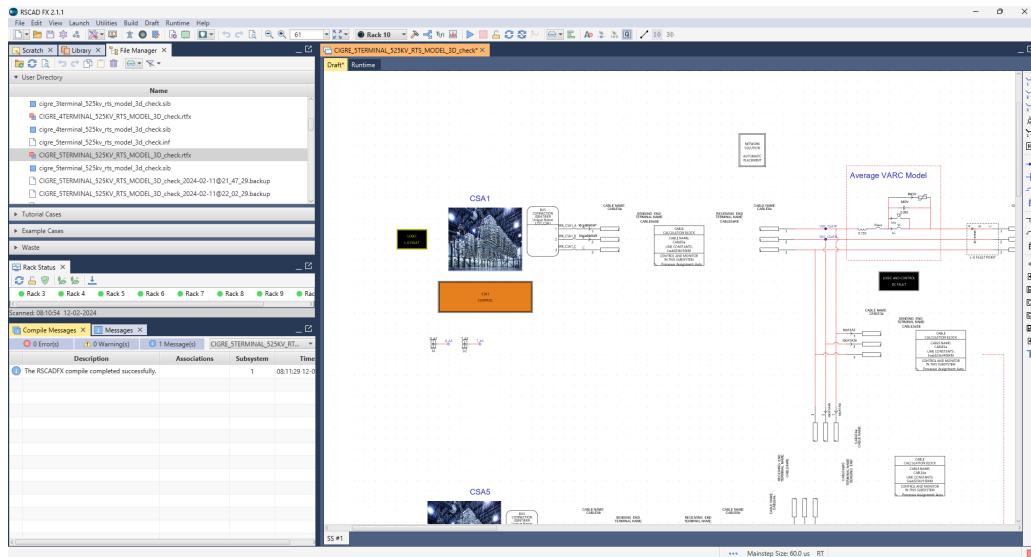


Figure 0.8.19: RSCAD messages and warnings in the bottom left part of the screen.

Step 7: Now go to the Runtime tab, and you will see the following image, as shown in Fig. 0.8.20.

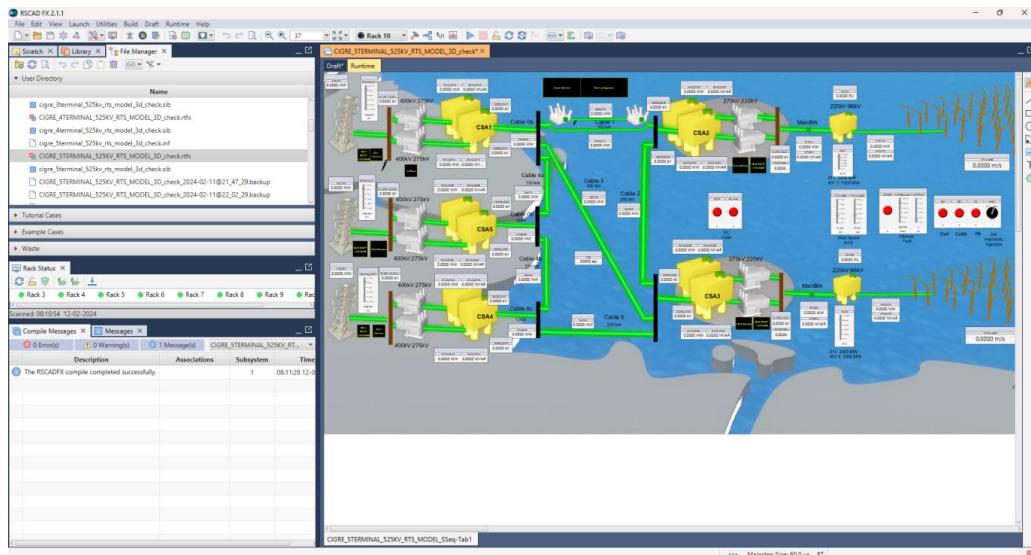


Figure 0.8.20: RSCAD working file runtime module.

Step 8: Now verify whether the scripting is enabled or not using view, check utility tabs as shown in Fig. 0.8.21.

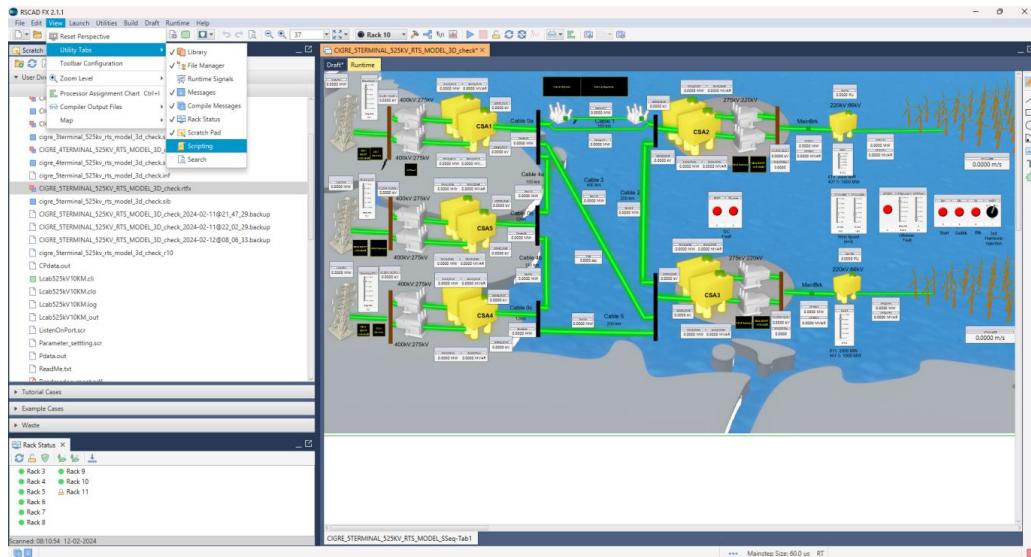


Figure 0.8.21: RSCAD working file: enabling scripting function.

Like Library, File Manager, and other tabs if there is a tick mark on the left side of the scripting it means it is enabled if not then click on the scripting to enable it. A new runtime scripting tab opens up on the left side of the software main page.

Step 9: Now you can create a new script, as visible in Fig. 0.8.22.

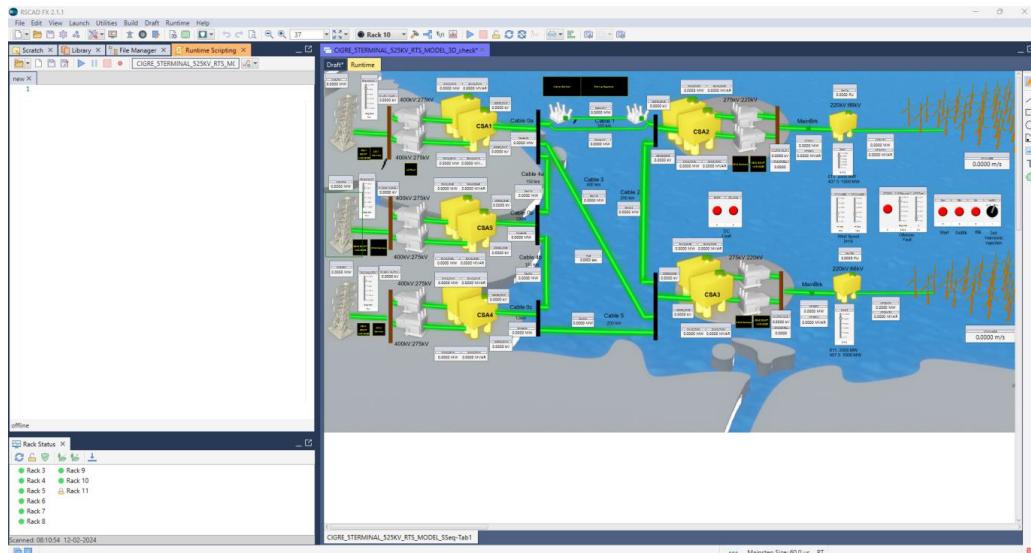


Figure 0.8.22: RSCAD create a script.

Similarly, you can open an already-written script. For this lecture, we will open and run the script for parameter setting, as seen in Fig. 0.8.23. This will configure the draft variables in the runtime.

Run it using the button in the runtime scripting tab.

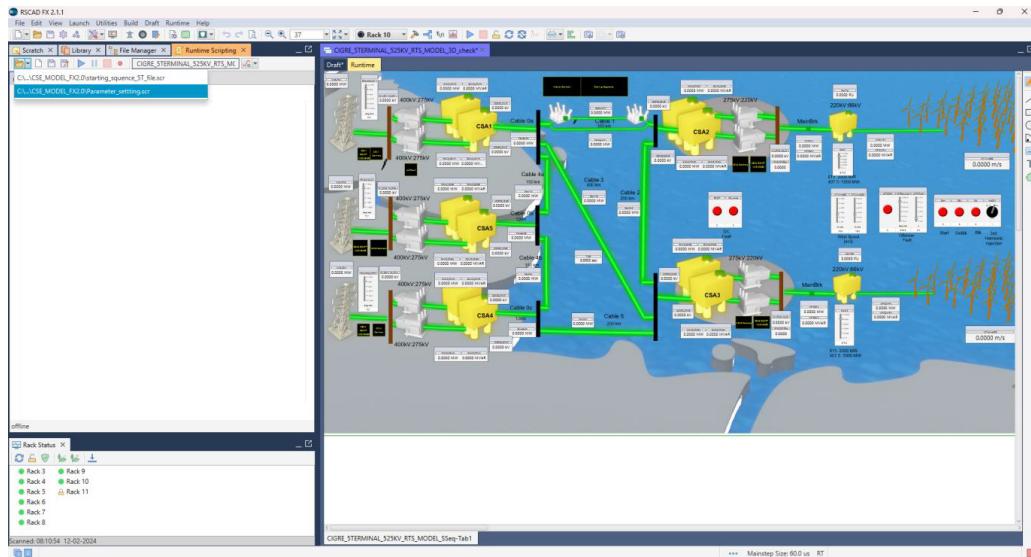


Figure 0.8.23: RSCAD open a script.

Step 9: Now open and run the script `starting_sequence_4T_file.scr`. This will start the simulation with a starting sequence as mentioned in the paper [20] and you can see the numbers running in the runtime module. Once the script is completed now as shown in Fig. 0.8.24, you can begin your study.

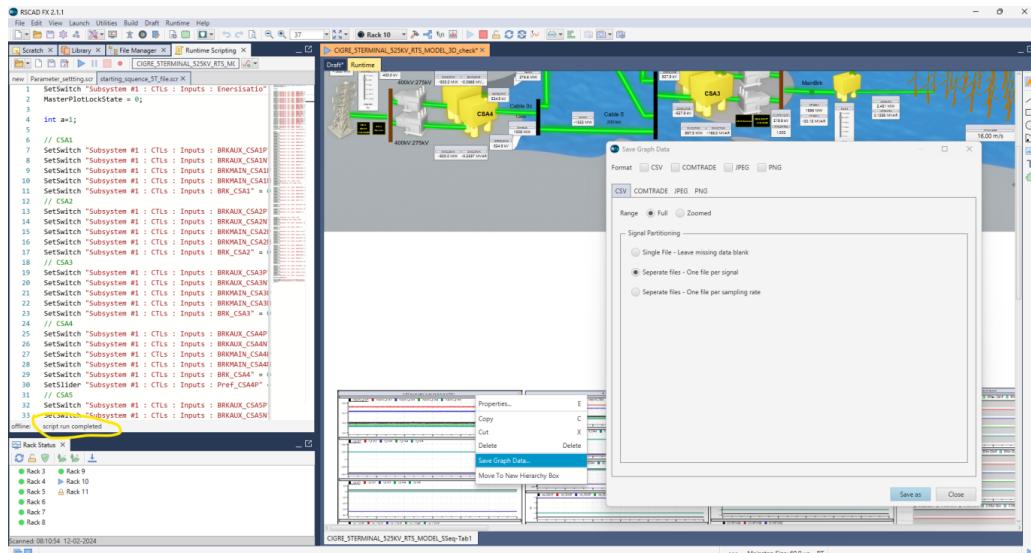


Figure 0.8.24: RSCAD completed script.

Graphs can be seen by scrolling below the runtime module graphics, and they can be easily saved by right-clicking on the graphs. A window pops up with different downloading features as shown in the Fig. 0.8.24

- Once the model starts running, click on the refresh plots button to update the plots. If any plots are not visible, make sure they are unlocked by clicking on the lock icon on the top right of the plot(s).
- Once you start the simulation by pressing the run button, the ‘Stop’ (red circle) button beside it will start glowing. Click on it anytime to stop the simulation. Click on ‘run’ to start again.
- Saving the plots is easy. Right-click on the top of a plot. Click on ‘Save’. Fill in the required plot name. Click on ‘Ok’. Note that all the plots might be saved in ‘fileman’.
- After saving the plot, if you think it is not clear enough, try adjusting the Compression Quality in the ‘Save Options’.

0.9 Hands on Session

Below is the description of the tasks for the HVDC model to be performed as a part of this session.

0.9.1 Overview of the Test System

A 4-bus multi-terminal grid (± 525 kV) is considered as the MMC-based HVDC configuration as shown in Fig. 1. MMC 1 and MMC 3 are connected to the power grid for the evacuation of generated power. MMC 2 is connected to the offshore wind park generating renewable power. As MMC 2 has to create its grid to extract the wind power, it operates in grid-forming mode (GFM) as shown in the Dispatch level in Fig. 1. This means that the system frequency is given externally as shown as θ_{vso} in the control level. MMC 1 is used to control the DC link voltage of the system whereas MMC 2 is controlled in the power reference mode as shown in Dispatch level. This intuitively means that MMC 2 evacuates a fixed amount of power whereas MMC 1 evacuates the intermittent difference of power $P_{MMC3} - P_{MMC2}$ to maintain the DC voltage of the system.

0.9.1.1 Elaboration of the test system in RTDS

Considering the *draft* file depicted in Fig. 0.9.1, the **A** region indicates the converter station and connection between the main and small timestep. It also consists of control and protection., meter, and draft variables. In the mentioned network, we have five such stations.

The **B** region indicates the disconnector, which disconnects the converter station from the land and sea land cables. In the above network, we have five such disconnectors. The **C** region is a DMR (Dedicated Metallica Return) land cable with a length of 20 km. This cable connected the onshore converter to the sea cable. In the above network, we have three such land cables. The **D** region is submarine cable. Considering the mentioned network, we have six cables. The length of these cables can be found in the paper.

E region indicates the VARC DC CB. This region also consists of fault logic and the operating time of VARC. In all the models, the VARC is connected to a positive pole and placed at either end of the cable. Region **F** consists of Wind turbines and scaling transformers to mimic the wind power pack/wind farm. We have two such wind power packs. Region **G** has general meters and master controls.

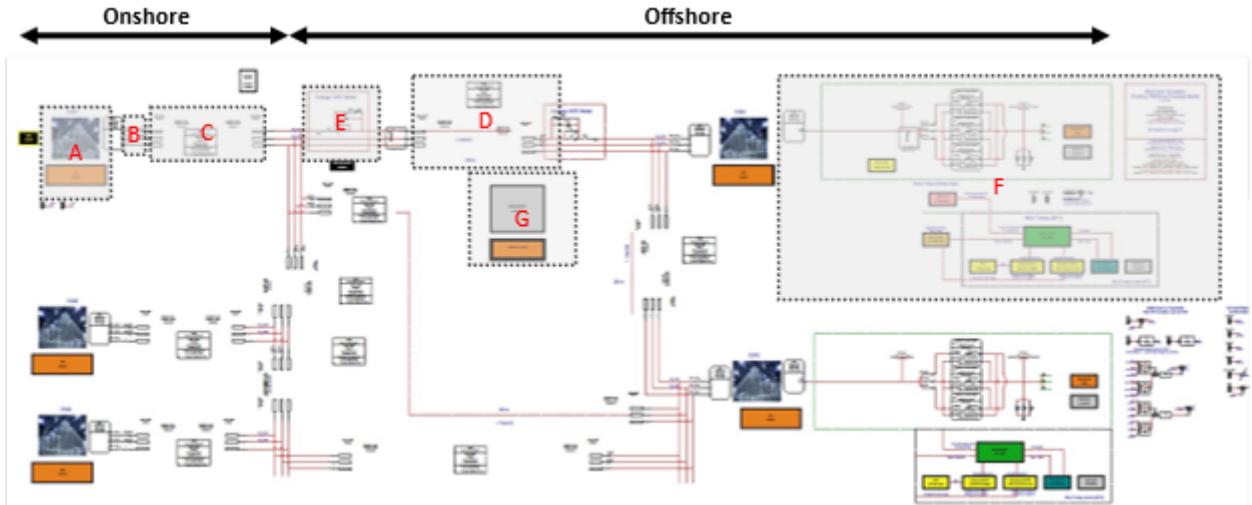


Figure 0.9.1: HVDC electrical grid in *draft* file.

In the *runtime* depicted in Fig. 0.9.2, we have six regions, region **A** indicates the control functions and setpoints, and Draft variables. These two blocks in this region remain the same for all the converters. Furthermore, region **B** indicates AC fault duration, fault button, and re-set signal near the CSA1 converter. Region **C** has two hierarchy boxes, namely Master control and Starting sequence. As the name indicates, the Master control has all necessary global setpoints and control functions. Similarly, the Starting sequence has control switches that give the breaker close command and de-block signal to the converter station.

Region **D** consists of wind turbine controls, draft variables, and setpoints. Furthermore, region **F** consists of a wind speed control slider, offshore fault and fault duration, and Energisation buttons of the wind turbine. Region **G** consists of DC fault and reclose command for DC breakers.

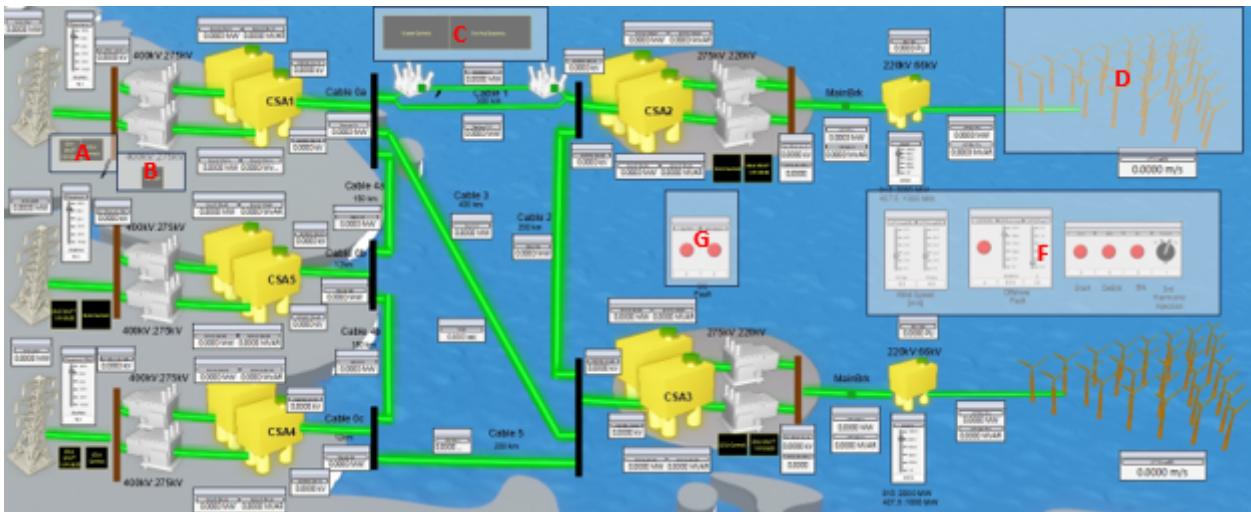


Figure 0.9.2: HVDC electrical grid in *runtime* file.

0.9.1.2 Proportional-Integral (PI) controllers

The subtraction of IDREF4 and id4 gives the error iderr4. The PI controller is a combination of proportional and integral functions designed to make the error converge to zero. A proportional gain is used to minimize the error while the integral gain is responsible for making the error converge to zero using the historic cumulative value of the errors. Rst4 is the input to reset the integral function in the PI controller to avoid saturation.

Please note that for this course we will use only PI implementation. For more information about other control principles, refer to publications [21].

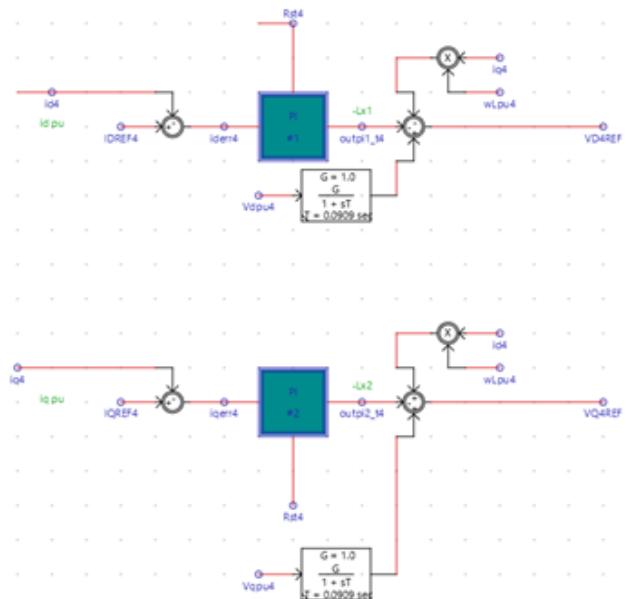


Figure 0.9.3: PI controls in RSCAD.

Perform the tasks using the model: **CIGRE_4TERMINAL_525KV_RTS_MODEL_3D_check**.

1. Inside **CSA4** controls, test the following active power references for PI:

- (a) Pref4 = 0 MW;
- (b) Pref4 = -250 MW;
- (c) Pref4 = -500 MW;
- (d) Pref4 = -1000 MW.

What is the active power through CSA 1 for each case? Is there a dependence on the different values of active power references (as given in (a)-(d)) and the total observed power of CSA 1.

2. Do you see the controller making the system unstable for any instant?

3. Inside the **Master Controls** block, change the VDCref (from 1pu i.e., $\pm 525\text{kV}$) to the following per unit values:

- (a) VDCref = 0.75pu;
- (b) VDCref = 1.25pu;
- (c) VDCref = 0.25pu;
- (d) VDCref = 2pu.

Do you see the system voltage changing for each of the case? Is there a case where the system voltage did not follow the reference?

4. For CSA 3, change the generated wind power to the following (from 2000MW):

- (a) PMMC_CSA3 = 1000MW;
- (b) PMMC_CSA3 = 500MW;

What is the effect on the change in wind power on the onshore converters power evacuation (i.e., power for CSA 1 and CSA 2)? Hint: Change the **Scale12** factor in runtime around CSA 3.

5. Simulate a DC fault in runtime for each controller by pressing the switch, **DC_FLT**.

6. Simulate an AC fault in runtime for each controller by pressing the switch for AC fault **AC_FLT**.

Bibliography

- [1] J. Rebled Lluch, “Modelling, control and simulation of lcc-hvdc systems for stability studies,” Master’s thesis, Universitat Politècnica de Catalunya, 2017.
- [2] Y. Xue and X. Zhang, “Reactive power and ac voltage control of lcc hvdc system with controllable capacitors,” *IEEE Transactions on Power Systems*, vol. 32, no. 1, pp. 753–764, 2017.
- [3] M. Ramamoorthy, *An Introduction to thyristors and their applications*. Macmillan International Higher Education, 1978.
- [4] M. Daryabak, “Modeling line-commutated converter hvdc transmission systems using dynamic phasors,” Ph.D. dissertation, University of Manitoba, 2014.
- [5] M. Daryabak, S. Filizadeh, J. Jatskevich, A. Davoudi, M. Saeedifard, V. Sood, J. Martinez, D. Aliprantis, J. Cano, and A. Mehrizi-Sani, “Modeling of lcc-hvdc systems using dynamic phasors,” *IEEE Transactions on Power Delivery*, vol. 29, no. 4, pp. 1989–1998, 2014.
- [6] W. Hammer, “Dynamic modeling of line and capacitor commutated converters for hvdc power transmission,” Ph.D. dissertation, ETH Zurich, 2003.
- [7] J. Pyrhonen, V. Hrabovcova, and R. S. Semken, *Electrical machine drives control: An introduction*. John Wiley & Sons, 2016.
- [8] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, “Vsc-based hvdc power transmission systems: An overview,” *IEEE Transactions on power electronics*, vol. 24, no. 3, pp. 592–602, 2009.
- [9] O. Anaya-Lara, D. Campos-Gaona, E. Moreno-Goytia, and G. Adam, *Offshore wind energy generation: control, protection, and integration to electrical systems*. John Wiley & Sons, 2014.
- [10] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, “Operation, control, and applications of the modular multilevel converter: A review,” *IEEE transactions on power electronics*, vol. 30, no. 1, pp. 37–53, 2014.
- [11] S. Du, A. Dekka, B. Wu, and N. Zargari, *Modular multilevel converters: analysis, control, and applications*. John Wiley & Sons, 2017.
- [12] G. Bergna-Diaz, J. Freytes, X. Guillaud, S. D’Arco, and J. A. Suul, “Generalized voltage-based state-space modeling of modular multilevel converters with constant equilibrium in steady state,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 2, pp. 707–725, 2018.
- [13] G. Bergna-Diaz, D. Zonetti, S. Sanchez, R. Ortega, and E. Tedeschi, “Pi passivity-based control and performance analysis of mmc multi-terminal hvdc systems,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2018.
- [14] Ö. C. Sakinci and J. Beerten, “Generalized dynamic phasor modeling of the mmc for small-signal stability analysis,” *IEEE Transactions on Power Delivery*, vol. 34, no. 3, pp. 991–1000, 2019.
- [15] J. Freytes, “Analyse de stabilité en petit signaux des convertisseurs modulaires multiniveaux et application à l’étude d’interopérabilité des mmc dans les réseaux hvdc,” Ph.D. dissertation, Ecole centrale de Lille, 2017.
- [16] T. K. Vrana, Y. Yang, D. Jovicic, S. Dennetière, J. Jardini, and H. Saad, “The cigre b4 dc grid test system,” *Electra*, vol. 270, no. 1, pp. 10–19, 2013.

- [17] C. Franck, R. Smeets, A. Adamczyk, H. Bahirat *et al.*, “Technical requirements and specifications of state-of-the-art hvdc switching equipment,” *Cigré Technical Brochure*, vol. 683, 2017.
- [18] J. Cao, P. Tuennenhoff, C. Gao, R. Smeets, Y. Yang, J. Liljeqvist, W. Li, T. Ishiguro, T. An, S. Azad *et al.*, “Design, test and application of hvdc circuit breakers,” 2022.
- [19] J. L. Rueda Torres and R. Bhandia, “Overview of RTDS hardware and RSCAD,” *RTDS Training course*, 2018.
- [20] A. Shetgaonkar, T. Karmokar, M. Popov, and A. Lekić, “Enhanced real-time multi-terminal hvdc power system benchmark models with performance evaluation strategies,” *CIGRE Science & Engineering*, vol. 32, pp. 1–29, 2024.
- [21] L. Liu, A. Shetgaonkar, and A. Lekić, “Interoperability of classical and advanced controllers in mmc based mtdc power system,” *International Journal of Electrical Power & Energy Systems*, vol. 148, p. 108980, 2023.

Appendix

A Transformations

The three-phase system's variables can be represented in the stationary abc-frame, as depicted in Fig. A.1. Each vector $\mathbf{f}_{abc}(t)$ is presented as sum of unit vector components f_a , f_b and f_c . It should be noted that the angle of the vector \mathbf{f}_{abc} is time dependent and is given by

$$\theta(t) = \theta_0 + \int_0^t \tau d\tau.$$

The vector \mathbf{f}_{abc} is obtained by projection to a, b and c axis, as:

$$\mathbf{f}_{abc}(t) = \frac{2}{3} \left(\exp(j0)f_a + \exp\left(j\frac{2\pi}{3}\right)f_b + \exp\left(j\frac{4\pi}{3}\right)f_c \right). \quad (57)$$

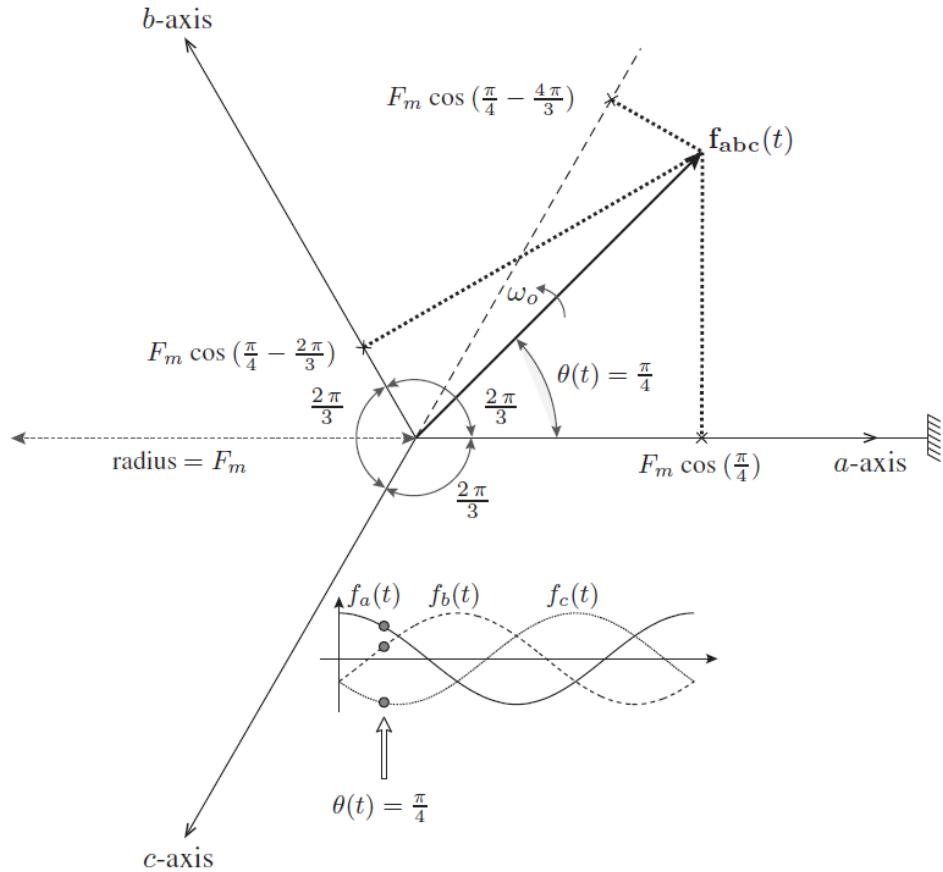


Figure A.1: Static abc-frame, picture taken from [11].

Since the phasor in abc-frame is complex in nature and time-varying, the often used frame is $\alpha\beta$ -frame depicted in Fig. A.2. Vector in this frame is represented by two components, α and β , obtained by projecting

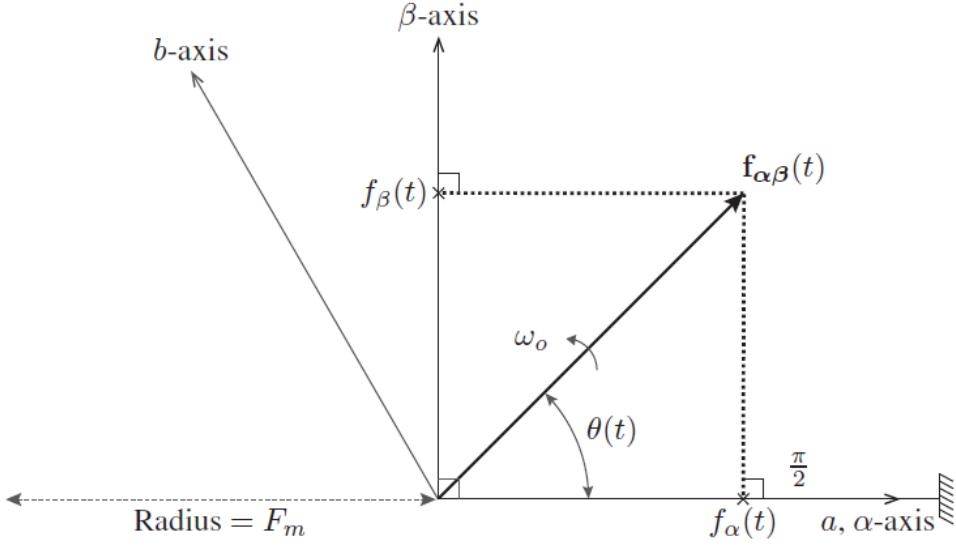


Figure A.2: Static $\alpha\beta$ -frame, picture taken from [11].

vector on the two orthogonal axes. Vector's value is then:

$$\mathbf{f}_{\alpha\beta}(t) = f_{\alpha}(t) + j f_{\beta}(t). \quad (58)$$

The transformation from abc-frame to $\alpha\beta$ -frame is obtained by applying Clarke's transformation:

$$\begin{bmatrix} f_{\alpha}(t) \\ f_{\beta}(t) \end{bmatrix} = \underbrace{\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}}_{\mathbf{T}_{abc \rightarrow \alpha\beta}} \times \begin{bmatrix} f_a(t) \\ f_b(t) \\ f_c(t) \end{bmatrix}, \quad (59)$$

while the inverse Clarke's transformation is:

$$\begin{bmatrix} f_a(t) \\ f_b(t) \\ f_c(t) \end{bmatrix} = \underbrace{\begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}}_{\mathbf{T}_{\alpha\beta \rightarrow abc}} \times \begin{bmatrix} f_{\alpha}(t) \\ f_{\beta}(t) \end{bmatrix}. \quad (60)$$

Further more, the power system is often modeled in the rotating dq-frame. This frame is two axes frame rotating with the synchronous frequency, depicted in Fig. A.3. The space phasor is given by:

$$\mathbf{f}_{dq}(t) = f_d(t) + j f_q(t),$$

where the space phasor has the static position θ towards the axes.

The complete AC power system is modeled in dqz -frame to fit the developed power converter model. For that purpose, it was necessary to apply abc to dqz transformation.

In order to transform three-phase voltages and currents from the stationary abc -frame to the rotating dqz -frame, Park's transformation defined as

$$\begin{bmatrix} f_d(t) \\ f_q(t) \end{bmatrix} = \underbrace{\frac{2}{3} \begin{bmatrix} \cos(\omega_0 t) & \cos(\omega_0 t - \frac{2\pi}{3}) & \cos(\omega_0 t - \frac{4\pi}{3}) \\ -\sin(\omega_0 t) & -\sin(\omega_0 t - \frac{2\pi}{3}) & -\sin(\omega_0 t - \frac{4\pi}{3}) \end{bmatrix}}_{\mathbf{T}_{abc \rightarrow dq}} \times \begin{bmatrix} f_a(t) \\ f_b(t) \\ f_c(t) \end{bmatrix}, \quad (61)$$

is employed. The inverse Park's transformation is given as

$$\begin{bmatrix} f_a(t) \\ f_b(t) \\ f_c(t) \end{bmatrix} = \underbrace{\begin{bmatrix} \cos(\omega t) & -\sin(\omega t) \\ \cos(\omega_0 t - \frac{2\pi}{3}) & -\sin(\omega_0 t - \frac{2\pi}{3}) \\ \cos(\omega_0 t - \frac{4\pi}{3}) & -\sin(\omega_0 t - \frac{4\pi}{3}) \end{bmatrix}}_{\mathbf{T}_{dq \rightarrow abc}} \times \begin{bmatrix} f_d(t) \\ f_q(t) \end{bmatrix}. \quad (62)$$

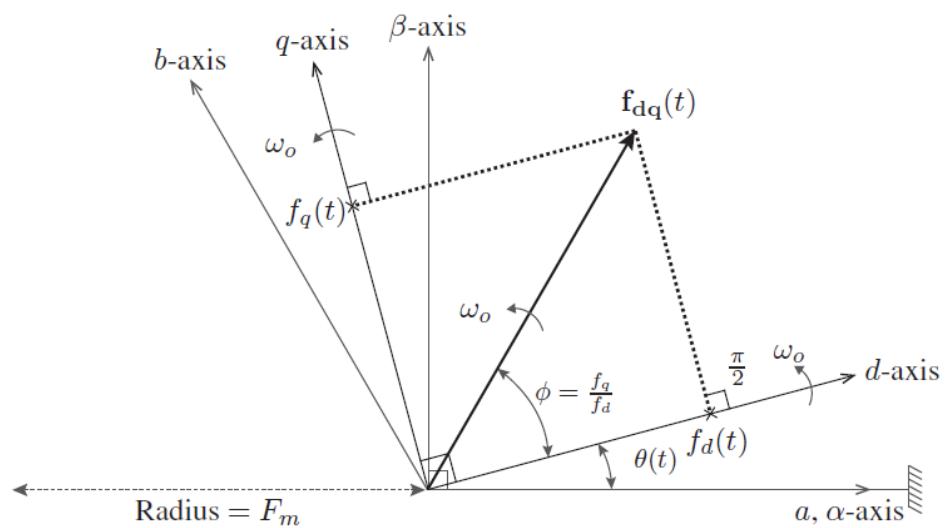


Figure A.3: Rotating dq-frame, picture taken from [11].