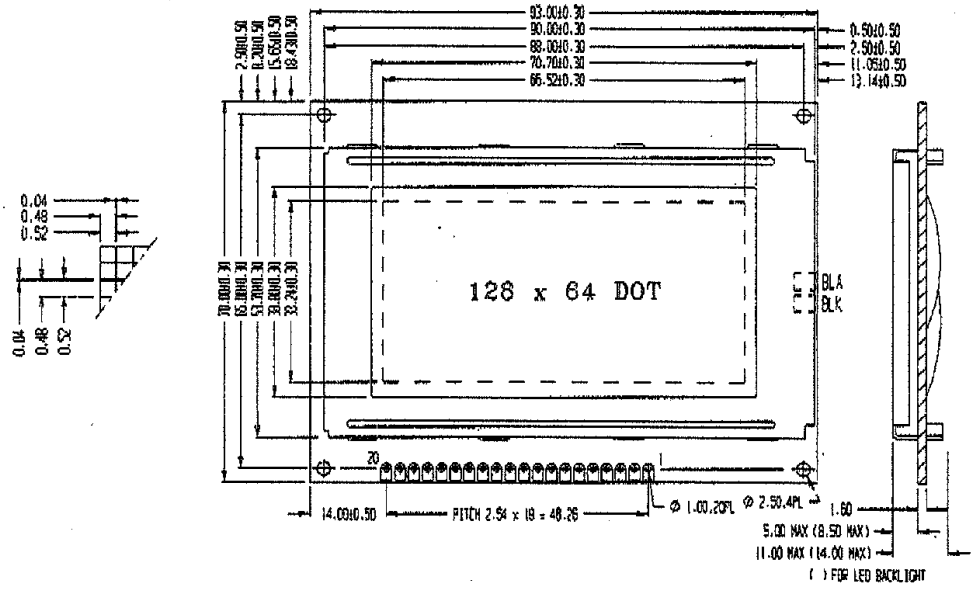
1. PHYSICAL DATA

1.1 **LCD TYPE :** STN
1.2 **VIEWING DIRECTION :** 6 o'clock or 12 o'clock
1.3 **MODULE SIZE :** 93 mm(3.66 ") L x 70 mm(2.76") W x 14.0 mm(0.55") H (Max.)
1.4 **VIEWING AREA :** 70.7 mm(2.78") W x 38.8 mm(1.53") H (Min.)
1.5 **NUMBER OF DOTS :** 128 x 64 Dots
1.6 **DOT SIZE :** 0.48 mm(0.019") W x 0.48 mm(0.019") H
1.7 **DOT PITCH :** 0.52 mm(0.02") W x 0.52 mm(0.02") H
1.8 **LCD DUTY :** 1/64, **LCD BIAS :** 1/9

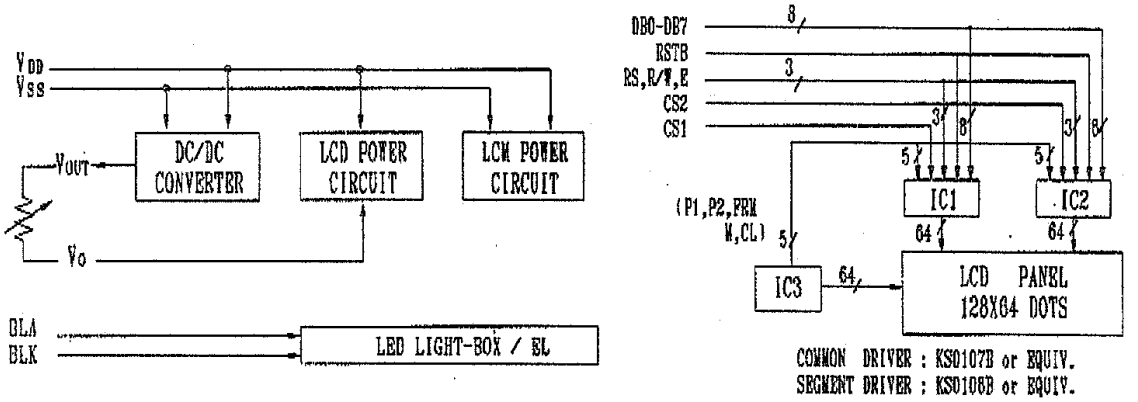
CERT. No. 946535

2. EXTERNAL DIMENSIONS



3. BLOCK DIAGRAM

20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
BLK	BLA	VOUT	RSTB	CS2	CS1	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	E	R/W	RS	Vo	VDD	Vss



4. ABSOLUTE MAXIMUM RATINGS FOR LED BACK-LIGHT

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
LED Forward Consumption Current	I_f	$T_a = 25°C$, $V_f = 4.2V$	---	560	840	mA
LED Allowable Dissipation	P_d	$V_r = 5.0V$ max	---	2352	3528	mW

5. ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT
Supply Voltage for Logic		V_{DD}	0	6.7	V
Supply Voltage for LCD *		V_{DD} -V_O	0	17	V
Input Voltage		V_I	0	V_{DD}	V
Normal Type	Operating temperature	T_{op}	0	+50	°C
	Storage temperature	T_{stg}	-10	+60	°C
Extended Type	Operating temperature	T_{op}	-20	+70	°C
	Storage temperature	T_{stg}	-30	+80	°C

* The second voltage source (variable voltage)should be added if the external resistor is not used.

6. ELECTRICAL CHARACTERISTICS

6.1 DC characteristics (V_{DD} = +5V±5%, V_{SS} = 0V, T_a = 25°C)

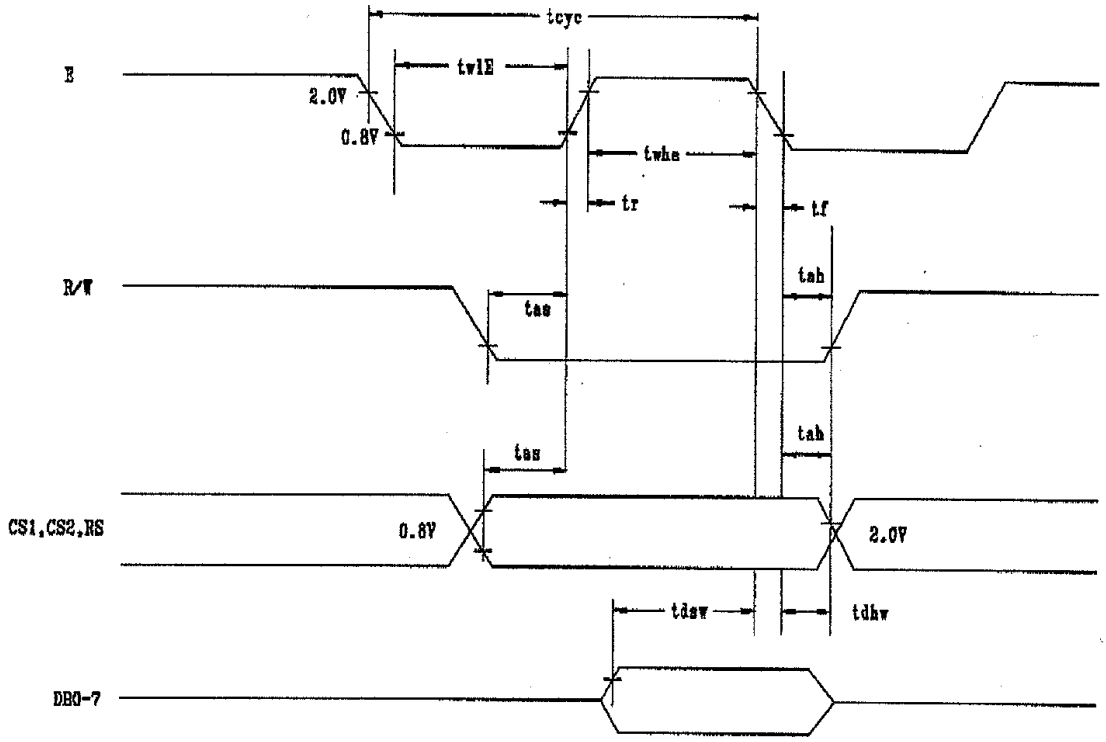
PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	---	4.75	5.0	5.25	V
Supply Current	I_{DD}	---	---	5.1	9.8	mA
Operating Voltage for LCD (Recommended)	V_{DD} -V_O	0°C	---	9	---	V
		25°C	---	8	---	V
		50°C	---	7.2	---	V
Input Voltage ' H ' Level	V_{IH}	---	0.8 V_{DD}	---	V_{DD}	V
Input Voltage ' L ' Level	V_{IL}	---	0	---	0.2 V_{DD}	V

6.2 AC characteristics (V_{DD} = +5V±5%, V_{SS} = 0V, T_a = 25°C)

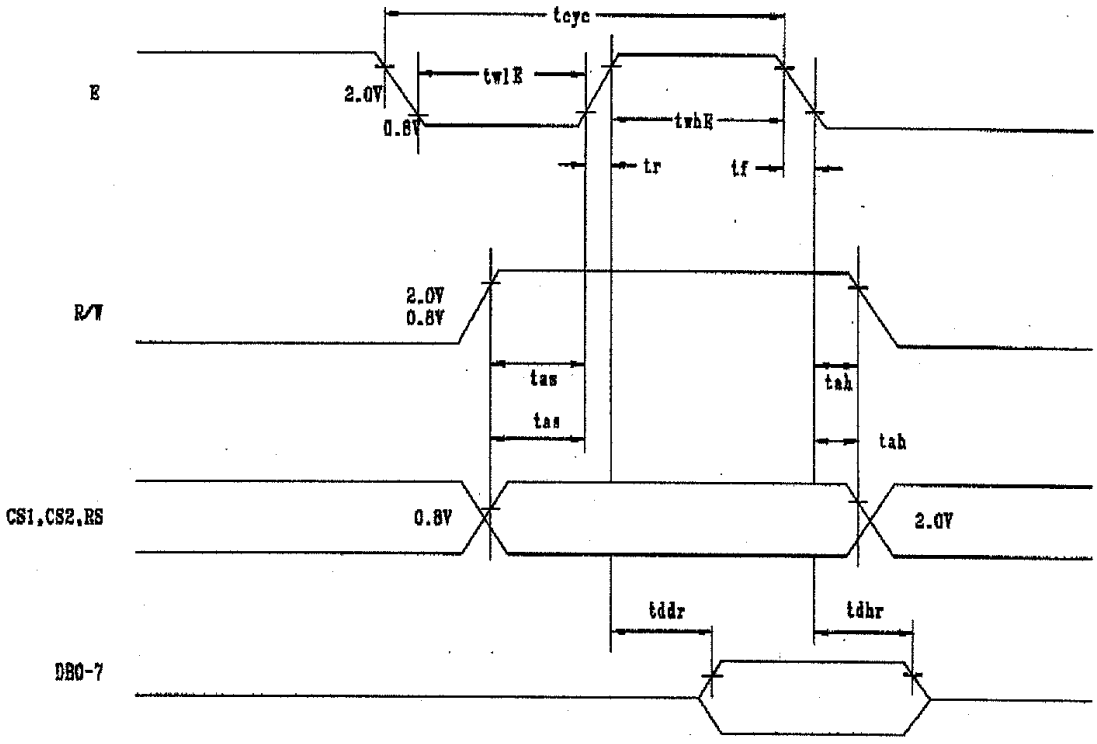
MPU Interface

Characteristic	Symbol	Min.	Typ.	Max.	Unit
E cycle	tcyc	1000	---	---	ns
E high level width	twh_E	450	---	---	ns
E low level width	twl_E	450	---	---	ns
E rise time	t_r	---	---	25	ns
E fall time	t_f	---	---	25	ns
Address set-up time	t_{as}	140	---	---	ns
Address hold time	t_{ah}	10	---	---	ns
Data set-up time	tdsw	200	---	---	ns
Data delay time	tddr	---	---	320	ns
Data hold time(write)	tdhw	10	---	---	ns
Data hold time(read)	tdhr	20	---	---	ns

MPU Write Timing



MPU Read Timing



7. OPERATING PRINCIPLES & METHODS

7.1 I/O Buffer

Input buffer controls the status between the enable and disable of chip. Unless the CS1 or CS2 is in active mode, input or output of data and instruction do not execute. Therefore internal state is not change. But RSTB can operate regardless of CS1 and CS2.

7.2 Input Register

Input register is provided to interface with MPU which is different operating frequency. Input register stores the data temporarily before writing it into display data RAM.

When CS1 or CS2 is in the active mode, R/W and RS select the input register. The data from MPU is written into input register and then write it into display data RAM. Data is latched when falling of the E signal and written automatically into the display data RAM by internal operation.

7.3 Output Register

Output register stores the data temporarily from display data RAM when CS1 or CS2 is in active mode and R/W and RS = H. Stored data in display data RAM is latched in output register. When CS1 or CS2 is in active mode and R/W = H, RS = L, status data (busy check) can be read out.

To read the contents of display data RAM, twice access of read instruction is needed. In first access, data in display data RAM is latched into output register. In second access, MPU can read data which is latched. That is, to read the data in display data RAM, it needs dummy read. But status read does not need dummy read.

RS	R/W	Function
0	0	Instruction
	1	Status read (busy check)
1	0	Data write (from input register to display data RAM)
	1	Data read (from display data RAM to output register)

7.4 Reset

System reset can be initialized by setting RSTB terminal at low level when turning power on, receiving instruction from MPU. When RSTB becomes low, following procedure is occurred.

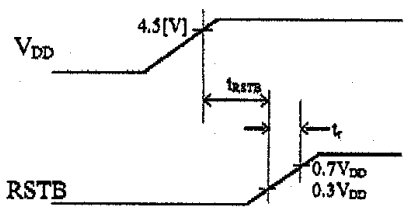
1. Display off
2. Display start line register become set by 0. (Z-address 0)

While RSTB is low level, no instruction except status read can be accepted. Reset status appears at DB4. After DB4 is low, any instruction can be accepted.

The Conditions of power supply at initial power up are shown in table 1.

Table 1. Power Supply Initial Conditions

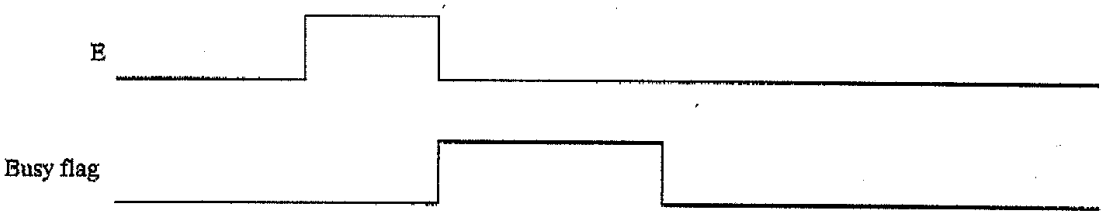
Item	Symbol	Min.	Typ.	Max.	Unit
Reset time	t_{RSTB}	1.0	---	---	us
Rise time	t_r	---	---	200	ns



7.5 Busy Flag

Busy flag indicates that KS0108B is operating or not operating. When busy flag is high, KS0108B is in internal operating. When busy flag is low, KS0108B can accept the data or instruction.

DB7 indicates busy flag of the KS0108B.



7.6 Display On/Off Flip-Flop

The display on/off flip-flop makes on/off of the liquid crystal display. When flip-flop is reset (logical low), selective voltage or non selective voltage appears on segment output terminals. When flip-flop is set (logical high), non selective voltage appears on segment output terminals regardless of display RAM data.

The display on/off flip-flop can changes status by instruction. The display data at all segment disappear while RSTB is low. The status of the flip-flop is output to DB5 by status read instruction.

7.7 X Page Register

X page register designates page of the internal display data RAM. It has not count function. An address is set by instruction.

7.8 Y Address Counter

Y address counter designates address of the internal display data RAM. An address is set by instruction and is increased by 1 automatically by read or write operations of display data.

7.9 Display Data RAM

Display data RAM stores a display data for liquid crystal display. To express on state of dot matrix of liquid crystal display, write data 1. The other way, off state writes 0.

DB<0:7>=0 → Y address 0 → S1
DB<0:7>=63 → Y address 63 → S64

7.10 Display Start Line Register

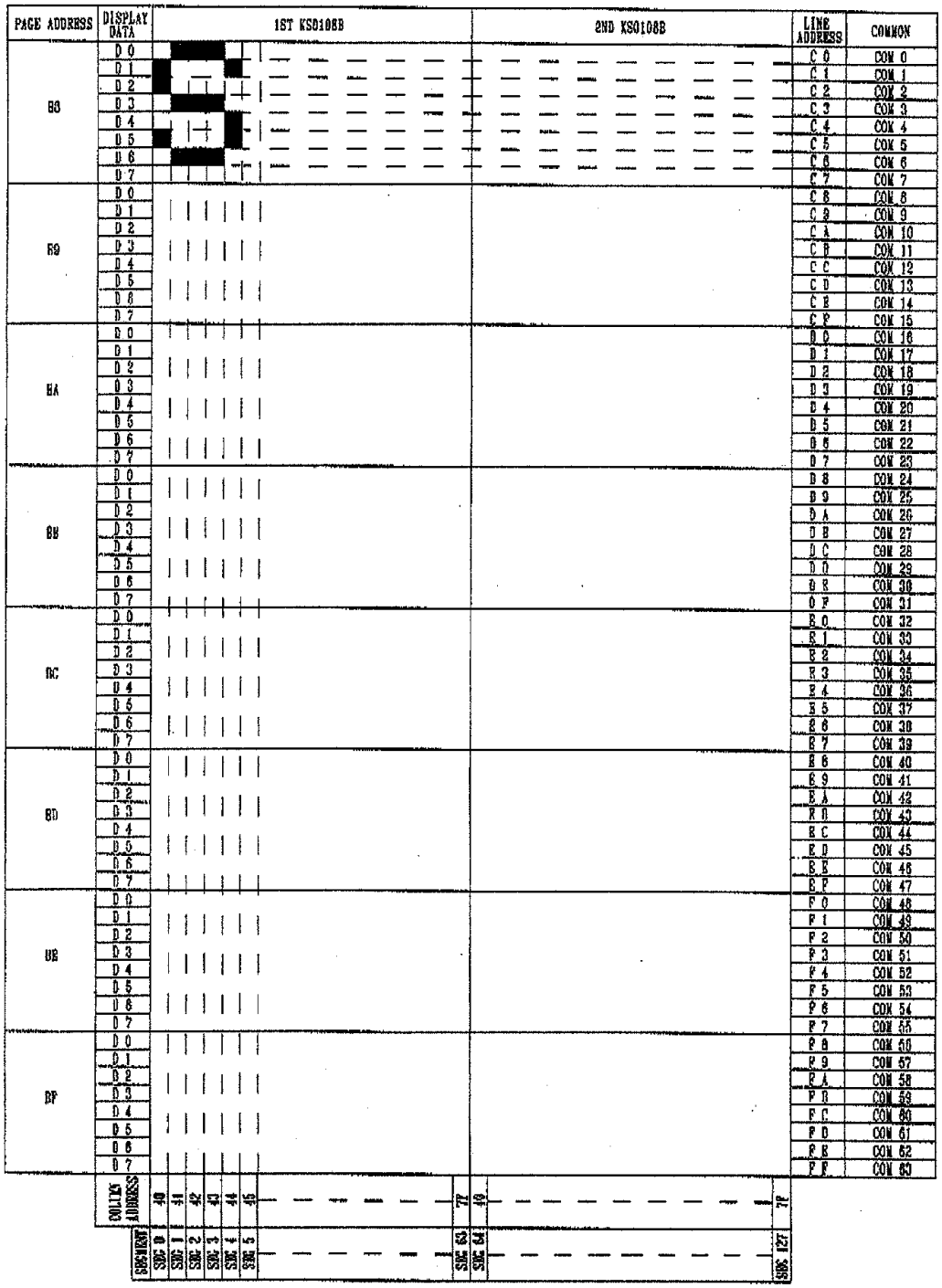
The display start line register indicates address of display data RAM to display top line of liquid crystal display. Bit data (DB<0:5>) of the display start line set instruction is latched in display start line register. It is used for scrolling of the liquid crystal display screen.

8. DISPLAY CONTROL INSTRUCTION

The display control instructions control the internal state of the KS0108B. Instruction is received form MPU to KS0108B for the display control. The following table shows various instructions.

Instruction	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
Display ON/OFF	0	0	0	0	1	1	1	1	1	0/1	Controls the display on or off. Internal status and display RAM data are not affected. 0:OFF, 1:ON
Set Address	0	0	0	1	Y address (0~63)						Sets the Y address in the Y address counter.
Set Page (X address)	0	0	1	0	1	1	1	Page (0~7)			Sets the X address at the X address register.
Display Start Line	0	0	1	1	Display start line (0~63)						Indicates the display data RAM displayed at the top of the screen.
Status Read	0	1	BUSY	0	ON/OFF	RESET	0	0	0	0	Read status. BUSY 0 : Ready 1 : In operation ON/OFF 0 : Display ON 1 : Display OFF RESET 0 : Normal 1 : Reset
Write Display Data	1	0	Display Data								Writes data (DB0:7) into display data RAM. After writing instruction, Y address is increased by 1 automatically.
Read Display Data	1	1	Display Data								Reads data (DB0:7) from display data RAM to the data bus.

9. DISPLAY DATA RAM ADDRESS MAP



11. INTERFACE PIN CONNECTIONS

PIN NO.	SYMBOL	LEVEL	DESCRIPTION
1	V_{SS}	0V	Ground
2	V_{DD}	5.0V	Supply voltage for logic and LCD (+)
3	V_O	---	Operating voltage for LCD (variable)
4	RS	H/L	H : Data, L : Instruction code
5	R/W	H/L	H : Read (MPU ← Module), L : Write (MPU → Module)
6	E	H, H → L	Chip enable signal
7	DB0	H/L	Data bit 0
8	DB1	H/L	Data bit 1
9	DB2	H/L	Data bit 2
10	DB3	H/L	Data bit 3
11	DB4	H/L	Data bit 4
12	DB5	H/L	Data bit 5
13	DB6	H/L	Data bit 6
14	DB7	H/L	Data bit 7
15	CS1	H	Chip select signal for IC1
16	CS2	H	Chip select signal for IC2
17	RSTB	L	Reset signal
18	V_{OUT}	-5V	Output voltage for LCD (-)
19	BLA	4.2V *	Back-Light Anode
20	BLK	0V	Back-Light Cathode

* For LED back-light.

12. PART LIST

Part Name	Quantity	Description
IC	1	KS0107B
IC	2	KS0108B
IC	1	SCI7660M
IC	1	NJM064M
LCD	1	TSD-4000-DYFDCN
PCB	1	MCG12864A1
Frame	1	MG12864-1 or MG12864-1B(with BL)
Rubber connector	2	83.7x3.0x3.0mm or 83.7x6.9x3.0mm(with BL)
Heatseal connector	1	6405
Resistor	4	3KΩ
Resistor	1	15KΩ
Resistor	1	1MΩ
Resistor	1	47KΩ
Capacitor	1	27pF ± 5%
Capacitor	2	10uF
Transistor	1	M5
Light box	1	LB12864-1