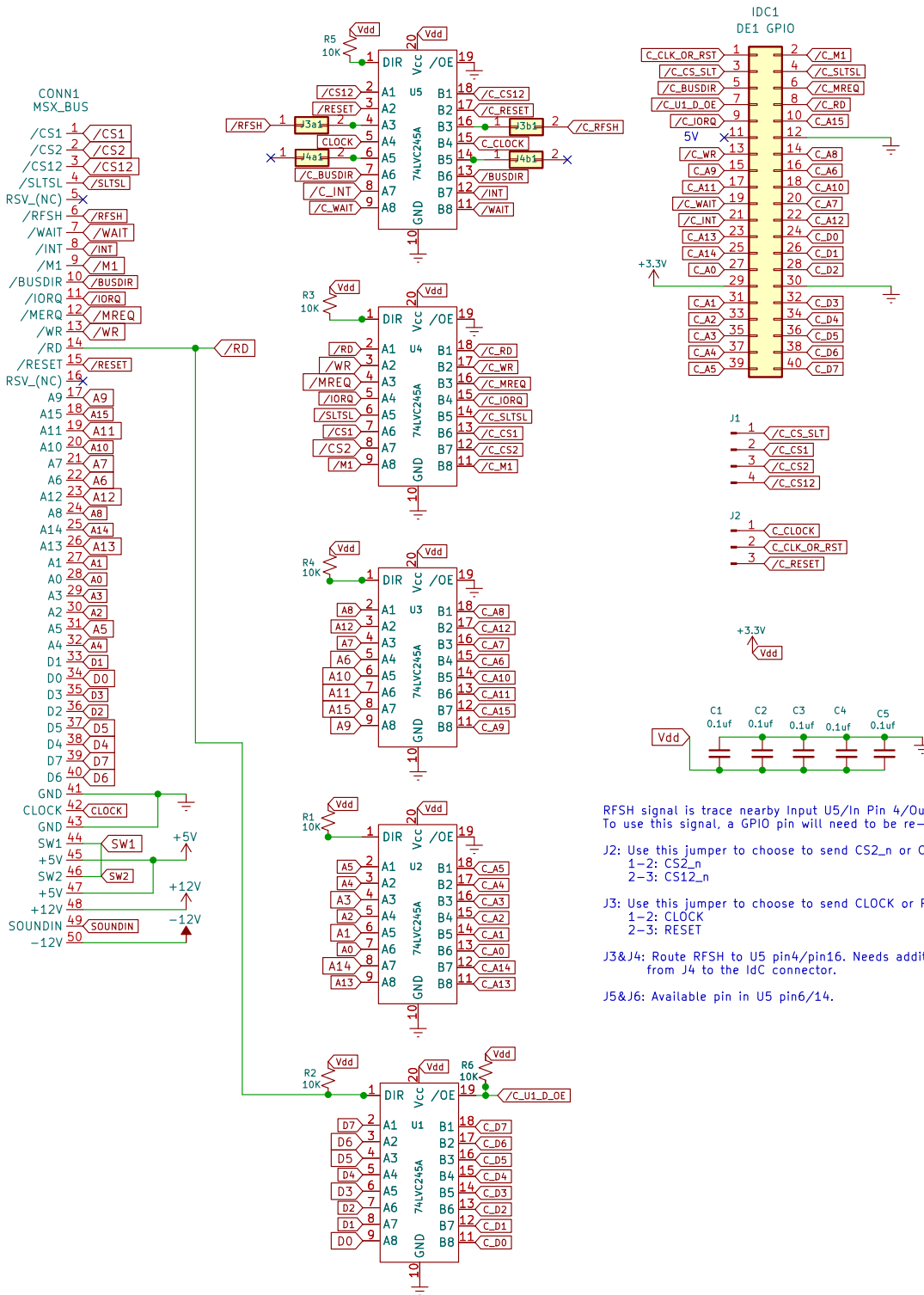


/C\_U1\_D\_OE pin must be asserted according to the direction of data in the MSX Data Bus (U1 in the interface)

PIN mappings was carefully designed to support the both DE0 and DE1 GPIO connector.  
DE0 board has 2xCLK\_IN (1,3) and 2xCLK\_OUT (19,21) pins, which are not present on DE1.



RFSH signal is trace nearby Input U5/In Pin 4/Out Pin 16.  
To use this signal, a GPIO pin will need to be re-wired to pin 16.

J2: Use this jumper to choose to send CS2\_n or CS12\_n to IDC pin 6:  
1-2: CS2\_n  
2-3: CS12\_n

J3: Use this jumper to choose to send CLOCK or RESET signal to IDC pin 2:  
1-2: CLOCK  
2-3: RESET

J3&J4: Route RFSH to U5 pin4/pin16. Needs additional wiring to use this signal, from J4 to the IdC connector.

J5&J6: Available pin in U5 pin6/14.

Designed for Terasic DE0 & DE1  
IDC connector pinout mapped for Altera DE1 FPGA Development Board  
Cartridge for MSX Computers that expose the MSX BUS  
to 3.3v systems with voltage conversion

#### RCC

Sheet: /  
File: MSX\_FPGA\_Hat.kicad\_sch

**Title: MSX FPGA Hat**

Size: A4 Date: 2023-02-17  
KiCad E.D.A. eeschema (6.0.7)

**Rev: 1.2**  
Id: 1/1