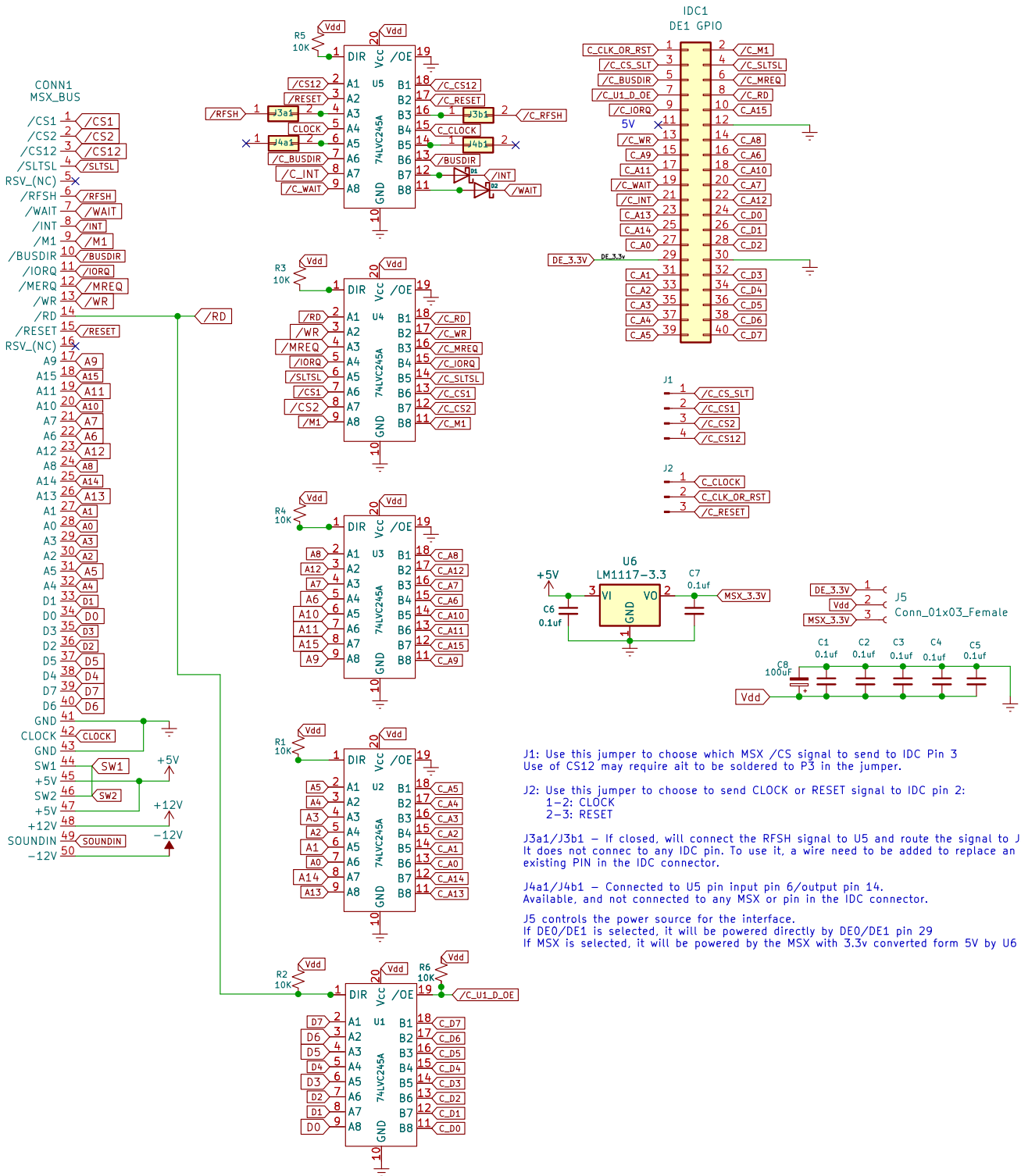


/C_U1_D_OE pin must be asserted for any write and read operation.
PIN mappings was carefully designed to support the both DE0 and DE1 GPIO connector.
DE0 board has 2xCLK_IN (1,3) and 2xCLK_OUT (19,21) pins, which are not present on DE1. These pins cannot operate as bi-directional IO signals, and therefore they were assigned to specific functions in the interface – the direction of their signals must not be changed.



- J1: Use this jumper to choose which MSX /CS signal to send to IDC Pin 3
Use of CS12 may require ait to be soldered to P3 in the jumper.
- J2: Use this jumper to choose to send CLOCK or RESET signal to IDC pin 2:
1-2: CLOCK
2-3: RESET
- J3a1/J3b1 – If closed, will connect the RFSH signal to U5 and route the signal to J3b1.
It does not connect to any IDC pin. To use it, a wire need to be added to replace an existing PIN in the IDC connector.
- J4a1/J4b1 – Connected to U5 pin input pin 6/output pin 14.
Available, and not connected to any MSX or pin in the IDC connector.
- J5 controls the power source for the interface.
If DE0/DE1 is selected, it will be powered directly by DE0/DE1 pin 29
If MSX is selected, it will be powered by the MSX with 3.3v converted form 5V by U6

Designed for Terasic DE0 & DE1
IDC connector pinout mapped for Altera DE1 FPGA Development Board
Cartridge for MSX Computers that expose the MSX BUS
to 3.3v systems with voltage conversion

RCC

Sheet: /
File: MSX_FPGA_Hat.kicad_sch

Title: MSX FPGA Hat

Size: A4 Date: 2023-02-21
KiCad E.D.A. eeschema (6.0.7)

Rev: 1.2
Id: 1/1