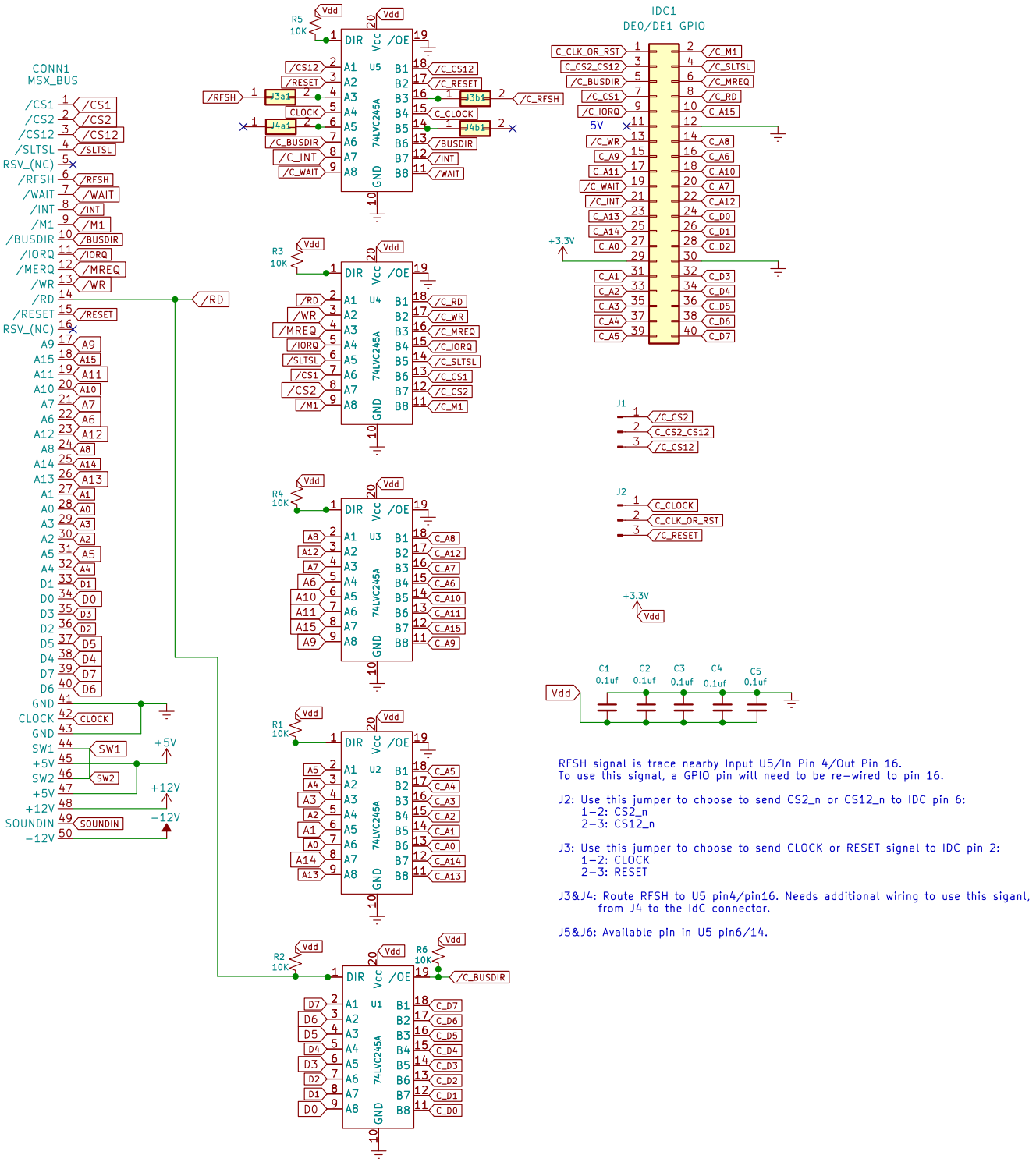
C_BUSIDR_n is very important signal and always need to be driven by the FPGA logic.
This signal controls the DIR pin 1 in the U1 CI (74LVC45), allowing data in the MSX Data bus
to flow on both directions. It also goes directly to the MSX BUSDIR_n pin, to be used by the MSX.

C_BUSDIR_n must be HIGH initially, for the FPGA to receive data from MSX.
Once the data is asserted in the datab bus, C_BUSDIR_n must be set LOW to allow
the MSX to receive it.

Ideally this signal is driven with a combinational logic using SLTSL_n, IORQ_n, RD_n at minimum,
since these signals allow to understand on which direction the data show be flowing.

PIN mapping for the IDC connector was carefully designed to make sure it supports
both DE0 and DE1 GPIOs in the IDC connector JP2.
DE0 board has 2 x CLK_IN (input only pn 1.3) and 2 x CLK_OUT (output pins 19.21)
which differ from the DE1. This version makes sure this project can be
used in both Boards without modification.



RFSH signal is trace nearby Input U5/In Pin 4/Out Pin 16.
To use this signal, a GPIO pin will need to be re-wired to pin 16.

J2: Use this jumper to choose to send CS2_n or CS12_n to IDC pin 6:
    1-2: CS2_n
    2-3: CS12_n

J3: Use this jumper to choose to send CLOCK or RESET signal to IDC pin 2:
    1-2: CLOCK
    2-3: RESET

J3&J4: Route RFSH to U5 pin4/pin16. Needs additional wiring to use this siganl,
       from J4 to the IdC connector.

J5&J6: Available pin in U5 pin6/14.

Designed for Terasic DE0 & DE1
Compatible with Terasic DE2-70 & DE2-115
RCC

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File: MSX_FPGA_Hat.kicad_sch

Title: MSX FPGA Hat

Size: A4	Date: 2023-01-31	**Rev: 1.1**
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