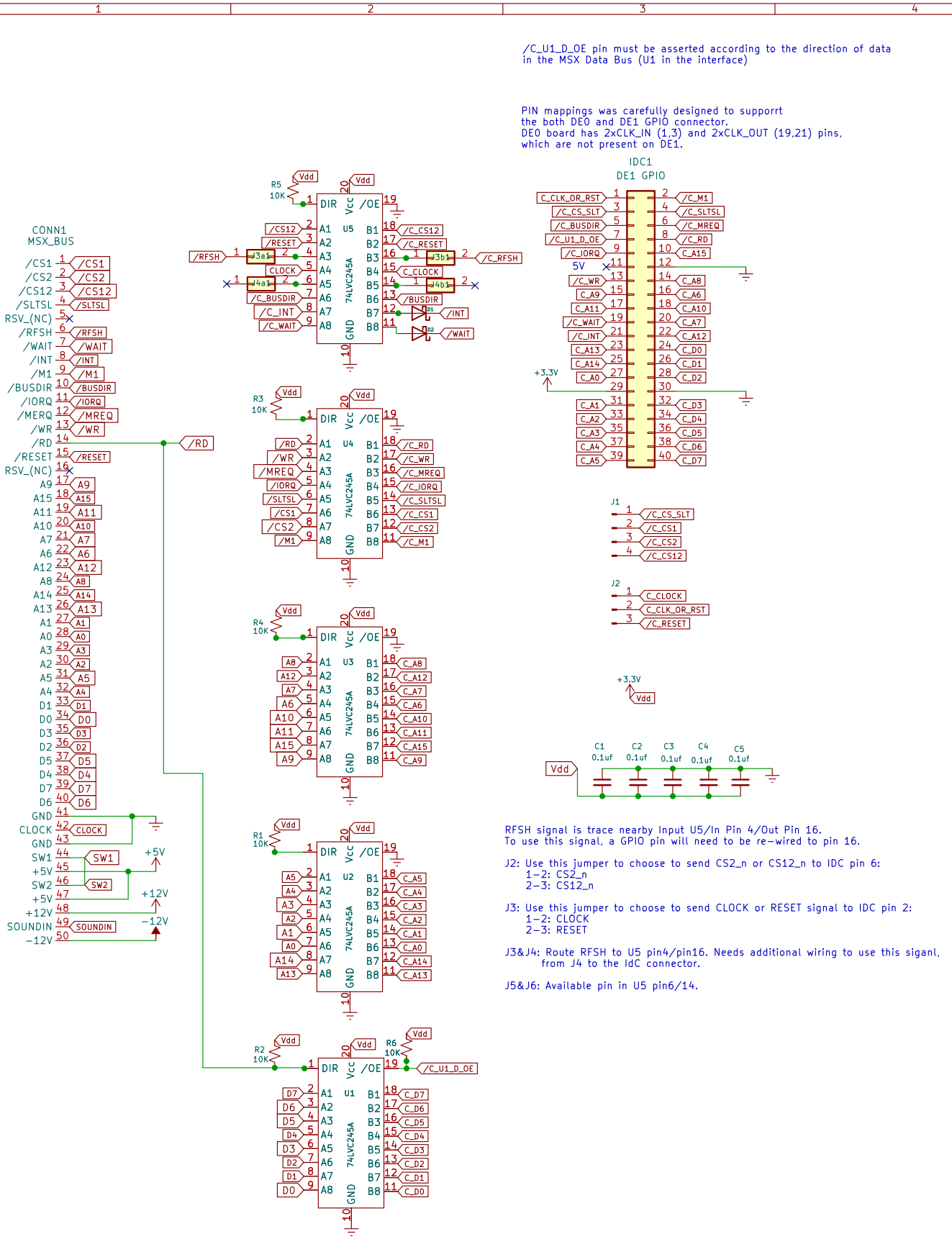
/C_U1_D_OE pin must be asserted according to the direction of data
in the MSX Data Bus (U1 in the interface)
PIN mappings was carefully designed to supporrt
the both DE0 and DE1 GPIO connector.
DE0 board has 2xCLK_IN (1,3) and 2xCLK_OUT (19,21) pins,
which are not present on DE1.
CONN1
MSX_BUS
IDC1
DE1 GPIO
74LVC245A
RFSH signal is trace nearby Input U5/In Pin 4/Out Pin 16.
To use this signal, a GPIO pin will need to be re-wired to pin 16.
J2: Use this jumper to choose to send CS2_n or CS12_n to IDC pin 6:
1-2: CS2_n
2-3: CS12_n
J3: Use this jumper to choose to send CLOCK or RESET signal to IDC pin 2:
1-2: CLOCK
2-3: RESET
J3&J4: Route RFSH to U5 pin4/pin16. Needs additional wiring to use this siganl,
from J4 to the IdC connector.
J5&J6: Available pin in U5 pin6/14.
Designed for Terasic DE0 & DE1
IDC connector pinout mapped for Altera DE1 FPGA Development Board
Cartridge for MSX Computers that expose the MSX BUS
to 3.3v systems with voltage conversion
RCC
Sheet: /
File: MSX_FPGA_Hat.kicad_sch
Title: MSX FPGA Hat
Size: A4
Date: 2023-02-20
Rev: 1.3
KiCad E.D.A. kicad (6.0.7)
Id: 1/1