C_BUSIDR_n is very important signal and always need to be driven by the FPGA logic. This signal controls the DIR pin 1 in the UI Cl (74LV45), allowing data in the MSX Data bus to flow on both directions. It also goes directly to the MSX BUSDIR.n pin, to be used by the MSX. C_BUSDIR_n must be HIGH initially, for the FPGA to receive data from MSX. Once the data is asserted in the datab bus, C_BUSDIR_n must be set LOW to allow the MSX to receive it. PIN mapping for the IDC connector was carefully designed to make sure it supports both DEO and DE1 GPIOs in the IDC connector JP2. DE0 board has $2 \times \text{CLK}_n \text{(input only p n 1.5)}$ and $2 \times \text{CLK}_n \text{OUT}$ (output pins 19.21) which differ from the DE1. This version makes sure this project can be used in both Boards without modification. Ideally this signal is driven with a combinational logic using SLTSL_n, IORQ_n, RD_n at minimum, since these signals allow to understand on which direction the data show be flowing. R5 Vdd QVdd N DIR S /OE 19 IDC1 DEO/DE1 GPIO 2 /C_M1 4 /C_SLTSL 6 /C_MREQ 8 /C_RD 10 (C_A15) 12 14 (C_A8 16 (C_A6) 18 (C_A10) 22 (C_A7) 22 (C_A12) 24 (C_D0) 26 (C_D1) 28 (C_D2) | VIK CCLK_OR_RST 1

C_CS2_CS12 3

C_BUSDIR 5

H /C_CS1 7

F/C_JORQ 9

F/C_JORQ 1

F/C_WAI 19

F/C_WAI 19

F/C_WAI 19

F/C_WAI 21

C_A3 23

C_A41 25

C_A41 25

C_A41 31

C_A3 35

C_A3 35

C_A3 37

C_A4 37

C_A5 39 CONN1 MSX_BUS /CS1 1 /CS1 /CS2 2 /CS2 /CS12 3 /CS12 /SLTSL 4 /SLTSL /C_RFSH SV_(NC) 5 (RFSH 6 RESH) /RFSH 6 RESH /WAIT 7 / WAIT /INT 8 /INT /M1 9 /M1 /M1 10 /BUSDIR /IORQ 11 /ORQ /WERQ 12 /MREQ /WERQ 12 /MREQ /WERQ 12 /MREQ /WERQ 12 /MREQ /WERQ 14 /MREQ 26 C_D1 28 C_D2 30 32 C_D3 34 C_D4 36 C_D5 38 C_D6 40 C_D7 R3 10K N Aqq DIR 5 /OE 19 U4 B1 18 CRD
B2 17 CWR
B1 15 CMREQ
B3 15 CMREQ
B4 15 CMREQ
B5 14 CS115L
B6 13 CCS1
B7 12 CCS2
B8 8 14 CM1 | RRD | 2 | A1 | U4 |
WR	3	A2
MREQ	4	A3
MORE	5	A4
SITSI	7	A6
CS2	8	A7
MI	9	A8
D6 3 A2
D5 4 A3
D4 5 A4
D3 6 A5
D2 7 A6
D1 8 A7
D0 9 A8 -A1 U1 B1 18 C_D7
-A2 B2 16 C_D5
-A3 & B3 15 C_D5 83 16 C.D5 4 15 C.D5 84 15 C.D5 85 14 C.D3 86 13 C.D2 87 12 C.D1 88 11 C.D0 Designed for Terasic DEO & DE1 Compatible with Terasic DE2-70 & DE2-115 **RCC** Sheet: File: MSX_FPGA_Hat.kicad_sch Title: MSX FPGA Hat Size: A4 Date: 2023-01-31 Rev: 1.1 KiCad E.D.A. kicad (6.0.9-0)