#### L41 - Lecture 5: The Network Stack (1)

Dr Robert N. M. Watson

19 January 2016



Long, long ago, but in a galaxy not so far away:

- ► Lecture 3: The Process Model (1)
- ► Lecture 4: The Process Model (2)



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- ► Lab 1: I/O performance



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- ▶ The probe effect doesn't matter in real workloads



#### This time: Introduction to the Network Stack

#### Rapid tour across hardware and software:

- 1. Networking and the sockets API
- 2. Network-stack design principles: 1980s and today
- 3. Memory flow across hardware and software
- 4. Network-stack construction and work flows
- Recent network-stack research





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- Dramatic changes over 30 years:
  - ▶ 1980s: Early packet-switched networks, UDP+TCP/IP, Ethernet
  - 1990s: Large-scale migration to IP; Ethernet VLANs
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- ▶ Vanishing technologies: UUCP, IPX/SPX, ATM, token ring, SLIP, ...

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- Multi-protocol (e.g., IPv4, IPv6, ISO, ...)
  - TCP-focused but not TCP-specific
  - Cross-protocol abstractions and libraries
  - Protocol-specific implementations
  - "Portable" applications



A framework for **multi-protocol**, **packet-oriented** network research:

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  - ► High-performance packet capture: Berkeley Packet Filter (BPF)





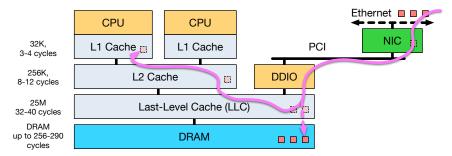
- Hardware:
  - Multi-processor scalability
  - NIC offload features (checksums, TSO/LRO, full TCP)
  - Multi-queue network cards with load balancing/flow direction
  - Performance to 10s or 100s of Gigabit/s
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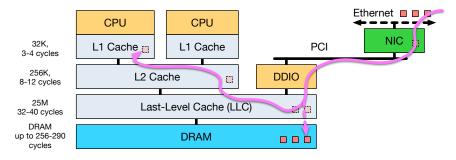
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- Software model:
  - Flexible memory model integrates with VM for zero-copy
  - Network-stack virtualisation
  - Userspace networking via netmap



# Memory flow in hardware

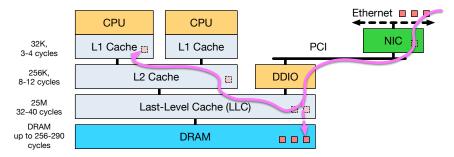


# Memory flow in hardware



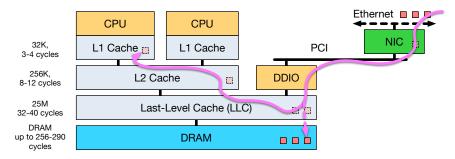
► Key idea: follow the memory

# Memory flow in hardware

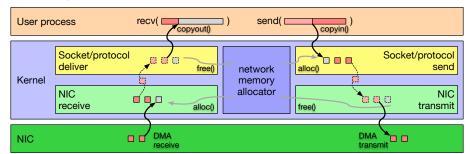


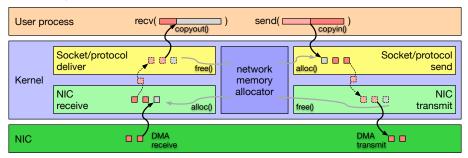
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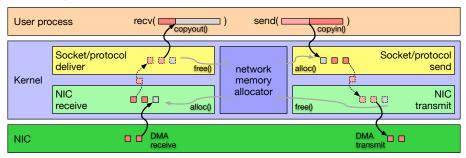


- Key idea: follow the memory
- Historically, memory copying avoided due to CPU cost
- Today, memory copying avoided due to cache footprint
- Recent Intel CPUs push and pull DMA via the LLC ("DDIO")
- ▶ NB: if we differentiate 'send' and 'transmit', is this a good idea?

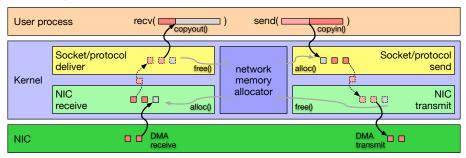




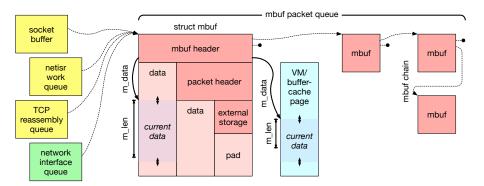
- Socket API implies one copy to/from user memory
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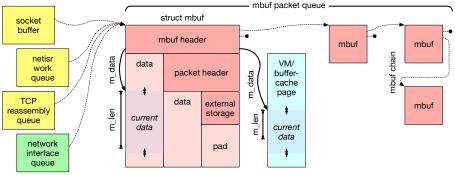


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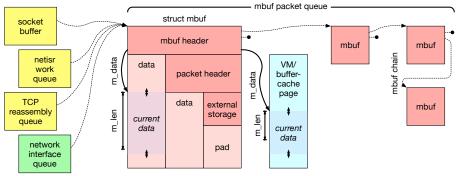


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- ▶ DMA performs second copy; can affect cache/memory bandwidth
  - ▶ NB: what if packet-buffer working set is larger than the cache?

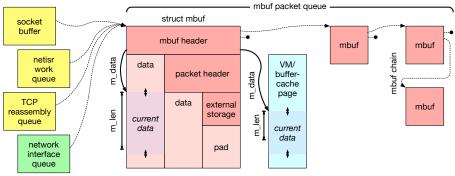




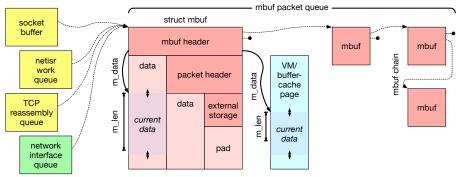
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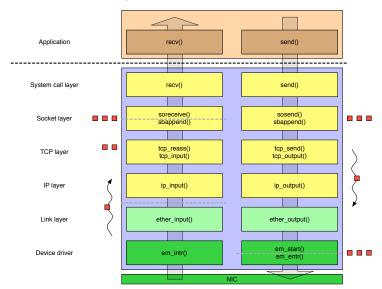


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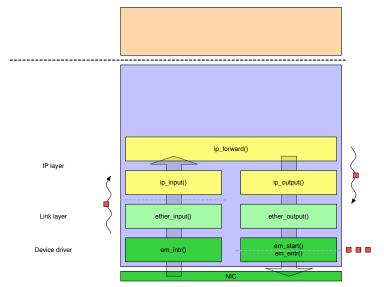


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- Similar structures in other OSes e.g., skbuff in Linux

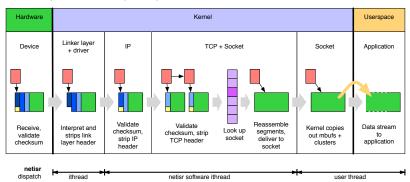
## Local send/receive paths in the network stack



#### Forwarding path in the network stack



## Work dispatch: input path

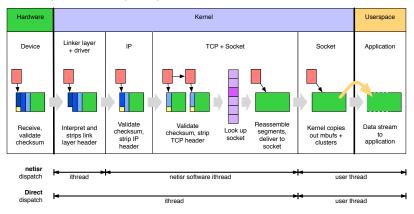


user thread

Direct dispatch

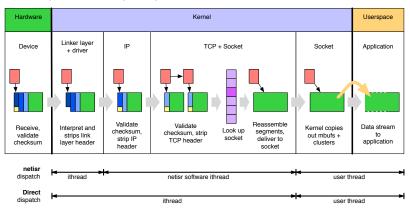
ithread

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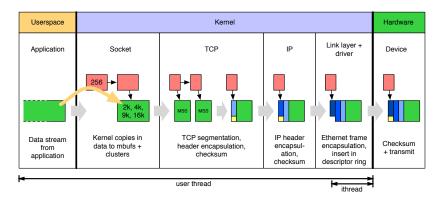
Deferred dispatch - ithread -> netisr thread -> user thread

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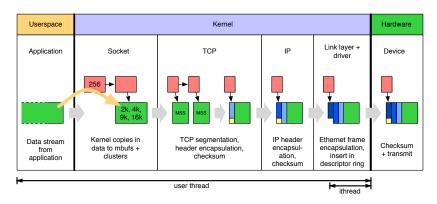


- Deferred dispatch ithread -> netisr thread -> user thread
- Now: direct dispatch ithread -> user thread
  - Pros: reduced latency, better cache locality, drop overload early
  - Cons: reduced parallelism and work placement opportunities

#### Work dispatch: output path

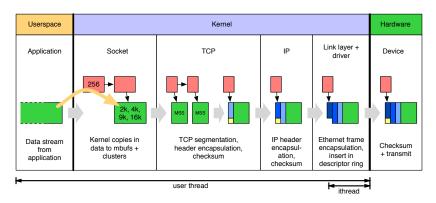


#### Work dispatch: output path



Fewer deferred dispatch opportunities implemented

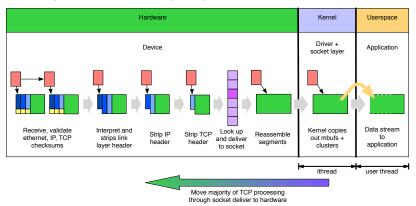
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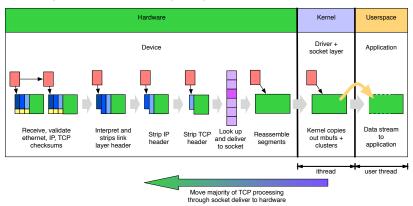
- Fewer deferred dispatch opportunities implemented
- Gradual shift of work from software to hardware
  - Checksum calculation, segmentation, ...



#### Work dispatch: TOE input path

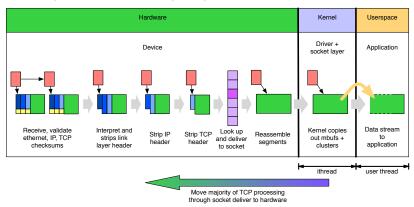


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  - Kernel provides socket buffers and resource allocation
  - Remainder, including state, retransmits, reassembly, etc, in NIC
- But: Two network stacks? Less flexible/updateable structure?
- ► Better with an explicit HW/SW architecture e.g., Microsoft Chimney? 

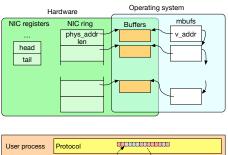
  Dr Robert N. M. Watson

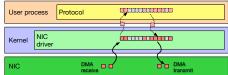
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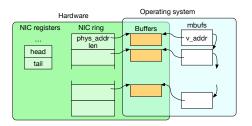
# netmap: a novel framework for fast packet I/O Luigi Rizzo, USENIX ATC 2012 (best paper).



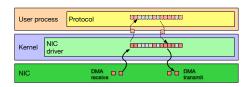


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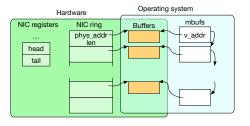


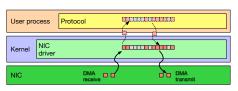
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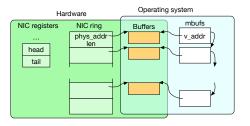


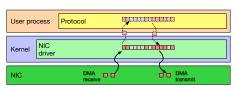


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- Ships in FreeBSD, patch available for Linux

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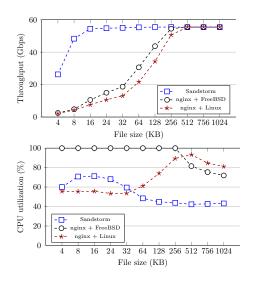
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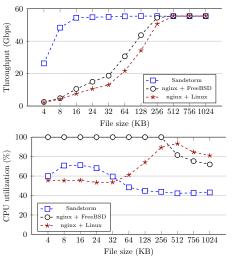


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- Userspace network stack can be specialized to task (e.g., packet forwarding)

Ilias Marinos, Robert N.M. Watson, Mark Handley, SIGCCOMM 2014.

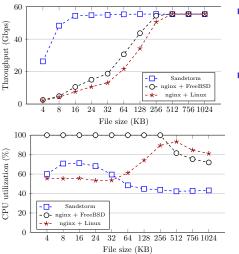


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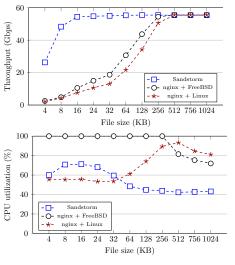
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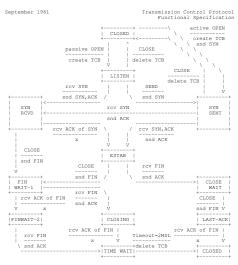


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- Massive changes in architecture, micro-architecture, memory, buses, NICs
  - Optimising compilers
  - Cache-centered CPUs
  - Multiprocessing, NUMA
  - DMA, multiqueue
  - 10 Gigabit/s Ethernet

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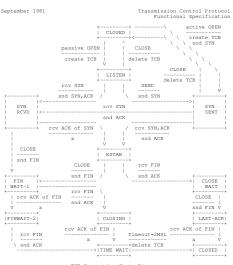


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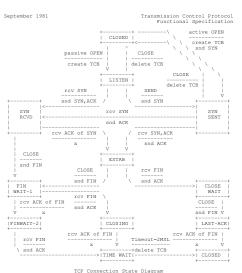


TCP Connection State Diagram Figure 6.

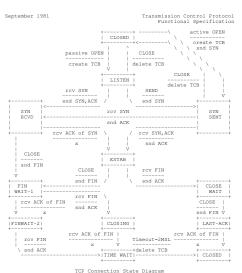




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