

The MSX system-clock is often set to 3.58MHz – aka, the same as the sub-carrier clock of NTSC.

Cartridge-dummy – to allow testing of the mechanical form-factor.

LEGEND:

VDP = Video Display Processor
CLK = Clock
SLTSL = Slot Select signal
CS = Chip Select
SYS_CLK = MSX System Clock

The schematic diagram illustrates the V9990 video chip interface, showing connections for various components and signals. The chip is represented by a central block labeled 'V9990' with multiple interfaces.

VRAM interface (U1B): This interface connects the V9990 to VRAM. It includes signals for V0_S0 through V0_S7, V0_D0 through V0_D7, V0_A0 through V0_A8, V0_TR/OE, V0_SOE, V0_CAS, V0_RAS, V0_WE, V0_SC, VMBG, and KOE. The signals are connected to V0A[0..8] and V0A[0..8].

PORT 0: This port connects the V9990 to the VRAM interface. It includes signals for V0_S0 through V0_S7, V0_D0 through V0_D7, V0_A0 through V0_A8, V0_TR/OE, V0_SOE, V0_CAS, V0_RAS, V0_WE, V0_SC, VMBG, and KOE. The signals are connected to V0A[0..8] and V0A[0..8].

PORT 1: This port connects the V9990 to the VRAM interface. It includes signals for V1_S0 through V1_S7, V1_D0 through V1_D7, V1_A0 through V1_A8, V1_TR/OE, V1_SOE, V1_CAS, V1_RAS, V1_WE, V1_SC, VMBG, and KOE. The signals are connected to V1A[0..8] and V1A[0..8].

Address Bus & Kanji Output: This interface connects the V9990 to the address bus. It includes signals for KA9 through KA17, KA9, KA10, KA11, KA12, KA13, KA14, KA15, KA16, and KA17. The signals are connected to the address bus.

CLOCK signals (U1C): This interface connects the V9990 to the clock signals. It includes signals for MCKIN (14MHz), XTAL1 (21MHz), XTAL2, HRESET, VRESET, R, G, B, (3.58MHz) CB6/FSC, HSYNC/LC, CSYNC/FLM, BLANK/M, and SHCK. The signals are connected to the clock signals.

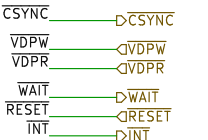
VIDEO interface (U1C): This interface connects the V9990 to the video signals. It includes signals for R, G, B, (3.58MHz) CB6/FSC, HSYNC/LC, CSYNC/FLM, BLANK/M, and SHCK. The signals are connected to the video signals.

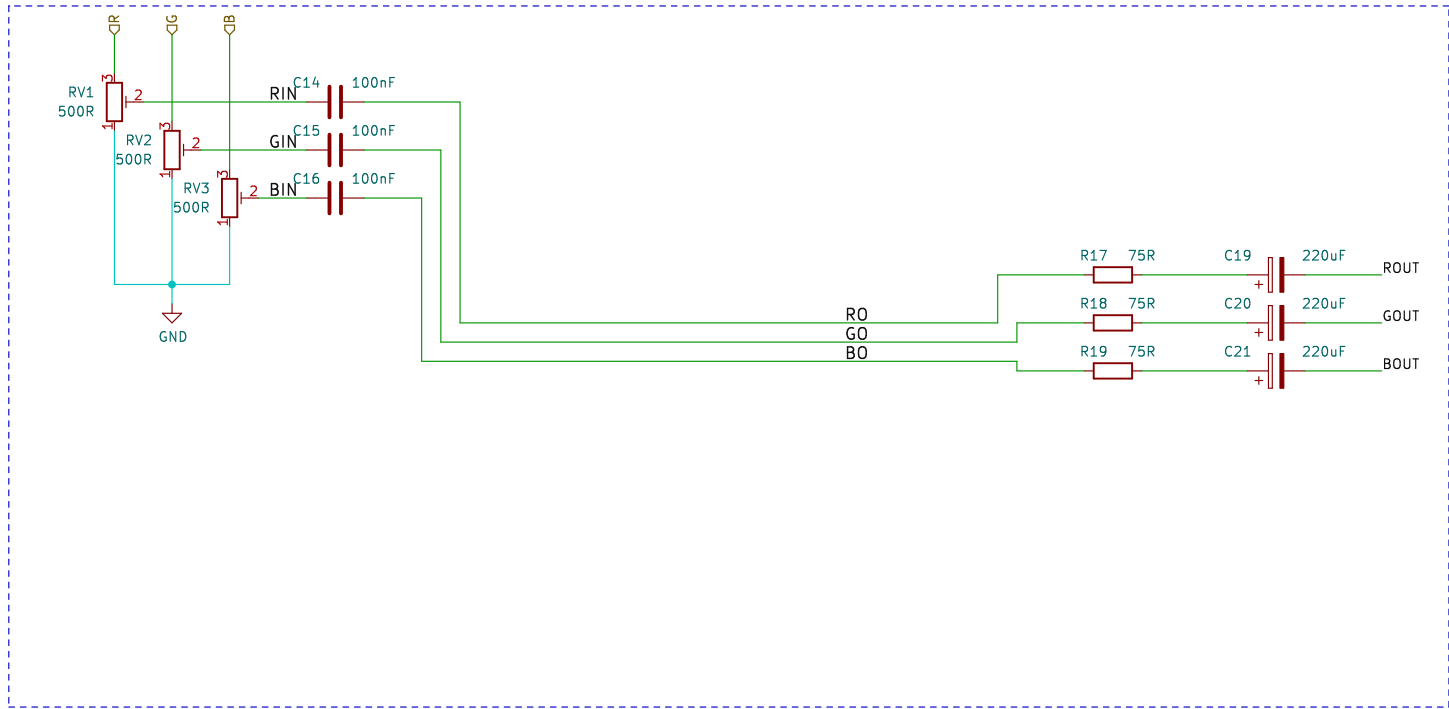
CPU Interface (U1A): This interface connects the V9990 to the CPU. It includes signals for RESET, WAIT, VMREQ, DREQ, INTO, INTI, CD0, CD1, CD2, CD3, CD4, CD5, CD6, CD7, VDPW, V DPR, CSR, and CSW. The signals are connected to the CPU.

The diagram also shows the power supply and timing components, including a 5V supply, a 14.31818MHz oscillator, a 21.47727MHz oscillator, and various capacitors and resistors.

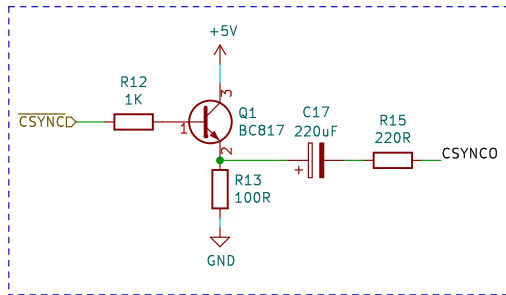
704x480 (60Hz) – 3.579545 MHz

The diagrams show the connection of two KM428C256 memory chips (U3A and U2A) to a microcontroller. Each chip has 256 Kbits of memory organized into four 64Kb banks. The diagrams show the address, data, and control signal connections for each chip, including V0A[0..8], V0D[0..7], V0S[0..7], V1A[0..8], V1D[0..7], and V1S[0..7].

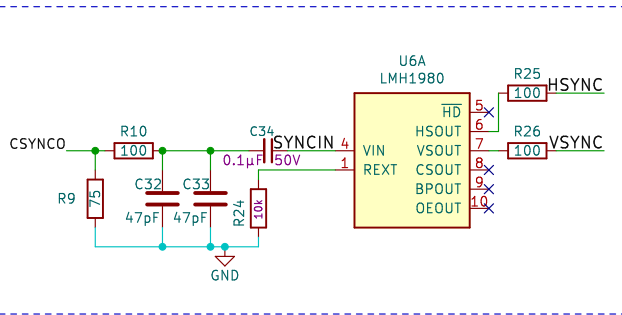




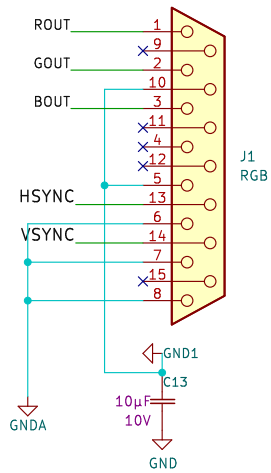
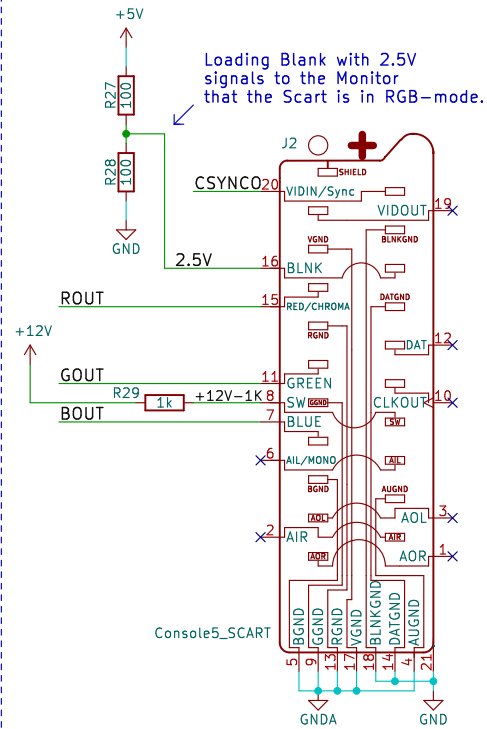
CSync Amplifier



Sync Separator



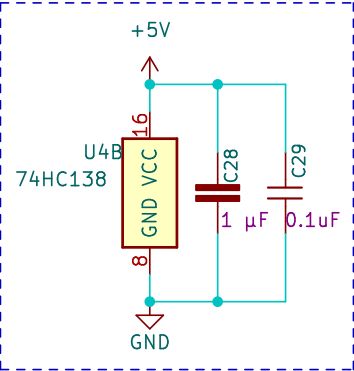
Video Output Connectors



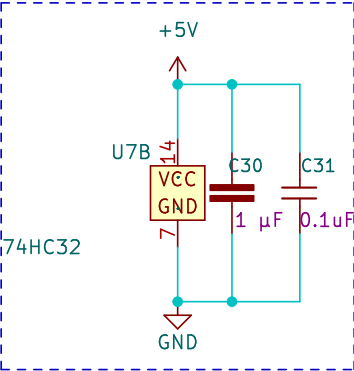
Implementing Superimpose:

1. Feed external HSYNC / VSYNC into V9990 HRESET / VRESET pins for synchronisation
 2. Combine external and internal R, G, B with an analog multiplexer, controlled by /Ys signal
- The principle is that the original external signal is passed through while /Ys is not superimposing.

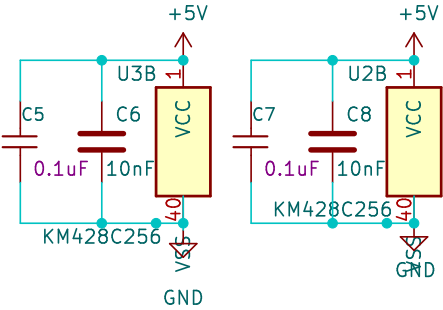
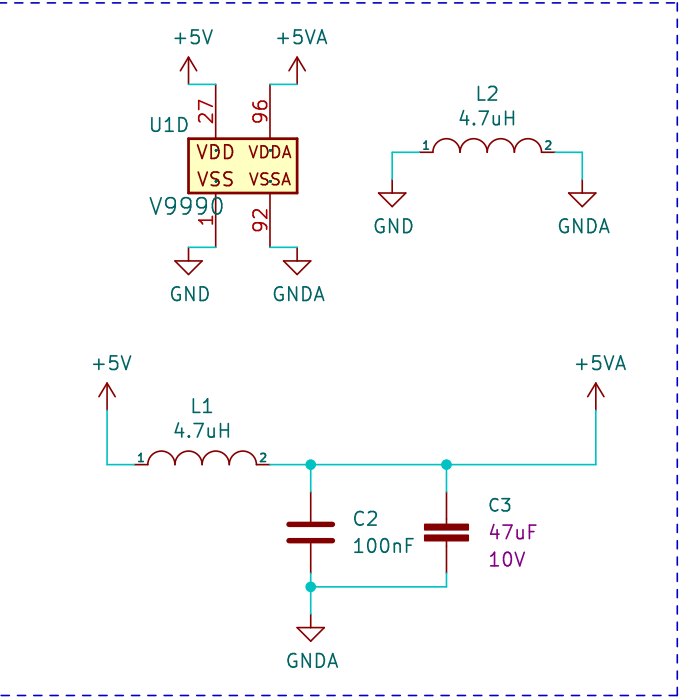
Demultiplexer Power



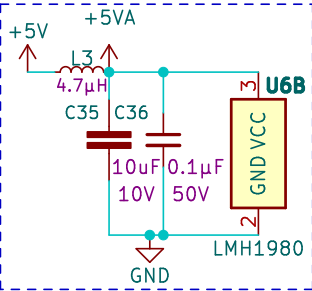
OR-gate Power



VDP Power



Sync Separator power



Power Nets

