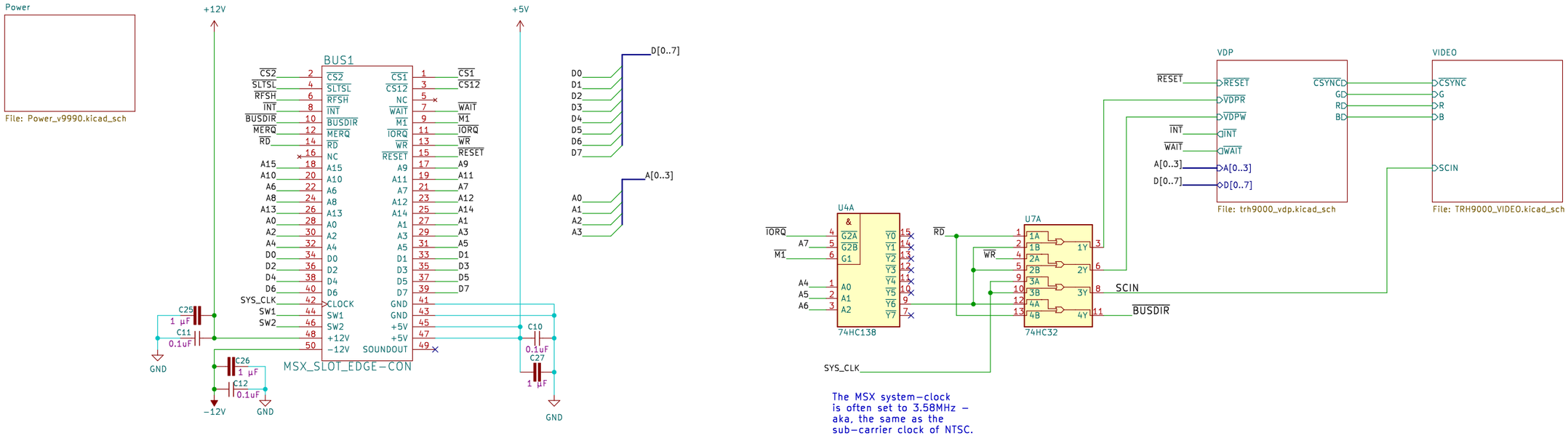


Cart1 Cartridge−dummy − to allow testing
of the mechanical form−factor.

LEGEND:
− − − − −
VDP = Video Display Processor
CLK = Clock
SLTSL = Slot Select signal
CS = Chip Select
SYS_CLK = MSX System Clock

Video Display Processor

VRAM

U1B
VRAM interface
PORT 0
PORT 1
Address Bus & Kanji Output
V9990

U3A
KM428C256

U2A
KM428C256

U1C
CLOCK signals
VIDEO interface
V9990

U1A
CPU Interface
V9990

X1
14.31818MHz

Y1
21.47727Mhz

R1 4K7
R2 4K7
R3 10M
R4 4K7
R5 4K7
R6 4K7

C1 27pF
C4 27pF

GND
+5V

VGA clocks:

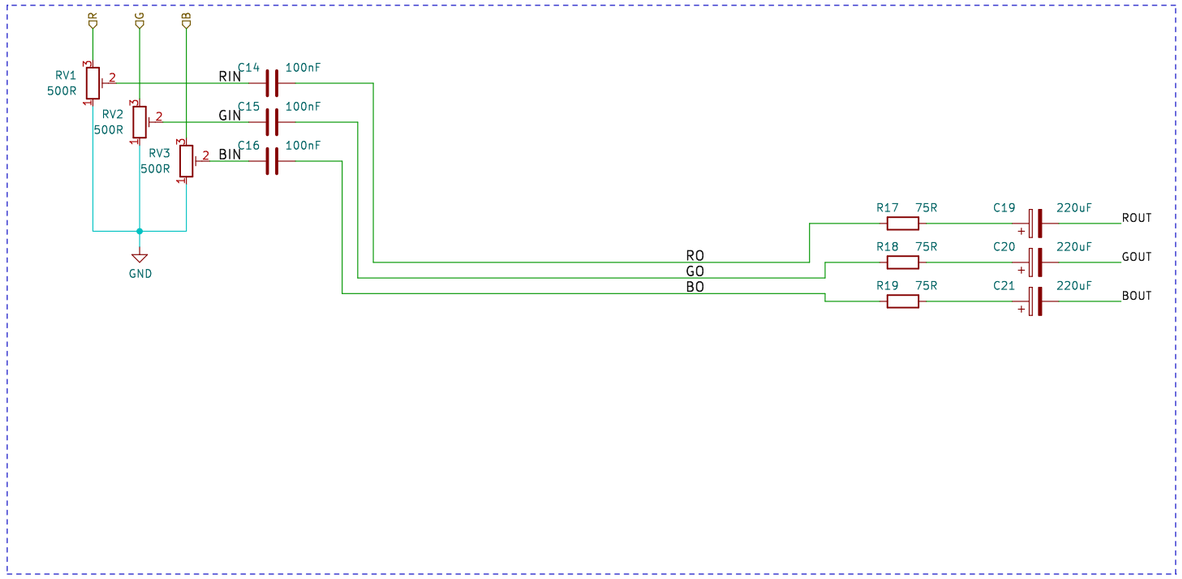
640x400 (70Hz) – 25.175 MHz
640x480 (60Hz) – 25.175 MHz

Pal clocks:

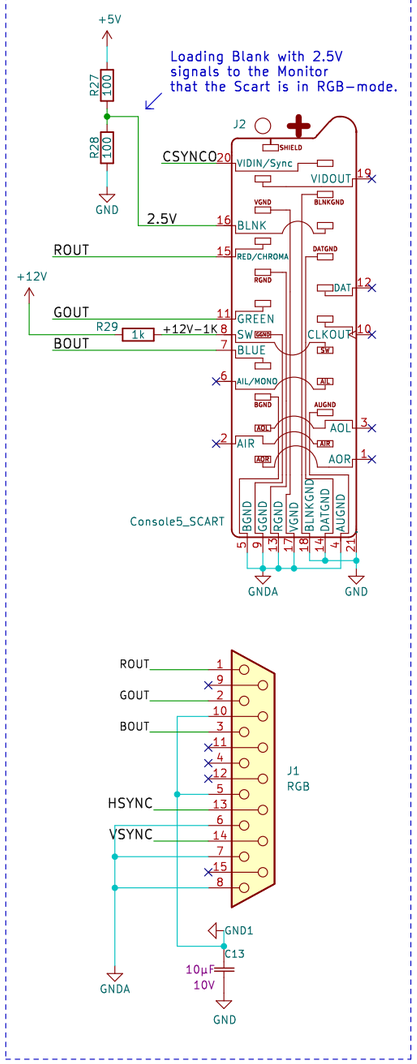
704x576 (50Hz) – 4.43361875 MHz

NTSC clocks:

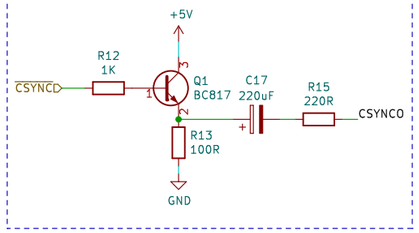
704x480 (60Hz) – 3.579545 MHz



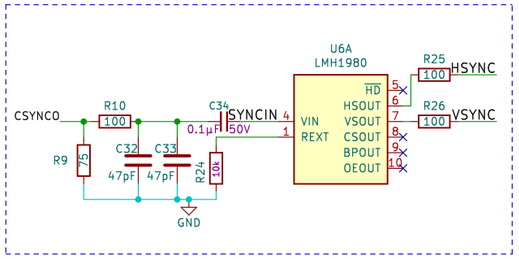
Video Output Connectors



CSync Amplifier



Sync Separator



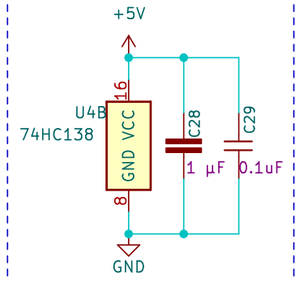
Implementing Superimpose:

1. Feed external HSYNC / VSYNC into V9990 HRESET / VRESET pins for synchronisation

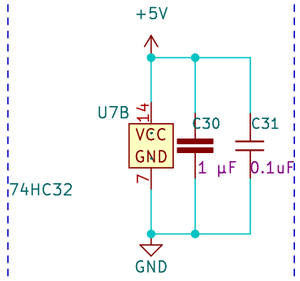
2. Combine external and internal R, G, B with an analog multiplexer, controlled by /Ys signal

The principle is that the original external signal is passed through while /Ys is not superimposing.

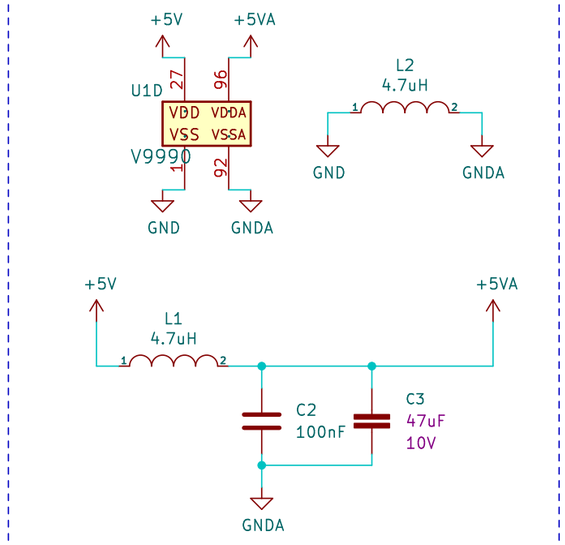
Demultiplexer Power

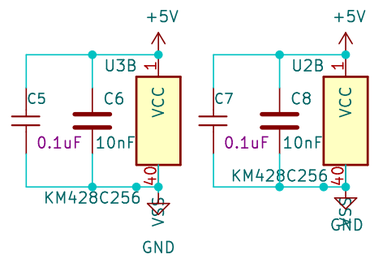


OR-gate Power

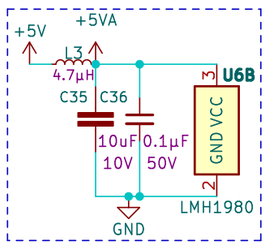


VDP Power





Sync Separator power



Power Nets