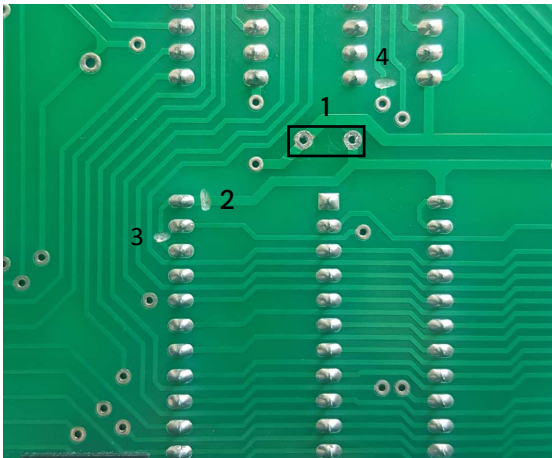


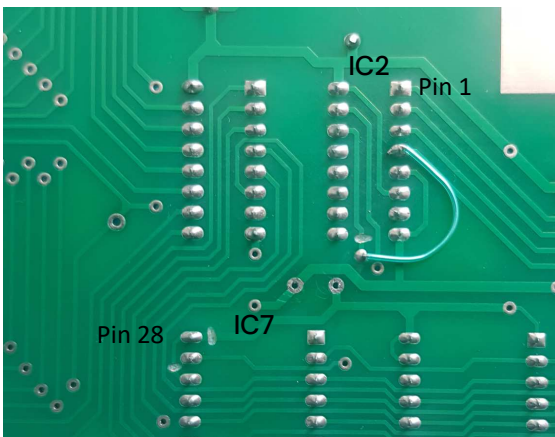
# 56K RAM upgrade for the Southern Cross SBC

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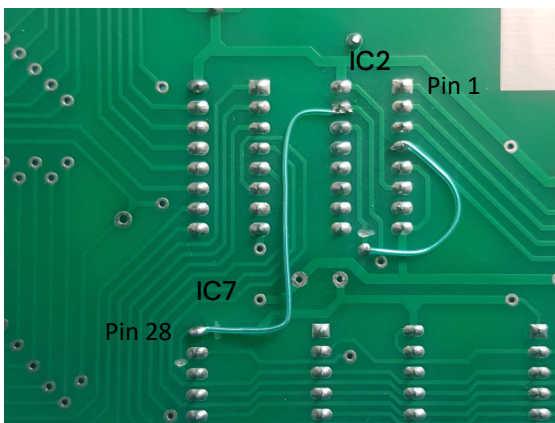
You will need a 32 pin IC socket, a 128K x 8 Static Ram (SRAM) and some thin solid core wire like wire wrap wire.



- 1.** Remove C7.
- 2.** Cut the track between Pin 28 IC7 (6264) and +5V.
- 3.** Cut the track between Pin 26 IC7 (6264) and Pin 28 IC7 (6264).
- 4.** Cut the track between Pin 20 IC7 (6264) and Pin 14 IC2 (74HC138).



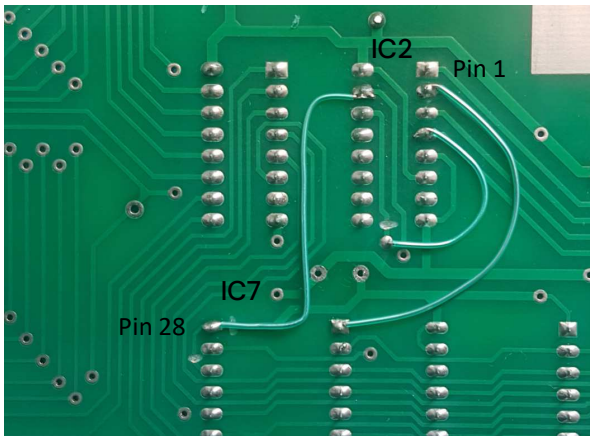
- 5.** Connect Pin 20 IC7 (6264) to nMREQ Pin 4 IC2 (74HC138).



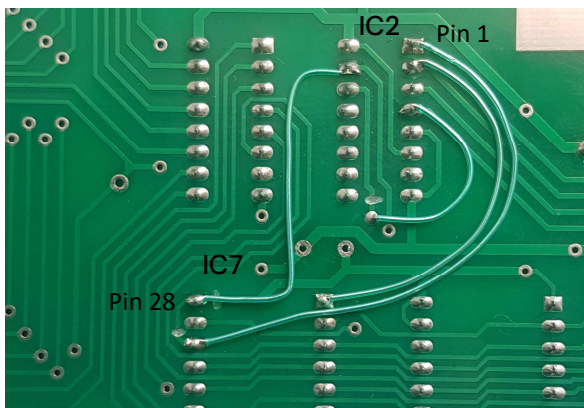
- 6.** Connect Pin 28 IC7 (6264) to Pin 15 IC2 (74HC138).

# 56K RAM upgrade for the Southern Cross SBC

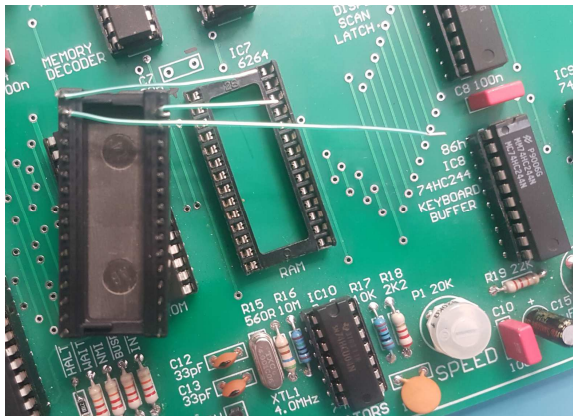
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**7.** Connect Pin 1 IC7 (6264) to A14 Pin 2 IC2 (74HC138).



**8.** Connect Pin 26 IC7 (6264) to A13 Pin 1 IC2 (74HC138).



**9.** Put a 128k x 8 SRAM (like HM628128) in a 32 Pin IC socket to dissipate the heat from soldering to stop the socket plastic from melting.

**10.** Solder short wires on Pins 2 and 32 and a 5 to 6 cm wire on Pin 31.



**11.** Connect the wire from Pin 2 to GND, the right pad of the removed C7.

**12.** Connect the wire from Pin 32 to +5V the left side of the removed C7.

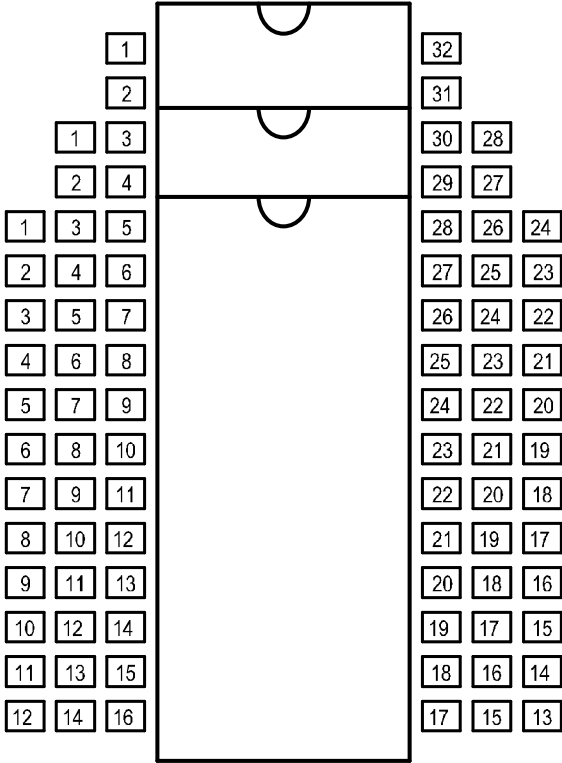
**13.** Connect the wire from Pin 31 to A15, the bottom via of the three diagonal vias to the left of C4.

**14.** Solder a 100nF Ceramic capacitor on the back of the board in the C7 position.



# Static RAM Pinouts

512k	128k	32k	8k	2k
628512	628128	62256	6264	6116
A18	NC			
A16	A16			
A14	A14	A14	NC	
A12	A12	A12	A12	
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
D0	D0	D0	D0	D0
D1	D1	D1	D1	D1
D2	D2	D2	D2	D2
GND	GND	GND	GND	GND



2k	8k	32k	128k	512k
6116	6264	62256	628128	628512
			VCC	VCC
			A15	A15
		VCC	VCC	CS2
		$\overline{WE}$	$\overline{WE}$	$\overline{WE}$
VCC	CS2	A13	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
$\overline{WE}$	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A10	A10	A10	A10	A10
$\overline{CE}$	$\overline{CS1}$	$\overline{CE}$	$\overline{CS1}$	$\overline{CE}$
D7	D7	D7	D7	D7
D6	D6	D6	D6	D6
D5	D5	D5	D5	D5
D4	D4	D4	D4	D4
D3	D3	D3	D3	D3