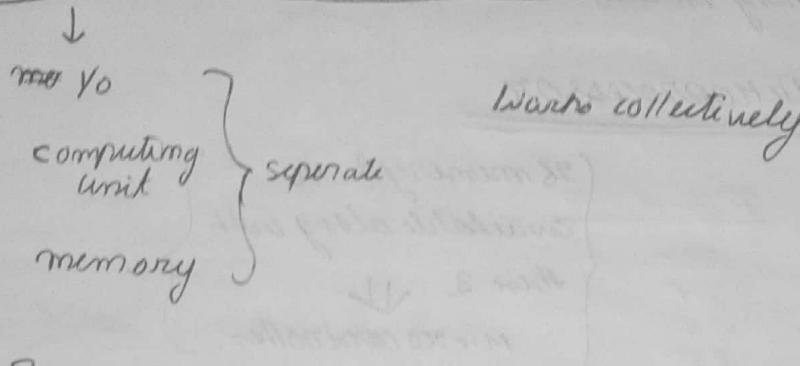


* MICROPROCESSORS

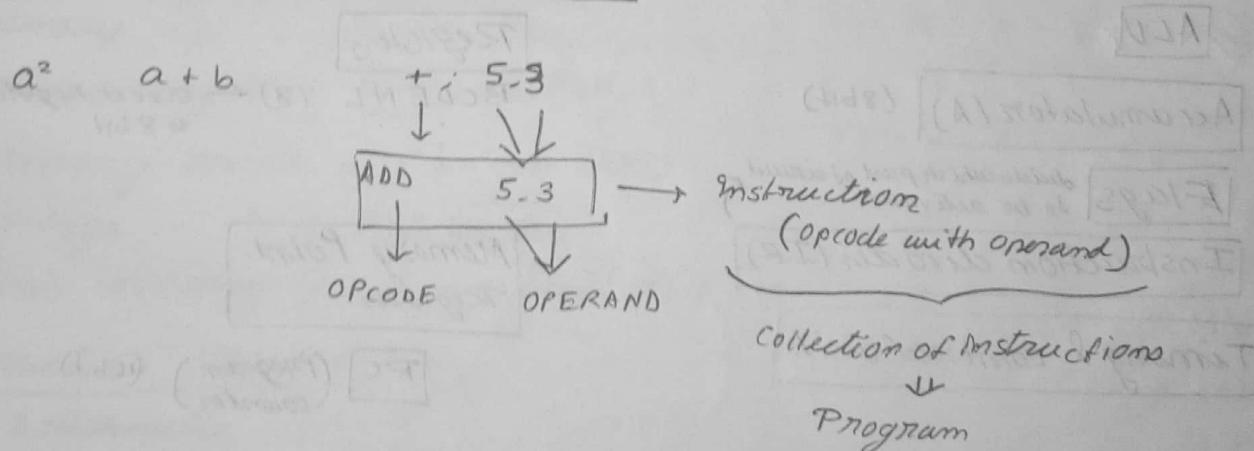
1. 8085
2. 8086
3. IBM 360/370

Placing instructions in the memory for the CPU to execute. ← microprocessor

Microprocessor and Microcontroller



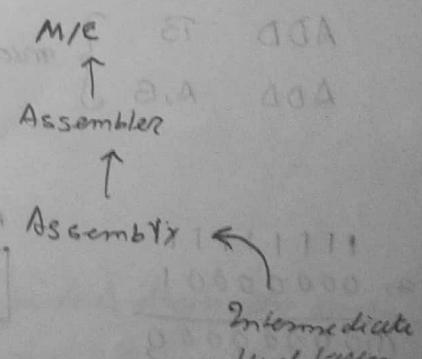
Instruction, opcode and operands.



Languages

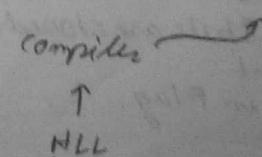
1. High LL
2. Assembly LL
3. Machine LL

ADC B...
10110...



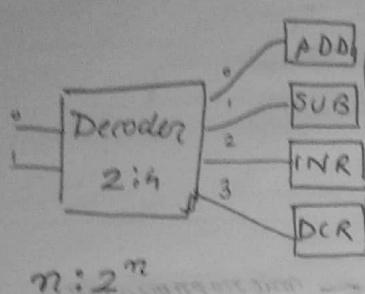
* Mnemonics: Opcode in Assembly LL.

* RAM: Accessing time - unique



24/7/19

Decoder



outputs, 28083054051M

Only one line is active & others are inactive
or
Only one inactive & others are active

Instruction :- part of the CPU which decodes the instruction

(IR)

* When we want to select something in a circuit, we use decoder.

* Basic components in a Microprocessor

1. ALU
2. Registers
3. Control unit.

{ 26 memory & 10 available along with these 3 }
↓
Microcontroller.

ALU

Accumulator (A) (8 bit)

Flags (bits which part of circuit is activated.)

Instruction decoder (IR)

Timing & control unit

Registers

BCDEHL (8) ← size of register is 8 bit.

Memory Point Register

PC (Program counter) (16 bit)

* Accumulator is a register which performs ALU operations

ADD B
ADD A, B } means the same

Implicit operand
By default ↓

Accumulator

11111111
00000001

00000000

8 bits are stored in Accumulator
Extra bit stored in Flag.

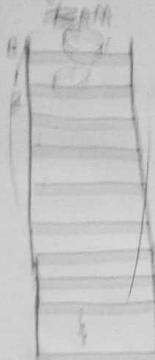
Flags

S	Z	Ac	P	Cy
---	---	----	---	----

1

Flags get activated whenever some data is overflowing.

* Program counter carries the next memory address to fetch.



It can add a specific address in the memory using Memory decoder.

Size of each memory location in RAM \rightarrow 8 bit

Last address FFFF

$$\begin{matrix} \downarrow & \downarrow & \downarrow & \downarrow \\ h & h & h & h \end{matrix} = 16 \text{ bits}$$

No. of memory blocks in 85 microprocessor $\rightarrow 2^{16}$

8 bit micro.

2017/19

* Some points

1. Word length = 8 bit

2. Address length = 16 bit

3. Memory size = 2^{16}

4. Base registers = A, B, C, D, E, H, L

5. Memory pointer = PC, SP (16bit)

6. Flags :- S, C, P, AC, Z

7. Each memory location contain 8bit

* Instruction classification

1. Arithmetic

2. Logical

3. Jump, Branch

} not dealing in 8085

In 8085 microprocessor; (Based on size class.)

* 1 Byte instruction

ADD A,B If both the operands are registers then the instruction
SUB B

is 1Byte.

CM^A

MOV A,B
dest reg source

2 Byte instruction

ADI A, 50H Immediate
 ↓ one operand is always register
 Last is I, then 2nd operand is immediate

ADI A	1st
50H	2nd. byte.

3 Byte instruction

LDA 2050H 2nd operand is memory location or any 16 bit address. Loading to memory pair.
 Last is A, then the first operand is accumulator.

STA 2050H Store from Acc. to memory location (2050H)

JMP 2050H Because we have memory location,

* A → Accumulator.

I → Immediate

X → Register pair.

Reg. Pair

BC
DE
HL
AF

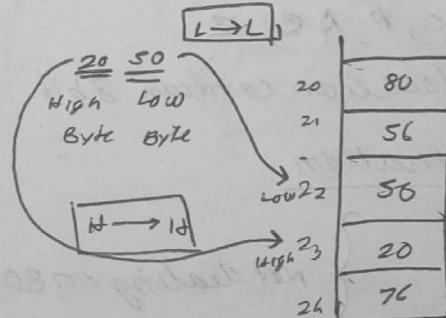
Eg: LXI D, 2060H }
 LXI H, 2080H }

3 Byte instruction.

*/ ADD B - 80H

LXI H, 2050H - 56 2050

HLT - 76



memory is twisted.

Addressing mode

1. Immediate addressing mode.

value of operand directly available in the instruction.

ADI A, 20H

LXI B, 2050H

2. Register addressing mode

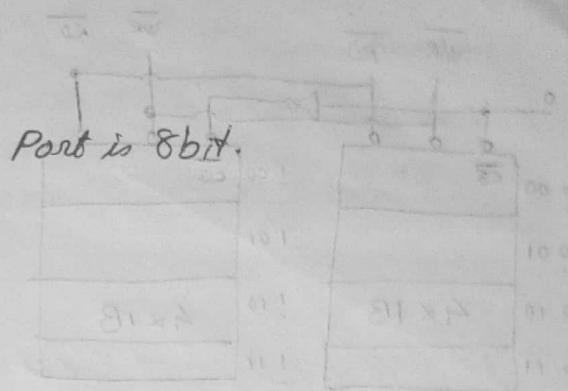
ADD A, C

3. Direct Addressing

LDA 2066M
memory location

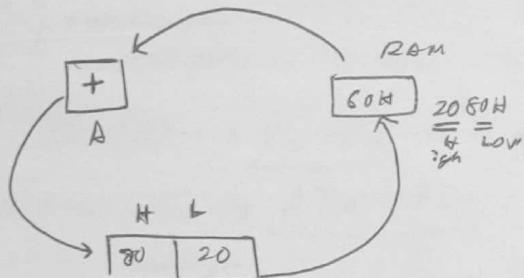
OUT 021H
Acc → Port 02H

IN 03H
Port 03H → Acc.



- Eg. LDA 2050H → Here, this is a memory loc. and hence direct add.
when I written ⇒ location
- LXI D 2050H → This is a memory value and not location ⇒ immediate add.
when I written ⇒ value

4. Indirect Addressing mode



A port (8bit) has some external device attached to it.

In between a reg. pair, HL is there which contains add. of memory location 02 part number.

ADD M
↳ here this is not a resistor.

31/7/19

* Virtual memory

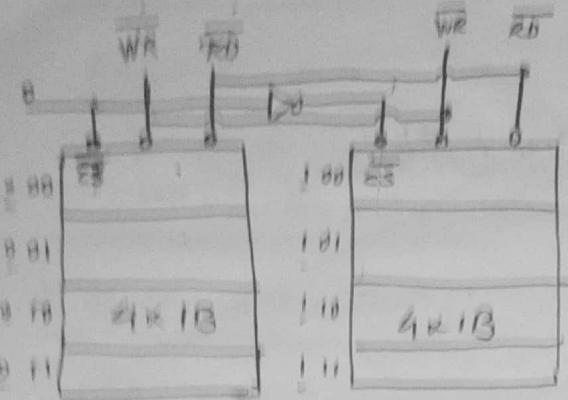
- a. write a program to add 2 numbers (immediate value) then after the result is sent to O/P port 01 and move the result to memory loc. 2050

solt-

```

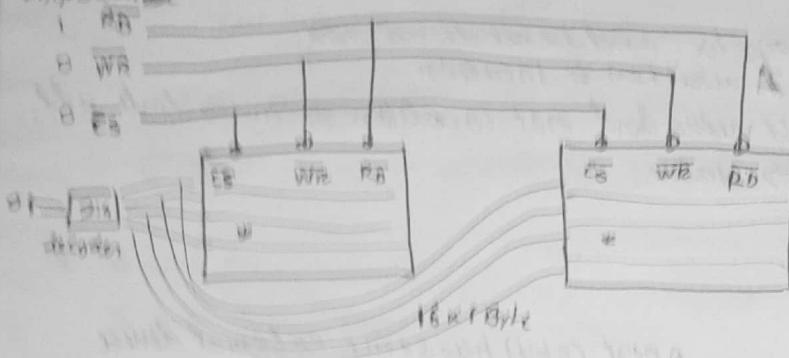
MVI A, 05H
ADI A, 03H
OUT 01H
STA 2050H
HLT
    
```

MVI B, 03H
ADD B



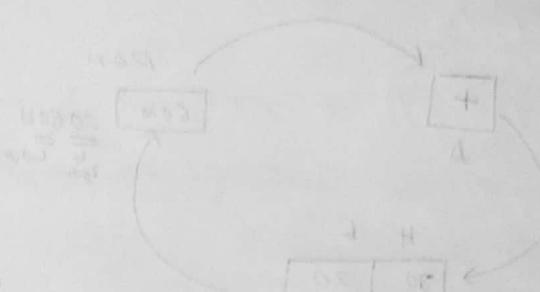
8K IB

chip select



Both are selected at the same time.

- i) Address bus
- ii) Data bus
- iii) System bus control



Q/8/m

Q. Suppose 2 operands are saved in 2 locations, 2050H & 2051H
^(by default)
 The size of operands are 1 byte each. Write a program to add these two numbers and save the ~~result~~ result in memory location 2052H.

Solⁿ.

LDA 2050H	(8byte instn)
MOV B,A	
LDA 2051H	
ADD B	
STA 2052H	(3byte instn)
HLT / RST 0	

Using memory,

LDA 2050H

LXI H, 2051H (also HL resistor pair)

ADD M (goes to HL resistor pair to get the address value)

STA 2052H

HLT / RST 0



Q. Suppose 10 elements are stored from starting address 2050H. Write a program to increment every value by 1 and save it in same location.

~~LDA 2050H
ENR A
ADI A, 01H
STA 2050H~~

LXI H, 2050H
INR M
INX H
INR M

LDA 2050H
ADI A, 01H
STA 2050H

These steps need to be repeated twice for 2 elements.

when 2 elements available and we need to increment them can be done in 4 steps

6/8/19

*Explanation of pins in 85

40 no. of pins {
 • data pin
 • address pin
 • control pin

→ Data pins (8) → D₀ - D₇ — Bidirectional microprocessor ↔ memory

→ Address pins (16) → A₀ - A₇, A₈ - A₁₅ → unidirectional from microprocessor → memory
 ↑ add-length

* Lower byte address bus is multitasking. In one clock cycle they may act as data pins and in the next, they act as address pins.

→ Control and status signals (6)

- ALE (Address Latch Enable)

(to separate address bus & data bus)

↗ 26 → data } i/p signal to control ALE
 ↑ → address }

• RD {
 • input
 • microprocessor
 works when input bit is low

• WR {
 • output
 • microprocessor
 works when input bit is low.

• IO / M (memory)
 ↓
 ↓
 0

Eg: Memory read

RD = 0 } MEMR = 0
IO/M = 0

Memory write

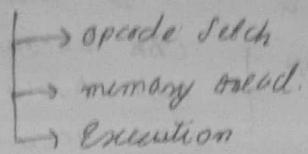
WR = 0 } MEMW = 0
IO/M = 0

• So, SI

Instⁿ → collection of machine cycles.

Eg: ADD B has 3 MC cycles

Done along with T0/T1
Specify which machine cycle is in operation



→ Power supply and clock frequency

Vcc, Vss

CLK (OUT)

Generate clock for other devices to maintain speed with the microprocessor.

X1 } 12 MHz.
X2 }

Specify the clock to be given to the microprocessor.

If we want 6MHz, we must give 12MHz

13/8/19

* Externally initiated signals including Interruptions

11 pins - Interrupt

Microprocessor

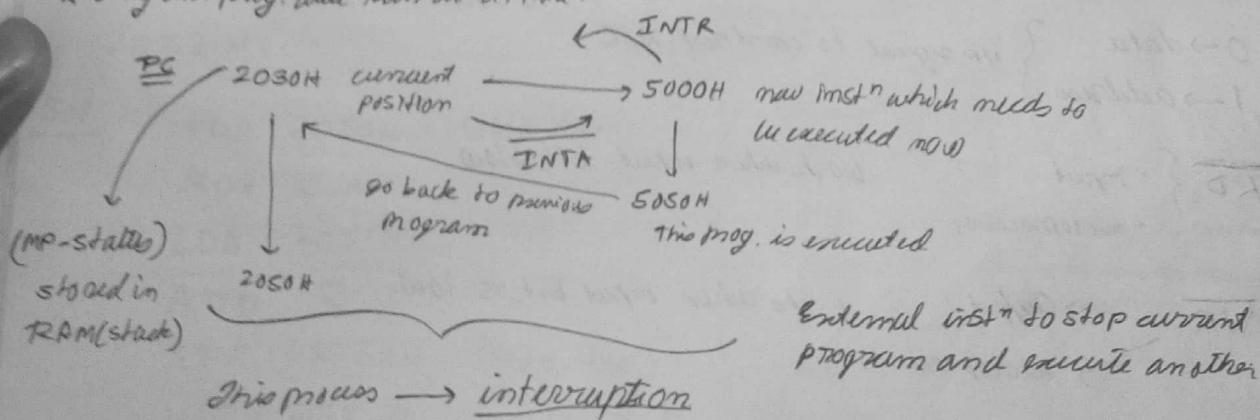
↓ to execute a program.

PC

2000H - 2050H (HLT/RST 0) Read to stop the program.

otherwise it will reach the last location, FFFF

* Only one prog. will run at a time.



If "Enable Int." then program can be interrupted.

Interrupt Request (INTR) is sent by new program to interrupt (to MP)

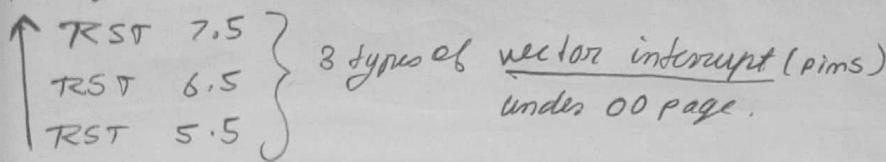
INTA → Interrupt Acknowledge bar.

(MP → Status) → stored in stack of RAM

Interrupt

- Vectorized (location of jumping loc. is fixed)
- Non-vector / Software Interrupt.

Priority



[INTR → RST 7.5]
The interrupted program
is stored in RST 7.5.

- * If RST 7.5 & RST 6.5 both contain interrupts, then we execute the one with higher priority

#

Interrupt

Maskable

RST 7.5
RST 6.5
RST 5.5

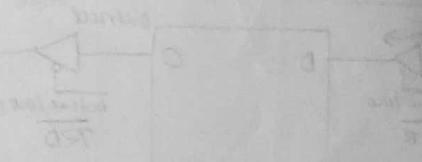
Non Maskable

TRAP

In case of situations like power failure, such interrupt is called TRAP

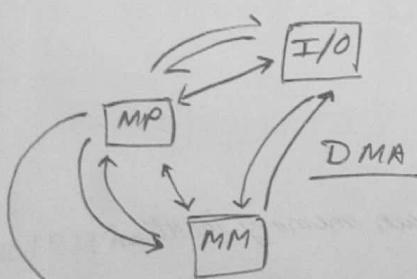
- * READY → Used to make sequence with the I/O device.
(In this case the MP leaves certain cycles blank. The clock keeps running.)

110 ————— 01
blank.



DMA Direct Memory Access

Directly access memory by I/O devices with the involvement of microprocessor.



→ Release Bus : - gives control to I/O devices to access & manipulate memory (releases for a certain time interval)

HOLD → request to MP from device to release the bus

HLDA → instruction from MP regarding release of bus.

RESET IN - resets the MP by releasing info from registers, Acc, flags.

RESET OUT - MP gives info that it has been reset externally.
signal to device.

* Serial communication

SOD - Serial Output Data

SID - Serial Input Data

Tri-State Buffer → Associates with input device

Before any data is transferred to MP, the TSB checks whether the data from input device is valid or not.

Latch - Holding the data which is for output devices.

Eg:

Keyboard → Tri-state → MP
buffer

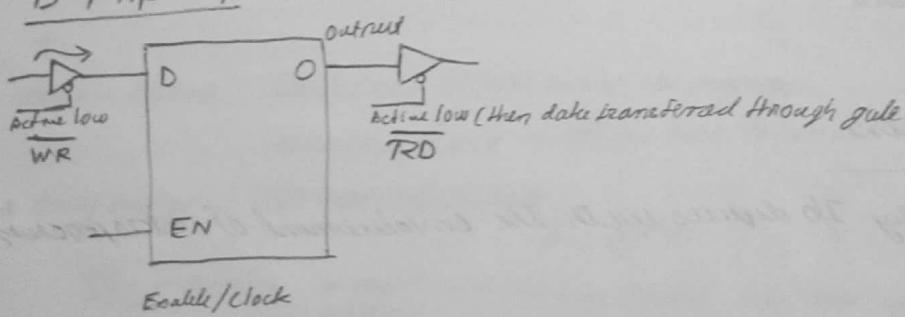
Eg:

MP → Latch → Printer

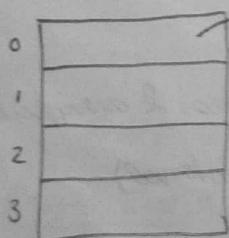
14/8/19

Flip flop / Latch / Memory unit

D-Flip Flop



#



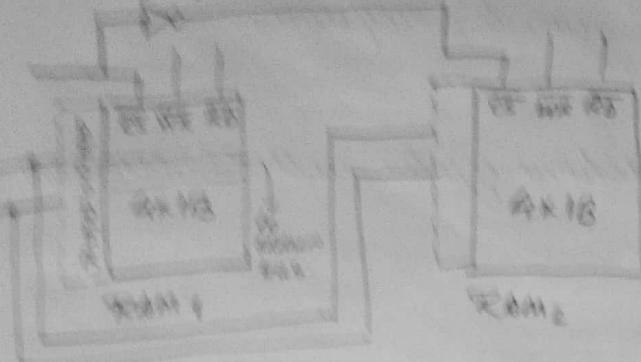
2 bits required to represent each memory location.

Word length - no. of bits in a memory component.

4B
111
 $4 \times 1B$

\overline{CS} (select) is present in each register.

* RAM is very expensive so we do not use it.

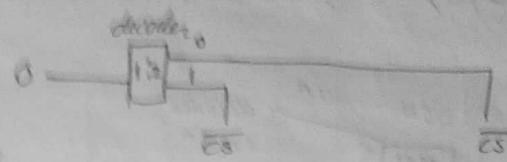


if both RAMs are selected

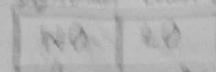
0 → RAM 1 selected

1 → RAM 2 selected.

For CS we can also use decoder.



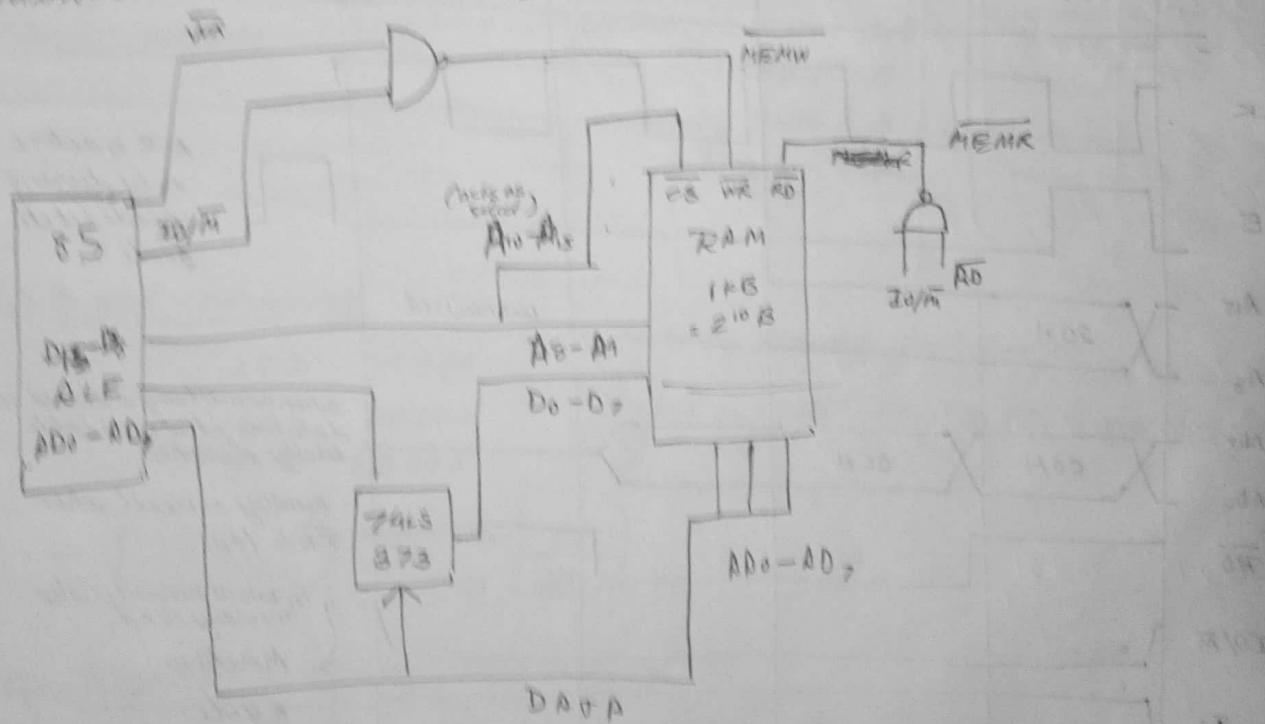
decoder from input.



chip select location select

Q. Design a 16 bit word length RAM using 4x1B, 4x1B

Q. Interface a RAM (1KB size) with 8085 microprocessor.



20/8/19

Timing Diagram

Any instruction is collection of small machine cycles.

e.g. opcode fetch, mem. read, mem. write, I/O read, I/O write.

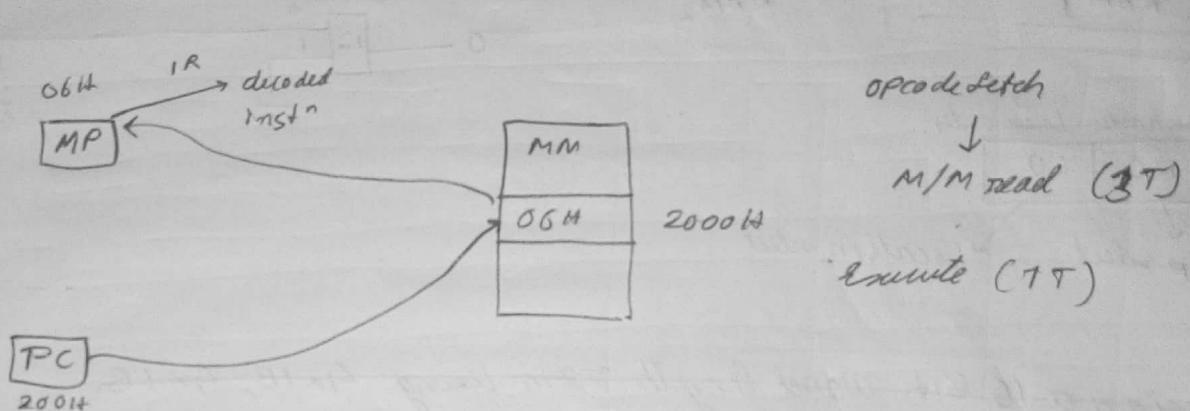
Any instruction always starts with opcode fetch machine cycle. After that based on the instruction time, if regd.

other machine cycles are required to execute. Each and every

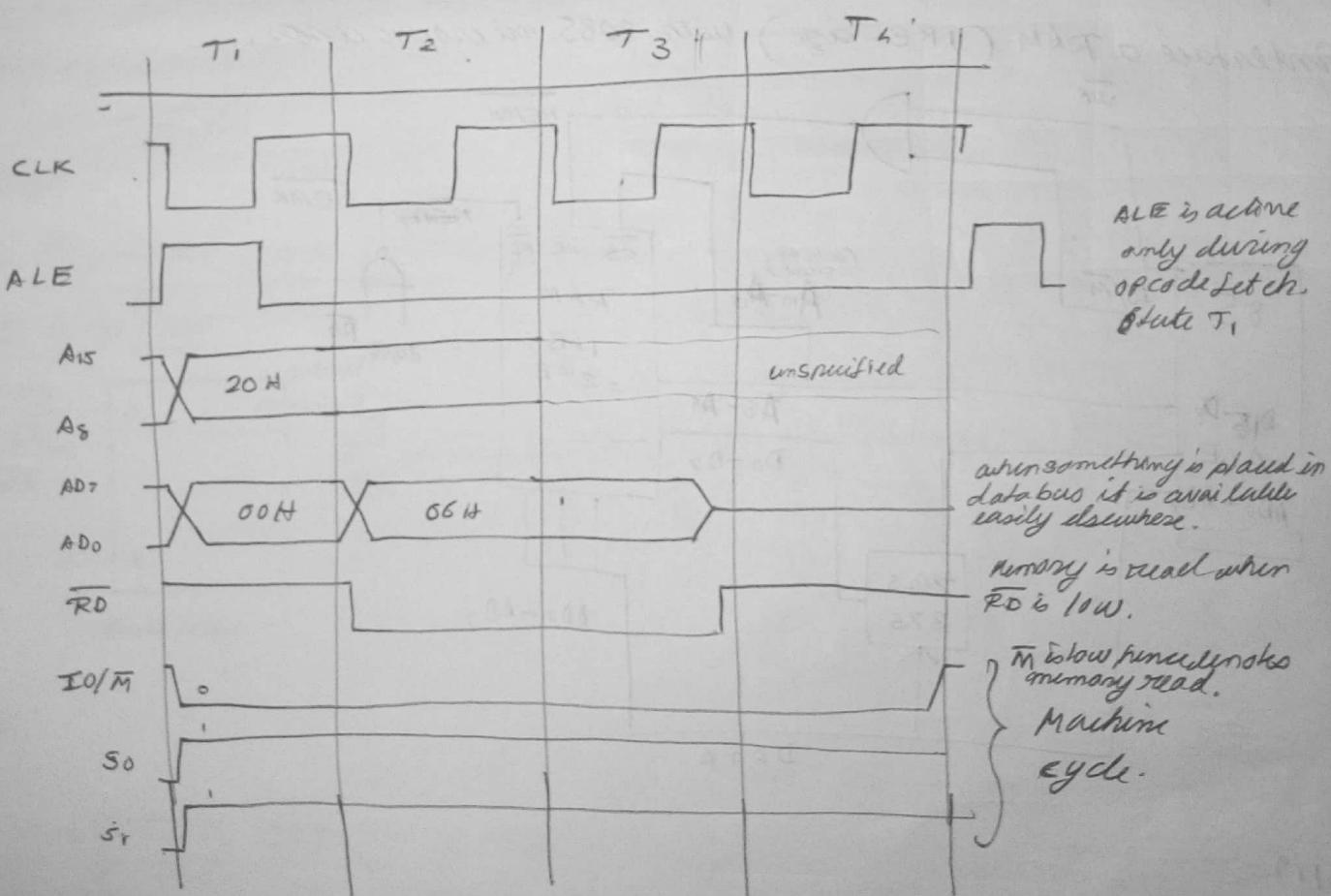
machine cycle having specified no. of T states.

Eg: opcode fetch, mem read, mem write requires
4, 3, 3 states.

Microprocessor identifies the machine cycles with combinations
of $I/O/M$, S_0, S_1 , pin value.



opcode fetch
↓
 M/M read (3T)
execute (1T)



011 → denotes opcode fetch.

AD1 B, 0111
2 byte instn

SO, SI → 1, 0

MM	
ADT B	100011
01W	200111

For 2 byte instruction,
the cycles are: op code fetch (3)
memory read (1)

4T

But in 1 byte instrn, the mem. is read within the op code fetch cycle.

(Tutorial) 20/8/19

* Addressing:

i) Immediate addressing mode:-

"Instn" "data" source

MVI A, 04H
LXI H, 3050H (3050H is loaded to HL register)
 PAIR
JMP 8000H

ii) Register addressing

both source & dest are registers.

MOV A,B ← { MVI B, 04H }
ADD B
INR A
INR H

iii) Direct addressing

LDA 2050H

content is directly loaded to acc.

LHLD 2050H

content is loaded directly to HL pair.

STA 8080H



HSO TWO

iv) Register indirect addressing

MOV A,M content of M is stored in acc.

LDAX B

LXI H 9570 (diff than LXI H 9570)

v) Implicit addressing

CMA (complement the acc.)

RRC

RLC

Q. Draw the timing diagram of MV1B,32H

Ans: MV1B,32H → 2 byte instrn

Let MV1B → 2000 H
(address)

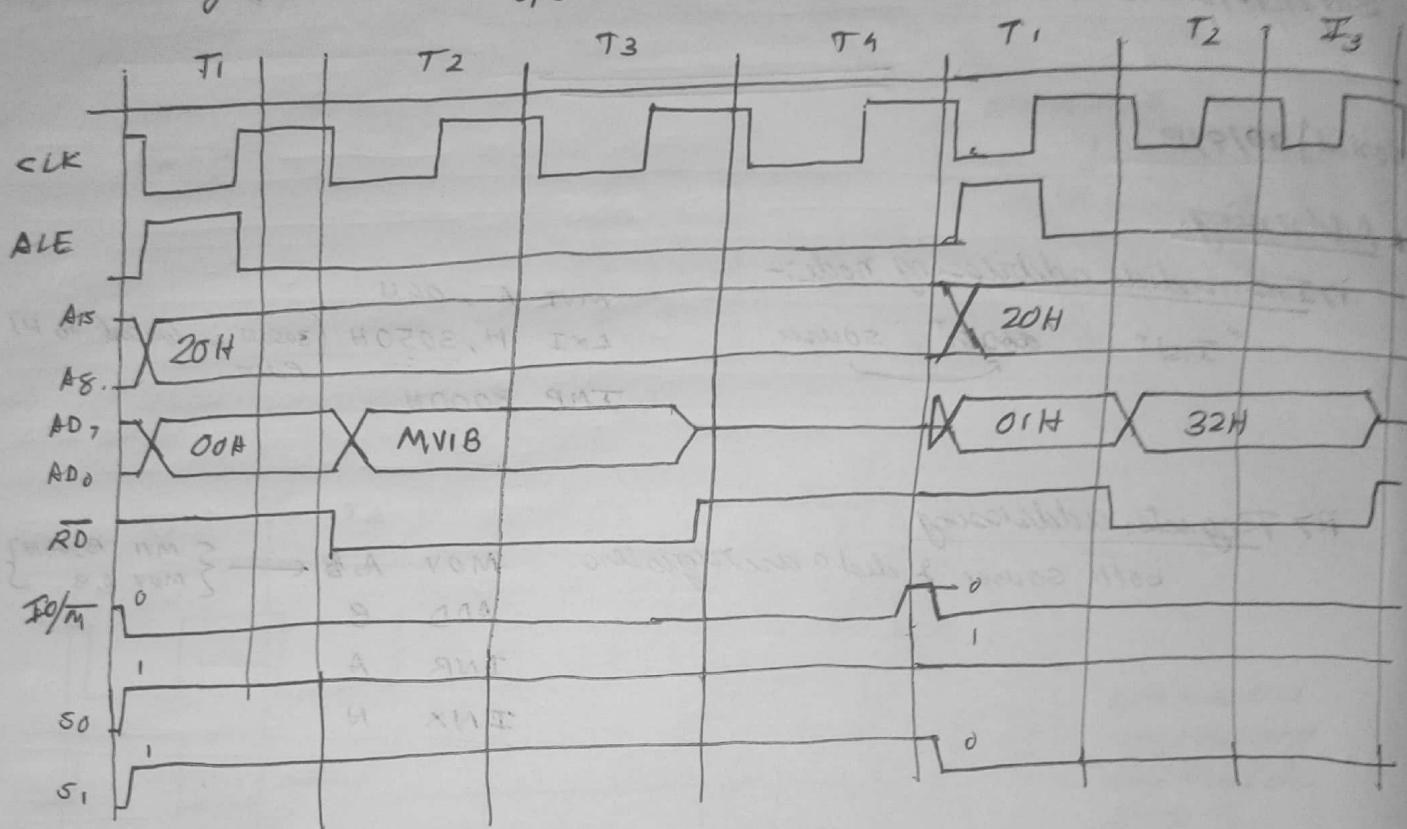
Machine cycles,

i) Opcode fetch

ii) Memory read.

Opcode fetch

Memory read



2nd & 3rd state performs mem. read operation in all cases (machine cycles).

ALE gets activated in case of any machine cycle.

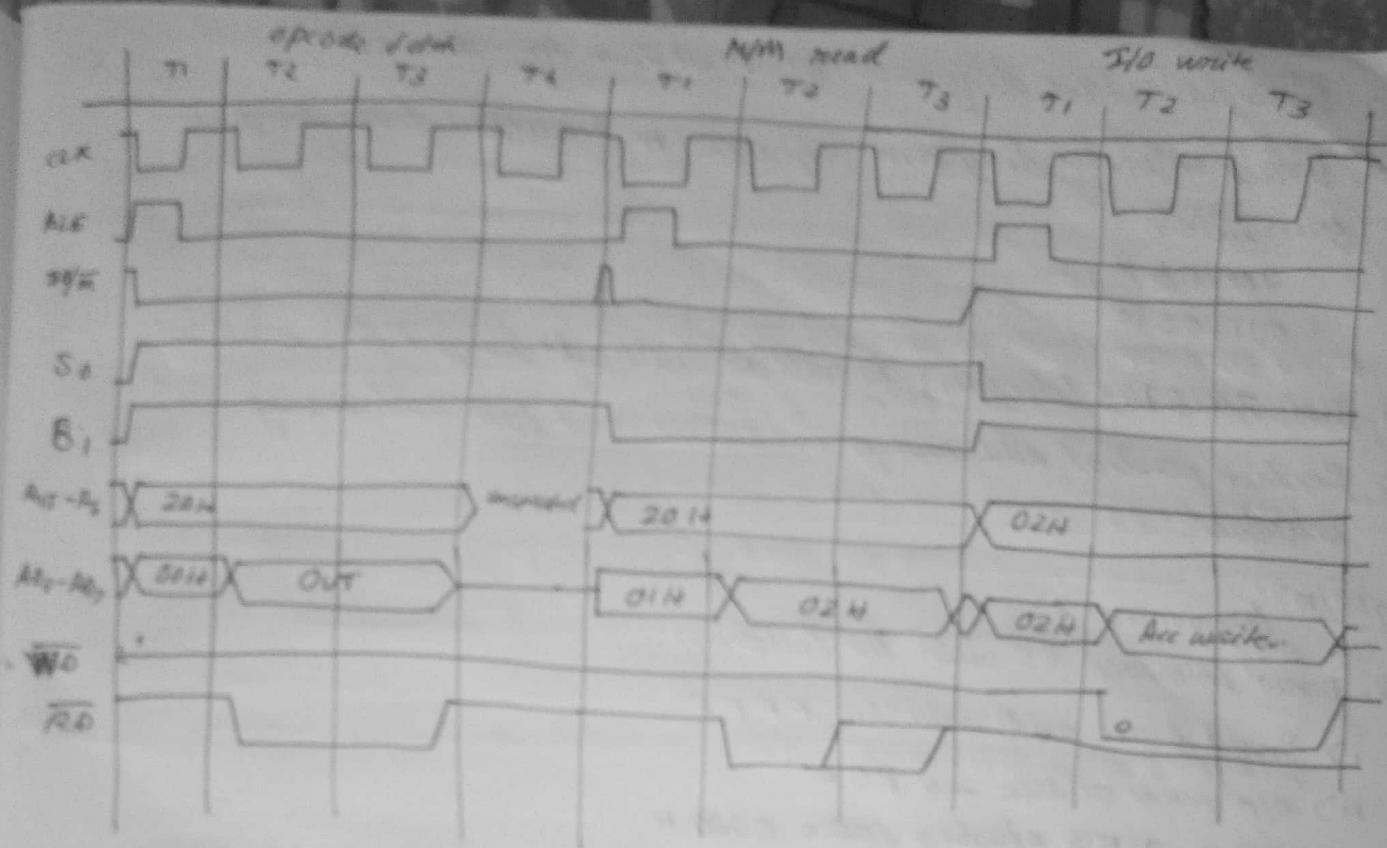
OUT 02H

↓
8bit instruction.



we need two cases where we need to read memory. Once during opcode fetch and other during mem read.

The data in the acc. is sent to port 02H through the bus.



Assignment

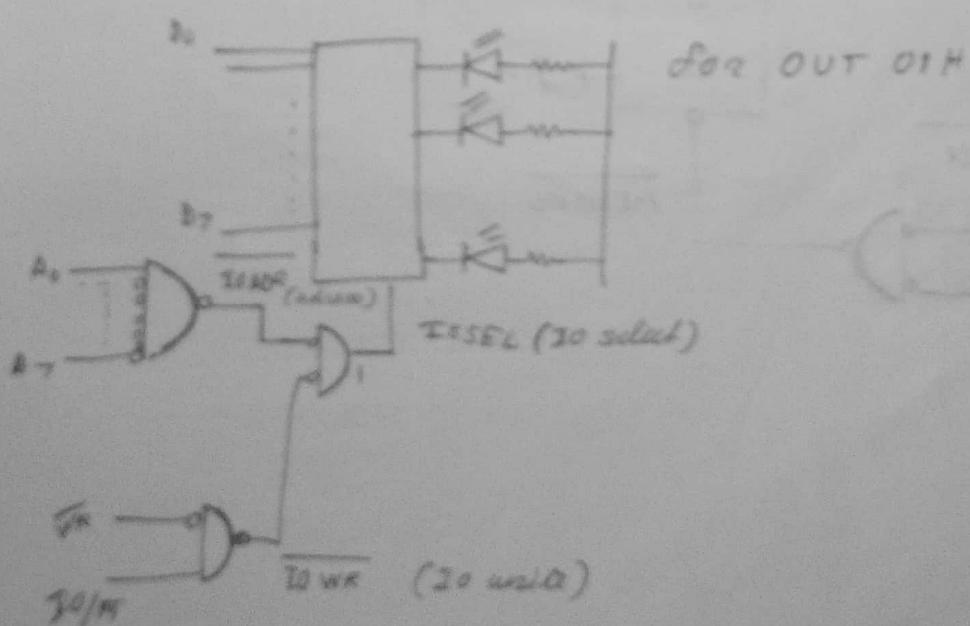
LDA 2050

STA 2050

Explain the meaning of memory mapped I/O and peripheral mapped I/O

2/8/19

* I/O Interfacing



- Draw interface diagram of input device for IN 01H
- Q. Draw interface diagram of input & output devices for given instruction
 IN 04H
 OUT 03H

- Q. Use 74LS143 (decoder) as well as with ORB using it.
- Q. Explain partial addressing interface and full addressing interface.

27/8/19 (Assignment 2)

- Q. Draw interface 85 with the following:

i) Input device with address FFFF

ii) O/R device address \rightarrow F0H

iii) RAM, 1 KB starting from 0000 H

iv) ROM, 1 KB starting from F000H

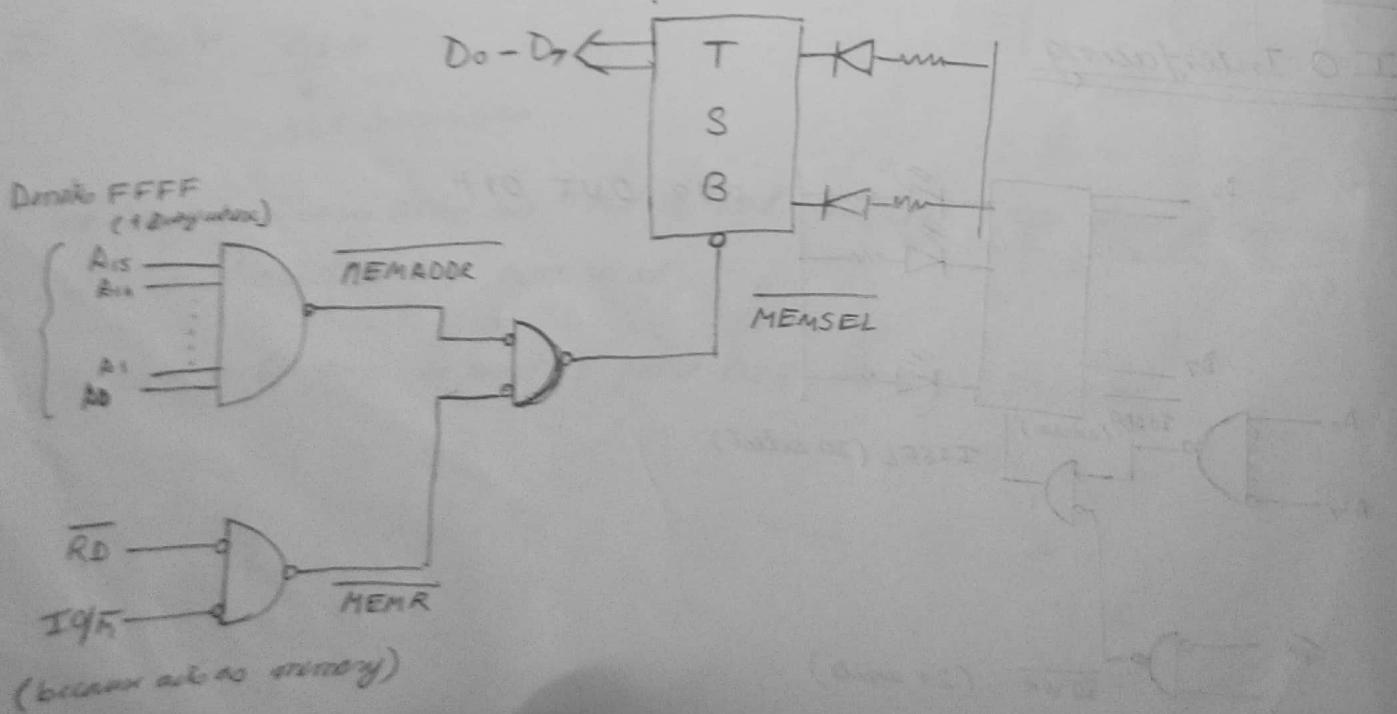
Memory interfacing

MEMSEL, MEMW/MEMR,
MEMADDR

I/O interfacing

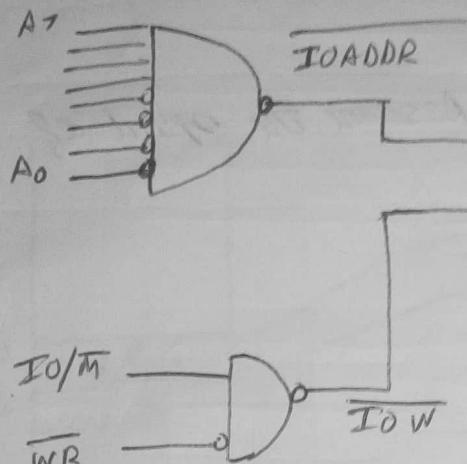
IOSSEL (only in case of latch)
IOSSEL, IOW / IOR,
IORDDR

i) How I/O acts as memory because we are dealing with 16 bit add. and hence mem. mapped I/O.



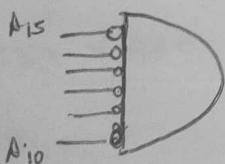
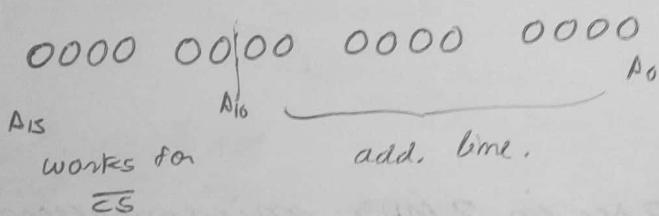
ii>

(denote FON)



IOSEL (no bar reqd. for Latch)

iii> 2^{10} B RAM \rightarrow 1KB RAM , 0000 H



28/8/19

Q. MVI C, OFH

label(L0): DCR C

JNZ L0



Find the time need. to complete the program. Assume the speed of the microprocessor is 2MHz.

Sol^r. $7T$ ($4+3$) \longrightarrow MVI C, OFH

$4T$ \longrightarrow L0: DCR C

$10T/7T$ \longrightarrow JNZ L0

$$7T + (4T \times 15) + (14 \times 10T) + 7T$$

$$= 7T + 60T + 140T + 7T$$

$$= 214T$$

Q. Make a delay function for ~~3sec~~ 3sec in 2MHz microprocessor.

Sol^r. For initial value of C $\rightarrow x$

3 sec delay

$$f = 2 \times 10^6 \text{ Hz}$$

$$T = 0.5 \times 10^{-6} \text{ sec}$$

(7T) MVI C, OFH
 (4T) L0: DCR C
 (10T/7T) JNZ L0

For $7T \rightarrow 0.5 \times 10^{-6} \text{ sec}$

$\rightarrow P \text{ sec}$

$$P \times T'_{\text{tot}} = 3$$

$$T'_{\text{tot}} = \frac{3}{P}$$

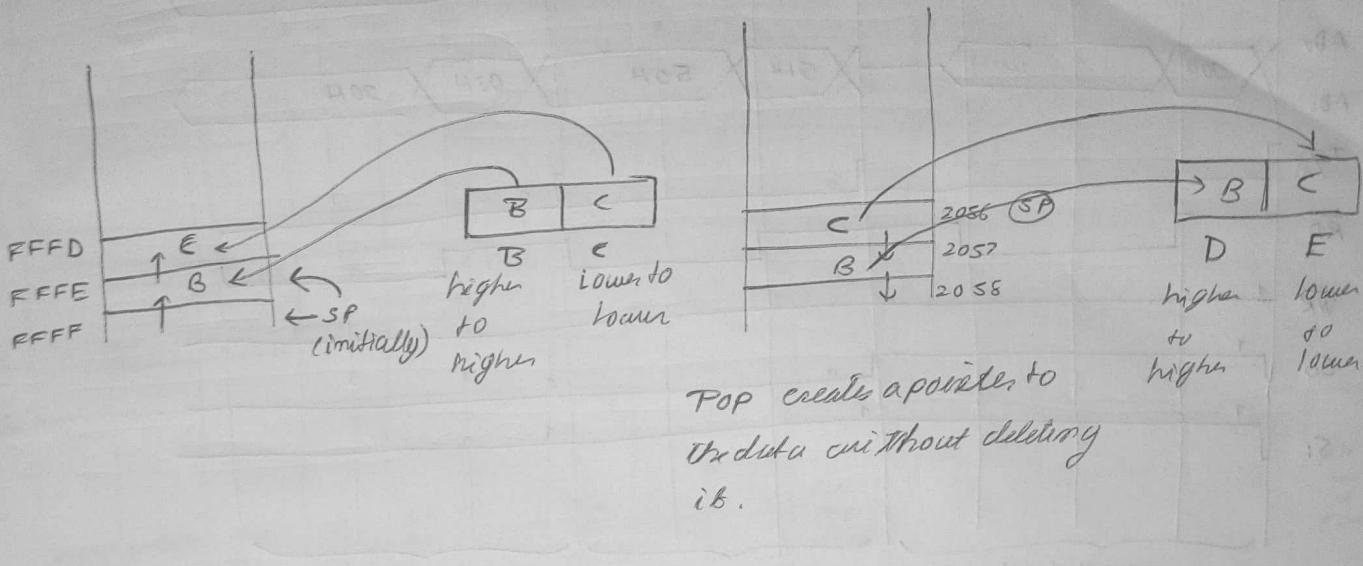
$$3 = 0.5 \times 10^{-6} \times x$$

$$\Rightarrow x = 6 \times 10^6 \text{ Ans}$$

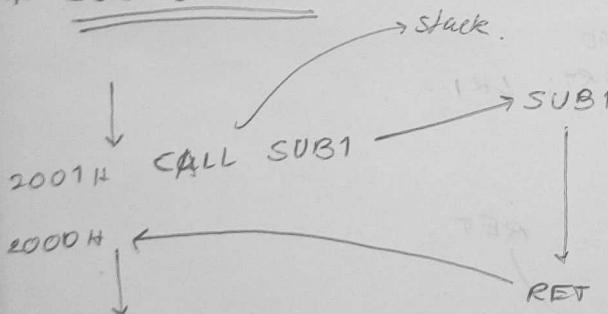
$$T'_{\text{tot}} - 7T \leq T''$$

* PUSH and POP in 8085 microprocessor

PUSH B ← Decrement; move
 POP D ← Move; Increment.



* Subroutine

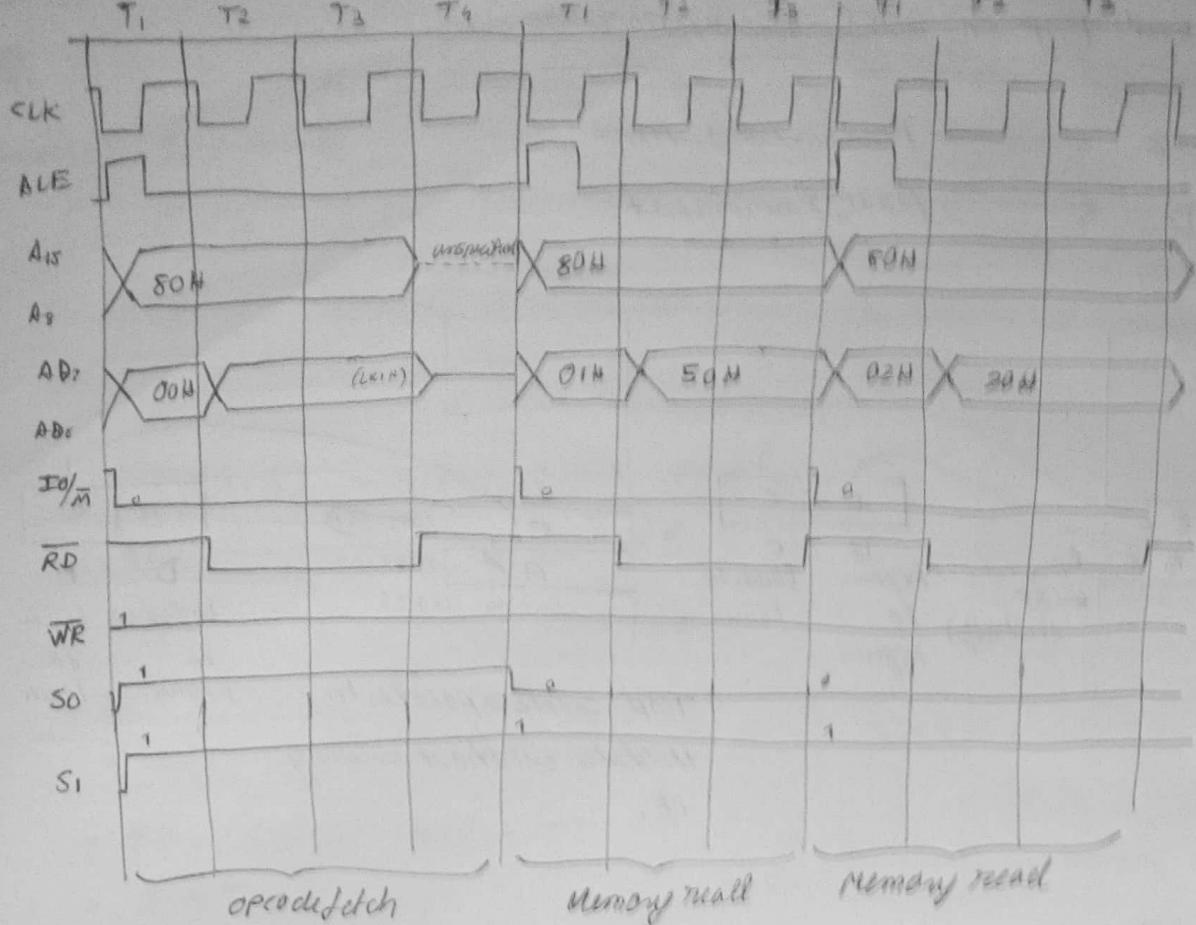


29/8/19

- Q1. Write a program to explain how subroutine calls are performed.
 Q2. Draw the timing diagram of LXI 2050H.

SOLN - LXI 2050H

Timing cycles → 4T + 3T + 3T = 10T
 ↑
 opcode
 fetch



Solⁿ1:-

MAIN: LXI ..

:

PUSH B

PUSH D

PUSH N

PUSH PSW

CALL 2040

POP PSW

POP R

POP D

POP B

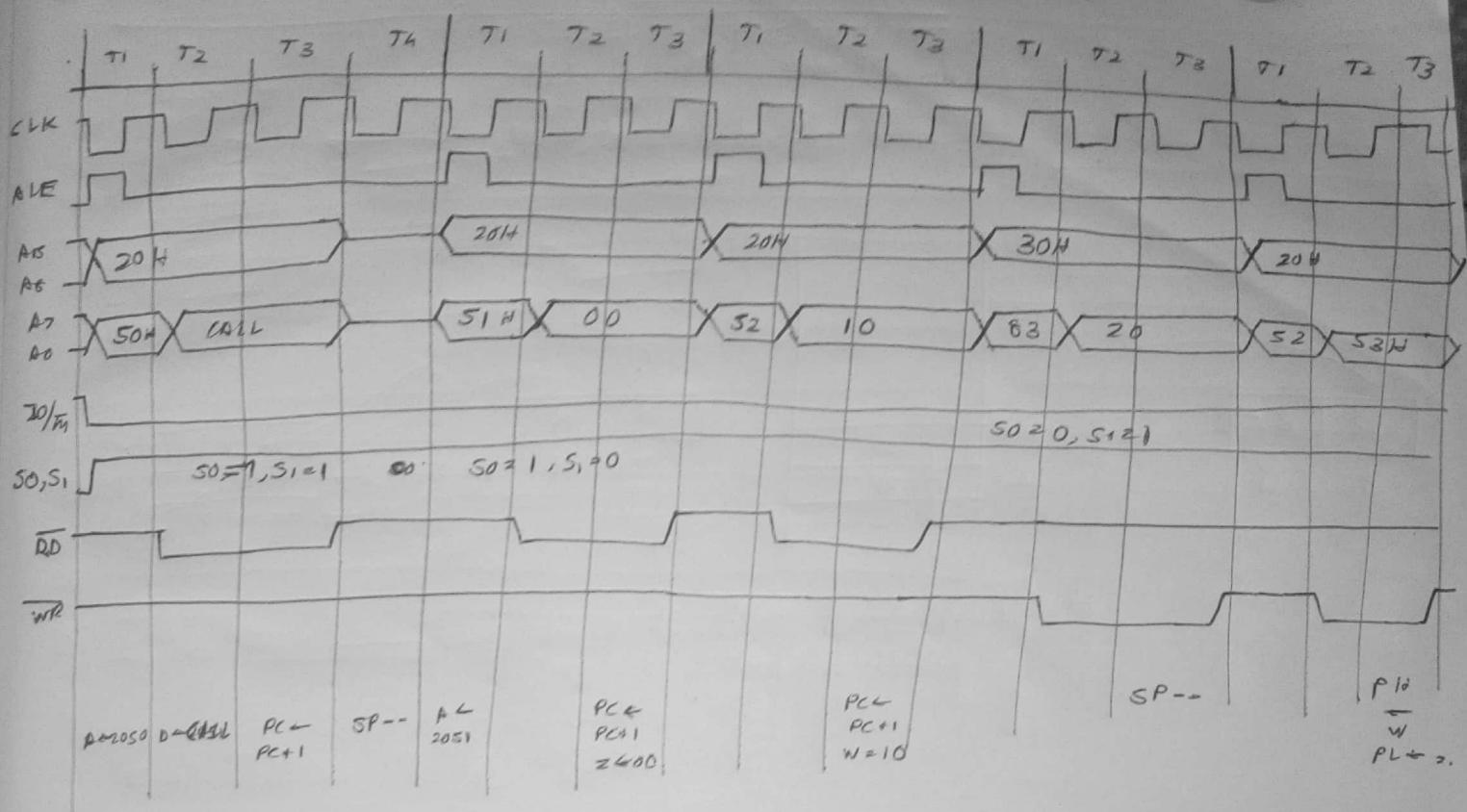
2040
SQRRT: LXI ..

RET

★ Time cycles for CALL 2040

- 1000 1. Opcode fetch
- 1001 2. Memory read (80)
- 1002 3. Memory read (20)
- A. SP \leftarrow 03
- E. SP \leftarrow 10

* Timing diagram for CALL instruction



CALL 1000

$$\left\{ \begin{array}{l} 2050 \\ 2051 \\ 2052 \end{array} \right| \text{CALL} \left\{ \begin{array}{l} 00 \\ 10 \end{array} \right\}$$

SP ← 3054H

First decrement then write.