

Microprocessor

some Points:-

- i) Word length = 8 bit
- ii) Address length = 16 bit.
- iii) Memory size = 2^{16} .
- iv) Basic register = A, B, C, D, E, HL, CX
- v) Memory pointer = PC, stack pointer (SP) (16 bit)
- vi) Flags \rightarrow S, C, P, Ac, Z

Inst. Classification:-

(i) Arithmetic.

\rightarrow 1 Byte
ADD A, B if its register then
its 1 byte inst. size

(ii) Logical

SUB
CM^A

(iii) Jump, Branch

\rightarrow 2 Byte Size Inst.

AD I A, 50H Immediate
represents second operands as immediate

\rightarrow 3 Byte Size Inst

LDA 2050H
Stores the content of accumulator to memory location.
STA 2050H

I \rightarrow Immediate
A \rightarrow Accumulator
X \rightarrow Reg-pair

Register Pair

BC

DE

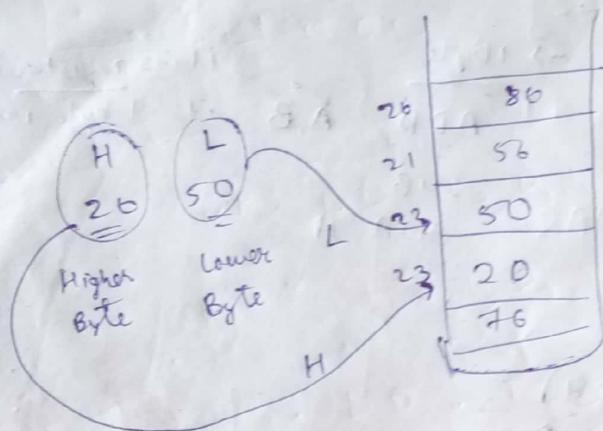
HL

AF

Ex: $LXI, D, 2050H$

$LXI, H, 2050H$

H



→ Little Endian

→ Big Endian

Addressing Mode

(i) Immediate Add. Mode

AD I A, 20H

LXI I B, 2050H

(ii) Reg. Add. Mode

ADD A, C

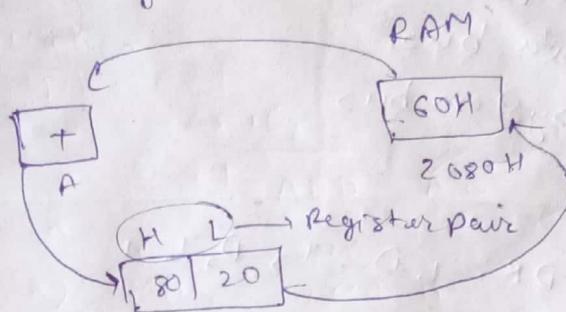
(iii) Direct Addressing Mode

→ M/M Port

LDA 2066 H
 ↑
 M/M
 OUT 02H
 AC → Port, 02H
 IN 03H

{ LXI - 2050H
 Difference LDA - 2050H

(iv) Indirect Addressing Mode:-



ADD M

$A \leftarrow A + M$
↓
Reg. Pair

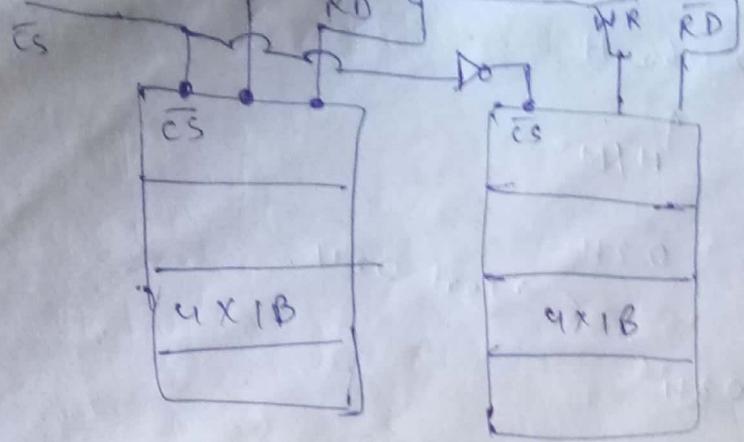
Virtual Memory:-

Write a program to add 2 nos (immediate values) then after the result is sent to output port ⁰¹ and then move the result to memory location 2050.

⇒ MVI A, 05H
 ADI A, 03H
 OUT 01H
 STA 2050 H
 HLT.

MVL B, 03H

ADD B



\Rightarrow Buses \rightarrow Behave as data carrier

Types

- \leftarrow Address bus
- \rightarrow Data bus
- \rightarrow System bus.

31-07-19

$$DR : LD = T_3 D_2 I_o +$$

$$R_1 : OE = T_3 D_2 I_o +$$

$$Acc : LD = T_4 D_2 I_o +$$

$$ALU : ADD = T_4 D_2 I_o +$$

$$SEQ\ CNTR, INCR = T_0 + T_1 + T_2 + T_3 D_2 I_o +$$

$$CLR = T_4 D_2 I_o +$$

MOV Acc, M

~~$DR : T_3 D_2 I_o$~~

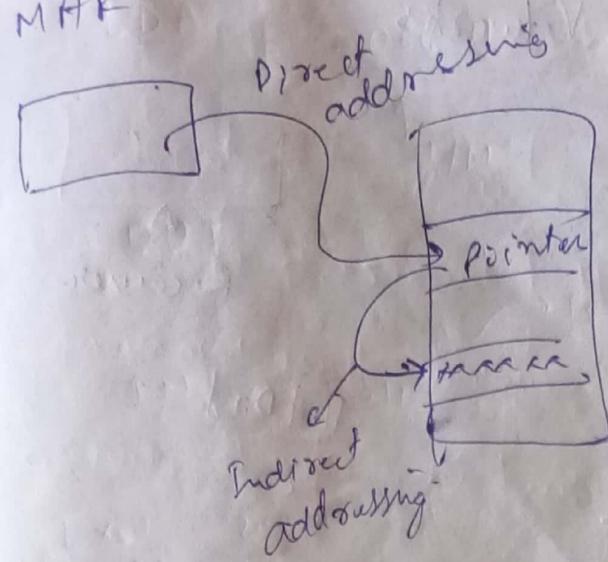
$$T_3 : Acc \leftarrow M[MAR]; T_0$$

$$Acc *: LD = T_4 D_2 I_o + T_3 D_1 +$$

SEQ CNTR

$$CLR = T_4 D_2 I_o + T_3 D_1 +$$

MAR



M OVI Acc, M

Acc. LD = T₃ D, I₁₅

⇒ Hardwired Control Unit Design:- (fast but not scalable)

⇒ Microprogrammed Control Unit Design (comp. to hardwired ctrl unit design) [Is scalable but requires control memory].

#

DNCR_{PC} - C₀

LD_{MAR} - C₀

OEP_{PC} - C₁

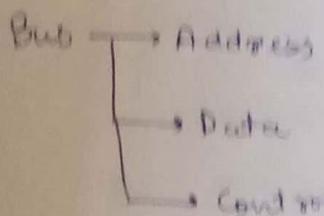
LD_{IR} - C₂

RD_M - C₃

DNCR_{PC} - C₄

OEI_{IR} - C₅

It holds the control words.



40 pins

- ① Data pins (8) → $[D_0 - D_7]$ → Bidirectional. ($MP \leftrightarrow M$)
- ② → Address pins (16) → $[AD_0 - AD_{15}]$, $A_{15} - A_1$ (unidirectional) ($MP \rightarrow M$)
- ③ → Control and Status Signals (6)

* ALE (Address Latch Enabled)

If the IOP bit is 0 then it's data else its address pins

behaves as

* \overline{RD} IOP
 Memory Op. Works when IOP bit is low.

* \overline{WR} OIP
 Memory Op. Works when IOP bit is high.

* $IO/M \rightarrow 0$
 ↓
 1.

* Memory read $\overline{RD} = 0$
 $IO/M = 0$ } $\overline{MEMR} = 0$

* Memory write $\overline{WR} = 0$
 $IO/M = 0$ } $\overline{MEMW} = 0$

* S_0, S_1
 ↓ Inst.

Its combination → collection of m/c cycle.

along with IO/M decides which machine cycle is being performed.

Ex ADD B

→ Op Code fetch
 Mem. read
 Exec.

④ Power Supply and Clock frequency

V_{cc} → Voltage Supply

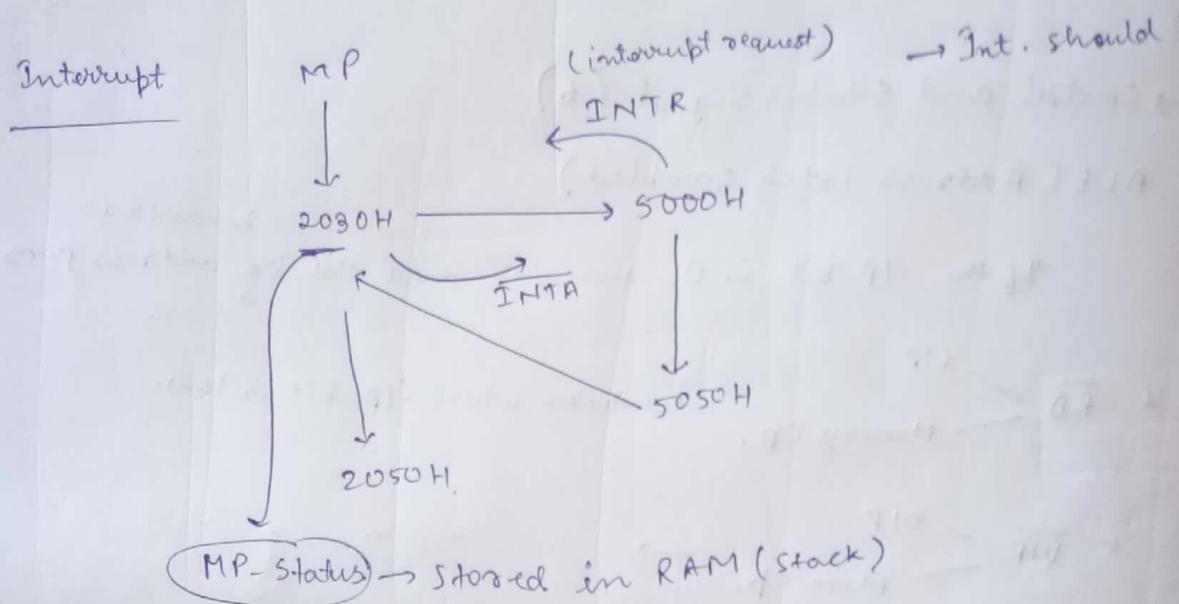
V_{ss} → Ground.

CLK (OUT) → Maintains the freq. of other devices.

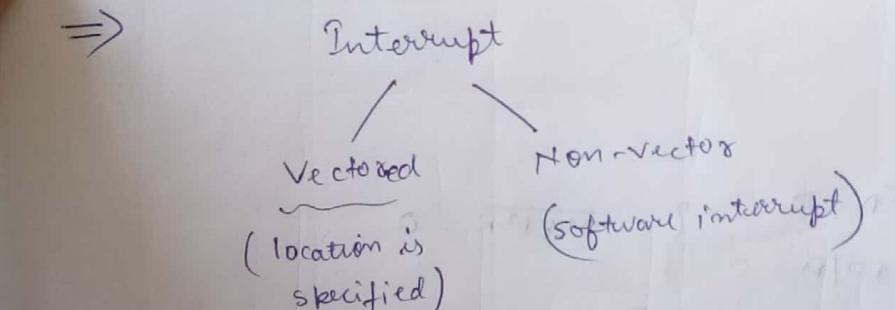
X_1

X_2

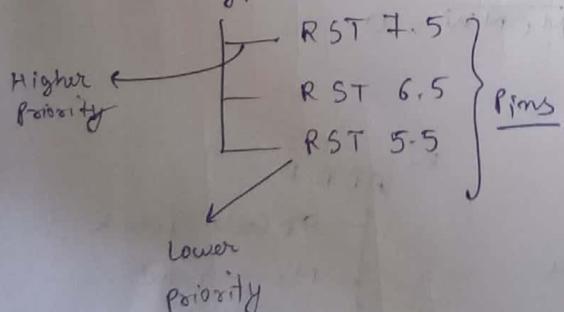
Externally Initiated Signals Including Interrupts (11)



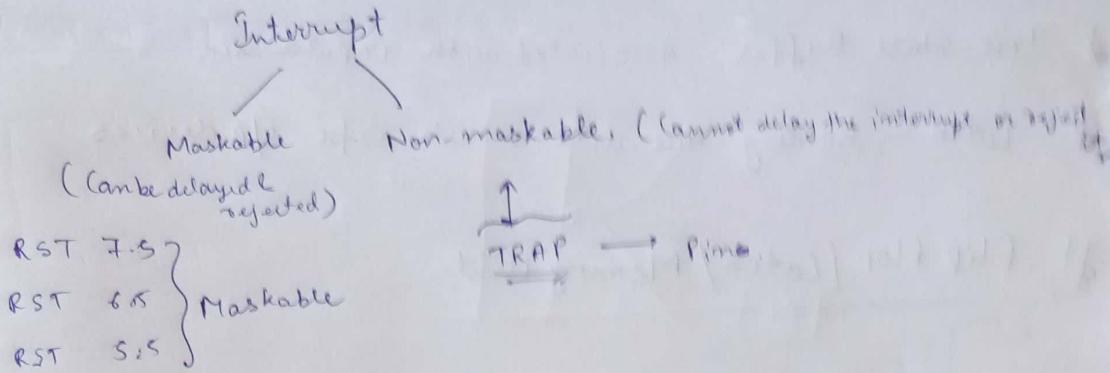
⇒



Types

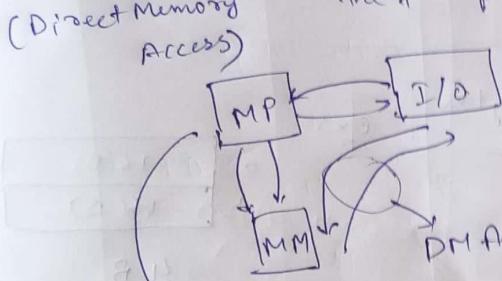


⇒



⇒ READ Y → This pin is used to make sequence with the other devices with the Microprocessor.

⇒ DMA → It allows the I/O devices to access the memory without the intervention of microprocessor in between



⇒ Releases bus (after this operation the I/O access the control of the bus in order to access the memory).

⇒ HOLD → request to MP from device to release the bus

⇒ HLDA → resp. from MP regarding release of bus

⇒ RESET IN → resets all the data in the MP

⇒ RESET OUT → gives signals to other devices that the MP is reset.

* Serial Communication

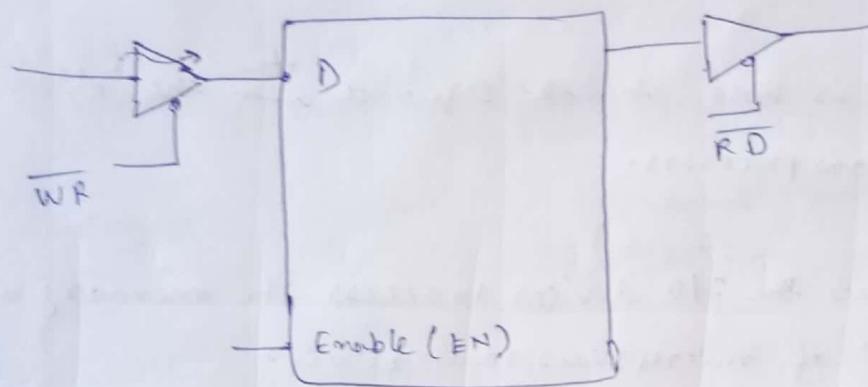
SID - serial i/p data

SOD → " o/p data,

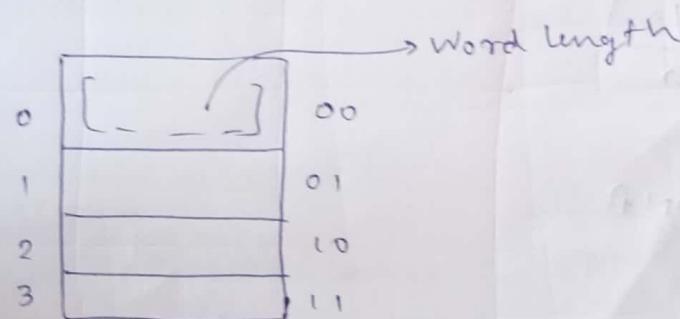
* Tri State Buffer:- Associated with input device.

* Latch - holding the data which is for o/p devices.

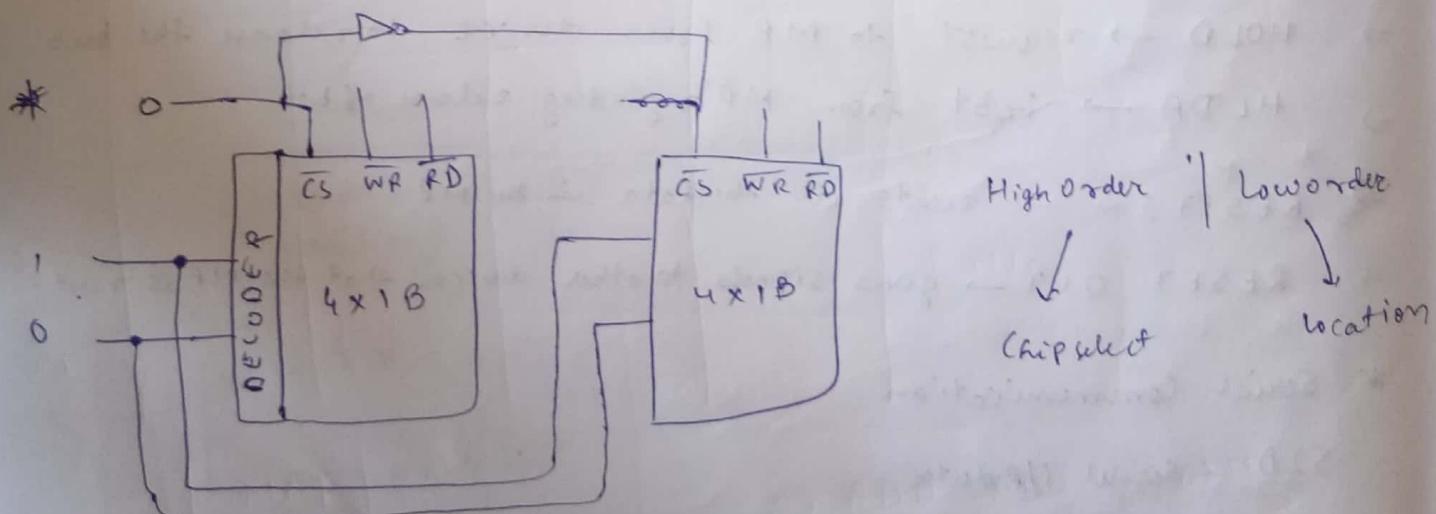
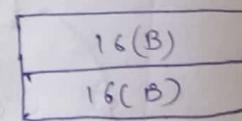
Flip flop / Latch / Memory Unit



=>



Ex:-

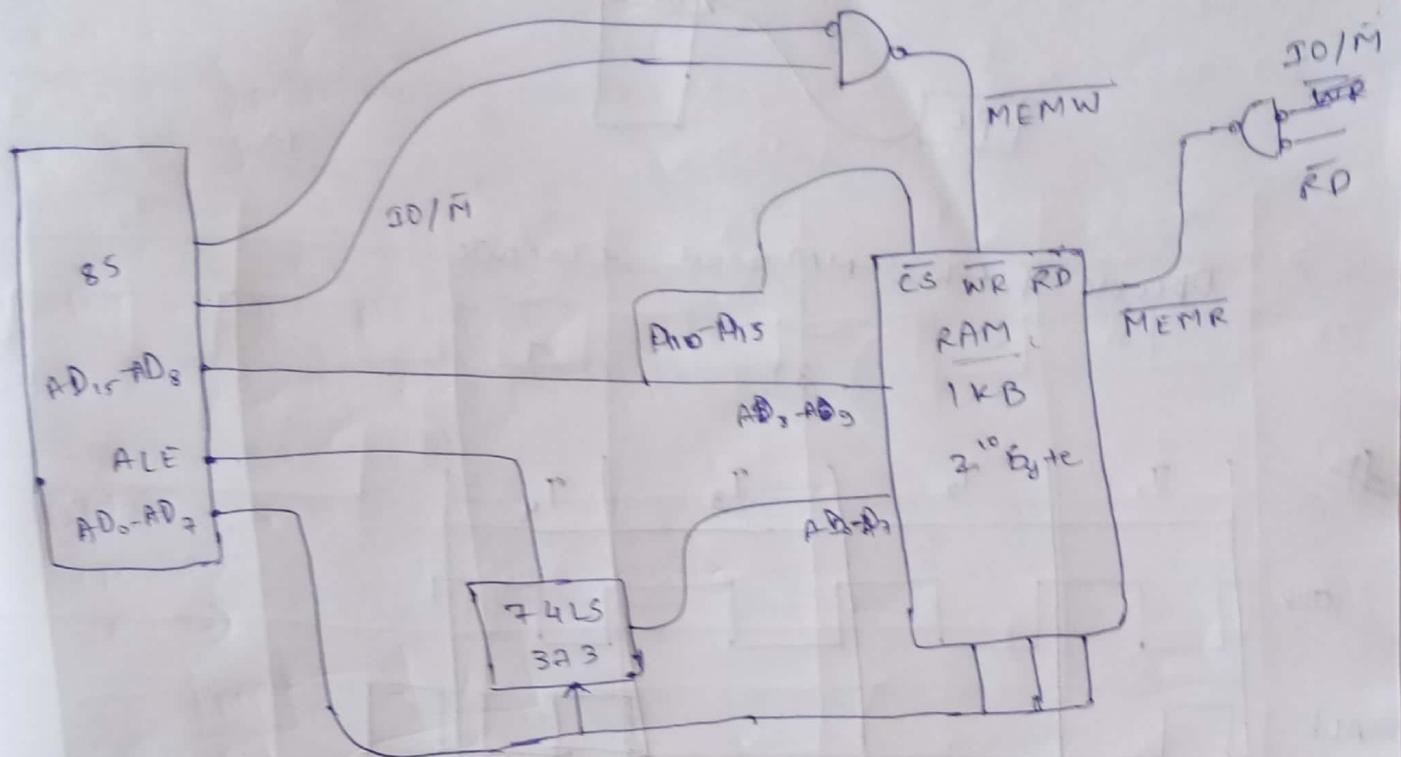


Chip select

High Order | Low Order
 ↓
 location

Design a 16 bit word length using $4 \times 1 B$

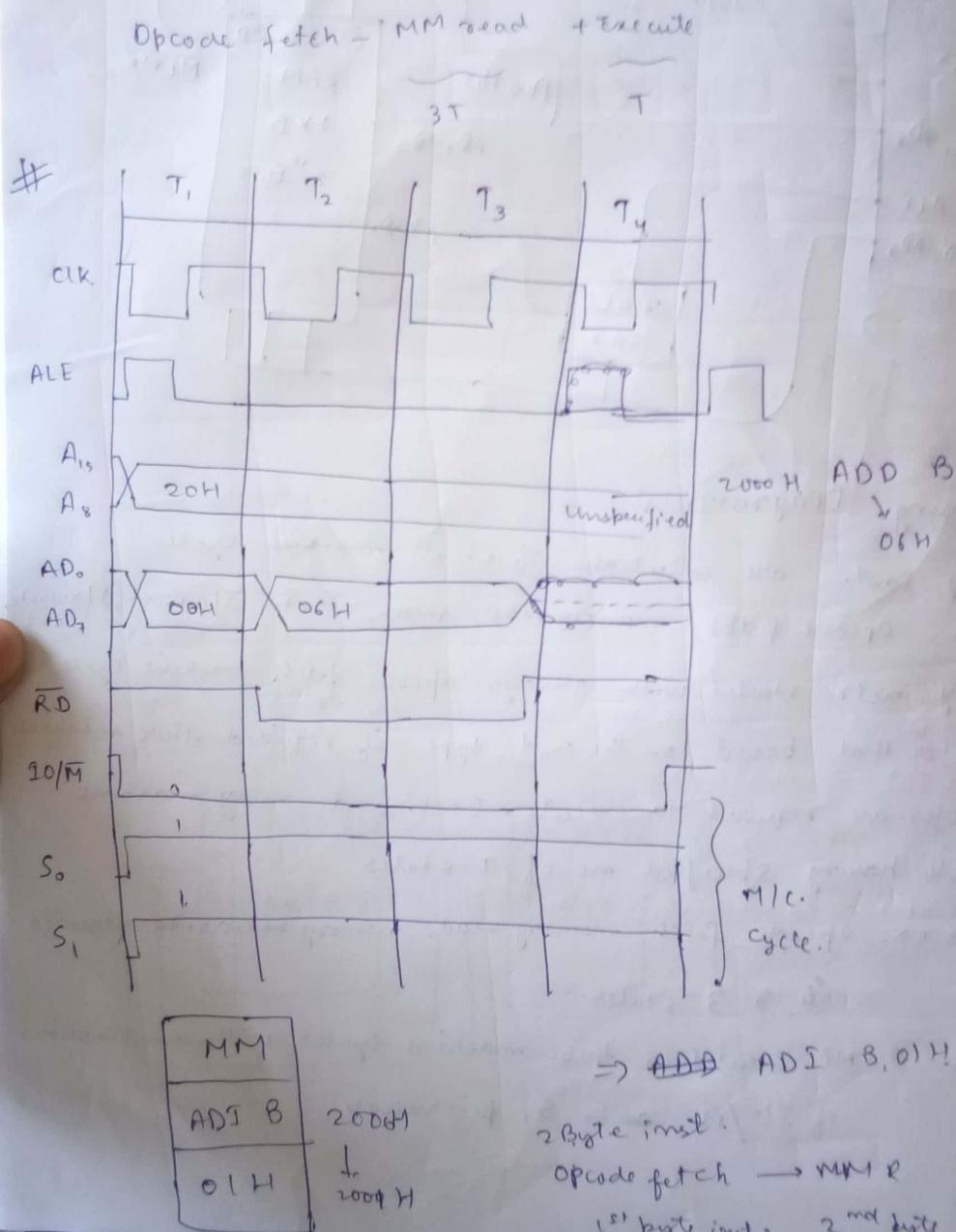
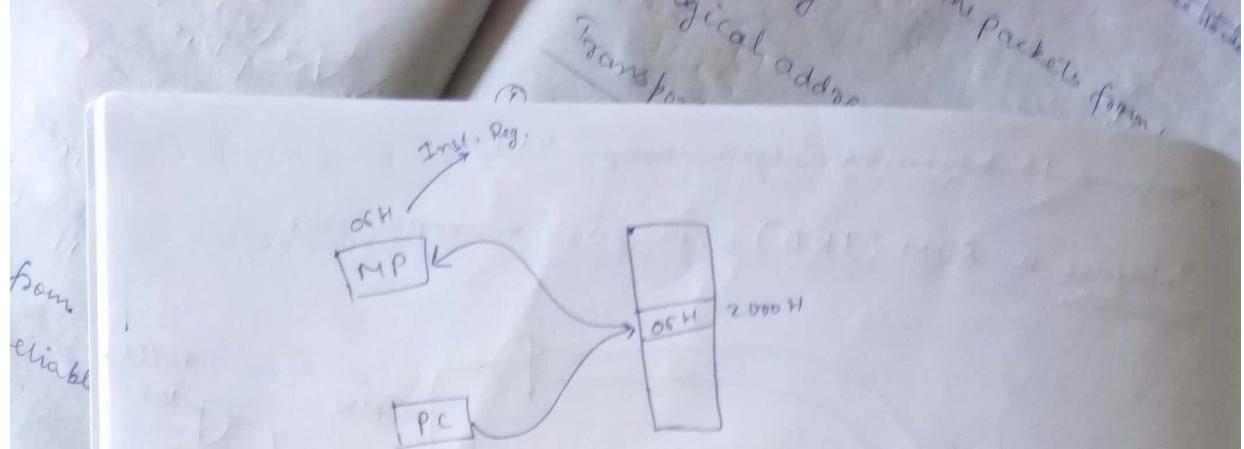
Interface a RAM (1KB) with 8085 microprocessor.



Timing Diagram:

- Any inst. are collections of small machine cycle.
Ex. Opcode fetch, memory read, mem. write, I/O read, I/O write.
- Any inst. started with always opcode fetch machine cycle.
After that based on the inst. type, if required other machine cycles are required to execute. Each and every machine cycle having specified no. of T-states.
For ex: Opcode fetch, memory read, memory ~~sta~~ write requires 4, 3, 3 states.

MP identifies these machine cycles with combination of I/O/M, S₀, S₁, pin values.



Initially $S_0, S_1 = 1$, to do of code fetch.

Tutorial :-

Addressing :-

(i) Immediate addressing mode.

Ex :
MOV A, 04H
LXI H, 3050H. (loading the address in HL pair?)
JMP 8000H.

(ii) Register addressing

Ex :
MOV A, B
ADD B
RINR A
INX H.

(iii) Direct addressing

LDA 2050H.

LHLD 2050H.

STA 2050H.

(load HL pair with the content of 2050H)

(iv) Register indirect addressing.

MOV A, M. (the memory content is indirectly stored in A)

(v) Implicit Addressing.

CMA

RR C

RL C

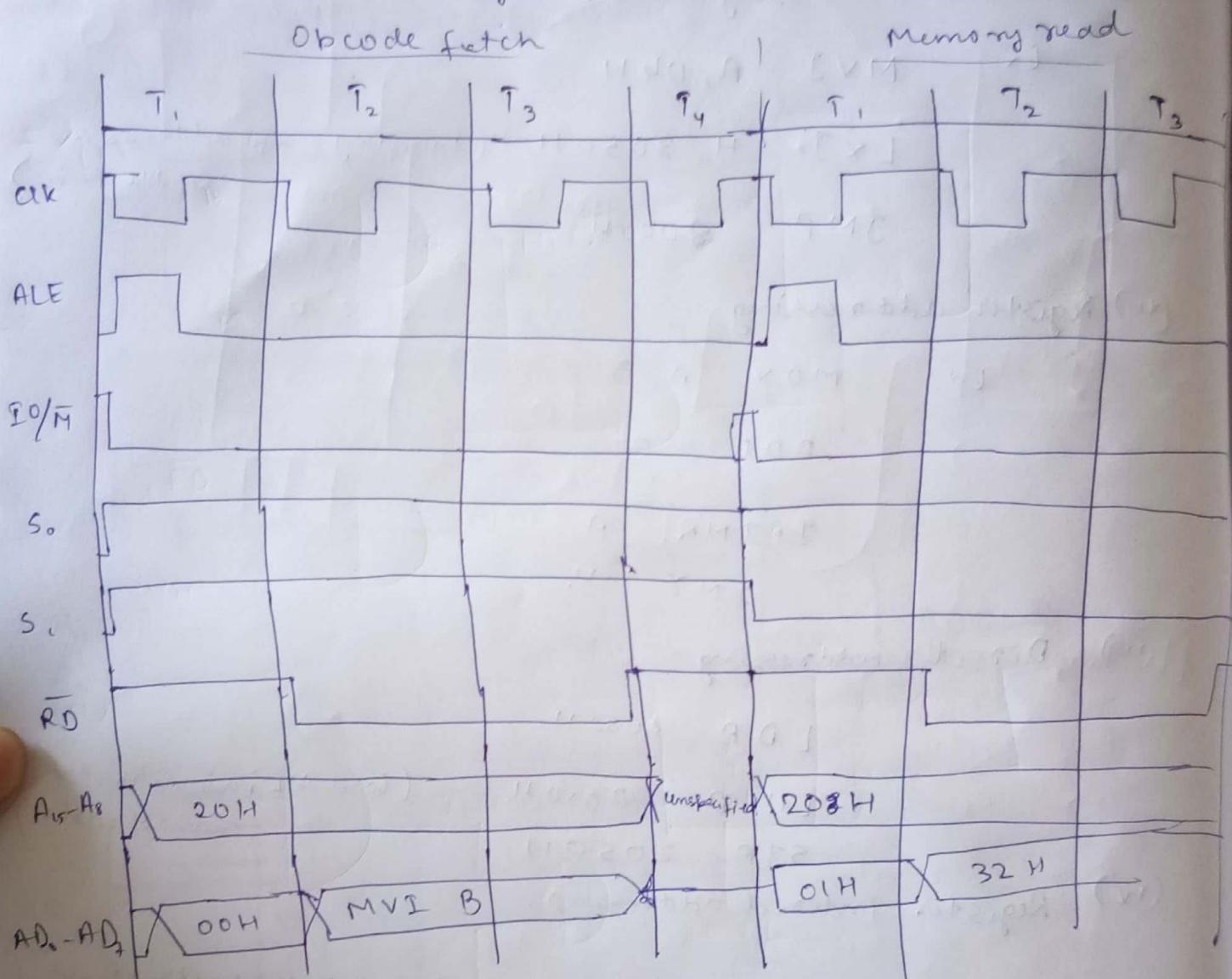
(Right bit shift to the data?)

Draw a timing diagram of MVII B, 32 H.

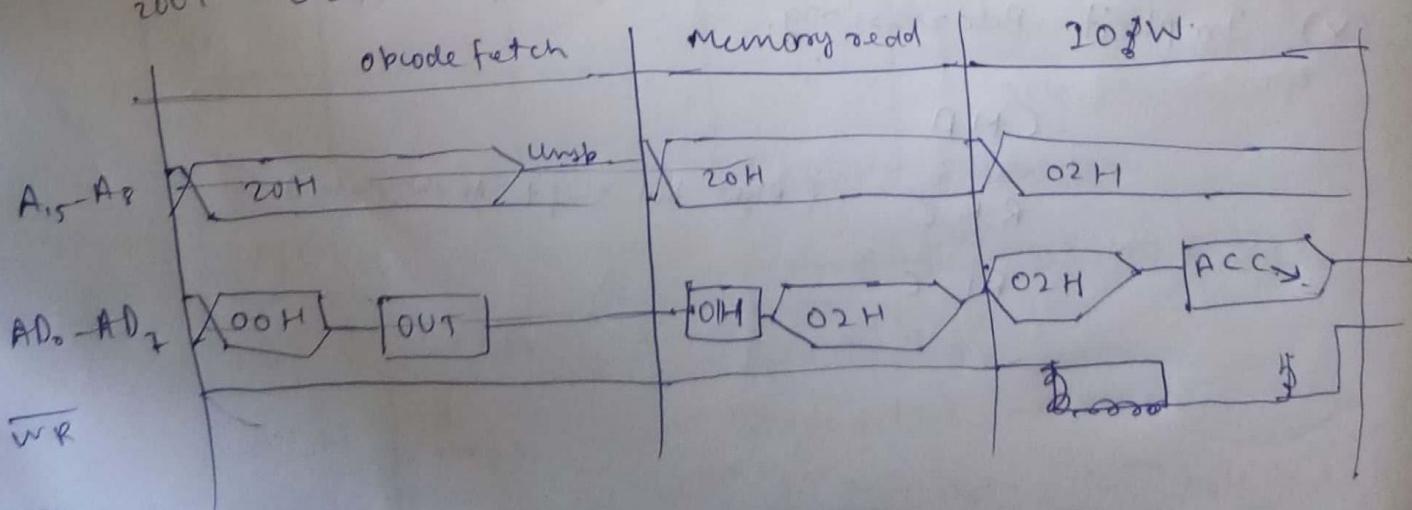
⇒ Size - 2 Byte

(i) Opcode fetch - M1C cycle

(ii) Mem. Read - M1C cycle.

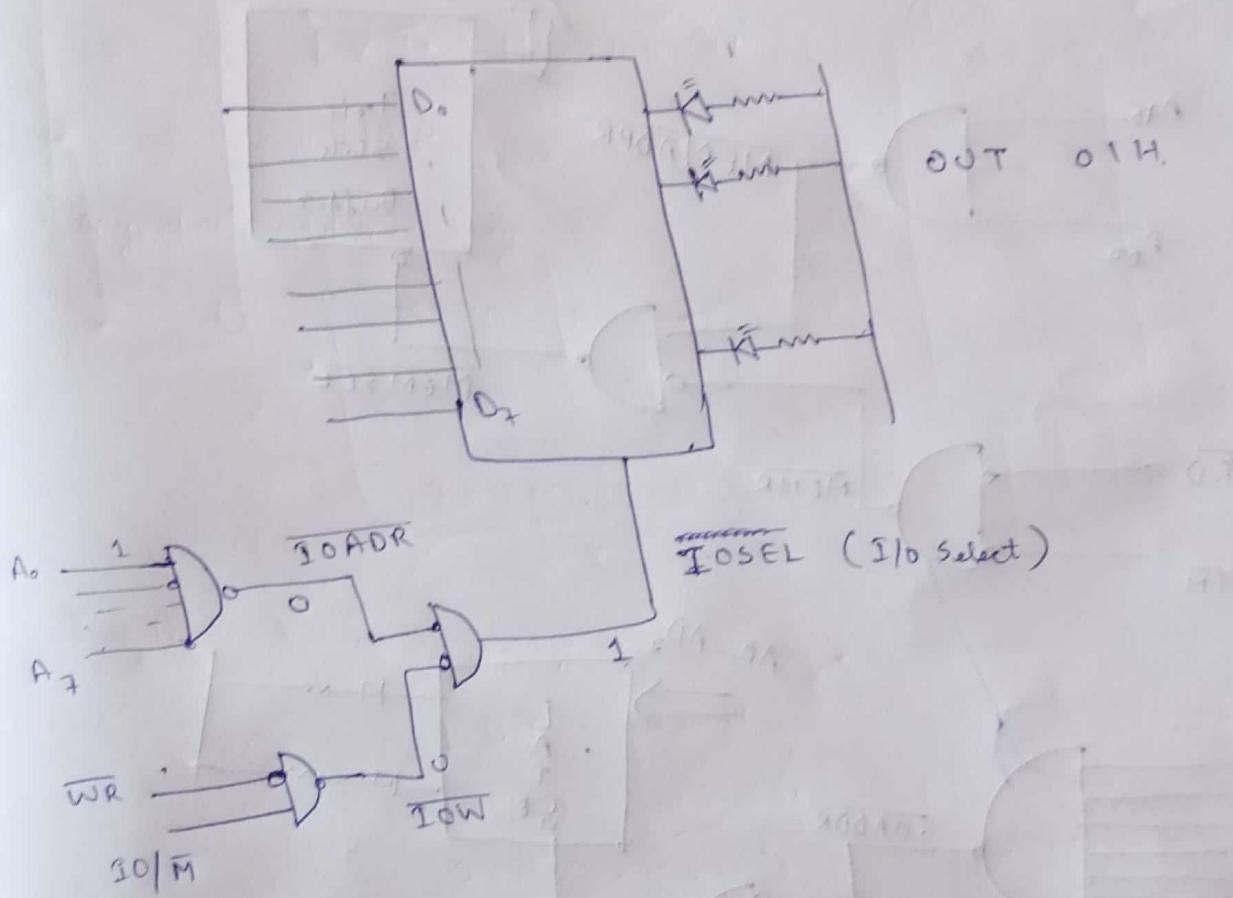


EX 2000 OUT
 2001 02H



Q.) write the timing diagram of STA 2050, LDA 2050,
 Explain the meaning of memory mapped I/O and peripheral
 mapped I/O.

I/O Interfacing



- Q.) Draw interface diagram of I/P device for IN 01H
- Q.) Draw interface diagram of I/P and O/P device g for given inst.
 IN 04H
 OUT 03H
- Q.) Use 74 LS 143 decoder as well as without using it.
- Q.) Explain partial addressing interface and full addressing interface.

Q) Draw interface 85 with the following

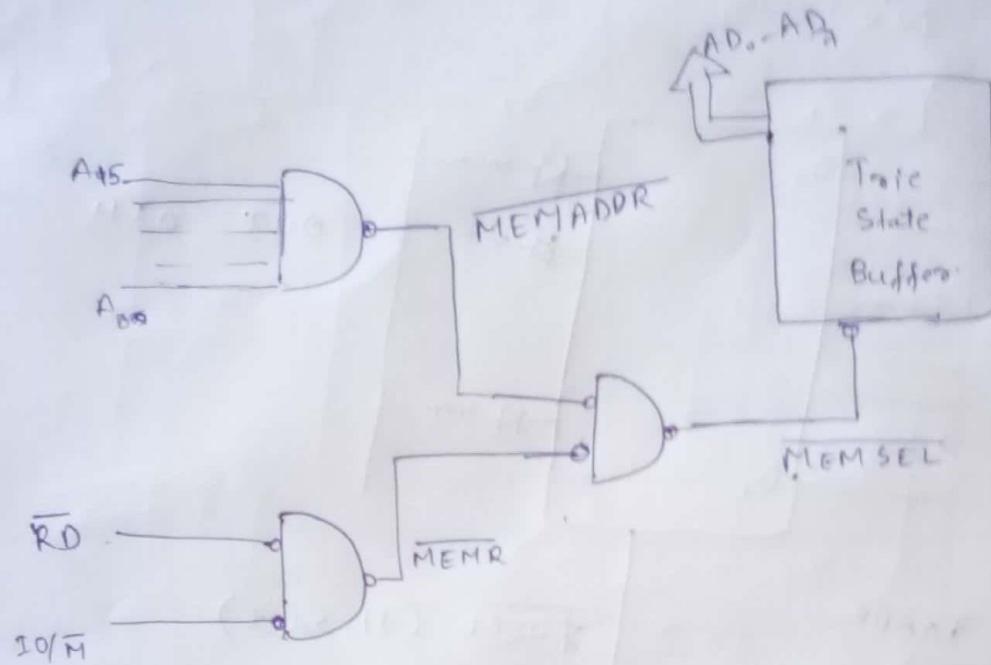
(i) Input device with address FFFFH

(ii) O/P " address F0H

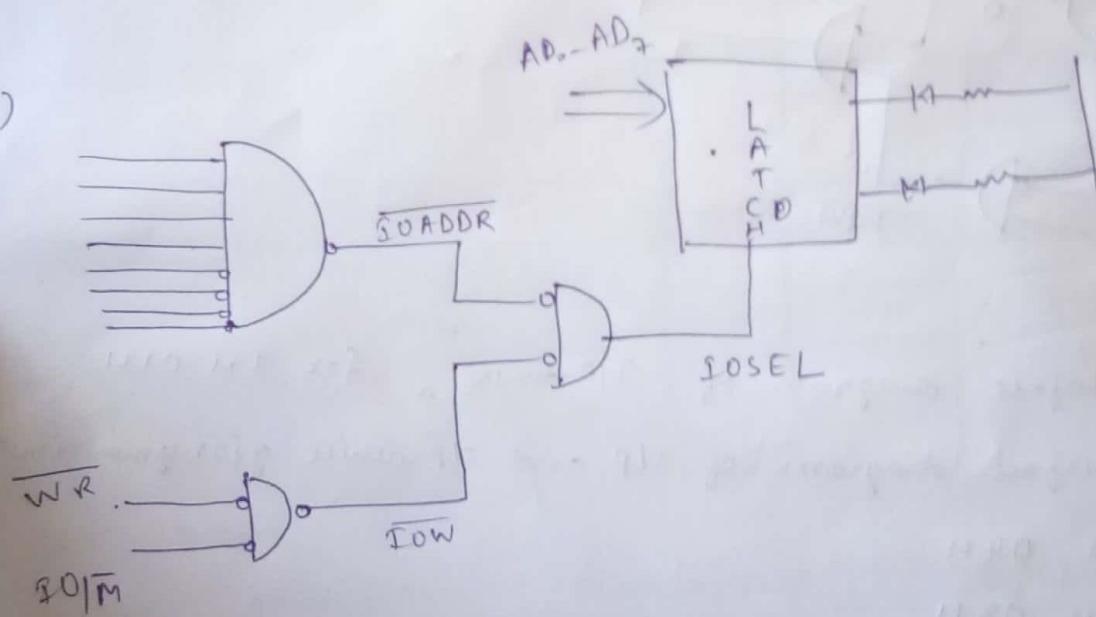
(iii) RAM , 1KB starting from 0000H

(iv) ROM, starting from F000H.

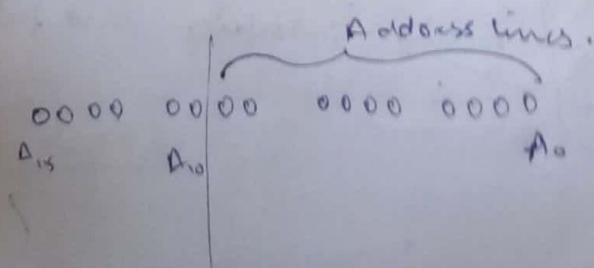
\Rightarrow (i)

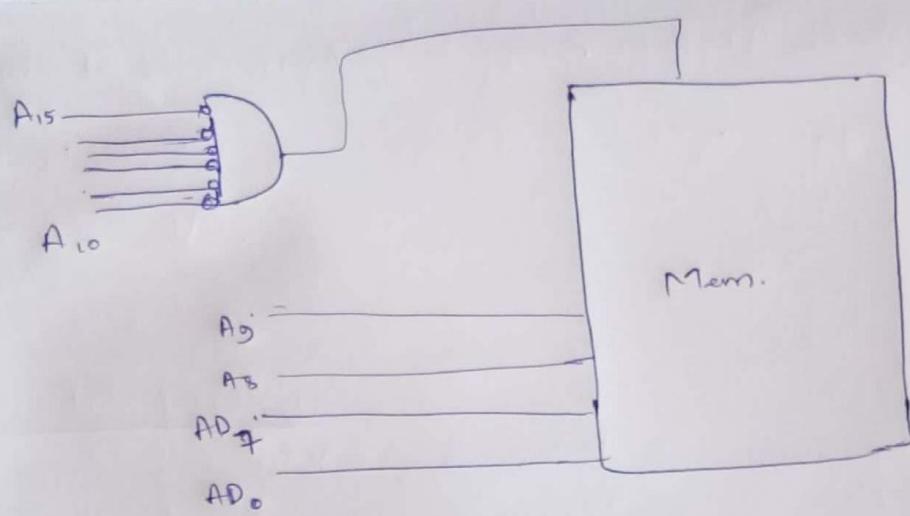


(ii)

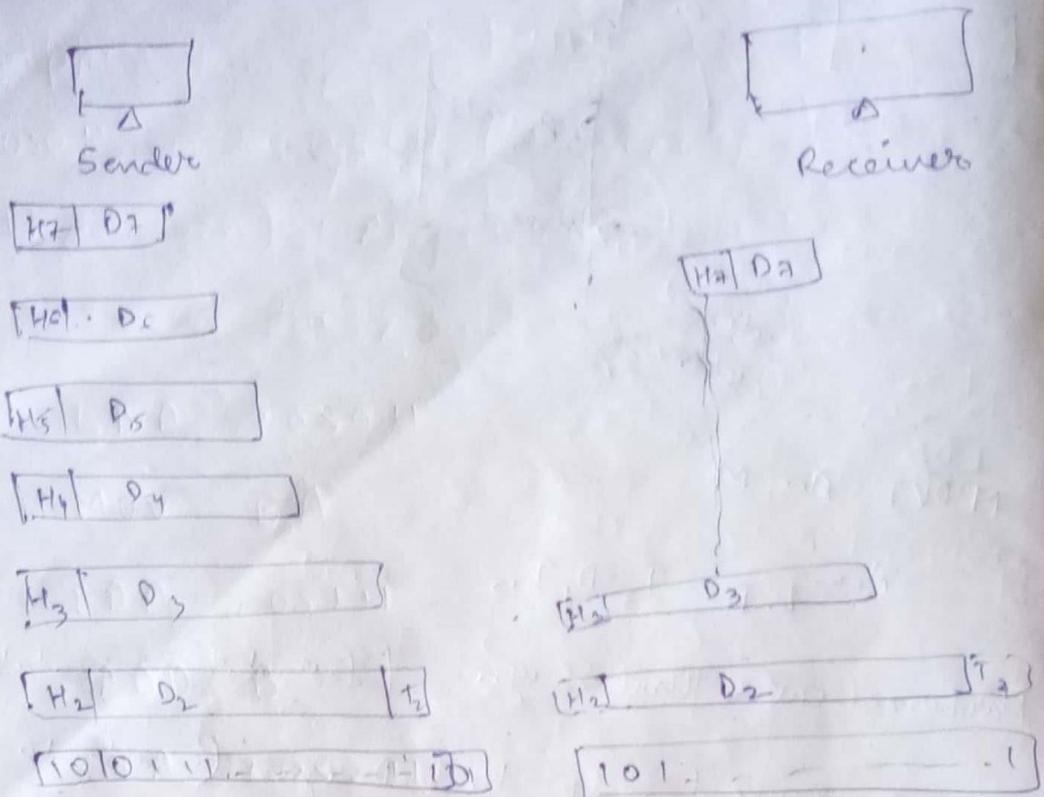


(iii) 1KB = $2^10 \times 8$ byte \Rightarrow 10 address lines.





Computer Networks



\Rightarrow Physical Layer

main ① Transmission of raw bits.

- ~~Ques P.~~

 - (2) Physical characteristics of interface and medium.
 - (3) Synchronization of bits
 - (4) Line Configuration
 - (5) Physical topology
 - (6) Transmission mode.
 - (7) Representation of bits
 - (8) Data rate.

\Rightarrow Data Link layer.

Main
obj. ① It transforms physical layer from being a raw transmission of bits to a reliable ~~code~~ ~~ent.~~

(2) Foaming.

③ Physical addressing

- at addressing

 - ① within the network - add sender + receiver address
 - ② outside the network - address of next node

Components of data communication



⑤ Protocol

Simplex → Unidirectional

Half Duplex → Bidirectional but not simultaneously

Full Duplex → Bidirectional simultaneously

Characteristics:

1) Performance

- throughput
- delay

2) Reliability

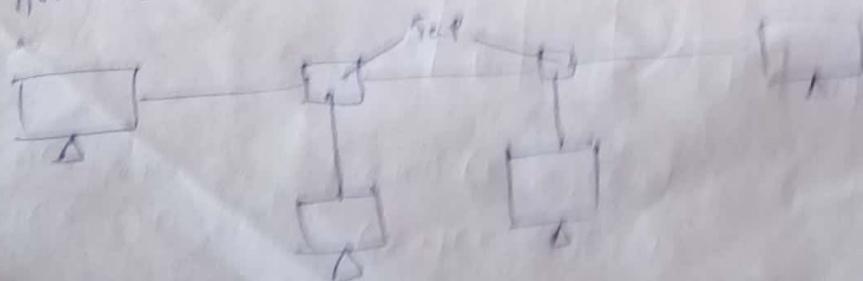
3) Security

Types of connection

(a) Point to point connection - no device present b/w the sender & receiver.

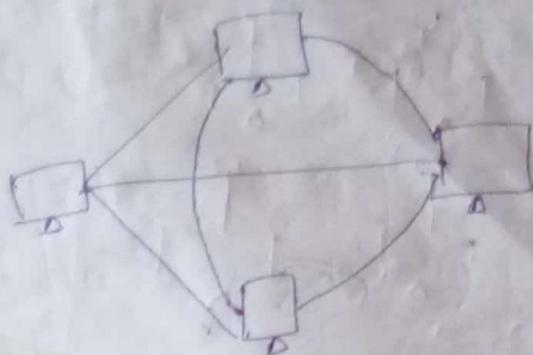


(b) Multipoint :- Presence of common connection from all the intermediate nodes



Physical Topology

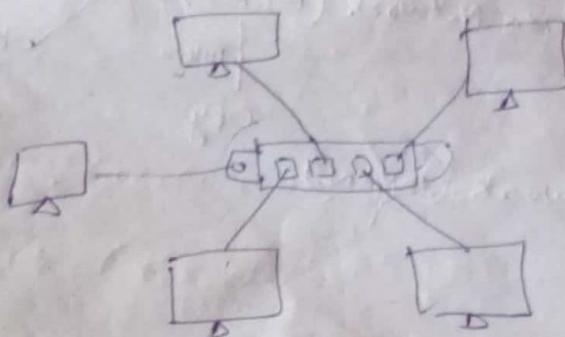
⇒ Mesh Topology → Every device connected to every other device with a pt. to pt. connection.



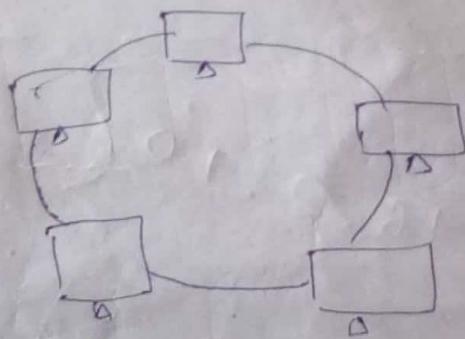
Disadvantages

→ Installation issues (cost, power etc.)

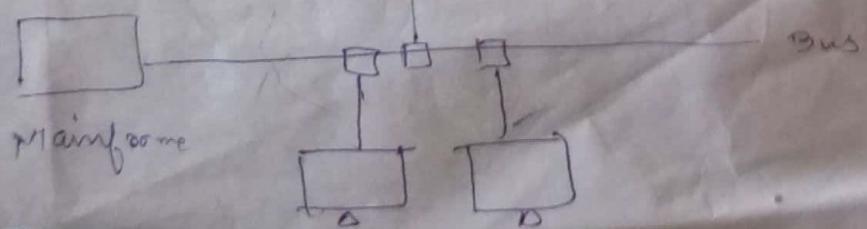
⇒ Star Topology -



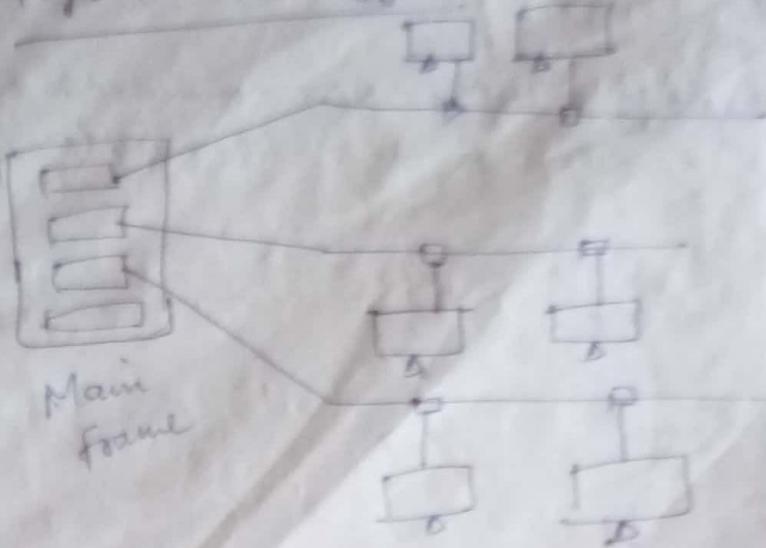
⇒ Ring Topology -



⇒ Bus Topology:-



Hybrid Topology



1) Local Area Network (LAN)

2.) Metropolitan Area network (MAN)

3.) Wide Area Network (WAN)

4.) Internet

Protocol

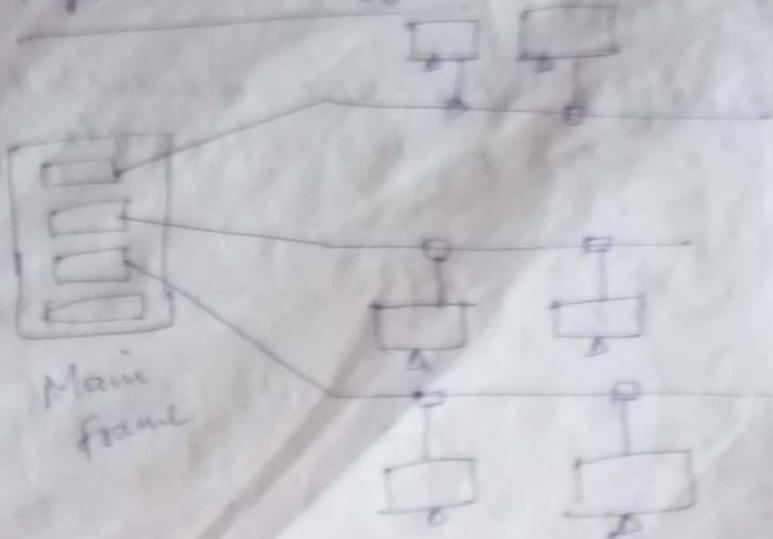
1.) Syntax :-

2.) Semantics

3.) Timing

Standards:

Hybrid Topology



Local Area Network (LAN)

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Protocol

1.) Syntax :-

2.) Semantics

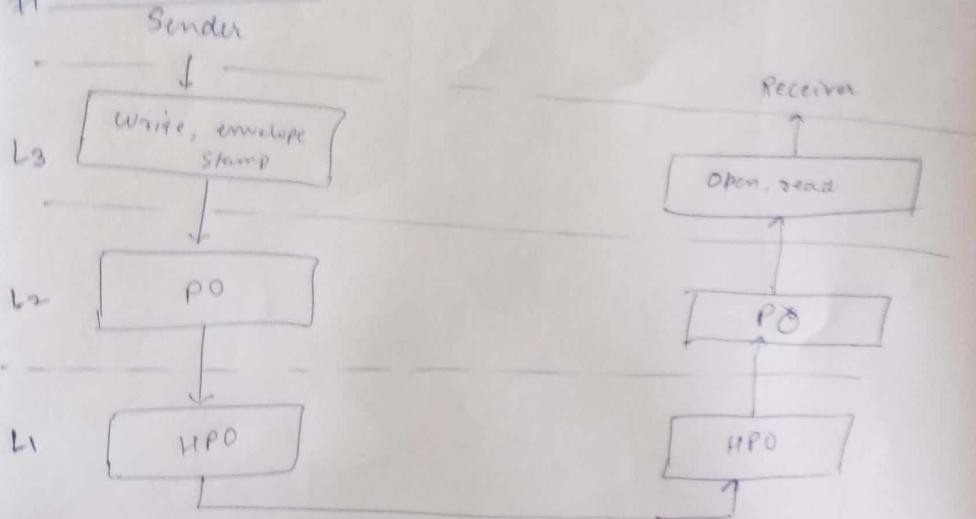
3.) Timing

Standards:

Network Models

- (1) Open System Interconnection (OSI) model
- (2) TCP/IP Model.

Post-Office Example:-



- 1) Layers
- 2) Services
- 3) Interface (how one accesses the service from the lower layer)
- 4.) Protocol.

Design Issues of Network Model:-

- (1) Process identification
- (2) Data Transfer
- (3) Error control.
- (4) Flow control.
- (5) Message size
- (6) Routing.

ISO Reference Model

