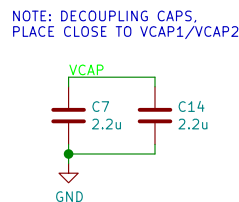
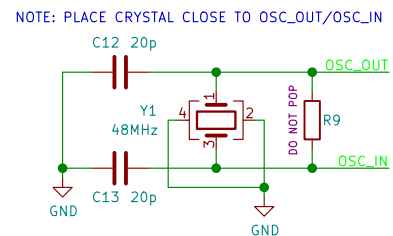
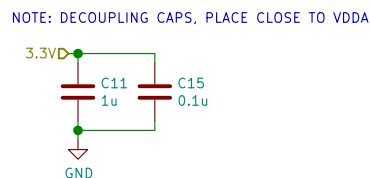
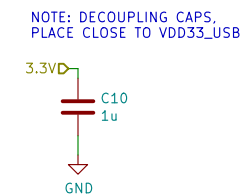
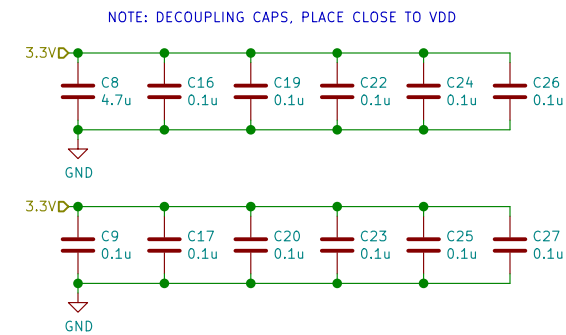


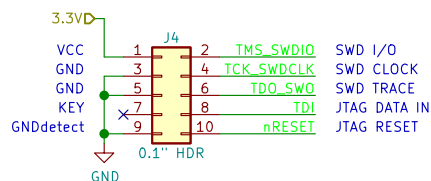
DT18 - I/O MASTER
THE UNIVERSITY OF AKRON
Sheet: /
File: io-master.sch
Title: I/O MASTER v1

Size: B	Date: 2020-02-07	Rev: A
KiCad E.D.A. kicad 5.1.5		Id: 1/10

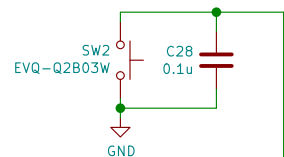
STM32H7 MICROCONTROLLER



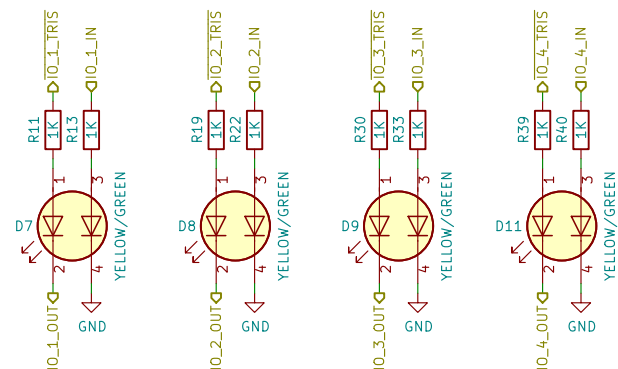
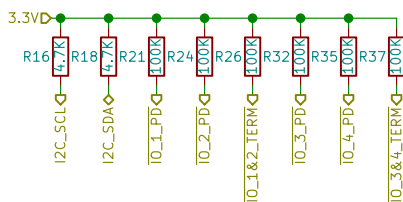
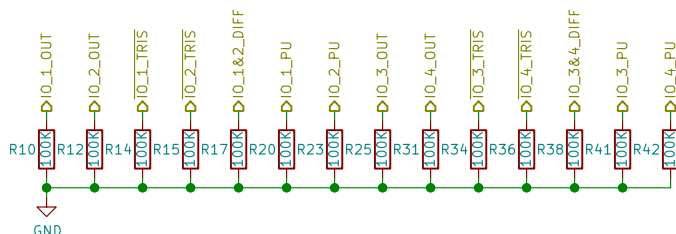
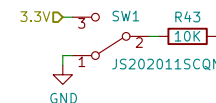
JTAG/SERIAL WIRE DEBUG



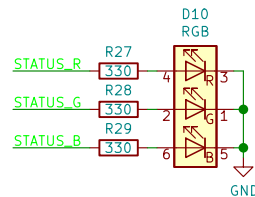
RESET BUTTON



BOOT SWITCH



RGB STATUS LED

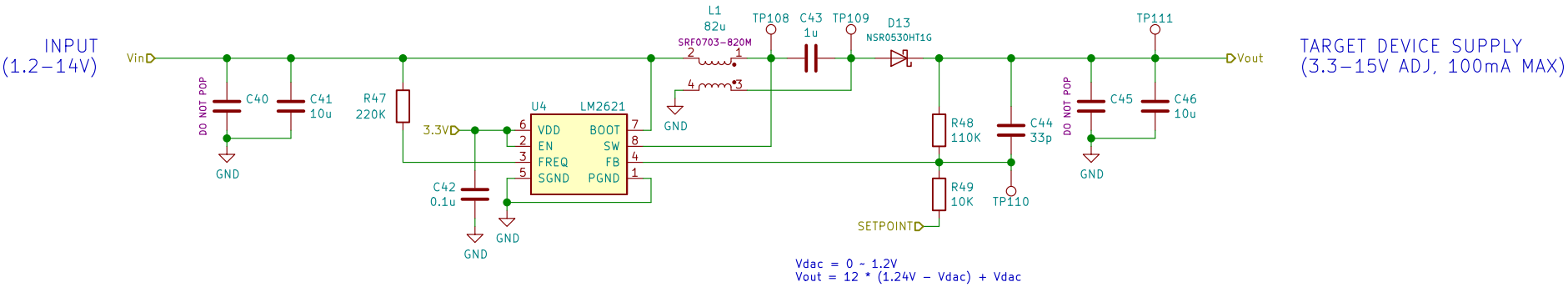


MCU ALTERNATE PIN FUNCTIONS:

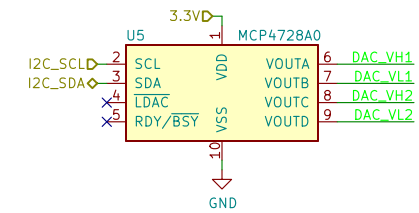
- PA0: TIM2_CH1
- PA1: TIM5_CH2
- PA2: TIM15_CH1
- PA4: DAC_OUT1
- PA7: TIM14_CH1
- PA8: I2C1_SCL
- PA9: USART1_TX
- PA10: USART1_RX
- PB7: TIM4_CH2
- PB8: TIM16_CH1
- PB9: TIM17_CH1
- PC6: TIM3_CH1
- PC9: I2C1_SDA



3.3–15V ADJUSTABLE REGULATOR



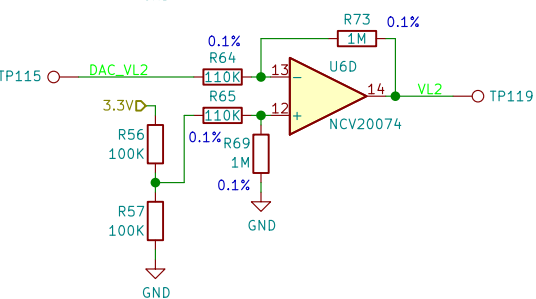
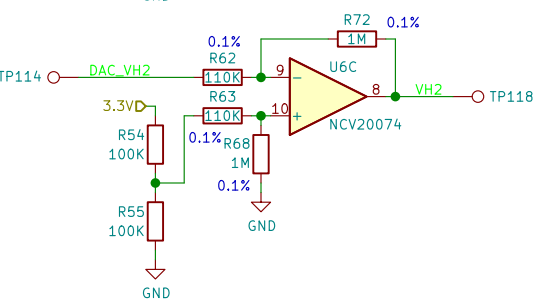
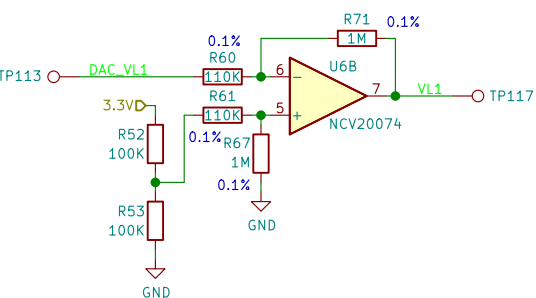
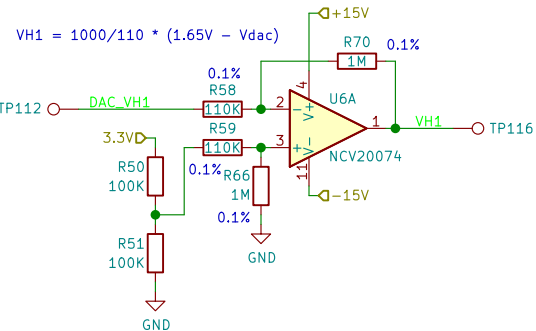
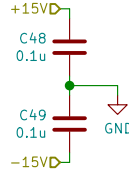
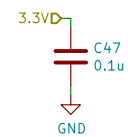
LOGIC LEVEL GENERATOR



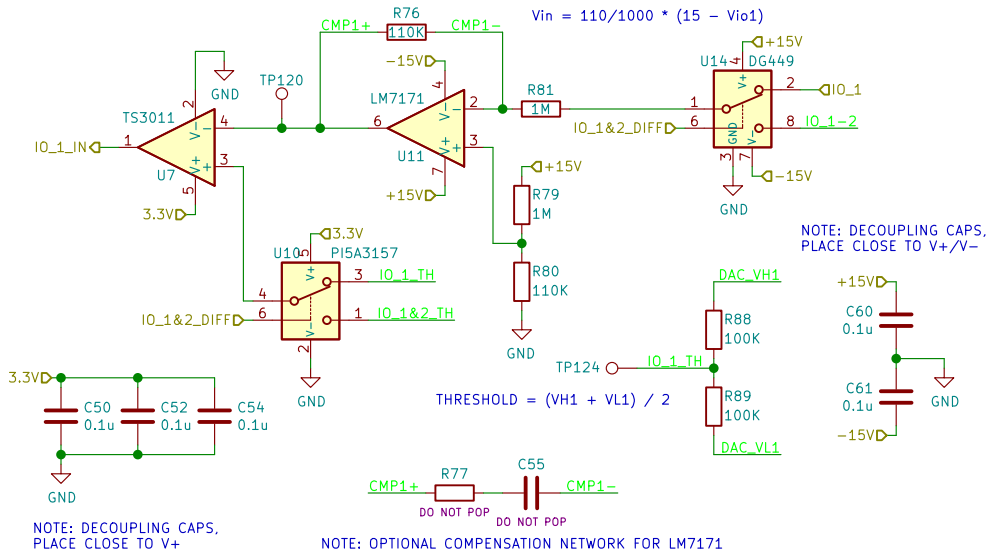
NOTE: P/N MCP4728A0 IS PRE-PROGRAMMED WITH I2C ADDRESS 0b1100000

NOTE: DECOUPLING CAP. PLACE CLOSE TO VDD

NOTE: DECOUPLING CAPS. PLACE CLOSE TO V+/V-



SINGLE-ENDED RECEIVER (I/O PIN 1)



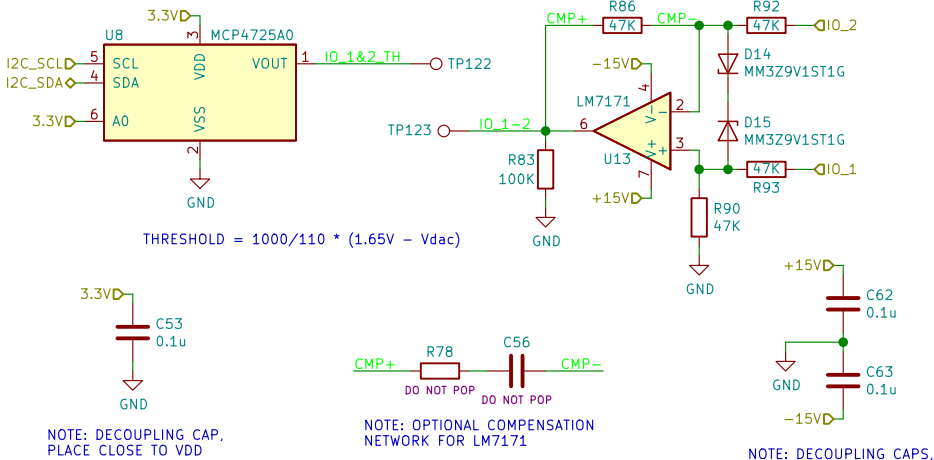
NOTE: DECOUPLING CAPS. PLACE CLOSE TO V+/V-

NOTE: DECOUPLING CAPS. PLACE CLOSE TO V+

NOTE: OPTIONAL COMPENSATION NETWORK FOR LM7171

DIFFERENTIAL RECEIVER (I/O PIN 1 - I/O PIN 2)

NOTE: P/N MCP4725A0 IS PRE-PROGRAMMED WITH I2C ADDRESS 0b1100001

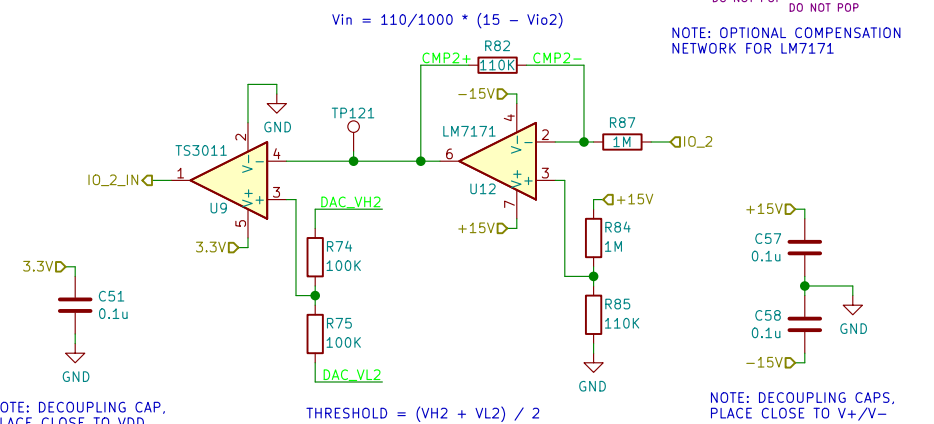


NOTE: DECOUPLING CAP. PLACE CLOSE TO VDD

NOTE: OPTIONAL COMPENSATION NETWORK FOR LM7171

NOTE: DECOUPLING CAPS. PLACE CLOSE TO V+/V-

SINGLE-ENDED RECEIVER (I/O PIN 2)

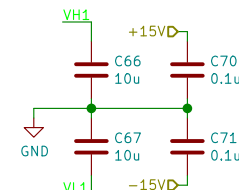


NOTE: DECOUPLING CAP. PLACE CLOSE TO VDD

THRESHOLD = $(V_{H2} + V_{L2}) / 2$

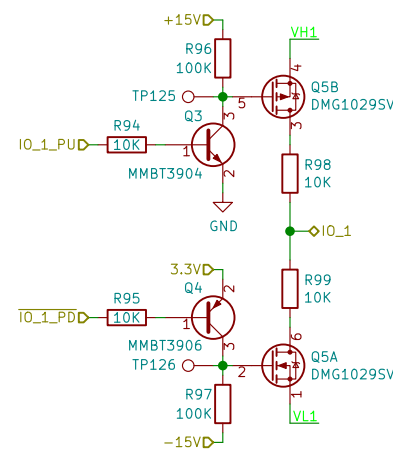
NOTE: DECOUPLING CAPS. PLACE CLOSE TO V+/V-

OUTPUT DRIVER (I/O PIN 1)

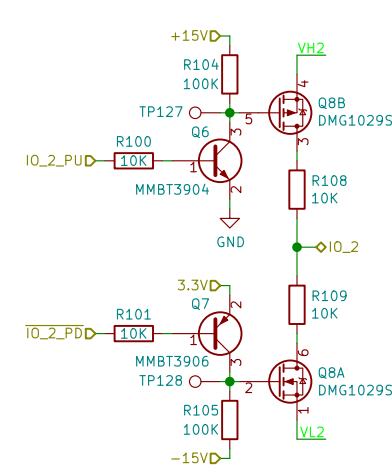


NOTE: DECOUPLING CAPS. PLACE CLOSE TO V+/V-

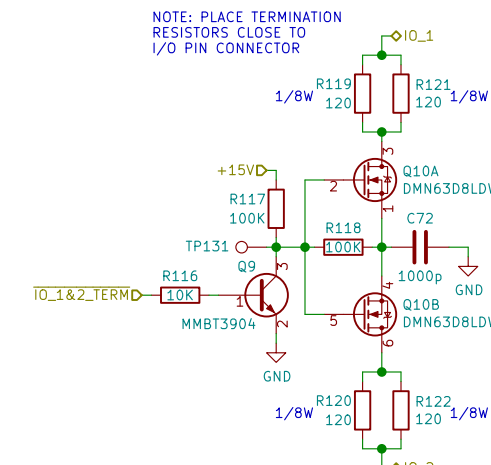
CONFIGURABLE RESISTORS



I/O PIN 1
10KΩ PULL-UP/DOWN

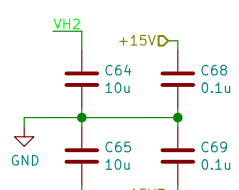


I/O PIN 2
10KΩ PULL-UP/DOWN

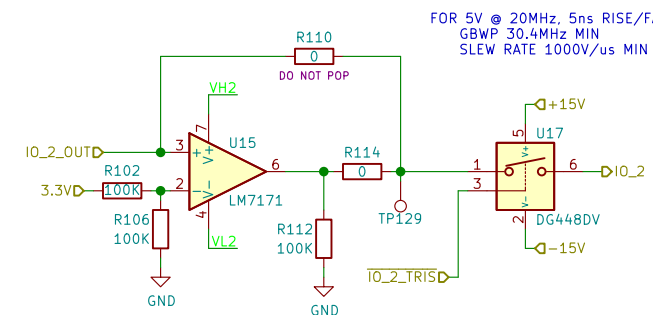


120Ω TERMINATION
BETWEEN I/O PINS 1 & 2

OUTPUT DRIVER (I/O PIN 2)

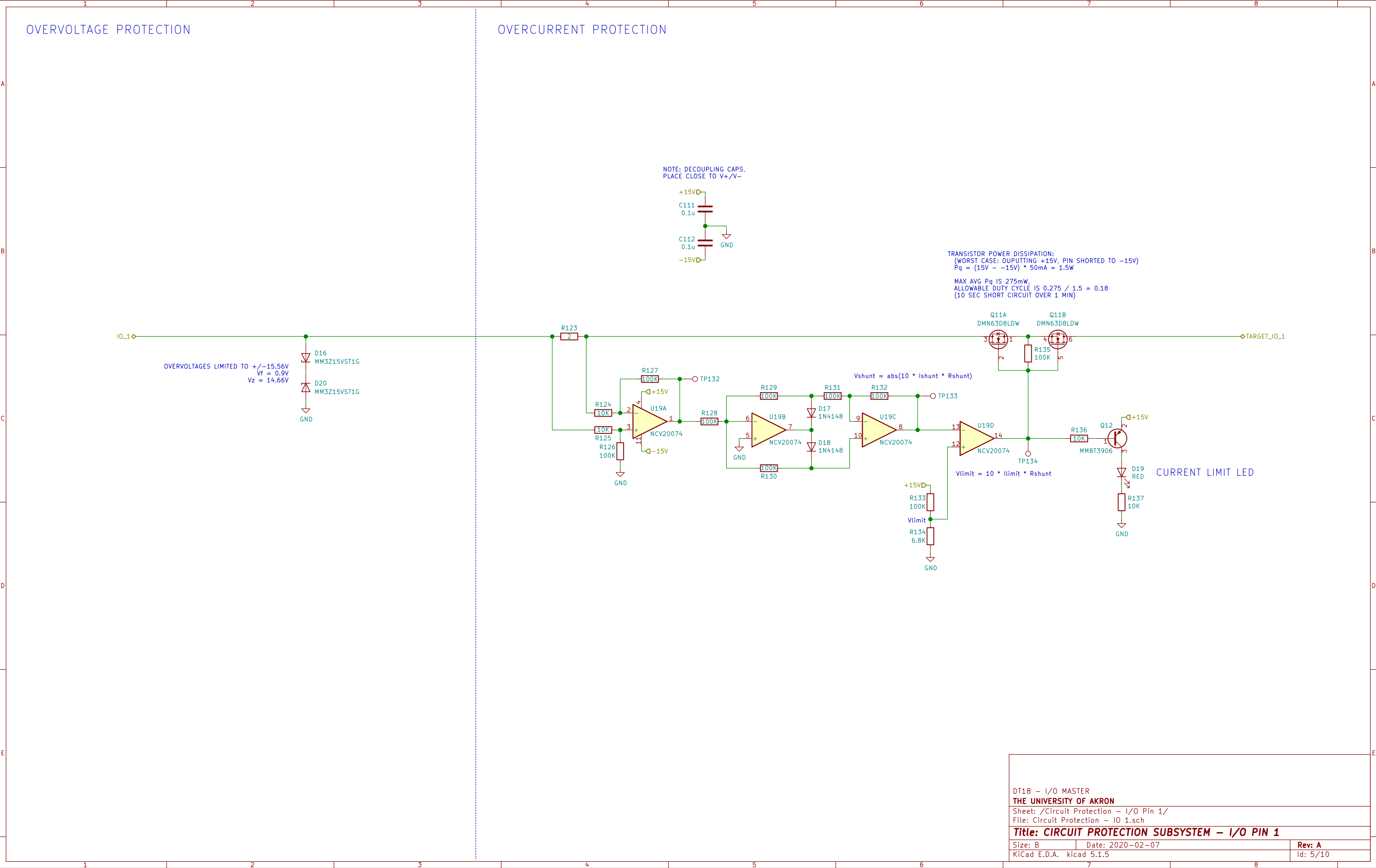


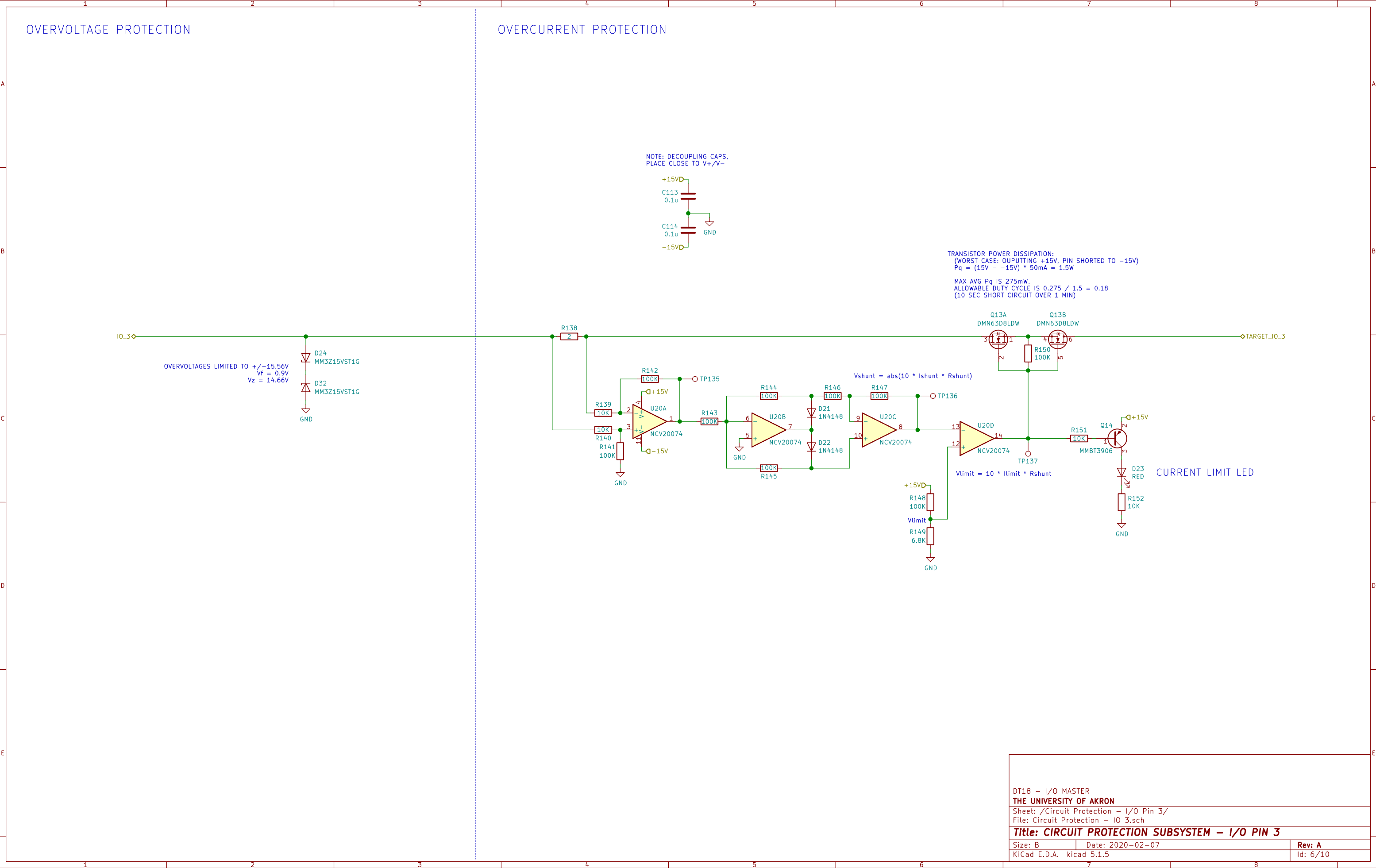
NOTE: DECOUPLING CAPS. PLACE CLOSE TO V+/V-

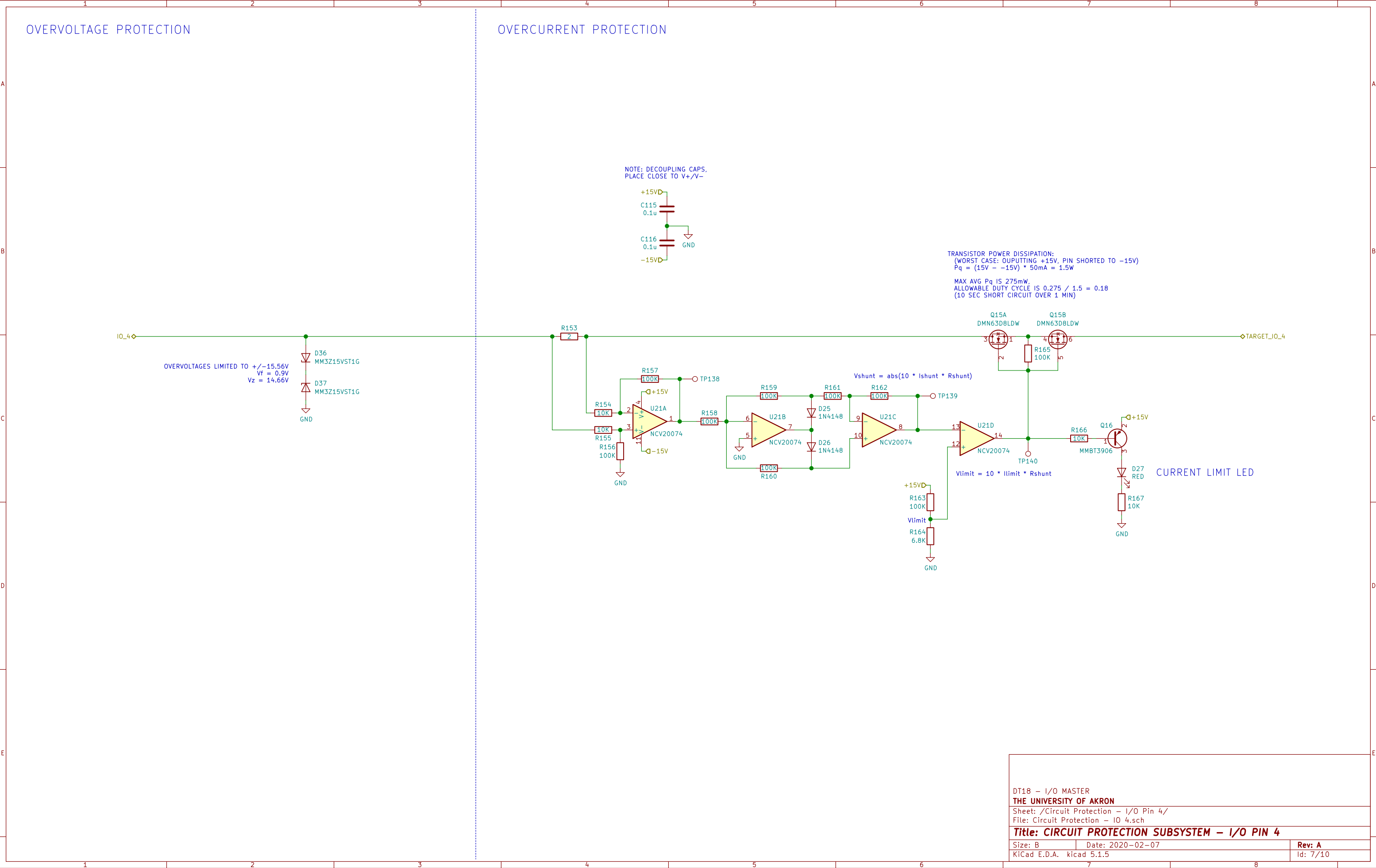


FOR 5V @ 20MHz, 5ns RISE/FALL:
GBWP 30.4MHz MIN
SLEW RATE 1000V/us MIN

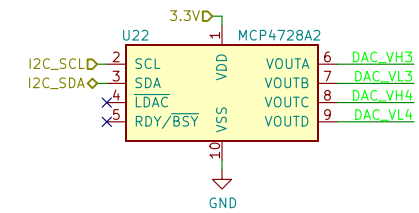
DT18 - I/O MASTER		
THE UNIVERSITY OF AKRON		
Sheet: /Level Shifter - I/O Pins 1&2/		
File: Level Shifter - IO 1-2.sch		
Title: LEVEL SHIFTER SUBSYSTEM - I/O PINS 1 & 2		
Size: B	Date: 2020-02-07	Rev: A
KiCad E.D.A.	kiCad 5.1.5	Id: 4/10







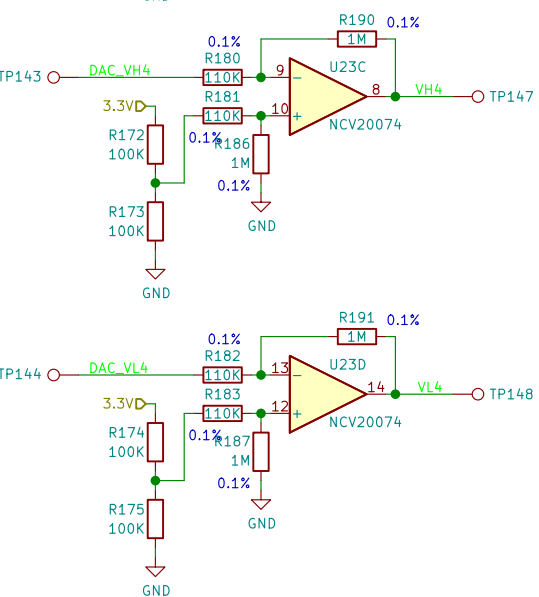
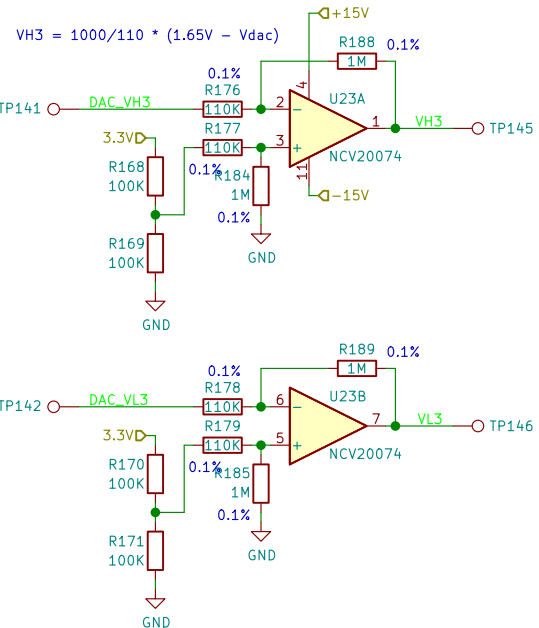
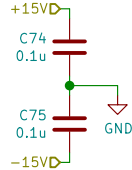
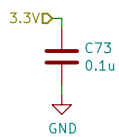
LOGIC LEVEL GENERATOR



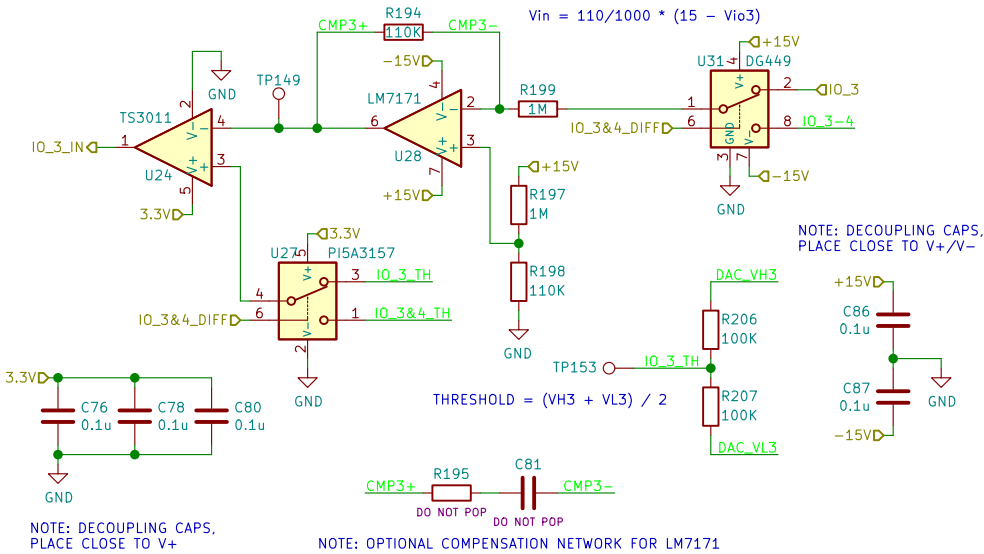
NOTE: P/N MCP4728A2 IS PRE-PROGRAMMED WITH I2C ADDRESS 0b1100010

NOTE: DECOUPLING CAP.
PLACE CLOSE TO VDD

NOTE: DECOUPLING CAPS.
PLACE CLOSE TO V+/V-



SINGLE-ENDED RECEIVER (I/O PIN 3)

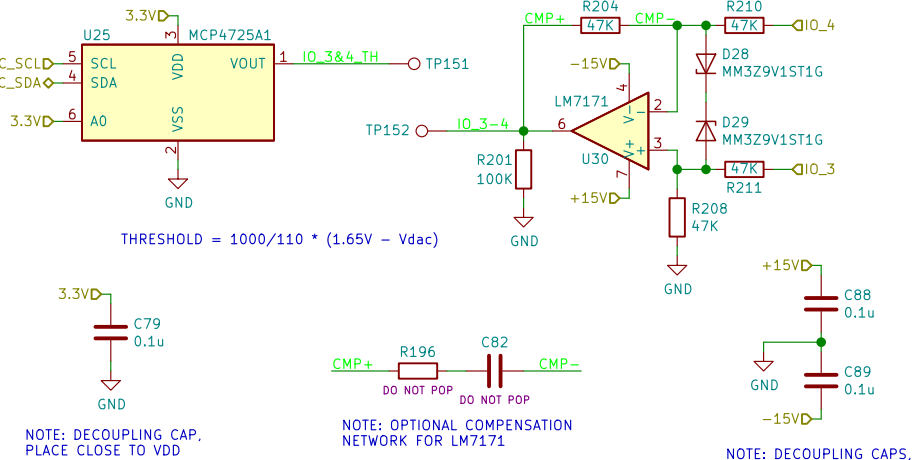


NOTE: DECOUPLING CAPS.
PLACE CLOSE TO V+

NOTE: OPTIONAL COMPENSATION NETWORK FOR LM7171

DIFFERENTIAL RECEIVER (I/O PIN 3 - I/O PIN 4)

NOTE: P/N MCP4725A1 IS PRE-PROGRAMMED WITH I2C ADDRESS 0b1100011

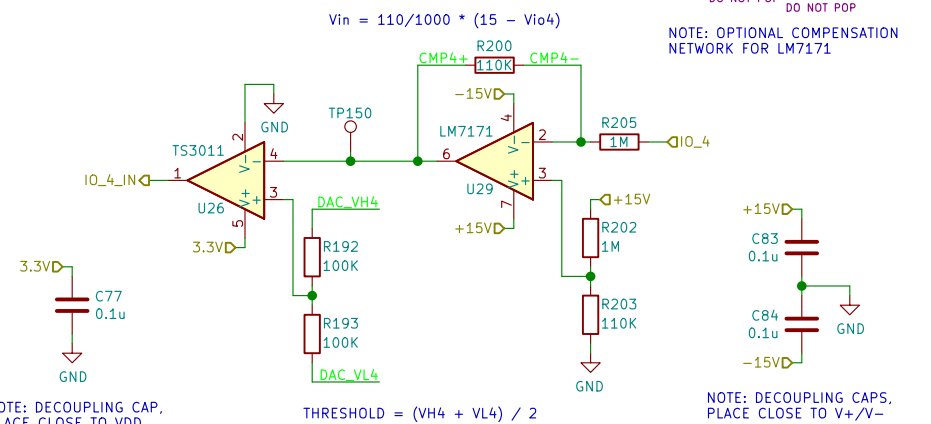


NOTE: DECOUPLING CAP.
PLACE CLOSE TO VDD

NOTE: OPTIONAL COMPENSATION NETWORK FOR LM7171

NOTE: DECOUPLING CAPS.
PLACE CLOSE TO V+/V-

SINGLE-ENDED RECEIVER (I/O PIN 4)

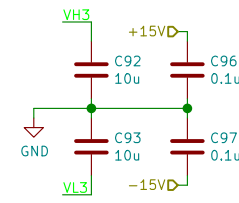


NOTE: DECOUPLING CAP.
PLACE CLOSE TO VDD

THRESHOLD = (VH4 + VL4) / 2

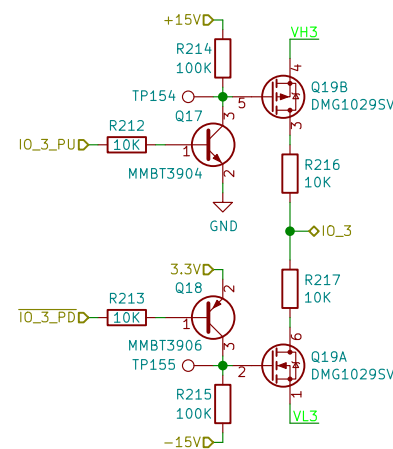
NOTE: DECOUPLING CAPS.
PLACE CLOSE TO V+/V-

OUTPUT DRIVER (I/O PIN 3)

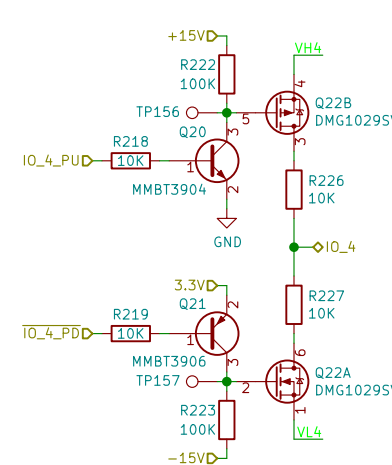


NOTE: DECOUPLING CAPS.
PLACE CLOSE TO V+/V-

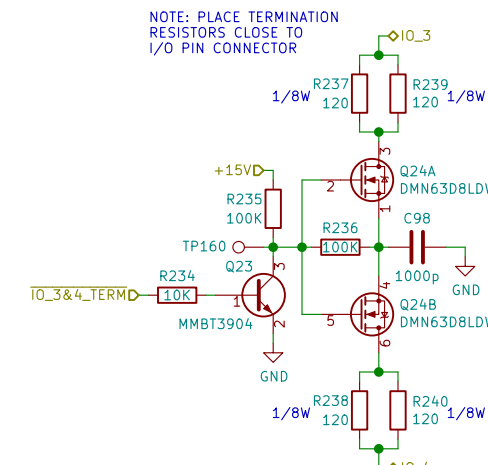
CONFIGURABLE RESISTORS



I/O PIN 3
10KΩ PULL-UP/DOWN

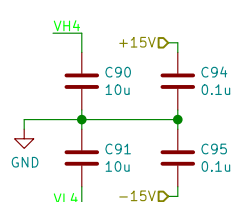


I/O PIN 4
10KΩ PULL-UP/DOWN

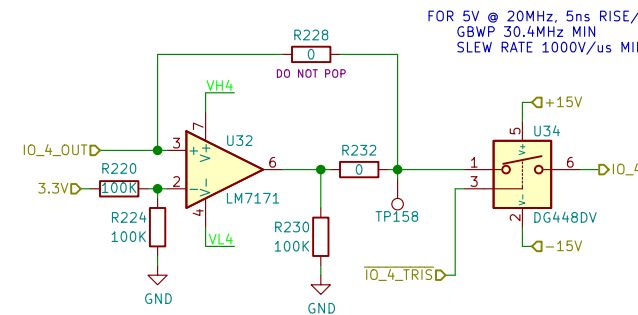


120Ω TERMINATION
BETWEEN I/O PINS 3 & 4

OUTPUT DRIVER (I/O PIN 4)



NOTE: DECOUPLING CAPS.
PLACE CLOSE TO V+/V-



FOR 5V @ 20MHz, 5ns RISE/FALL:
GBWP 30.4MHz MIN
SLEW RATE 1000V/us MIN

DT18 - I/O MASTER

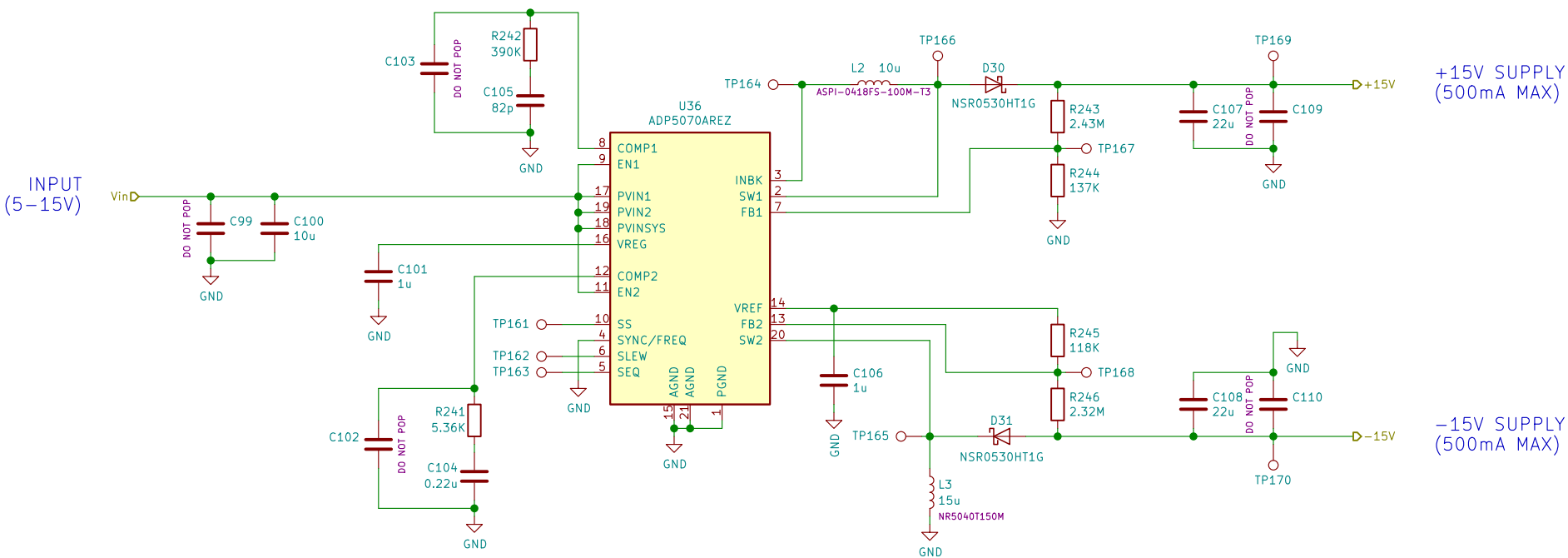
THE UNIVERSITY OF AKRON

Sheet: /Level Shifter - I/O Pins 3&4/

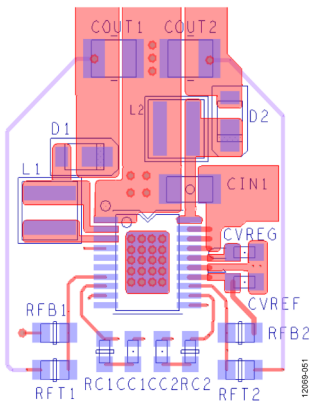
File: Level Shifter - IO 3-4.sch

Title: LEVEL SHIF

+/-15V REGULATOR



RECOMMENDED PCB LAYOUT



OVERVOLTAGE PROTECTION

OVERCURRENT PROTECTION

