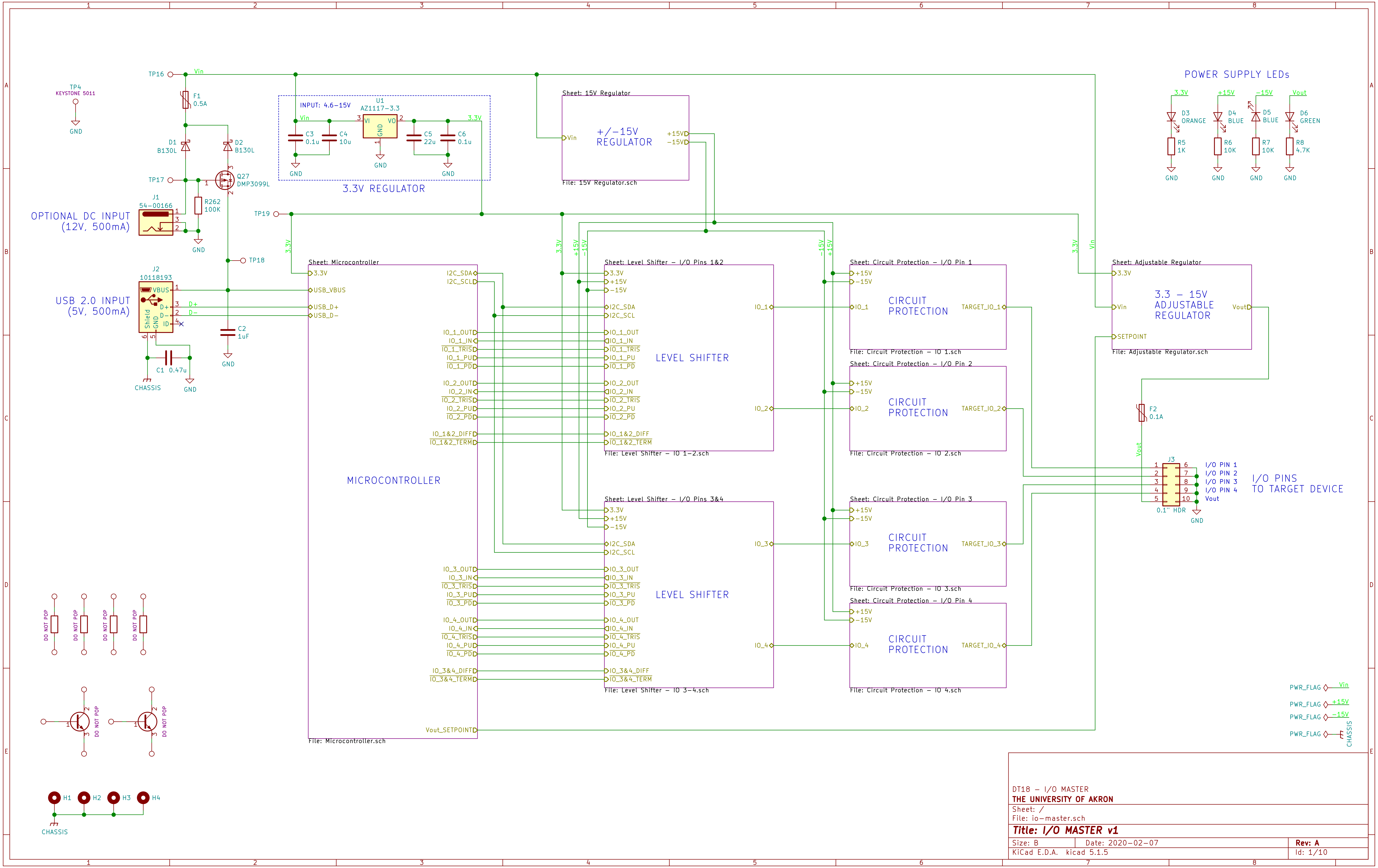
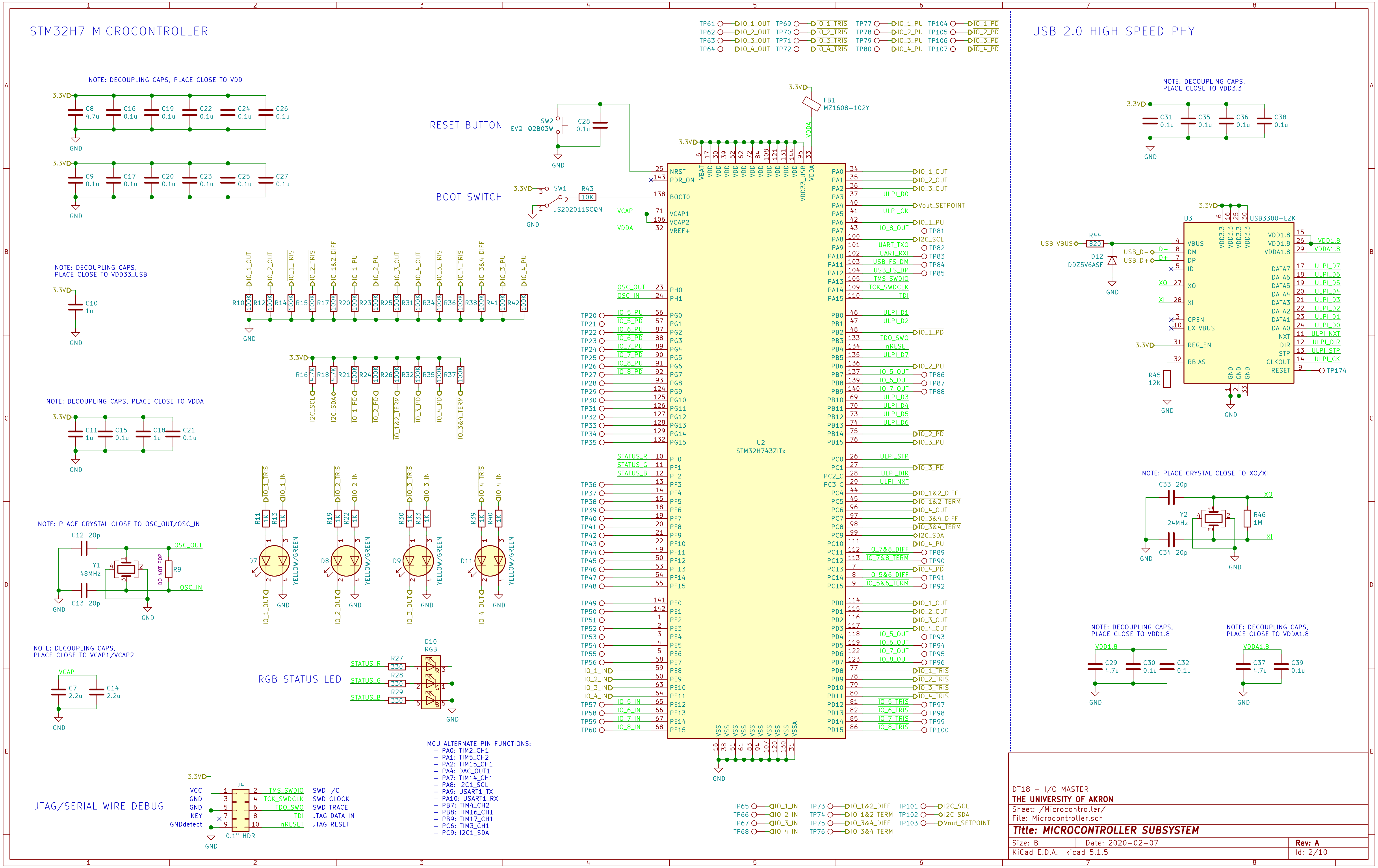


DT18 - I/O MASTER
THE UNIVERSITY OF AKRON
Sheet: /
File: io-master.sch

Title: I/O MASTER v1

Size: B Date: 2020-02-07 **Rev: A**
KiCad E.D.A. kicad 5.1.5 Id: 1/10



MCU ALTERNATE PIN FUNCTIONS:
- PA0: TIM2_CH1
- PA1: TIM5_CH2
- PA2: TIM15_CH1
- PA4: DAC_OUT1
- PA7: TIM14_CH1
- PA8: I2C1_SCL
- PA9: USART1_TX
- PA10: USART1_RX
- PB7: TIM4_CH2
- PB8: TIM16_CH1
- PB9: TIM17_CH1
- PC6: TIM3_CH1
- PC9: I2C1_SDA

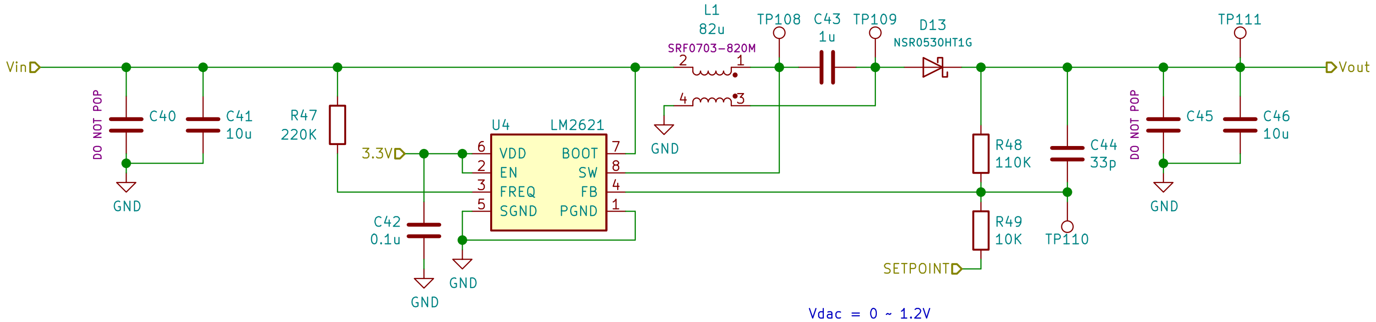
DT18 – I/O MASTER
THE UNIVERSITY OF AKRON
Sheet: /Microcontroller/
File: Microcontroller.sch

Title: MICROCONTROLLER SUBSYSTEM

Size: B
Date: 2020-02-07
Rev: A
KiCad E.D.A. kicad 5.1.5
Id: 2/10

3.3–15V ADJUSTABLE REGULATOR

INPUT
(1.2–14V)



TARGET DEVICE SUPPLY
(3.3–15V ADJ, 100mA MAX)

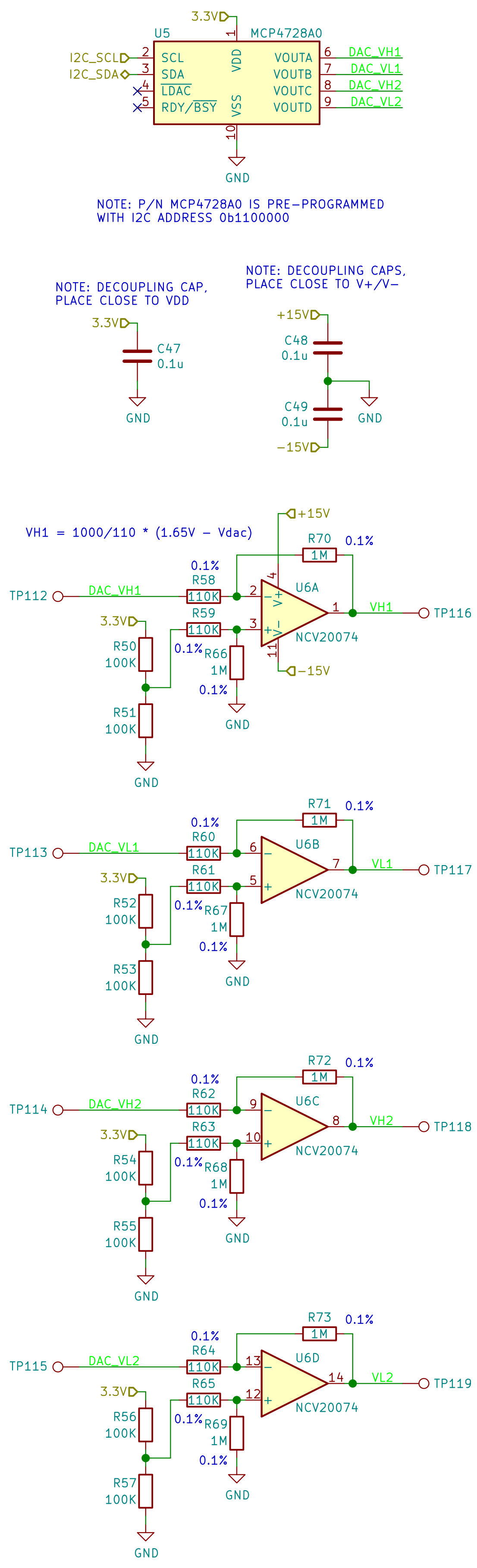
Vdac = 0 ~ 1.2V
Vout = 12 * (1.24V – Vdac) + Vdac

DT18 – I/O MASTER
THE UNIVERSITY OF AKRON
Sheet: /Adjustable Regulator/
File: Adjustable Regulator.sch

Title: 3.3–15V ADJUSTABLE REGULATOR

Size: B	Date: 2020-02-07	**Rev: A**
KiCad E.D.A. kicad 5.1.5		Id: 3/10

LOGIC LEVEL GENERATOR

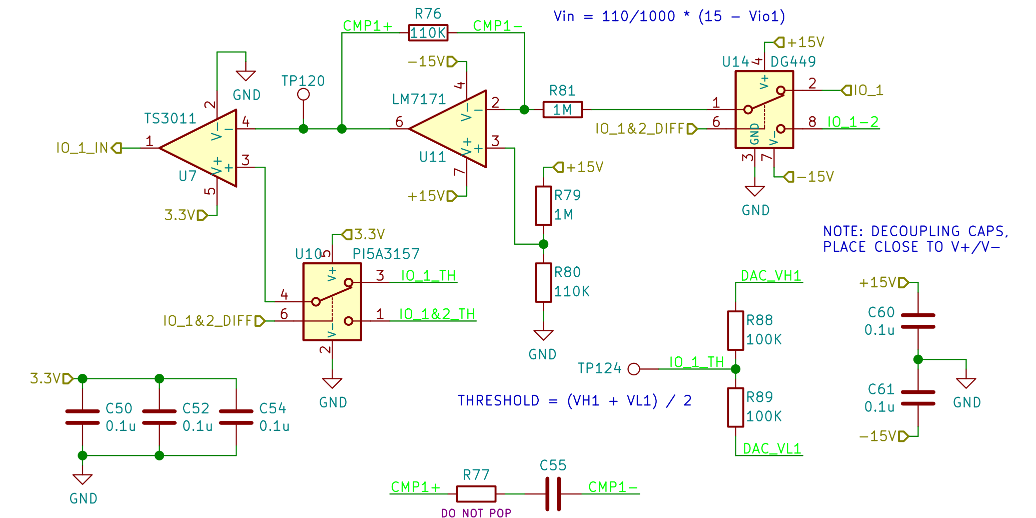


NOTE: P/N MCP4728A0 IS PRE-PROGRAMMED
WITH I2C ADDRESS 0b1100000

NOTE: DECOUPLING CAP,
PLACE CLOSE TO VDD

NOTE: DECOUPLING CAPS,
PLACE CLOSE TO V+/V−

SINGLE-ENDED RECEIVER (I/O PIN 1)

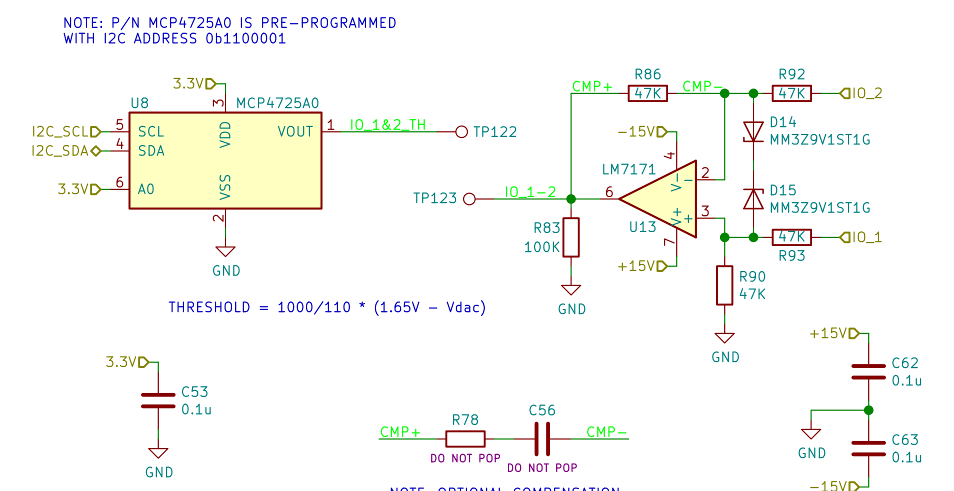


NOTE: DECOUPLING CAPS,
PLACE CLOSE TO V+

NOTE: OPTIONAL COMPENSATION NETWORK FOR LM7171

NOTE: DECOUPLING CAPS,
PLACE CLOSE TO V+/V−

DIFFERENTIAL RECEIVER (I/O PIN 1 – I/O PIN 2)



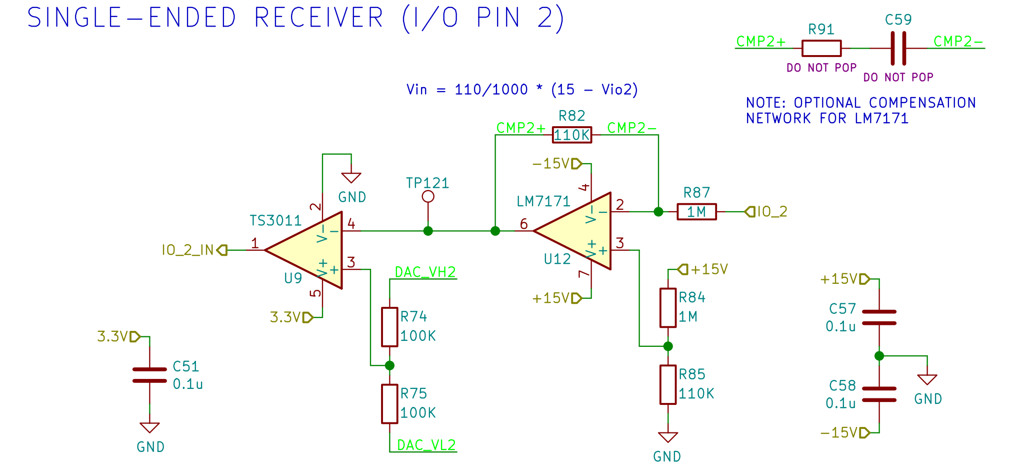
NOTE: P/N MCP4725A0 IS PRE-PROGRAMMED
WITH I2C ADDRESS 0b1100001

NOTE: DECOUPLING CAP,
PLACE CLOSE TO VDD

NOTE: OPTIONAL COMPENSATION
NETWORK FOR LM7171

NOTE: DECOUPLING CAPS,
PLACE CLOSE TO V+/V−

SINGLE-ENDED RECEIVER (I/O PIN 2)

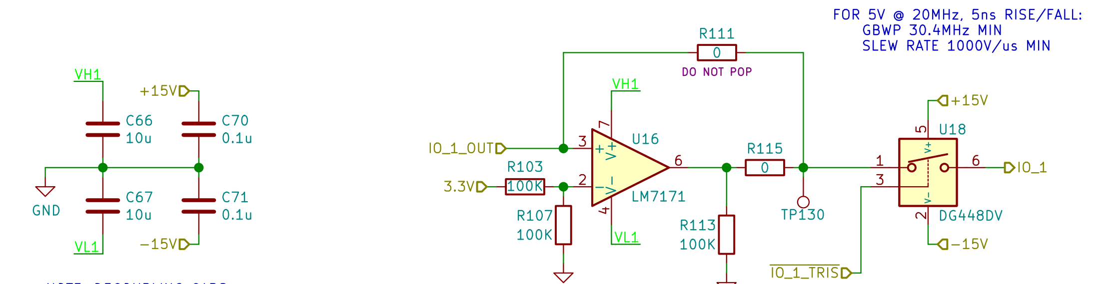


NOTE: OPTIONAL COMPENSATION
NETWORK FOR LM7171

NOTE: DECOUPLING CAP,
PLACE CLOSE TO VDD

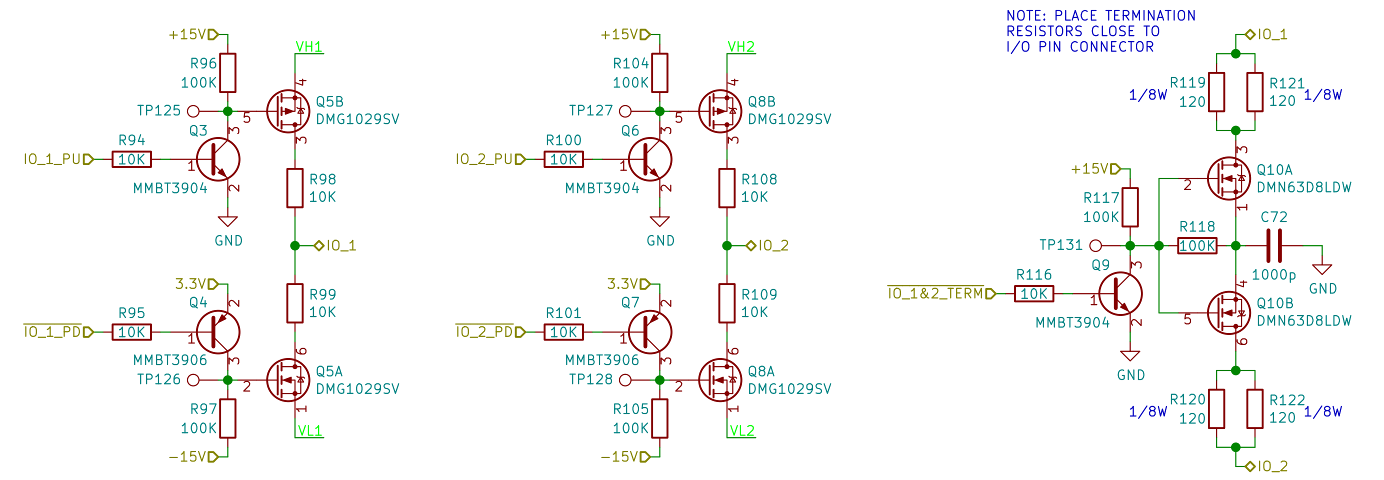
NOTE: DECOUPLING CAPS,
PLACE CLOSE TO V+/V−

OUTPUT DRIVER (I/O PIN 1)



NOTE: DECOUPLING CAPS,
PLACE CLOSE TO V+/V−

CONFIGURABLE RESISTORS

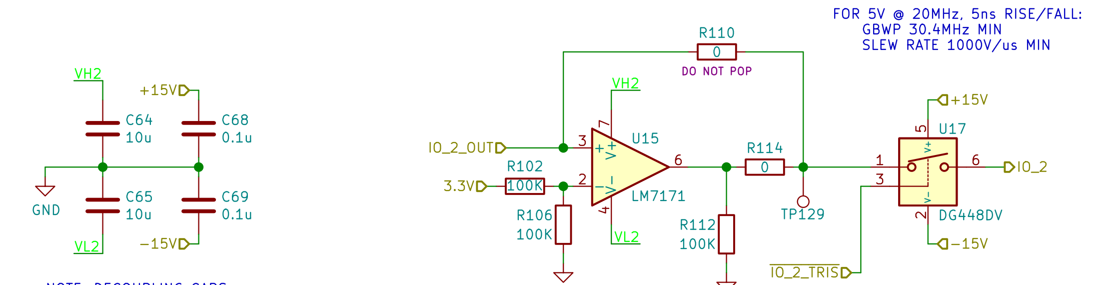


I/O PIN 1
10KΩ PULL-UP/DOWN

I/O PIN 2
10KΩ PULL-UP/DOWN

120Ω TERMINATION
BETWEEN I/O PINS 1 & 2

OUTPUT DRIVER (I/O PIN 2)

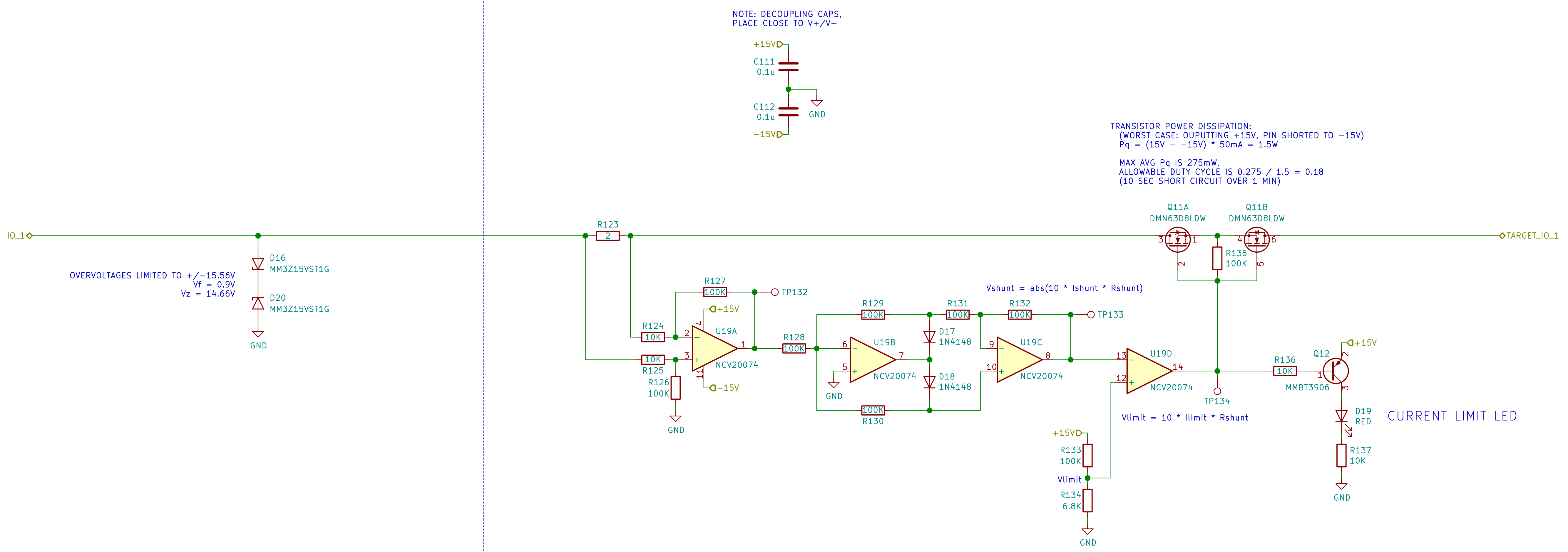


NOTE: DECOUPLING CAPS,
PLACE CLOSE TO V+/V−

DT18 – I/O MASTER
THE UNIVERSITY OF AKRON
Sheet: /Level Shifter – I/O Pins 1&2/
File: Level Shifter – IO 1-2.sch
Title: LEVEL SHIFTER SUBSYSTEM – I/O PINS 1 & 2
Size: B   Date: 2020-02-07   **Rev: A**
KiCad E.D.A. kicad 5.1.5   Id: 4/10

OVERVOLTAGE PROTECTION

OVERCURRENT PROTECTION


NOTE: DECOUPLING CAPS,
PLACE CLOSE TO V+/V–

OVERVOLTAGES LIMITED TO +/–15.56V
Vf = 0.9V
Vz = 14.66V

TRANSISTOR POWER DISSIPATION:
(WORST CASE: OUPUTTING +15V, PIN SHORTED TO –15V)
Pq = (15V – –15V) * 50mA = 1.5W

MAX AVG Pq IS 275mW,
ALLOWABLE DUTY CYCLE IS 0.275 / 1.5 = 0.18
(10 SEC SHORT CIRCUIT OVER 1 MIN)

Vshunt = abs(10 * Ishunt * Rshunt)

Vlimit = 10 * Ilimit * Rshunt

CURRENT LIMIT LED

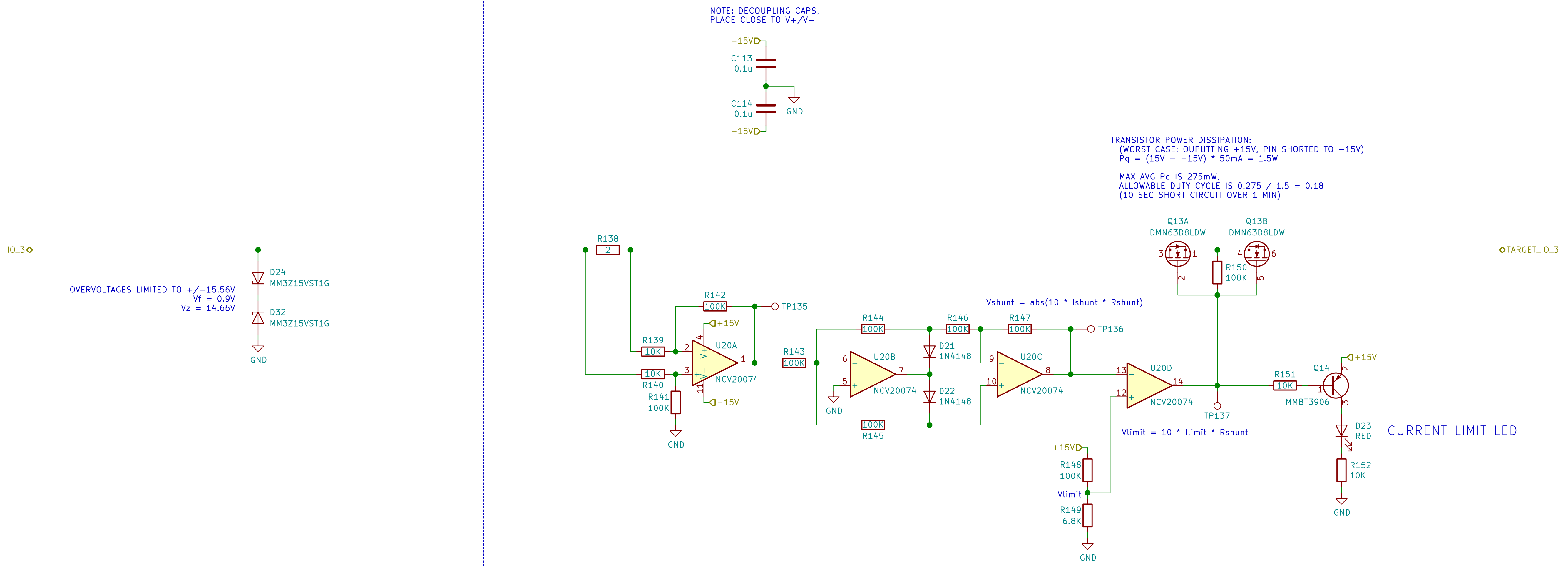
DT18 – I/O MASTER
THE UNIVERSITY OF AKRON
Sheet: /Circuit Protection – I/O Pin 1/
File: Circuit Protection – IO 1.sch

Title: CIRCUIT PROTECTION SUBSYSTEM – I/O PIN 1

Size: B	Date: 2020-02-07	**Rev: A**
KiCad E.D.A. kicad 5.1.5		Id: 5/10

OVERVOLTAGE PROTECTION

OVERCURRENT PROTECTION



NOTE: DECOUPLING CAPS,
PLACE CLOSE TO V+/V-

OVERVOLTAGES LIMITED TO +/-15.56V
Vf = 0.9V
Vz = 14.66V

TRANSISTOR POWER DISSIPATION:
(WORST CASE: OUPUTTING +15V, PIN SHORTED TO -15V)
Pq = (15V - -15V) * 50mA = 1.5W

MAX AVG Pq IS 275mW,
ALLOWABLE DUTY CYCLE IS 0.275 / 1.5 = 0.18
(10 SEC SHORT CIRCUIT OVER 1 MIN)

Vshunt = abs(10 * Ishunt * Rshunt)

Vlimit = 10 * Ilimit * Rshunt

CURRENT LIMIT LED

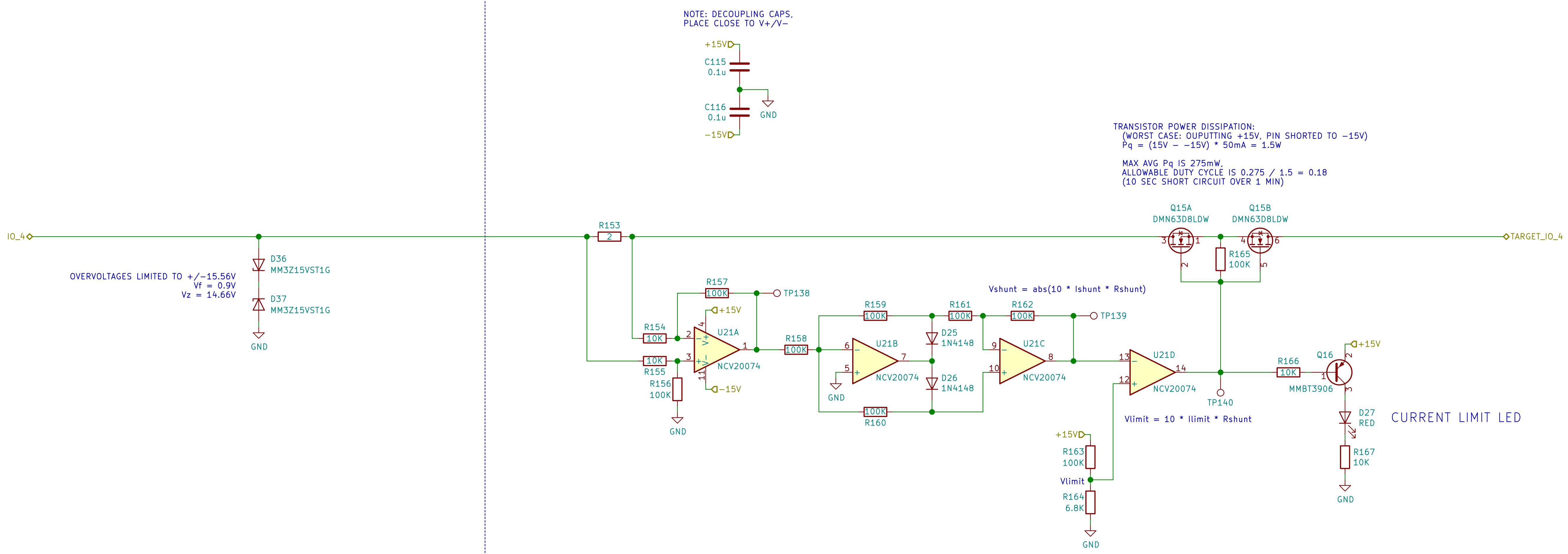
DT18 - I/O MASTER
THE UNIVERSITY OF AKRON
Sheet: /Circuit Protection - I/O Pin 3/
File: Circuit Protection - IO 3.sch

Title: CIRCUIT PROTECTION SUBSYSTEM - I/O PIN 3

Size: B
Date: 2020-02-07
Rev: A
KiCad E.D.A. kicad 5.1.5
Id: 6/10

OVERVOLTAGE PROTECTION

OVERCURRENT PROTECTION



NOTE: DECOUPLING CAPS,
PLACE CLOSE TO V+/V−

OVERVOLTAGES LIMITED TO +/−15.56V
Vf = 0.9V
Vz = 14.66V

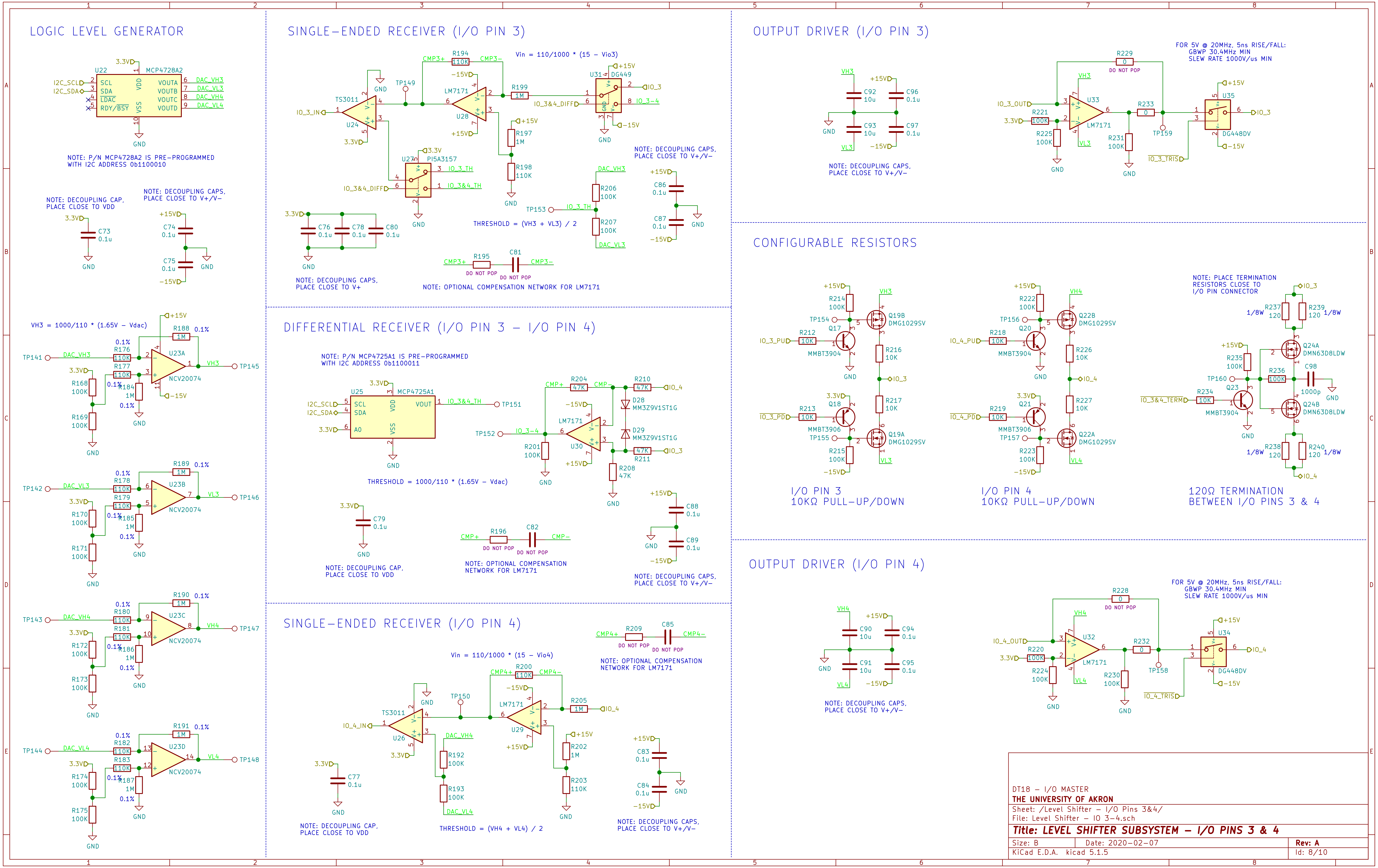
TRANSISTOR POWER DISSIPATION:
(WORST CASE: OUPUTTING +15V, PIN SHORTED TO −15V)
Pq = (15V − −15V) * 50mA = 1.5W

MAX AVG Pq IS 275mW,
ALLOWABLE DUTY CYCLE IS 0.275 / 1.5 = 0.18
(10 SEC SHORT CIRCUIT OVER 1 MIN)

Vshunt = abs(10 * Ishunt * Rshunt)

Vlimit = 10 * Ilimit * Rshunt

DT18 − I/O MASTER
THE UNIVERSITY OF AKRON
Sheet: /Circuit Protection − I/O Pin 4/
File: Circuit Protection − IO 4.sch
Title: CIRCUIT PROTECTION SUBSYSTEM − I/O PIN 4
Size: B
Date: 2020−02−07
Rev: A
KiCad E.D.A. kicad 5.1.5
Id: 7/10



NOTE: P/N MCP4728A2 IS PRE-PROGRAMMED WITH I2C ADDRESS 0b1100010

NOTE: DECOUPLING CAP, PLACE CLOSE TO VDD

NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+/V-

NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+

NOTE: OPTIONAL COMPENSATION NETWORK FOR LM7171

NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+/V-

NOTE: P/N MCP4725A1 IS PRE-PROGRAMMED WITH I2C ADDRESS 0b1100011

NOTE: DECOUPLING CAP, PLACE CLOSE TO VDD

NOTE: OPTIONAL COMPENSATION NETWORK FOR LM7171

NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+/V-

NOTE: OPTIONAL COMPENSATION NETWORK FOR LM7171

NOTE: DECOUPLING CAP, PLACE CLOSE TO VDD

NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+/V-

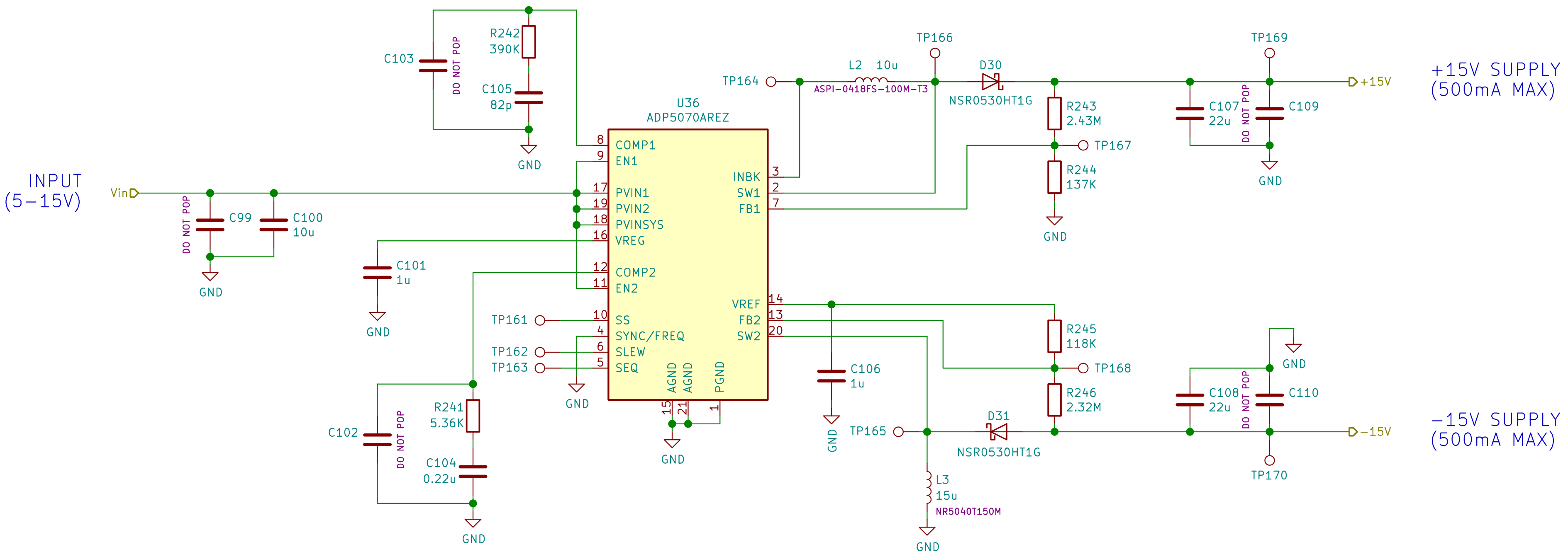
NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+/V-

NOTE: PLACE TERMINATION RESISTORS CLOSE TO I/O PIN CONNECTOR

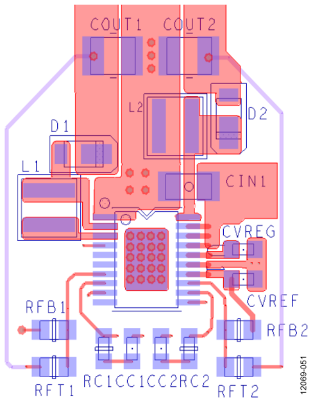
NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+/V-

DT18 – I/O MASTER
THE UNIVERSITY OF AKRON
Sheet: /Level Shifter – I/O Pins 3&4/
File: Level Shifter – IO 3-4.sch
Title: LEVEL SHIFTER SUBSYSTEM – I/O PINS 3 & 4
Size: B Date: 2020-02-07 Rev: A
KiCad E.D.A. kicad 5.1.5 Id: 8/10

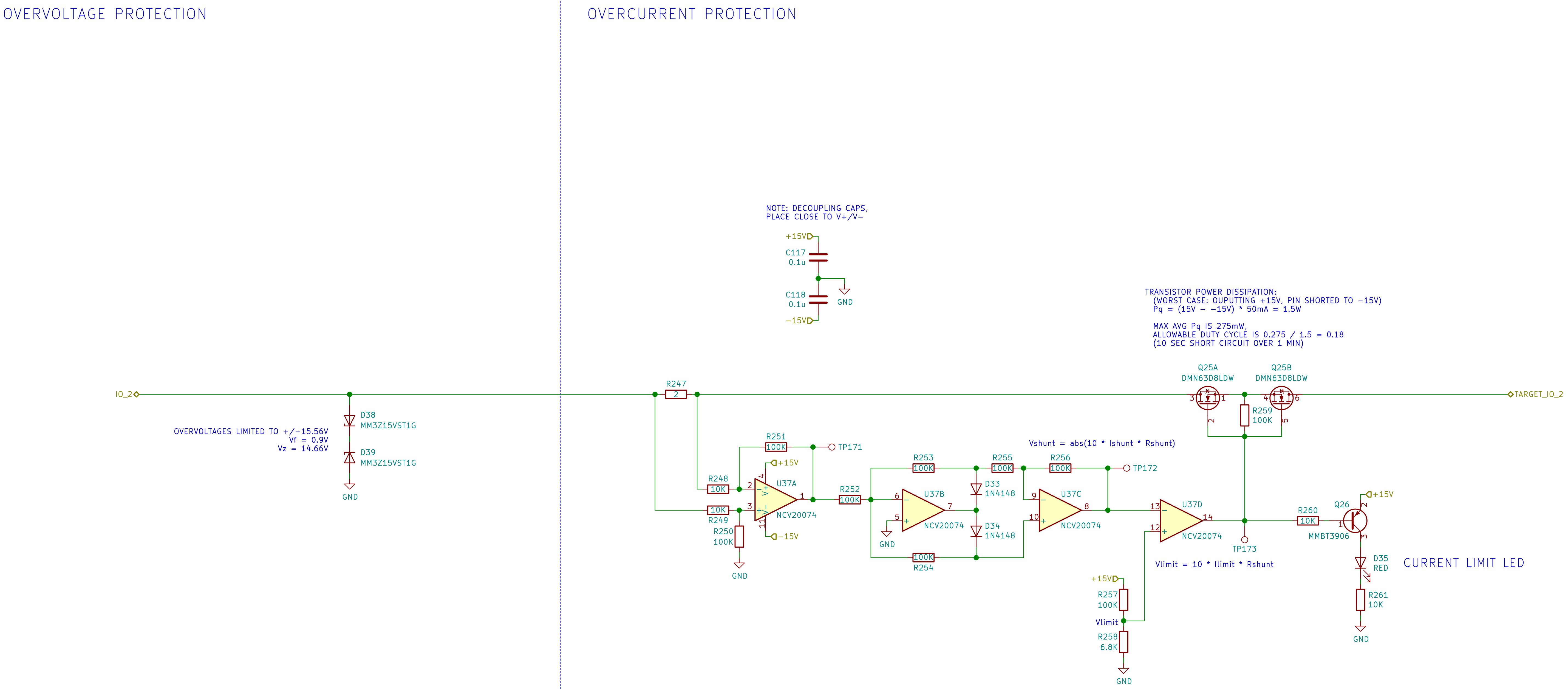
+/-15V REGULATOR



RECOMMENDED PCB LAYOUT



DT18 – I/O MASTER
THE UNIVERSITY OF AKRON
Sheet: /15V Regulator/
File: 15V Regulator.sch
Title: +/-15V REGULATOR
Size: B
Date: 2020-02-07
Rev: A
KiCad E.D.A. kicad 5.1.5
Id: 9/10



OVERVOLTAGES LIMITED TO +/-15.56V
Vf = 0.9V
Vz = 14.66V

NOTE: DECOUPLING CAPS,
PLACE CLOSE TO V+/V-

TRANSISTOR POWER DISSIPATION:
(WORST CASE: OUPUTTING +15V, PIN SHORTED TO -15V)
Pq = (15V - -15V) * 50mA = 1.5W

MAX AVG Pq IS 275mW.
ALLOWABLE DUTY CYCLE IS 0.275 / 1.5 = 0.18
(10 SEC SHORT CIRCUIT OVER 1 MIN)

Vshunt = abs(10 * Ishunt * Rshunt)

Vlimit = 10 * Ilimit * Rshunt

DT18 - I/O MASTER
THE UNIVERSITY OF AKRON
Sheet: /Circuit Protection - I/O Pin 2/
File: Circuit Protection - IO 2.sch

Title: CIRCUIT PROTECTION SUBSYSTEM - I/O PIN 2

Size: B
Date: 2020-02-07
Rev: A
KiCad E.D.A. kicad 5.1.5
Id: 10/10