TP4
KEYSTONE 5011
GND

TP16
Vin
D1
B130L
D2
B130L
TP17
Q27
DMP3099L
R262
100K
J1
PJ-037A
OPTIONAL DC INPUT
(12V, 500mA)
GND
TP18
J2
10118193
USB 2.0 INPUT
(5V, 500mA)
VBUS
D+
D-
ID
GND
Shield
C2
1uF
C1 0.47u
CHASSIS
GND

INPUT: 4.6-15V
U1
AZ1117-3.3
Vin
VI
VO
GND
3.3V
C3
0.1u
C4
10u
C5
22u
C6
0.1u
GND
3.3V REGULATOR

Sheet: 15V Regulator
Vin
+/-15V
REGULATOR
+15V
-15V
File: 15V Regulator.sch

TP19
3.3V

Sheet: Microcontroller
3.3V
USB_VBUS
USB_D+
USB_D-
I2C_SDA
I2C_SCL
IO_1_OUT
IO_1_IN
IO_1_TRIS
IO_1_PU
IO_1_PD
IO_2_OUT
IO_2_IN
IO_2_TRIS
IO_2_PU
IO_2_PD
IO_1&2_DIFF
IO_1&2_TERM
IO_3_OUT
IO_3_IN
IO_3_TRIS
IO_3_PU
IO_3_PD
IO_4_OUT
IO_4_IN
IO_4_TRIS
IO_4_PU
IO_4_PD
IO_3&4_DIFF
IO_3&4_TERM
Vout_SETPOINT
MICROCONTROLLER
File: Microcontroller.sch

Sheet: Level Shifter - I/O Pins 1&2
3.3V
+15V
-15V
I2C_SDA
I2C_SCL
IO_1_OUT
IO_1_IN
IO_1_TRIS
IO_1_PU
IO_1_PD
IO_2_OUT
IO_2_IN
IO_2_TRIS
IO_2_PU
IO_2_PD
IO_1&2_DIFF
IO_1&2_TERM
LEVEL SHIFTER
File: Level Shifter - IO 1-2.sch

Sheet: Level Shifter - I/O Pins 3&4
3.3V
+15V
-15V
I2C_SDA
I2C_SCL
IO_3_OUT
IO_3_IN
IO_3_TRIS
IO_3_PU
IO_3_PD
IO_4_OUT
IO_4_IN
IO_4_TRIS
IO_4_PU
IO_4_PD
IO_3&4_DIFF
IO_3&4_TERM
LEVEL SHIFTER
File: Level Shifter - IO 3-4.sch

Sheet: Circuit Protection - I/O Pin 1
+15V
-15V
IO_1
CIRCUIT
PROTECTION
TARGET_IO_1
File: Circuit Protection - IO 1.sch

Sheet: Circuit Protection - I/O Pin 2
+15V
-15V
IO_2
CIRCUIT
PROTECTION
TARGET_IO_2
File: Circuit Protection - IO 2.sch

Sheet: Circuit Protection - I/O Pin 3
+15V
-15V
IO_3
CIRCUIT
PROTECTION
TARGET_IO_3
File: Circuit Protection - IO 3.sch

Sheet: Circuit Protection - I/O Pin 4
+15V
-15V
IO_4
CIRCUIT
PROTECTION
TARGET_IO_4
File: Circuit Protection - IO 4.sch

Sheet: Adjustable Regulator
3.3V
Vin
SETPOINT
3.3 - 15V
ADJUSTABLE
REGULATOR
Vout
File: Adjustable Regulator.sch

POWER SUPPLY LEDs
3.3V
D3
ORANGE
R5
1K
+15V
D4
BLUE
R6
10K
-15V
D5
BLUE
R7
10K
Vout
D6
GREEN
R8
4.7K
GND

J3
0.1" HDR
I/O PIN 1
I/O PIN 2
I/O PIN 3
I/O PIN 4
Vout
GND
I/O PINS
TO TARGET DEVICE

PWR_FLAG
Vin
+15V
-15V
CHASSIS

DO NOT POP
H1
H2
H3
H4
CHASSIS

DT18 - I/O MASTER
THE UNIVERSITY OF AKRON
Sheet: /
File: io-master.sch
Title: I/O MASTER v1
Size: B
Date: 2020-02-04
Rev: A
KiCad E.D.A. kicad 5.1.5
Id: 1/10

STM32H7 MICROCONTROLLER

NOTE: DECOUPLING CAPS, PLACE CLOSE TO VDD

3.3V C8 4.7u C16 0.1u C19 0.1u C22 0.1u C24 0.1u C26 0.1u — GND
3.3V C9 0.1u C17 0.1u C20 0.1u C23 0.1u C25 0.1u C27 0.1u — GND

NOTE: DECOUPLING CAPS, PLACE CLOSE TO VDD33_USB

3.3V C10 1u — GND

NOTE: DECOUPLING CAPS, PLACE CLOSE TO VDDA

3.3V C11 1u C15 0.1u C18 1u C21 0.1u — GND

NOTE: PLACE CRYSTAL CLOSE TO OSC_OUT/OSC_IN

C12 20p — OSC_OUT — Y1 48MHz — R9 1M DO NOT POP — OSC_IN — C13 20p — GND

NOTE: DECOUPLING CAPS, PLACE CLOSE TO VCAP1/VCAP2

VCAP — C7 2.2u C14 2.2u — GND

RESET BUTTON

SW2 EVQ-Q2B03W — C28 0.1u — GND

BOOT SWITCH

3.3V — SW1 JS202011SCQN — R43 10K — GND

IO_1_OUT IO_2_OUT IO_1_TRIS IO_2_TRIS IO_1&2_DIFF IO_1_PU IO_2_PU IO_3_OUT IO_4_OUT IO_3_TRIS IO_4_TRIS IO_3&4_DIFF IO_3_PU IO_4_PU
R10 R12 R14 R15 R17 R20 R23 R25 R31 R34 R36 R38 R41 R42 100R — GND

3.3V R16 4.7K R18 4.7K R21 R24 R26 R32 R35 R37 100R
I2C_SCL I2C_SDA IO_1_PD IO_2_PD IO_1&2_TERM IO_3_PD IO_4_PD IO_3&4_TERM

IO_1_TRIS IO_1_IN — R11 R13 1K — D7 YELLOW/GREEN — IO_1_OUT — GND
IO_2_TRIS IO_2_IN — R19 R22 1K — D8 YELLOW/GREEN — IO_2_OUT — GND
IO_3_TRIS IO_3_IN — R30 R33 1K — D9 YELLOW/GREEN — IO_3_OUT — GND
IO_4_TRIS IO_4_IN — R39 R40 1K — D11 YELLOW/GREEN — IO_4_OUT — GND

RGB STATUS LED

STATUS_R — R27 330 — D10 RGB
STATUS_G — R28 330
STATUS_B — R29 330 — GND

3.3V — FB1 MZ1608-102Y — VDDA

U2 STM32H743ZITx

		VBAT	6
3.3V		VDD	17
		VDD	30
		VDD	39
		VDD	52
		VDD	62
		VDD	72
		VDD	84
		VDD	108
		VDD	121
		VDD	131
		VDD	144
		VDD33_USB	95
		VDDA	33
	NRST		25
	PDR_ON		143
	BOOT0		138
VCAP	VCAP1		71
	VCAP2		106
VDDA	VREF+		32
OSC_OUT	PH0		23
OSC_IN	PH1		24
IO_5_PU	PG0		56
IO_5_PD	PG1		57
IO_6_PU	PG2		87
IO_6_PD	PG3		88
IO_7_PU	PG4		89
IO_7_PD	PG5		90
IO_8_PU	PG6		91
IO_8_PD	PG7		92
	PG8		93
	PG9		124
	PG10		125
	PG11		126
	PG12		127
	PG13		128
	PG14		129
	PG15		132
STATUS_R	PF0		10
STATUS_G	PF1		11
STATUS_B	PF2		12
	PF3		13
	PF4		14
	PF5		15
	PF6		18
	PF7		19
	PF8		20
	PF9		21
	PF10		22
	PF11		49
	PF12		50
	PF13		53
	PF14		54
	PF15		55
	PE0		141
	PE1		142
	PE2		1
	PE3		2
	PE4		3
	PE5		4
	PE6		5
	PE7		58
IO_1_IN	PE8		59
IO_2_IN	PE9		60
IO_3_IN	PE10		63
IO_4_IN	PE11		64
IO_5_IN	PE12		65
IO_6_IN	PE13		66
IO_7_IN	PE14		67
IO_8_IN	PE15		68
		VSS	16
		VSS	38
		VSS	51
		VSS	61
		VSS	83
		VSS	94
		VSS	107
		VSS	120
		VSS	130
		VSSA	31
	PA0		34
	PA1		35
	PA2		36
	PA3		37
	PA4		40
	PA5		41
	PA6		42
	PA7		43
	PA8		100
	PA9		101
	PA10		102
	PA11		103
	PA12		104
	PA13		105
	PA14		109
	PA15		110
	PB0		46
	PB1		47
	PB2		48
	PB3		133
	PB4		134
	PB5		135
	PB6		136
	PB7		137
	PB8		139
	PB9		140
	PB10		69
	PB11		70
	PB12		73
	PB13		74
	PB14		75
	PB15		76
	PC0		26
	PC1		27
	PC2_C		28
	PC3_C		29
	PC4		44
	PC5		45
	PC6		96
	PC7		97
	PC8		98
	PC9		99
	PC10		111
	PC11		112
	PC12		113
	PC13		7
	PC14		8
	PC15		9
	PD0		114
	PD1		115
	PD2		116
	PD3		117
	PD4		118
	PD5		119
	PD6		122
	PD7		123
	PD8		77
	PD9		78
	PD10		79
	PD11		80
	PD12		81
	PD13		82
	PD14		85
	PD15		86

PA0 IO_1_OUT
PA1 IO_2_OUT
PA2 IO_3_OUT
PA3 ULPI_D0
PA4 Vout_SETPOINT
PA5 ULPI_CK
PA6 IO_1_PU
PA7 IO_8_OUT — TP81
PA8 I2C_SCL
PA9 UART_TXO — TP82
PA10 UART_RXI — TP83
PA11 USB_FS_DM — TP84
PA12 USB_FS_DP — TP85
PA13 TMS_SWDIO
PA14 TCK_SWDCLK
PA15 TDI

PB0 ULPI_D1
PB1 ULPI_D2
PB2 IO_1_PD
PB3 TDO_SWO
PB4 nRESET
PB5 ULPI_D7
PB6 IO_2_PU
PB7 IO_5_OUT — TP86
PB8 IO_6_OUT — TP87
PB9 IO_7_OUT — TP88
PB10 ULPI_D3
PB11 ULPI_D4
PB12 ULPI_D5
PB13 ULPI_D6
PB14 IO_2_PD
PB15 IO_3_PU

PC0 ULPI_STP
PC1 IO_3_PD
PC2_C ULPI_DIR
PC3_C ULPI_NXT
PC4 IO_1&2_DIFF
PC5 IO_1&2_TERM
PC6 IO_4_OUT
PC7 IO_3&4_DIFF
PC8 IO_3&4_TERM
PC9 I2C_SDA
PC10 IO_4_PU
PC11 IO_7&8_DIFF — TP89
PC12 IO_7&8_TERM — TP90
PC13 IO_4_PD
PC14 IO_5&6_DIFF — TP91
PC15 IO_5&6_TERM — TP92

PD0 IO_1_OUT
PD1 IO_2_OUT
PD2 IO_3_OUT
PD3 IO_4_OUT
PD4 IO_5_OUT — TP93
PD5 IO_6_OUT — TP94
PD6 IO_7_OUT — TP95
PD7 IO_8_OUT — TP96
PD8 IO_1_TRIS
PD9 IO_2_TRIS
PD10 IO_3_TRIS
PD11 IO_4_TRIS
PD12 IO_5_TRIS — TP97
PD13 IO_6_TRIS — TP98
PD14 IO_7_TRIS — TP99
PD15 IO_8_TRIS — TP100

TP20 IO_5_PU
TP21 IO_5_PD
TP22 IO_6_PU
TP23 IO_6_PD
TP24 IO_7_PU
TP25 IO_7_PD
TP26 IO_8_PU
TP27 IO_8_PD
TP28 TP29 TP30 TP31 TP32 TP33 TP34 TP35
TP36 TP37 TP38 TP39 TP40 TP41 TP42 TP43 TP44 TP45 TP46 TP47 TP48
TP49 TP50 TP51 TP52 TP53 TP54 TP55 TP56

MCU ALTERNATE PIN FUNCTIONS:
- PA0: TIM2_CH1
- PA1: TIM5_CH2
- PA2: TIM15_CH1
- PA4: DAC_OUT1
- PA7: TIM14_CH1
- PA8: I2C1_SCL
- PA9: USART1_TX
- PA10: USART1_RX
- PB7: TIM4_CH2
- PB8: TIM16_CH1
- PB9: TIM17_CH1
- PC6: TIM3_CH1
- PC9: I2C1_SDA

JTAG/SERIAL WIRE DEBUG

3.3V — J4 0.1" HDR — GND

VCC	1	2	TMS_SWDIO — SWD I/O
GND	3	4	TCK_SWDCLK — SWD CLOCK
GND	5	6	TDO_SWO — SWD TRACE
KEY	7	8	TDI — JTAG DATA IN
GNDdetect	9	10	nRESET — JTAG RESET

TP61 IO_1_OUT — TP69 IO_1_TRIS — TP77 IO_1_PU — TP104 IO_1_PD
TP62 IO_2_OUT — TP70 IO_2_TRIS — TP78 IO_2_PU — TP105 IO_2_PD
TP63 IO_3_OUT — TP71 IO_3_TRIS — TP79 IO_3_PU — TP106 IO_3_PD
TP64 IO_4_OUT — TP72 IO_4_TRIS — TP80 IO_4_PU — TP107 IO_4_PD

TP65 IO_1_IN — TP73 IO_1&2_DIFF — TP101 I2C_SCL
TP66 IO_2_IN — TP74 IO_1&2_TERM — TP102 I2C_SDA
TP67 IO_3_IN — TP75 IO_3&4_DIFF — TP103 Vout_SETPOINT
TP68 IO_4_IN — TP76 IO_3&4_TERM

USB 2.0 HIGH SPEED PHY

NOTE: DECOUPLING CAPS, PLACE CLOSE TO VDD3.3

3.3V C31 0.1u C35 0.1u C36 0.1u C38 0.1u — GND

3.3V — U3 USB3300-EZK

USB_VBUS — R44 820 — D12 DDZ5V6ASF — GND
USB_D- — D-
USB_D+ — D+

	VDD33		6
	VDD33		16
	VDD33		25
	VDD33		30
	VBUS		4
	DM	D-	8
	DP	D+	7
	ID		5
XO	XO		27
XI	XI		28
	CPEN		3
	EXTVBUS		10
3.3V	REG_EN		31
	RBIAS		32
	GND		1
	GND		2
	GND		33
	VDD1.8		15
	VDD1.8		26
	VDDA1.8		29
	DATA7	ULPI_D7	17
	DATA6	ULPI_D6	18
	DATA5	ULPI_D5	19
	DATA4	ULPI_D4	20
	DATA3	ULPI_D3	21
	DATA2	ULPI_D2	22
	DATA1	ULPI_D1	23
	DATA0	ULPI_D0	24
	NXT	ULPI_NXT	11
	DIR	ULPI_DIR	12
	STP	ULPI_STP	13
	CLKOUT	ULPI_CK	14
	RESET	TP174	9

R45 12K — GND
GND GND GND — GND

NOTE: PLACE CRYSTAL CLOSE TO XO/XI

C33 20p — XO — Y2 24MHz — R46 1M — XI — C34 20p — GND

NOTE: DECOUPLING CAPS, PLACE CLOSE TO VDD1.8

VDD1.8 — C29 4.7u C30 0.1u C32 0.1u — GND

NOTE: DECOUPLING CAPS, PLACE CLOSE TO VDDA1.8

VDDA1.8 — C37 4.7u C39 0.1u — GND

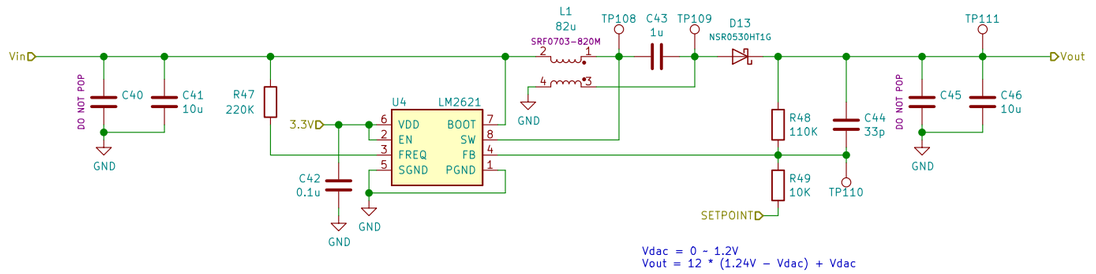
DT18 – I/O MASTER
THE UNIVERSITY OF AKRON
Sheet: /Microcontroller/
File: Microcontroller.sch

Title: MICROCONTROLLER SUBSYSTEM

Size: B	Date: 2020-02-04	Rev: A
KiCad E.D.A. kicad 5.1.5		Id: 2/10

3.3–15V ADJUSTABLE REGULATOR

INPUT
(1.2–14V)



TARGET DEVICE SUPPLY
(3.3–15V ADJ, 100mA MAX)

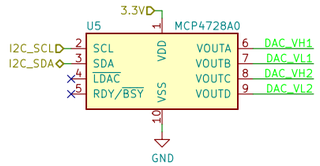
Vdac = 0 ~ 1.2V
Vout = 12 * (1.24V – Vdac) + Vdac

DT18 – I/O MASTER
THE UNIVERSITY OF AKRON

Sheet: /Adjustable Regulator/	
File: Adjustable Regulator.sch	
Title: 3.3–15V ADJUSTABLE REGULATOR	
Size: B	Date: 2020–02–04
KiCad E.D.A. kicad 5.1.5	Id: 3/10

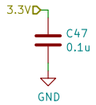
Rev: A

LOGIC LEVEL GENERATOR

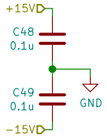


NOTE: P/N MCP4728A0 IS PRE-PROGRAMMED WITH I2C ADDRESS 0b1100000

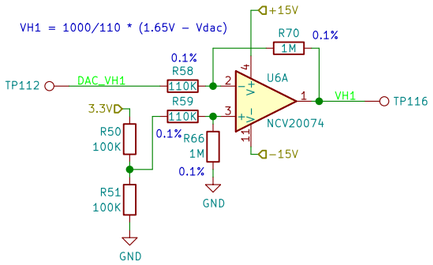
NOTE: DECOUPLING CAP, PLACE CLOSE TO VDD

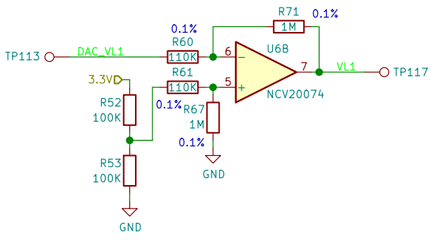


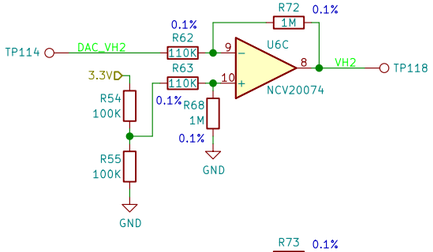
NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+/V-

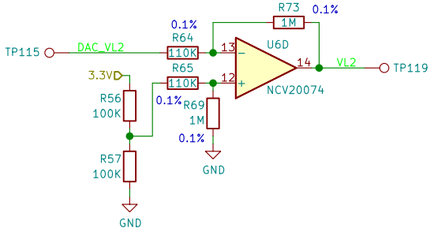


VH1 = 1000/110 * (1.65V - Vdac)



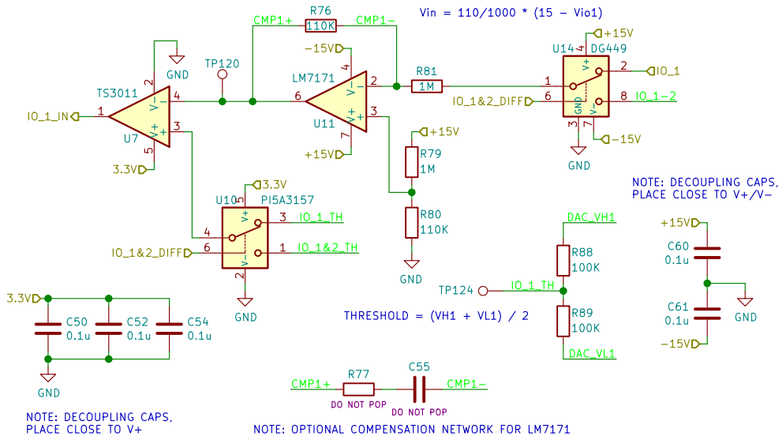






SINGLE-ENDED RECEIVER (I/O PIN 1)

Vin = 110/1000 * (15 - Vio1)



NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+/V-

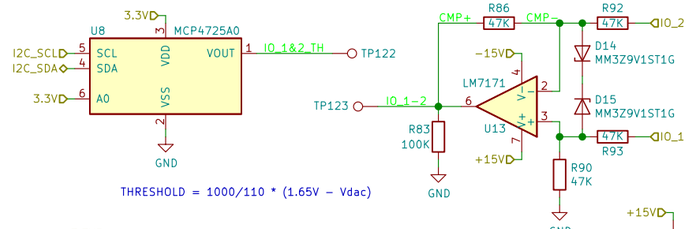
THRESHOLD = (VH1 + VL1) / 2

NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+

NOTE: OPTIONAL COMPENSATION NETWORK FOR LM7171

DIFFERENTIAL RECEIVER (I/O PIN 1 - I/O PIN 2)

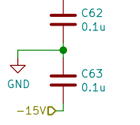
NOTE: P/N MCP4725A0 IS PRE-PROGRAMMED WITH I2C ADDRESS 0b1100001



THRESHOLD = 1000/110 * (1.65V - Vdac)

NOTE: DECOUPLING CAP, PLACE CLOSE TO VDD

NOTE: OPTIONAL COMPENSATION NETWORK FOR LM7171

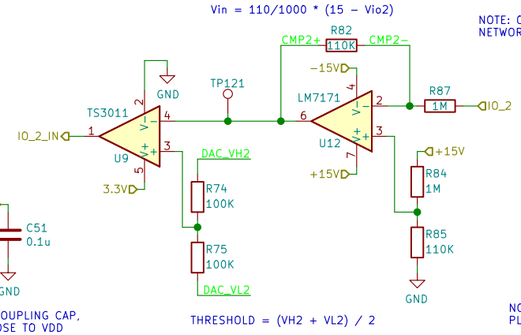


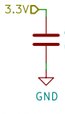
NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+/V-

SINGLE-ENDED RECEIVER (I/O PIN 2)

NOTE: OPTIONAL COMPENSATION NETWORK FOR LM7171

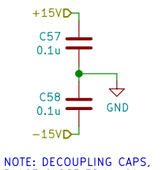
Vin = 110/1000 * (15 - Vio2)





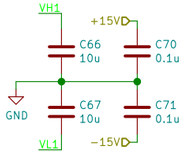
NOTE: DECOUPLING CAP, PLACE CLOSE TO VDD

THRESHOLD = (VH2 + VL2) / 2



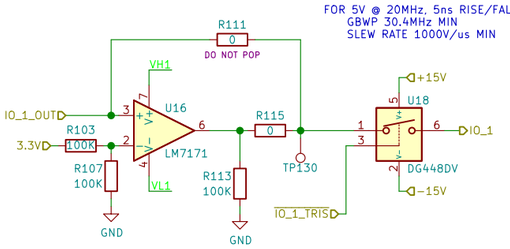
NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+/V-

OUTPUT DRIVER (I/O PIN 1)

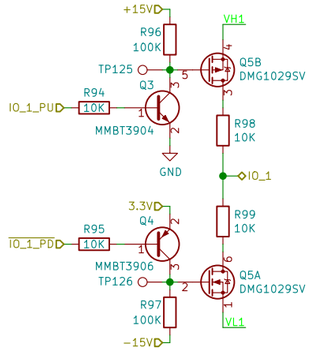


NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+/V-

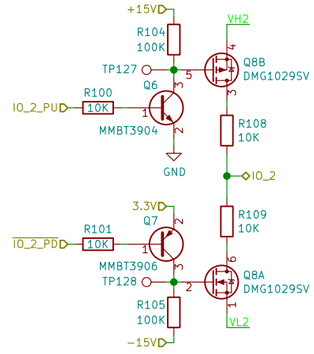
FOR 5V @ 20MHz, 5ns RISE/FALL:
GBWP 30.4MHz MIN
SLEW RATE 1000V/us MIN



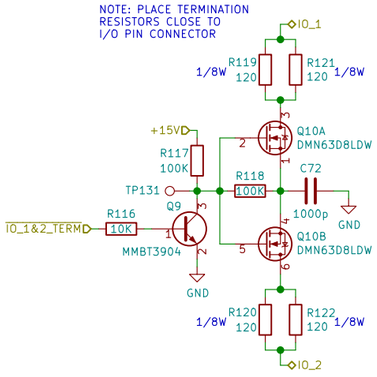
CONFIGURABLE RESISTORS



I/O PIN 1
10KΩ PULL-UP/DOWN

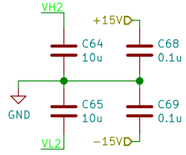


I/O PIN 2
10KΩ PULL-UP/DOWN



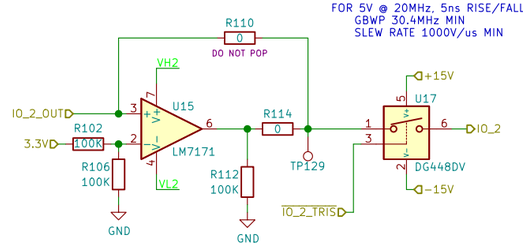
120Ω TERMINATION
BETWEEN I/O PINS 1 & 2

OUTPUT DRIVER (I/O PIN 2)



NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+/V-

FOR 5V @ 20MHz, 5ns RISE/FALL:
GBWP 30.4MHz MIN
SLEW RATE 1000V/us MIN



DT18 - I/O MASTER
THE UNIVERSITY OF AKRON

Sheet: /Level Shifter - I/O Pins 1&2/
File: Level Shifter - IO 1-2.sch

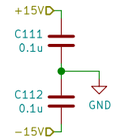
Title: LEVEL SHIFTER SUBSYSTEM - I/O PINS 1 & 2

Size: B	Date: 2020-02-04	**Rev: A**
KiCad E.D.A. kicad 5.1.5		Id: 4/10

OVERVOLTAGE PROTECTION

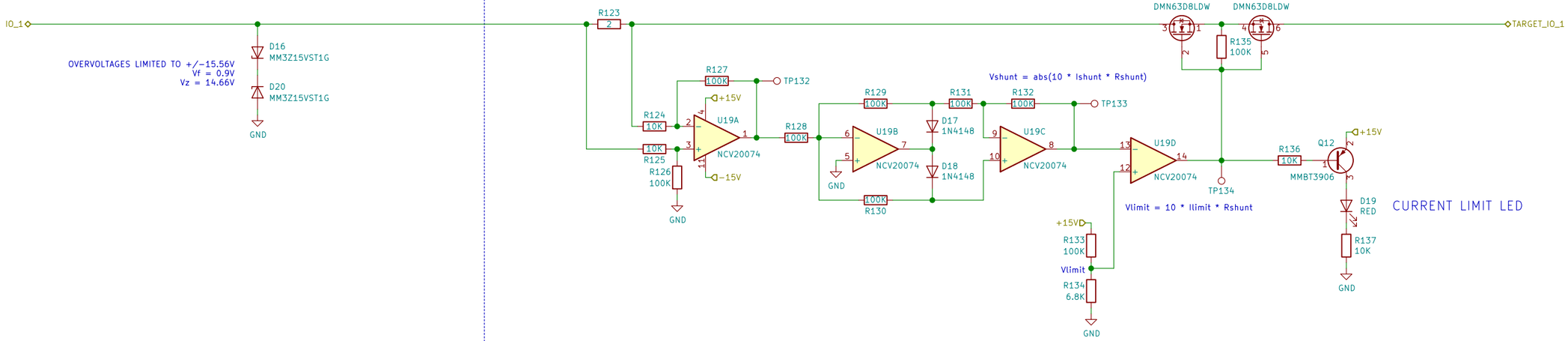
OVERCURRENT PROTECTION

NOTE: DECOUPLING CAPS,
PLACE CLOSE TO V+/V-



TRANSISTOR POWER DISSIPATION:
(WORST CASE: OUPUTTING +15V, PIN SHORTED TO -15V)
Pq = (15V - -15V) * 50mA = 1.5W

MAX AVG Pq IS 275mW.
ALLOWABLE DUTY CYCLE IS 0.275 / 1.5 = 0.18
(10 SEC SHORT CIRCUIT OVER 1 MIN)



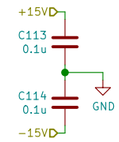
DT18 - I/O MASTER
THE UNIVERSITY OF AKRON

Sheet: /Circuit Protection - I/O Pin 1/		
File: Circuit Protection - IO 1.sch		
Title: CIRCUIT PROTECTION SUBSYSTEM - I/O PIN 1		
Size: B	Date: 2020-02-04	**Rev: A**
KiCad E.D.A. kicad 5.1.5		Id: 5/10

OVERVOLTAGE PROTECTION

OVERCURRENT PROTECTION

NOTE: DECOUPLING CAPS,
PLACE CLOSE TO V+/V−



TRANSISTOR POWER DISSIPATION:
(WORST CASE: OUPUTTING +15V, PIN SHORTED TO −15V)
Pq = (15V − −15V) * 50mA = 1.5W

MAX AVG Pq IS 275mW.
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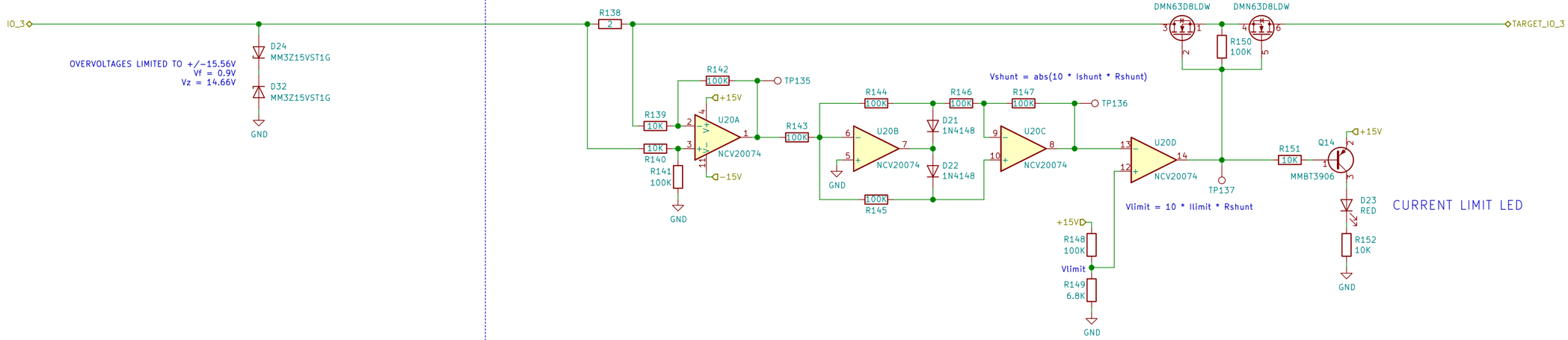
(10 SEC SHORT CIRCUIT OVER 1 MIN)



CURRENT LIMIT LED

DT18 – I/O MASTER
THE UNIVERSITY OF AKRON

Sheet: /Circuit Protection – I/O Pin 3/		
File: Circuit Protection – IO 3.sch		
Title: CIRCUIT PROTECTION SUBSYSTEM – I/O PIN 3		
Size: B	Date: 2020-02-04	**Rev: A**
KiCad E.D.A. kicad 5.1.5		Id: 6/10

OVERVOLTAGE PROTECTION

OVERCURRENT PROTECTION

NOTE: DECOUPLING CAPS,
PLACE CLOSE TO V+/V-

+15V
C115 0.1u
C116 0.1u
GND
-15V

TRANSISTOR POWER DISSIPATION:
(WORST CASE: OUPUTTING +15V, PIN SHORTED TO -15V)
Pq = (15V - -15V) * 50mA = 1.5W

MAX AVG Pq IS 275mW.
ALLOWABLE DUTY CYCLE IS 0.275 / 1.5 = 0.18
(10 SEC SHORT CIRCUIT OVER 1 MIN)

IO_4

OVERVOLTAGES LIMITED TO +/-15.56V
Vf = 0.9V
Vz = 14.66V

D36 MM3Z15VST1G
D37 MM3Z15VST1G
GND

R153 2

Q15A DMN63D8LDW
Q15B DMN63D8LDW
R165 100K

TARGET_IO_4

R157 100K
TP138
+15V
R154 10K
R155 10K
R156 100K
U21A NCV20074
-15V
GND
R158 100K

Vshunt = abs(10 * Ishunt * Rshunt)

R159 100K
R161 100K
R162 100K
TP139
U21B NCV20074
U21C NCV20074
D25 1N4148
D26 1N4148
R160 100K

U21D NCV20074
TP140
Vlimit = 10 * Ilimit * Rshunt

R166 10K
Q16 MMBT3906
+15V
D27 RED
R167 10K
GND

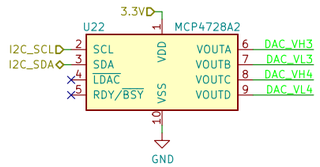
CURRENT LIMIT LED

+15V
R163 100K
Vlimit
R164 6.8K
GND

DT18 - I/O MASTER
THE UNIVERSITY OF AKRON

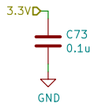
Sheet: /Circuit Protection - I/O Pin 4/		
File: Circuit Protection - IO 4.sch		
Title: CIRCUIT PROTECTION SUBSYSTEM - I/O PIN 4		
Size: B	Date: 2020-02-04	**Rev: A**
KiCad E.D.A. kicad 5.1.5		Id: 7/10

LOGIC LEVEL GENERATOR

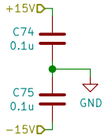


NOTE: P/N MCP4728A2 IS PRE-PROGRAMMED WITH I2C ADDRESS 0b1100010

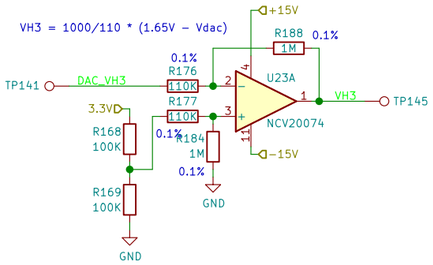
NOTE: DECOUPLING CAP, PLACE CLOSE TO VDD

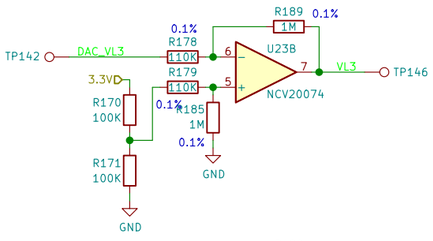


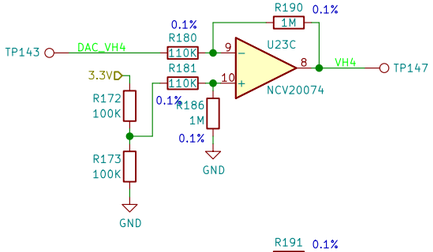
NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+/V-

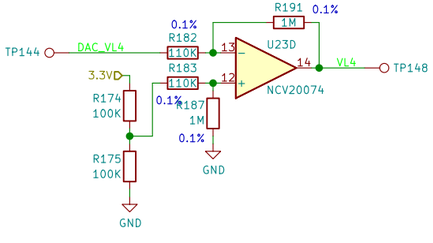


VH3 = 1000/110 * (1.65V - Vdac)



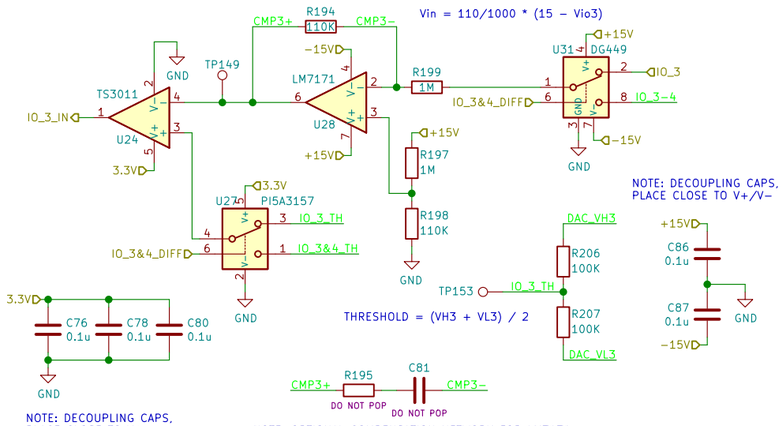






SINGLE-ENDED RECEIVER (I/O PIN 3)

Vin = 110/1000 * (15 - Vio3)



NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+/V-

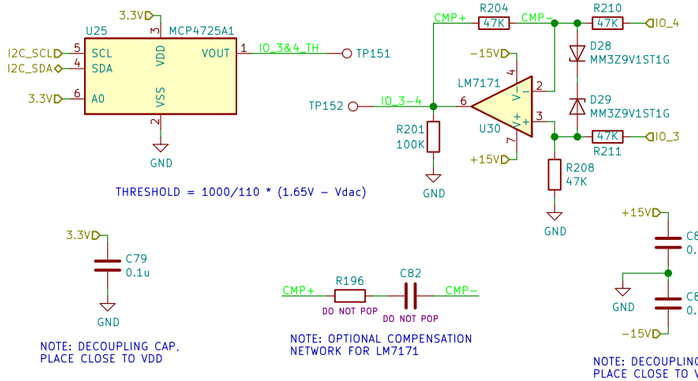
THRESHOLD = (VH3 + VL3) / 2

NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+

NOTE: OPTIONAL COMPENSATION NETWORK FOR LM7171

DIFFERENTIAL RECEIVER (I/O PIN 3 - I/O PIN 4)

NOTE: P/N MCP4725A1 IS PRE-PROGRAMMED WITH I2C ADDRESS 0b1100011



THRESHOLD = 1000/110 * (1.65V - Vdac)

NOTE: DECOUPLING CAP, PLACE CLOSE TO VDD

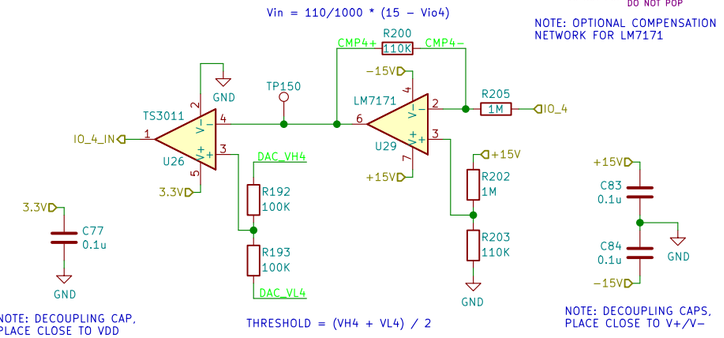
NOTE: OPTIONAL COMPENSATION NETWORK FOR LM7171

NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+/V-

SINGLE-ENDED RECEIVER (I/O PIN 4)

NOTE: OPTIONAL COMPENSATION NETWORK FOR LM7171

Vin = 110/1000 * (15 - Vio4)

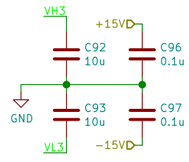


NOTE: DECOUPLING CAP, PLACE CLOSE TO VDD

THRESHOLD = (VH4 + VL4) / 2

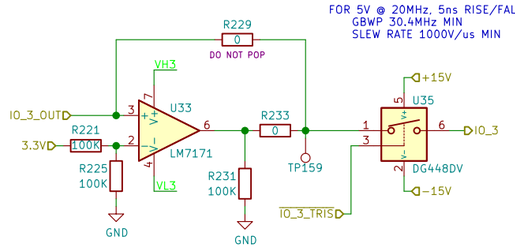
NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+/V-

OUTPUT DRIVER (I/O PIN 3)

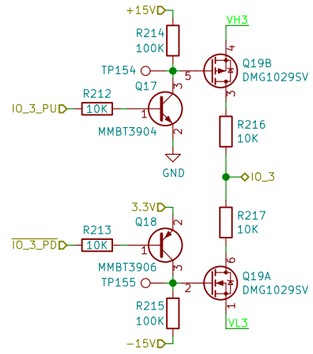


NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+/V-

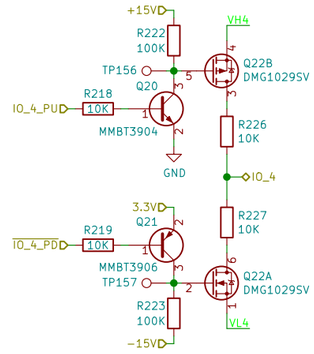
FOR 5V @ 20MHz, 5ns RISE/FALL:
GBWP 30.4MHz MIN
SLEW RATE 1000V/us MIN



CONFIGURABLE RESISTORS

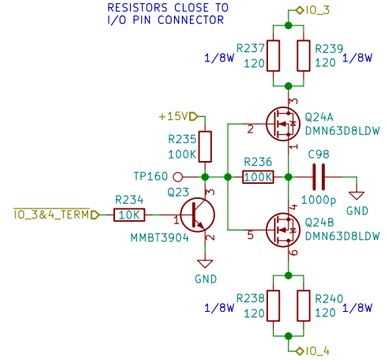


I/O PIN 3
10KΩ PULL-UP/DOWN



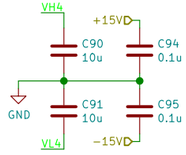
I/O PIN 4
10KΩ PULL-UP/DOWN

NOTE: PLACE TERMINATION RESISTORS CLOSE TO I/O PIN CONNECTOR



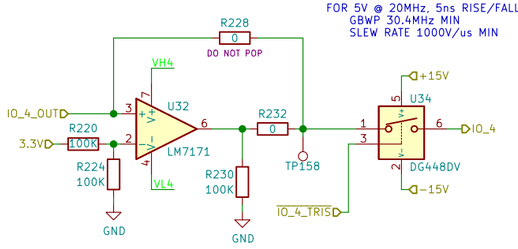
120Ω TERMINATION
BETWEEN I/O PINS 3 & 4

OUTPUT DRIVER (I/O PIN 4)



NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+/V-

FOR 5V @ 20MHz, 5ns RISE/FALL:
GBWP 30.4MHz MIN
SLEW RATE 1000V/us MIN



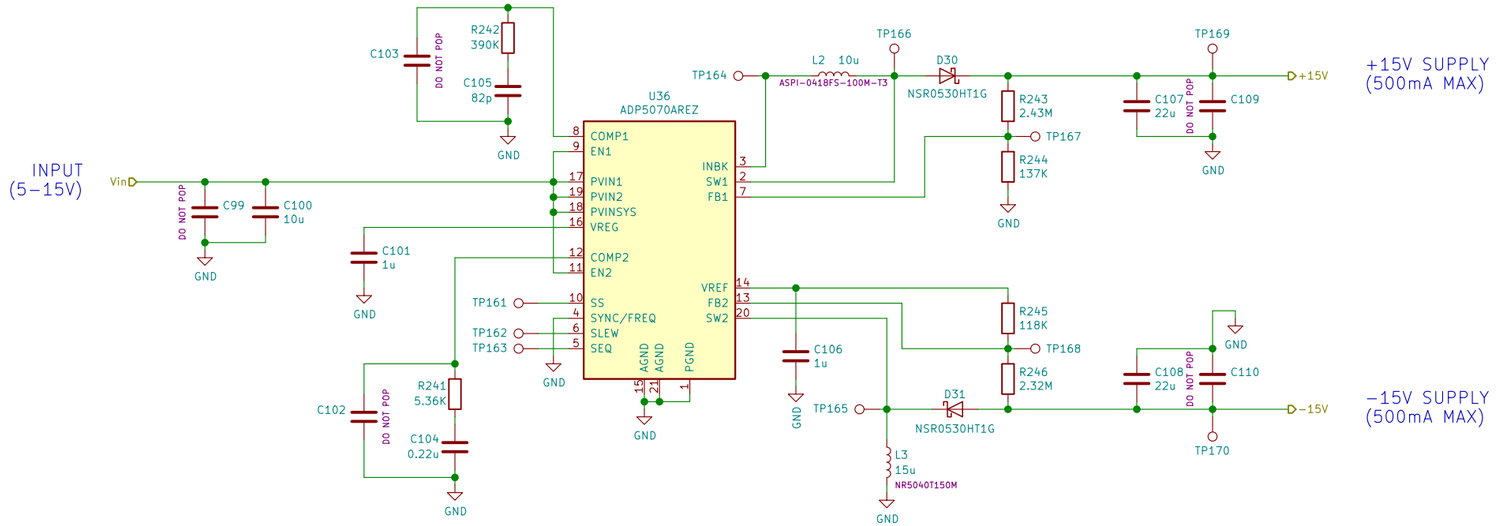
DT18 - I/O MASTER
THE UNIVERSITY OF AKRON

Sheet: /Level Shifter - I/O Pins 3&4/
File: Level Shifter - IO 3-4.sch

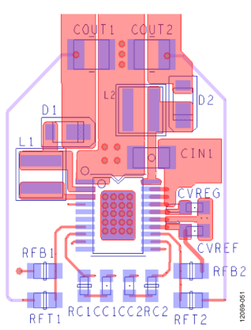
Title: LEVEL SHIFTER SUBSYSTEM - I/O PINS 3 & 4

Size: B	Date: 2020-02-04	**Rev: A**
KiCad E.D.A. kicad 5.1.5		Id: 8/10

+/−15V REGULATOR



RECOMMENDED PCB LAYOUT



DT18 – I/O MASTER
THE UNIVERSITY OF AKRON
Sheet: /15V Regulator/
File: 15V Regulator.sch

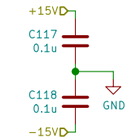
Title: +/−15V REGULATOR

Size: B	Date: 2020−02−04	**Rev: A**
KiCad E.D.A. kicad 5.1.5		Id: 9/10

OVERVOLTAGE PROTECTION

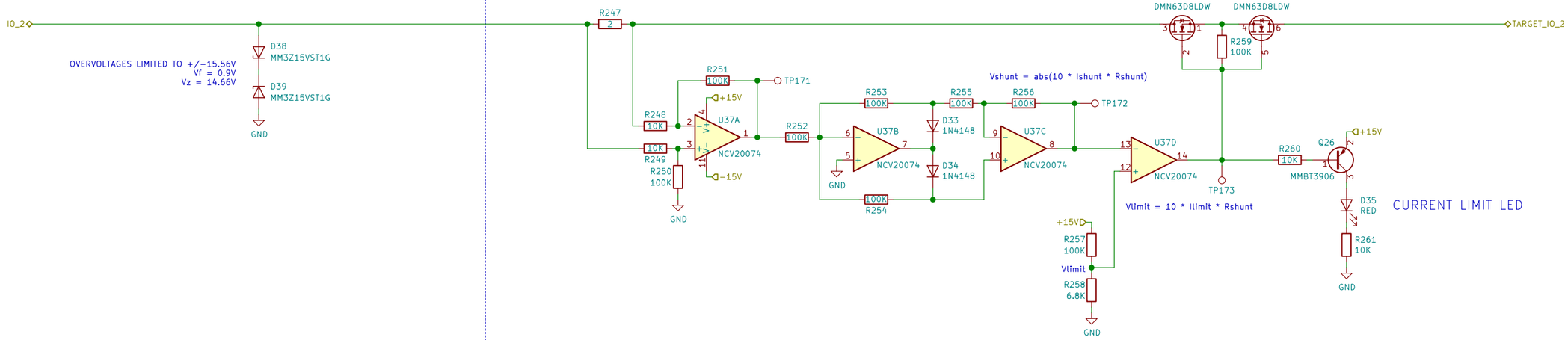
OVERCURRENT PROTECTION

NOTE: DECOUPLING CAPS,
PLACE CLOSE TO V+/V−



TRANSISTOR POWER DISSIPATION:
(WORST CASE: OUPUTTING +15V, PIN SHORTED TO −15V)
Pq = (15V − −15V) * 50mA = 1.5W

MAX AVG Pq IS 275mW.
ALLOWABLE DUTY CYCLE IS 0.275 / 1.5 = 0.18
(10 SEC SHORT CIRCUIT OVER 1 MIN)



CURRENT LIMIT LED

DT18 – I/O MASTER
THE UNIVERSITY OF AKRON

Sheet: /Circuit Protection – I/O Pin 2/
File: Circuit Protection – IO 2.sch

Title: CIRCUIT PROTECTION SUBSYSTEM – I/O PIN 2

Size: B	Date: 2020-02-04	**Rev: A**
KiCad E.D.A. kicad 5.1.5		Id: 10/10