TP4
KEYSTONE 5011
GND

TP16
Vin
F1
0.5A
D1
B130L
D2
B130L
TP17
Q27
DMP3099L
R262
100K
J1
54-00166
OPTIONAL DC INPUT
(12V, 500mA)
GND
TP18
TP19
J2
10118193
USB 2.0 INPUT
(5V, 500mA)
VBUS
D+
D-
ID
Shield
GND
C2
1uF
C1 0.47u
CHASSIS
GND

INPUT: 4.6-15V
U1
AZ1117-3.3
Vin
VI
VO
GND
C3
0.1u
C4
10u
C5
22u
C6
0.1u
3.3V
3.3V REGULATOR

Sheet: 15V Regulator
Vin
+/-15V
REGULATOR
+15V
-15V
File: 15V Regulator.sch

POWER SUPPLY LEDs
3.3V
+15V
-15V
Vout
D3
ORANGE
D4
BLUE
D5
BLUE
D6
GREEN
R5
1K
R6
10K
R7
10K
R8
4.7K
GND

Sheet: Microcontroller
3.3V
USB_VBUS
USB_D+
USB_D-
I2C_SDA
I2C_SCL
IO_1_OUT
IO_1_IN
IO_1_TRIS
IO_1_PU
IO_1_PD
IO_2_OUT
IO_2_IN
IO_2_TRIS
IO_2_PU
IO_2_PD
IO_1&2_DIFF
IO_1&2_TERM
IO_3_OUT
IO_3_IN
IO_3_TRIS
IO_3_PU
IO_3_PD
IO_4_OUT
IO_4_IN
IO_4_TRIS
IO_4_PU
IO_4_PD
IO_3&4_DIFF
IO_3&4_TERM
Vout_SETPOINT
MICROCONTROLLER
File: Microcontroller.sch

Sheet: Level Shifter - I/O Pins 1&2
3.3V
+15V
-15V
I2C_SDA
I2C_SCL
IO_1_OUT
IO_1_IN
IO_1_TRIS
IO_1_PU
IO_1_PD
IO_2_OUT
IO_2_IN
IO_2_TRIS
IO_2_PU
IO_2_PD
IO_1&2_DIFF
IO_1&2_TERM
LEVEL SHIFTER
File: Level Shifter - IO 1-2.sch

Sheet: Level Shifter - I/O Pins 3&4
3.3V
+15V
-15V
I2C_SDA
I2C_SCL
IO_3_OUT
IO_3_IN
IO_3_TRIS
IO_3_PU
IO_3_PD
IO_4_OUT
IO_4_IN
IO_4_TRIS
IO_4_PU
IO_4_PD
IO_3&4_DIFF
IO_3&4_TERM
LEVEL SHIFTER
File: Level Shifter - IO 3-4.sch

Sheet: Circuit Protection - I/O Pin 1
+15V
-15V
IO_1
CIRCUIT
PROTECTION
TARGET_IO_1
File: Circuit Protection - IO 1.sch

Sheet: Circuit Protection - I/O Pin 2
+15V
-15V
IO_2
CIRCUIT
PROTECTION
TARGET_IO_2
File: Circuit Protection - IO 2.sch

Sheet: Circuit Protection - I/O Pin 3
+15V
-15V
IO_3
CIRCUIT
PROTECTION
TARGET_IO_3
File: Circuit Protection - IO 3.sch

Sheet: Circuit Protection - I/O Pin 4
+15V
-15V
IO_4
CIRCUIT
PROTECTION
TARGET_IO_4
File: Circuit Protection - IO 4.sch

Sheet: Adjustable Regulator
3.3V
Vin
SETPOINT
3.3 - 15V
ADJUSTABLE
REGULATOR
Vout
File: Adjustable Regulator.sch

Vout
F2
0.1A
J3
0.1" HDR
I/O PIN 1
I/O PIN 2
I/O PIN 3
I/O PIN 4
Vout
GND
I/O PINS
TO TARGET DEVICE

PWR_FLAG
Vin
+15V
-15V
CHASSIS

DO NOT POP
H1
H2
H3
H4
CHASSIS

DT18 - I/O MASTER
THE UNIVERSITY OF AKRON
Sheet: /
File: io-master.sch
Title: I/O MASTER v1
Size: B
Date: 2020-02-10
Rev: A
KiCad E.D.A. kicad 5.1.5
Id: 1/10

STM32H7 MICROCONTROLLER

NOTE: DECOUPLING CAPS, PLACE CLOSE TO VDD

3.3V
C8 4.7u
C16 0.1u
C19 0.1u
C22 0.1u
C24 0.1u
C26 0.1u
GND

3.3V
C9 0.1u
C17 0.1u
C20 0.1u
C23 0.1u
C25 0.1u
C27 0.1u
GND

NOTE: DECOUPLING CAPS, PLACE CLOSE TO VDD33_USB

3.3V
C10 1u
GND

NOTE: DECOUPLING CAPS, PLACE CLOSE TO VDDA

3.3V
C11 1u
C15 0.1u
GND

NOTE: PLACE CRYSTAL CLOSE TO OSC_OUT/OSC_IN

C12 20p
Y1 48MHz
C13 20p
DO NOT POP
R9
OSC_OUT
OSC_IN
GND

NOTE: DECOUPLING CAPS, PLACE CLOSE TO VCAP1/VCAP2

VCAP
C7 2.2u
C14 2.2u
GND

JTAG/SERIAL WIRE DEBUG

3.3V
J4 0.1" HDR
VCC 1 — 2 TMS_SWDIO — SWD I/O
GND 3 — 4 TCK_SWDCLK — SWD CLOCK
GND 5 — 6 TDO_SWO — SWD TRACE
KEY 7 — 8 TDI — JTAG DATA IN
GNDdetect 9 — 10 nRESET — JTAG RESET
GND

RESET BUTTON

SW2 EVQ-Q2B03W
C28 0.1u
GND

BOOT SWITCH

3.3V
SW1 JS202011SCQN
R43 10K
GND

R10 R12 R14 R15 R17 R20 R23 R25 R31 R34 R36 R38 R41 R42 100R
IO_1_OUT IO_2_OUT IO_1_TRIS IO_2_TRIS IO_1&2_DIFF IO_1_PU IO_2_PU IO_3_OUT IO_4_OUT IO_3_TRIS IO_4_TRIS IO_3&4_DIFF IO_3_PU IO_4_PU
GND

R16 4.7K
R18 4.7K
R21 100R
R24 100R
R26 100R
R32 100R
R35 100R
R37 100R
I2C_SCL I2C_SDA IO_1_PD IO_2_PD IO_1&2_TERM IO_3_PD IO_4_PD IO_3&4_TERM

R11 R13 4K — IO_1_TRIS IO_1_IN — D7 YELLOW/GREEN — IO_1_OUT
R19 R22 4K — IO_2_TRIS IO_2_IN — D8 YELLOW/GREEN — IO_2_OUT
R30 R33 4K — IO_3_TRIS IO_3_IN — D9 YELLOW/GREEN — IO_3_OUT
R39 R40 4K — IO_4_TRIS IO_4_IN — D11 YELLOW/GREEN — IO_4_OUT
GND

RGB STATUS LED

D10 RGB
STATUS_R R27 330
STATUS_G R28 330
STATUS_B R29 330
GND

MCU ALTERNATE PIN FUNCTIONS:
- PA0: TIM2_CH1
- PA1: TIM5_CH2
- PA2: TIM15_CH1
- PA4: DAC_OUT1
- PA7: TIM14_CH1
- PA8: I2C1_SCL
- PA9: USART1_TX
- PA10: USART1_RX
- PB7: TIM4_CH2
- PB8: TIM16_CH1
- PB9: TIM17_CH1
- PC6: TIM3_CH1
- PC9: I2C1_SDA

TP61 IO_1_OUT — TP69 IO_1_TRIS — TP77 IO_1_PU — TP104 IO_1_PD
TP62 IO_2_OUT — TP70 IO_2_TRIS — TP78 IO_2_PU — TP105 IO_2_PD
TP63 IO_3_OUT — TP71 IO_3_TRIS — TP79 IO_3_PU — TP106 IO_3_PD
TP64 IO_4_OUT — TP72 IO_4_TRIS — TP80 IO_4_PU — TP107 IO_4_PD

3.3V
FB1 MZ1608-102Y
VDDA

U2 STM32H743ZITx

		PA0 34	IO_1_OUT
		PA1 35	IO_2_OUT
		PA2 36	IO_3_OUT
		PA3 37	ULPI_D0
		PA4 40	Vout_SETPOINT
		PA5 41	ULPI_CK
		PA6 42	IO_1_PU
		PA7 43	IO_8_OUT — TP81
		PA8 100	I2C_SCL
		PA9 101	UART_TXO — TP82
		PA10 102	UART_RXI — TP83
		PA11 103	USB_FS_DM — TP84
		PA12 104	USB_FS_DP — TP85
		PA13 105	TMS_SWDIO
		PA14 109	TCK_SWDCLK
		PA15 110	TDI
TP20 IO_5_PU	56 PG0	PB0 46	ULPI_D1
TP21 IO_5_PD	57 PG1	PB1 47	ULPI_D2
TP22 IO_6_PU	87 PG2	PB2 48	IO_1_PD
TP23 IO_6_PD	88 PG3	PB3 133	TDO_SWO
TP24 IO_7_PU	89 PG4	PB4 134	nRESET
TP25 IO_7_PD	90 PG5	PB5 135	ULPI_D7
TP26 IO_8_PU	91 PG6	PB6 136	IO_2_PU
TP27 IO_8_PD	92 PG7	PB7 137	IO_5_OUT — TP86
TP28	93 PG8	PB8 139	IO_6_OUT — TP87
TP29	124 PG9	PB9 140	IO_7_OUT — TP88
TP30	125 PG10	PB10 69	ULPI_D3
TP31	126 PG11	PB11 70	ULPI_D4
TP32	127 PG12	PB12 73	ULPI_D5
TP33	128 PG13	PB13 74	ULPI_D6
TP34	129 PG14	PB14 75	IO_2_PD
TP35	132 PG15	PB15 76	IO_3_PU
STATUS_R	10 PF0	PC0 26	ULPI_STP
STATUS_G	11 PF1	PC1 27	IO_3_PD
STATUS_B	12 PF2	PC2_C 28	ULPI_DIR
TP36	13 PF3	PC3_C 29	ULPI_NXT
TP37	14 PF4	PC4 44	IO_1&2_DIFF
TP38	15 PF5	PC5 45	IO_1&2_TERM
TP39	18 PF6	PC6 96	IO_4_OUT
TP40	19 PF7	PC7 97	IO_3&4_DIFF
TP41	20 PF8	PC8 98	IO_3&4_TERM
TP42	21 PF9	PC9 99	I2C_SDA
TP43	22 PF10	PC10 111	IO_4_PU
TP44	49 PF11	PC11 112	IO_7&8_DIFF — TP89
TP45	50 PF12	PC12 113	IO_7&8_TERM — TP90
TP46	53 PF13	PC13 7	IO_4_PD
TP47	54 PF14	PC14 8	IO_5&6_DIFF — TP91
TP48	55 PF15	PC15 9	IO_5&6_TERM — TP92
TP49	141 PE0	PD0 114	IO_1_OUT
TP50	142 PE1	PD1 115	IO_2_OUT
TP51	1 PE2	PD2 116	IO_3_OUT
TP52	2 PE3	PD3 117	IO_4_OUT
TP53	3 PE4	PD4 118	IO_5_OUT — TP93
TP54	4 PE5	PD5 119	IO_6_OUT — TP94
TP55	5 PE6	PD6 122	IO_7_OUT — TP95
TP56	58 PE7	PD7 123	IO_8_OUT — TP96
IO_1_IN	59 PE8	PD8 77	IO_1_TRIS
IO_2_IN	60 PE9	PD9 78	IO_2_TRIS
IO_3_IN	63 PE10	PD10 79	IO_3_TRIS
IO_4_IN	64 PE11	PD11 80	IO_4_TRIS
TP57 IO_5_IN	65 PE12	PD12 81	IO_5_TRIS — TP97
TP58 IO_6_IN	66 PE13	PD13 82	IO_6_TRIS — TP98
TP59 IO_7_IN	67 PE14	PD14 85	IO_7_TRIS — TP99
TP60 IO_8_IN	68 PE15	PD15 86	IO_8_TRIS — TP100

VBAT 6; VDD 17, 30, 39, 52, 62, 72, 84, 108, 121, 131, 144; VDDA 95; VDD33_USB 33
VSS 16, 38, 51, 61, 83, 94, 107, 120, 130, 31; VSSA

TP65 IO_1_IN — TP73 IO_1&2_DIFF — TP101 I2C_SCL
TP66 IO_2_IN — TP74 IO_1&2_TERM — TP102 I2C_SDA
TP67 IO_3_IN — TP75 IO_3&4_DIFF — TP103 Vout_SETPOINT
TP68 IO_4_IN — TP76 IO_3&4_TERM

USB 2.0 HIGH SPEED PHY

NOTE: DECOUPLING CAPS, PLACE CLOSE TO VDD3.3

3.3V
C31 0.1u
C35 0.1u
C36 0.1u
C38 0.1u
GND

3.3V
U3 USB3300-EZK
VDD3.3 6, 16, 25, 30
VBUS 4
DM D- 8
DP D+ 7
ID 5
XO 27
XI 28
CPEN 3
EXTVBUS 10
REG_EN 31
RBIAS 32
GND 1, 2, 33
VDD1.8 15, 26, 29
DATA7 17
DATA6 18
DATA5 19
DATA4 20
DATA3 21
DATA2 22
DATA1 23
DATA0 24
NXT 11
DIR 12
STP 13
CLKOUT 14
RESET 9 — TP174

USB_VBUS — R44 820 — VBUS
USB_D- — D-
USB_D+ — D+
D12 DDZ5V6ASF
GND
R45 12K
GND
GND

NOTE: PLACE CRYSTAL CLOSE TO XO/XI

C33 20p
Y2 24MHz
C34 20p
R46 1M
XO
XI
GND
GND

NOTE: DECOUPLING CAPS, PLACE CLOSE TO VDD1.8

VDD1.8
C29 4.7u
C30 0.1u
C32 0.1u
GND

NOTE: DECOUPLING CAPS, PLACE CLOSE TO VDDA1.8

VDDA1.8
C37 4.7u
C39 0.1u
GND

DT18 – I/O MASTER
THE UNIVERSITY OF AKRON

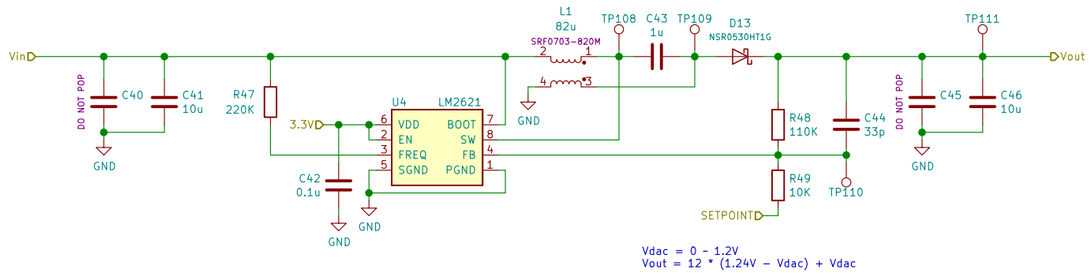
Sheet: /Microcontroller/
File: Microcontroller.sch

Title: MICROCONTROLLER SUBSYSTEM

Size: B	Date: 2020-02-10	**Rev: A**
KiCad E.D.A. kicad 5.1.5		Id: 2/10

3.3–15V ADJUSTABLE REGULATOR

INPUT
(1.2–14V)



TARGET DEVICE SUPPLY
(3.3–15V ADJ, 100mA MAX)

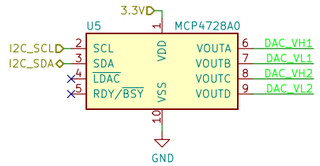
Vdac = 0 ~ 1.2V
Vout = 12 * (1.24V – Vdac) + Vdac

DT18 – I/O MASTER
THE UNIVERSITY OF AKRON

Sheet: /Adjustable Regulator/	
File: Adjustable Regulator.sch	
Title: 3.3–15V ADJUSTABLE REGULATOR	
Size: B	Date: 2020–02–10
KiCad E.D.A. kicad 5.1.5	Id: 3/10

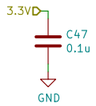
Rev: A

LOGIC LEVEL GENERATOR

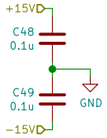


NOTE: P/N MCP4728A0 IS PRE-PROGRAMMED WITH I2C ADDRESS 0b1100000

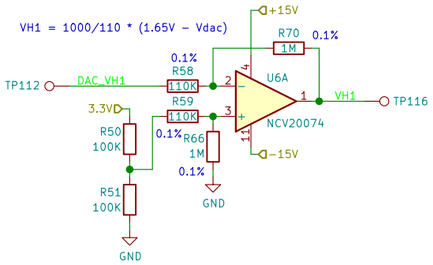
NOTE: DECOUPLING CAP, PLACE CLOSE TO VDD

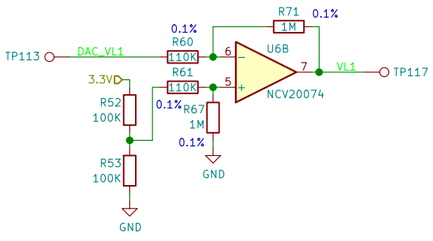


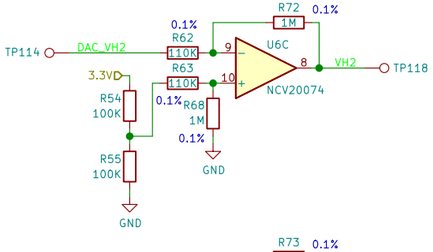
NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+/V-

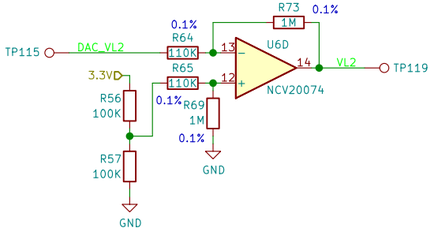


VH1 = 1000/110 * (1.65V - Vdac)



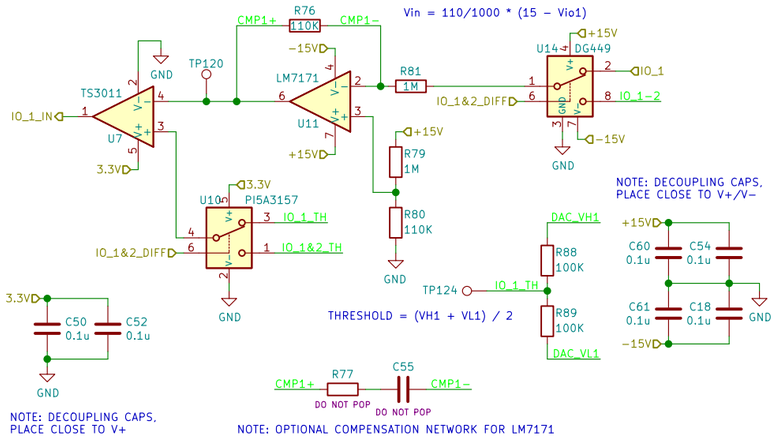






SINGLE-ENDED RECEIVER (I/O PIN 1)

Vin = 110/1000 * (15 - Vio1)



NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+/V-

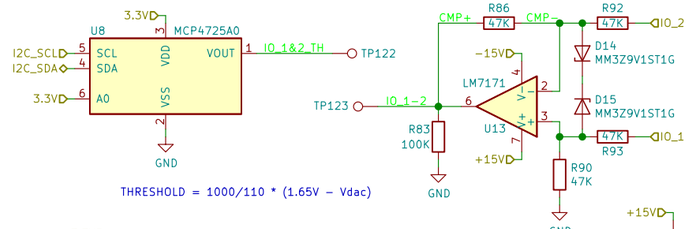
THRESHOLD = (VH1 + VL1) / 2

NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+

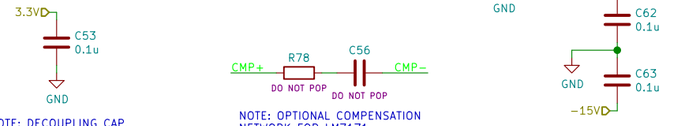
NOTE: OPTIONAL COMPENSATION NETWORK FOR LM7171

DIFFERENTIAL RECEIVER (I/O PIN 1 - I/O PIN 2)

NOTE: P/N MCP4725A0 IS PRE-PROGRAMMED WITH I2C ADDRESS 0b1100001



THRESHOLD = 1000/110 * (1.65V - Vdac)



NOTE: DECOUPLING CAP, PLACE CLOSE TO VDD

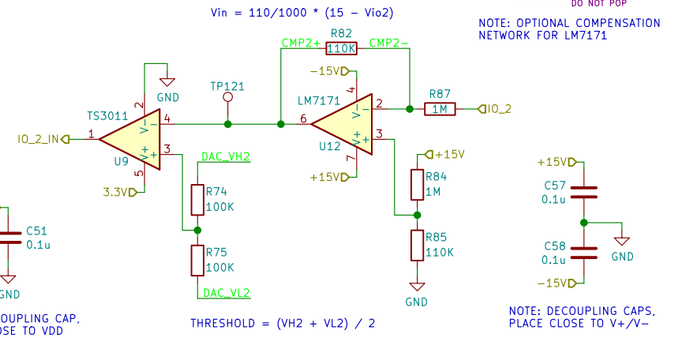
NOTE: OPTIONAL COMPENSATION NETWORK FOR LM7171

NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+/V-

SINGLE-ENDED RECEIVER (I/O PIN 2)

NOTE: OPTIONAL COMPENSATION NETWORK FOR LM7171

Vin = 110/1000 * (15 - Vio2)

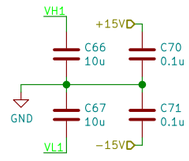


NOTE: DECOUPLING CAP, PLACE CLOSE TO VDD

THRESHOLD = (VH2 + VL2) / 2

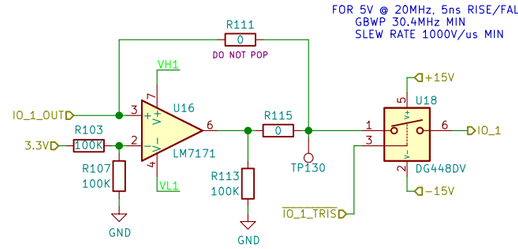
NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+/V-

OUTPUT DRIVER (I/O PIN 1)

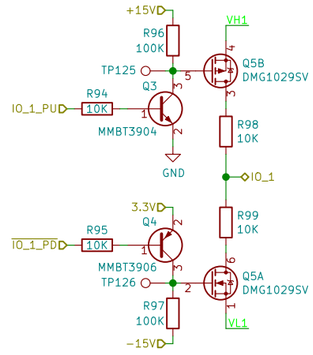


NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+/V-

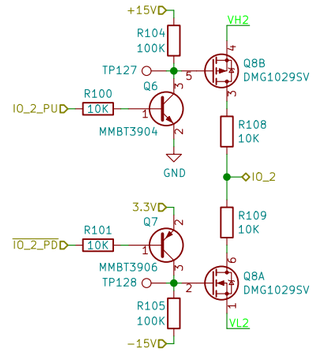
FOR 5V @ 20MHz, 5ns RISE/FALL:
GBWP 30.4MHz MIN
SLEW RATE 1000V/us MIN



CONFIGURABLE RESISTORS

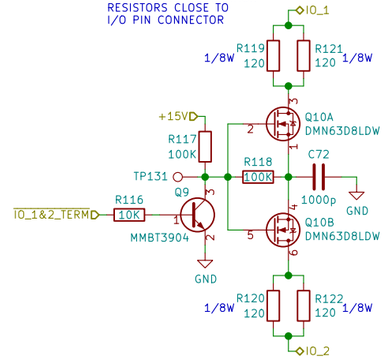


I/O PIN 1
10KΩ PULL-UP/DOWN



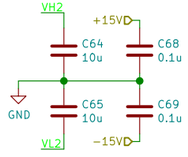
I/O PIN 2
10KΩ PULL-UP/DOWN

NOTE: PLACE TERMINATION RESISTORS CLOSE TO I/O PIN CONNECTOR



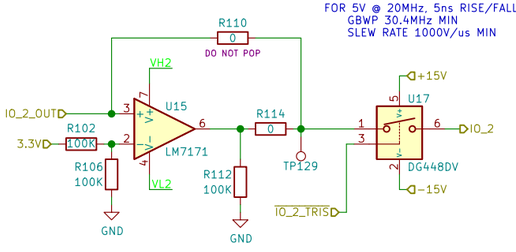
120Ω TERMINATION
BETWEEN I/O PINS 1 & 2

OUTPUT DRIVER (I/O PIN 2)



NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+/V-

FOR 5V @ 20MHz, 5ns RISE/FALL:
GBWP 30.4MHz MIN
SLEW RATE 1000V/us MIN



DT18 - I/O MASTER
THE UNIVERSITY OF AKRON

Sheet: /Level Shifter - I/O Pins 1&2/
File: Level Shifter - IO 1-2.sch

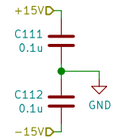
Title: LEVEL SHIFTER SUBSYSTEM - I/O PINS 1 & 2

Size: B	Date: 2020-02-10	**Rev: A**
KiCad E.D.A. kicad 5.1.5		Id: 4/10

OVERVOLTAGE PROTECTION

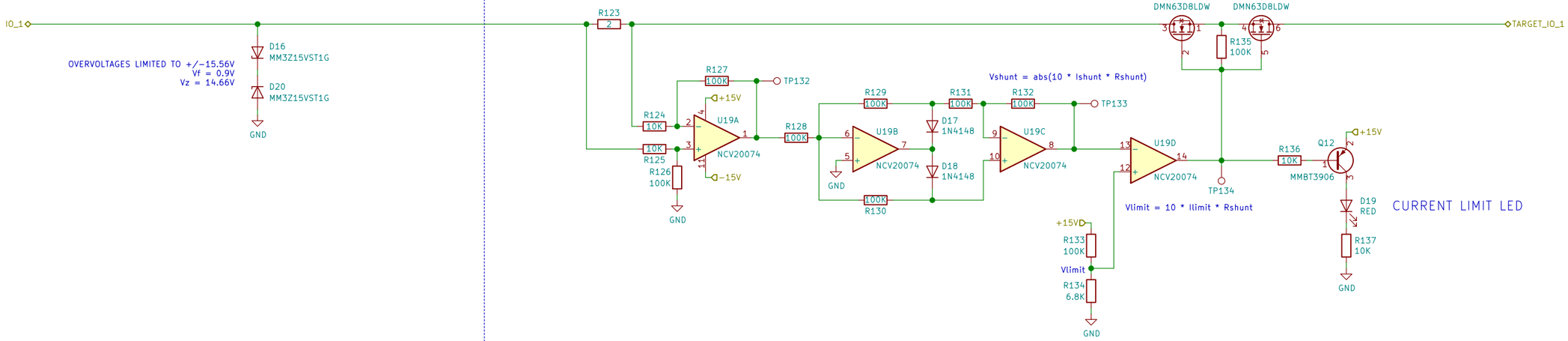
OVERCURRENT PROTECTION

NOTE: DECOUPLING CAPS,
PLACE CLOSE TO V+/V-



TRANSISTOR POWER DISSIPATION:
(WORST CASE: OUPUTTING +15V, PIN SHORTED TO -15V)
Pq = (15V - -15V) * 50mA = 1.5W

MAX AVG Pq IS 275mW.
ALLOWABLE DUTY CYCLE IS 0.275 / 1.5 = 0.18
(10 SEC SHORT CIRCUIT OVER 1 MIN)



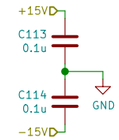
DT18 - I/O MASTER
THE UNIVERSITY OF AKRON

Sheet: /Circuit Protection - I/O Pin 1/		
File: Circuit Protection - IO 1.sch		
Title: CIRCUIT PROTECTION SUBSYSTEM - I/O PIN 1		
Size: B	Date: 2020-02-10	**Rev: A**
KiCad E.D.A. kicad 5.1.5		Id: 5/10

OVERVOLTAGE PROTECTION

OVERCURRENT PROTECTION

NOTE: DECOUPLING CAPS,
PLACE CLOSE TO V+/V−



TRANSISTOR POWER DISSIPATION:
(WORST CASE: OUPUTTING +15V, PIN SHORTED TO −15V)
Pq = (15V − −15V) * 50mA = 1.5W

MAX AVG Pq IS 275mW.
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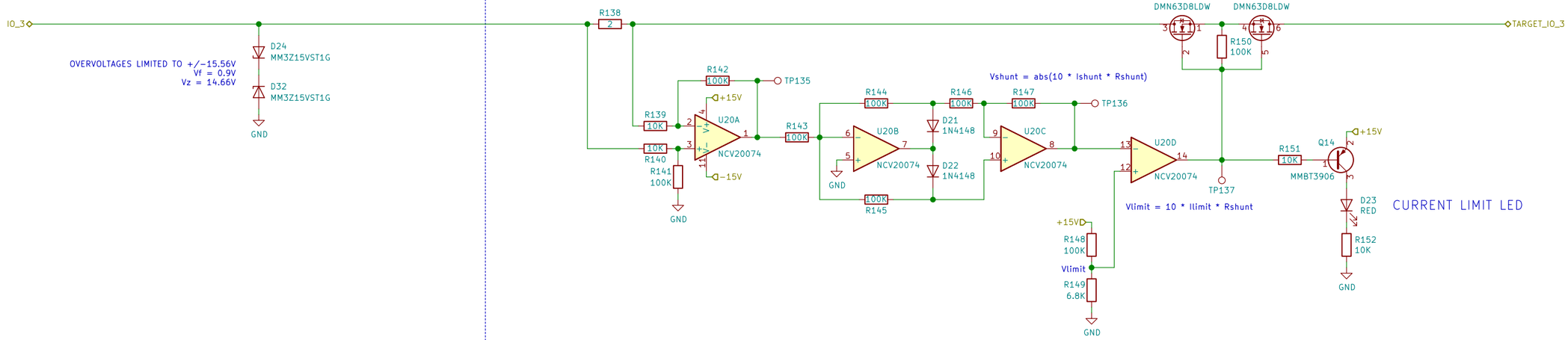
(10 SEC SHORT CIRCUIT OVER 1 MIN)



DT18 − I/O MASTER		
THE UNIVERSITY OF AKRON		
Sheet: /Circuit Protection − I/O Pin 3/		
File: Circuit Protection − IO 3.sch		
Title: CIRCUIT PROTECTION SUBSYSTEM − I/O PIN 3		
Size: B	Date: 2020−02−10	**Rev: A**
KiCad E.D.A. kicad 5.1.5		Id: 6/10

OVERVOLTAGE PROTECTION

OVERCURRENT PROTECTION

NOTE: DECOUPLING CAPS,
PLACE CLOSE TO V+/V-

+15V
C115
0.1u
C116
0.1u
GND
-15V

TRANSISTOR POWER DISSIPATION:
(WORST CASE: OUPUTTING +15V, PIN SHORTED TO -15V)
Pq = (15V - -15V) * 50mA = 1.5W

MAX AVG Pq IS 275mW.
ALLOWABLE DUTY CYCLE IS 0.275 / 1.5 = 0.18
(10 SEC SHORT CIRCUIT OVER 1 MIN)

IO_4

OVERVOLTAGES LIMITED TO +/-15.56V
Vf = 0.9V
Vz = 14.66V

D36
MM3Z15VST1G
D37
MM3Z15VST1G
GND

R153
2

Q15A
DMN63D8LDW
Q15B
DMN63D8LDW
R165
100K

TARGET_IO_4

R157
100K
TP138
+15V
R154
10K
R155
10K
R156
100K
GND
U21A
NCV20074
-15V
R158
100K

Vshunt = abs(10 * Ishunt * Rshunt)

R159
100K
R161
100K
R162
100K
TP139
D25
1N4148
D26
1N4148
U21B
NCV20074
U21C
NCV20074
GND
R160
100K

U21D
NCV20074
TP140
Vlimit = 10 * Ilimit * Rshunt

R166
10K
Q16
MMBT3906
+15V
D27
RED
R167
10K
GND

CURRENT LIMIT LED

+15V
R163
100K
Vlimit
R164
6.8K
GND

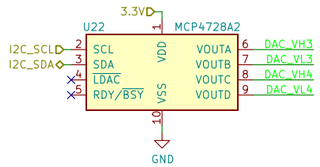
DT18 - I/O MASTER
THE UNIVERSITY OF AKRON

Sheet: /Circuit Protection - I/O Pin 4/
File: Circuit Protection - IO 4.sch

Title: CIRCUIT PROTECTION SUBSYSTEM - I/O PIN 4

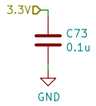
Size: B	Date: 2020-02-10	**Rev: A**
KiCad E.D.A. kicad 5.1.5		Id: 7/10

LOGIC LEVEL GENERATOR

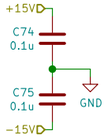


NOTE: P/N MCP4728A2 IS PRE-PROGRAMMED WITH I2C ADDRESS 0b1100010

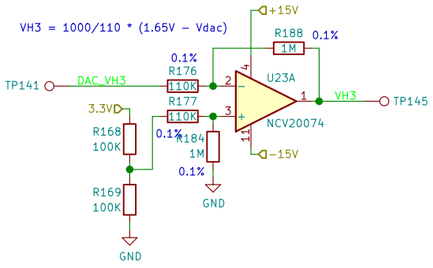
NOTE: DECOUPLING CAP, PLACE CLOSE TO VDD

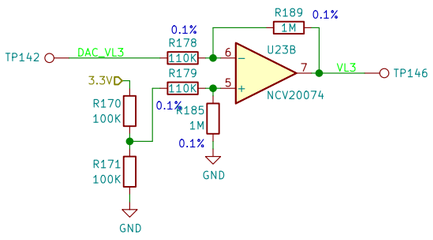


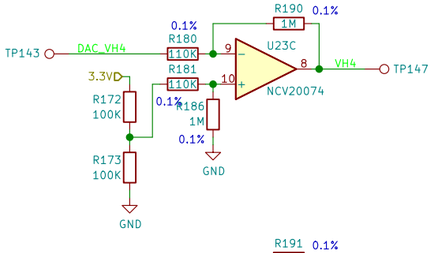
NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+/V-

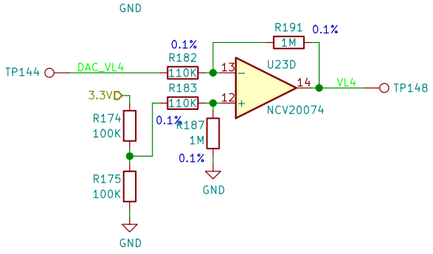


VH3 = 1000/110 * (1.65V - Vdac)



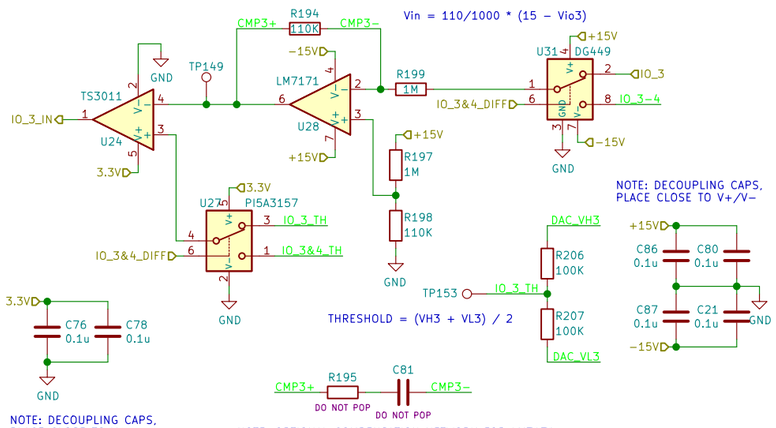






SINGLE-ENDED RECEIVER (I/O PIN 3)

Vin = 110/1000 * (15 - Vio3)



NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+/V-

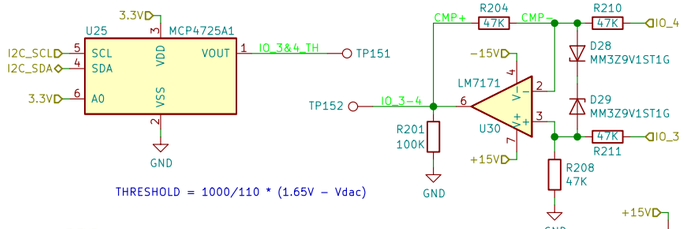
THRESHOLD = (VH3 + VL3) / 2

NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+

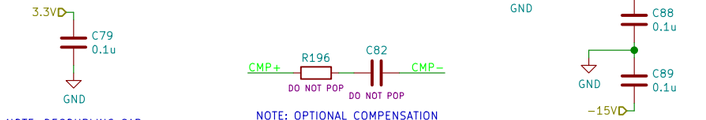
NOTE: OPTIONAL COMPENSATION NETWORK FOR LM7171

DIFFERENTIAL RECEIVER (I/O PIN 3 - I/O PIN 4)

NOTE: P/N MCP4725A1 IS PRE-PROGRAMMED WITH I2C ADDRESS 0b1100011



THRESHOLD = 1000/110 * (1.65V - Vdac)



NOTE: DECOUPLING CAP, PLACE CLOSE TO VDD

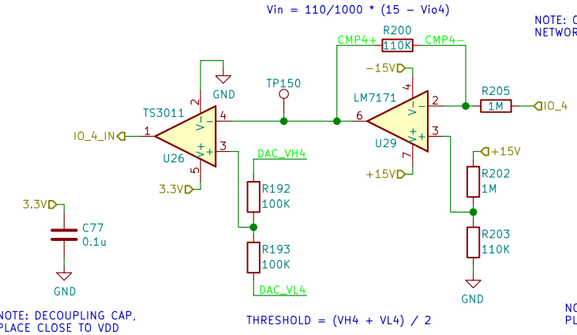
NOTE: OPTIONAL COMPENSATION NETWORK FOR LM7171

NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+/V-

SINGLE-ENDED RECEIVER (I/O PIN 4)

NOTE: OPTIONAL COMPENSATION NETWORK FOR LM7171

Vin = 110/1000 * (15 - Vio4)

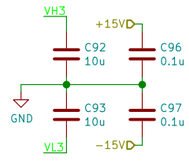


NOTE: DECOUPLING CAP, PLACE CLOSE TO VDD

THRESHOLD = (VH4 + VL4) / 2

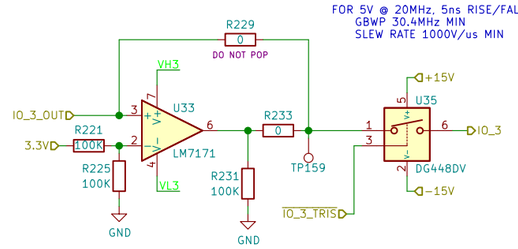
NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+/V-

OUTPUT DRIVER (I/O PIN 3)

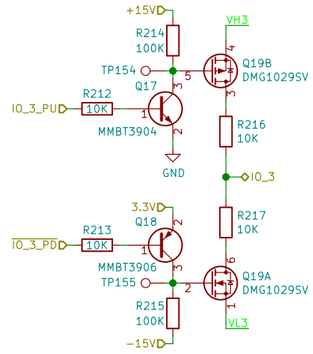


NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+/V-

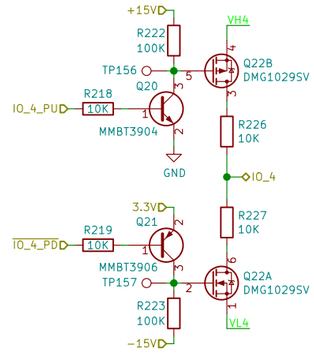
FOR 5V @ 20MHz, 5ns RISE/FALL:
GBWP 30.4MHz MIN
SLEW RATE 1000V/us MIN



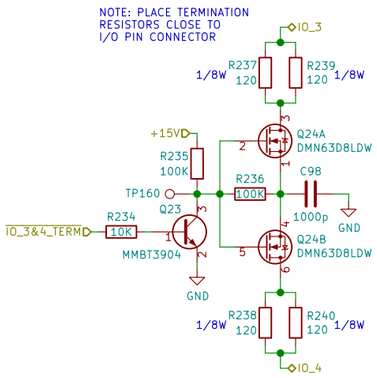
CONFIGURABLE RESISTORS



I/O PIN 3
10KΩ PULL-UP/DOWN

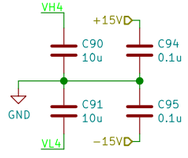


I/O PIN 4
10KΩ PULL-UP/DOWN



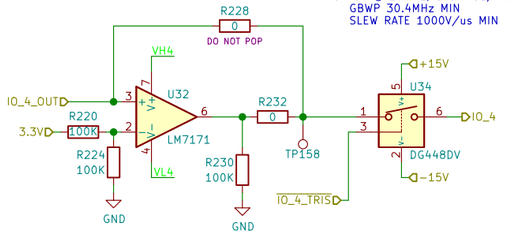
120Ω TERMINATION
BETWEEN I/O PINS 3 & 4

OUTPUT DRIVER (I/O PIN 4)



NOTE: DECOUPLING CAPS, PLACE CLOSE TO V+/V-

FOR 5V @ 20MHz, 5ns RISE/FALL:
GBWP 30.4MHz MIN
SLEW RATE 1000V/us MIN



DT18 - I/O MASTER
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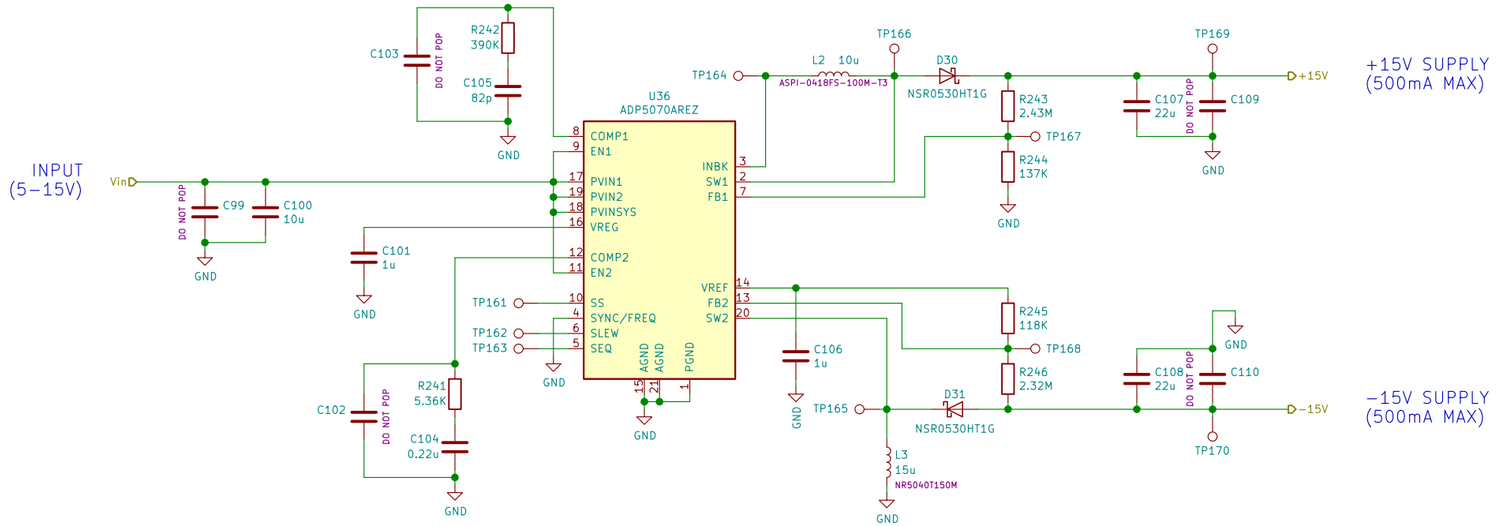
Sheet: /Level Shifter - I/O Pins 3&4/
File: Level Shifter - IO 3-4.sch

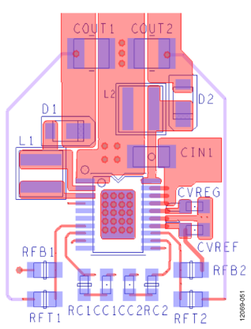
Title: LEVEL SHIFTER SUBSYSTEM - I/O PINS 3 & 4

Size: B	Date: 2020-02-10	**Rev: A**
KiCad E.D.A. kicad 5.1.5		Id: 8/10

+/−15V REGULATOR



RECOMMENDED PCB LAYOUT



DT18 – I/O MASTER
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Sheet: /15V Regulator/
File: 15V Regulator.sch

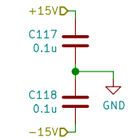
Title: +/−15V REGULATOR

Size: B	Date: 2020−02−10	**Rev: A**
KiCad E.D.A. kicad 5.1.5		Id: 9/10

OVERVOLTAGE PROTECTION

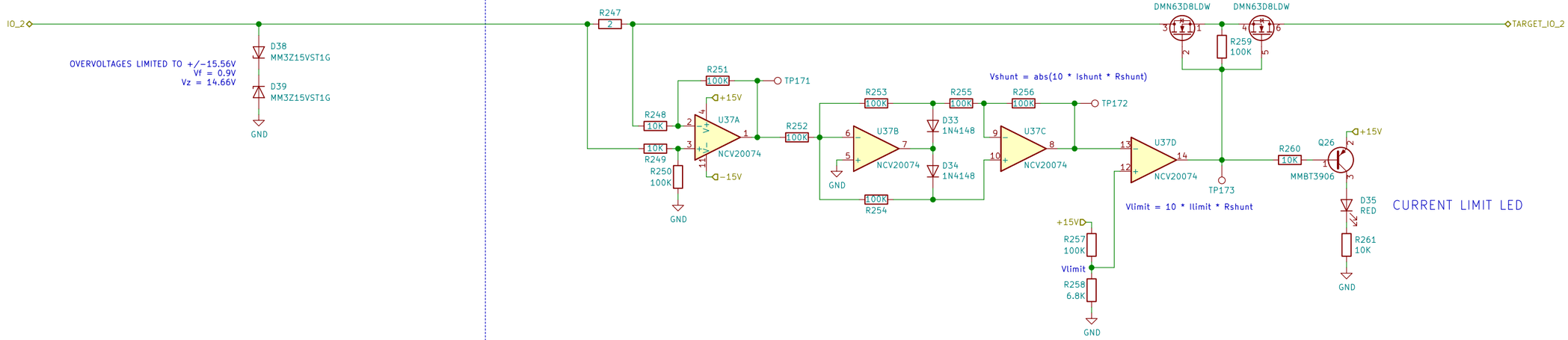
OVERCURRENT PROTECTION

NOTE: DECOUPLING CAPS,
PLACE CLOSE TO V+/V−



TRANSISTOR POWER DISSIPATION:
(WORST CASE: OUPUTTING +15V, PIN SHORTED TO −15V)
Pq = (15V − −15V) * 50mA = 1.5W

MAX AVG Pq IS 275mW.
ALLOWABLE DUTY CYCLE IS 0.275 / 1.5 = 0.18
(10 SEC SHORT CIRCUIT OVER 1 MIN)



DT18 − I/O MASTER
THE UNIVERSITY OF AKRON

Sheet: /Circuit Protection − I/O Pin 2/		
File: Circuit Protection − IO 2.sch		
Title: CIRCUIT PROTECTION SUBSYSTEM − I/O PIN 2		
Size: B	Date: 2020−02−10	**Rev: A**
KiCad E.D.A. kicad 5.1.5		Id: 10/10