CIS 415 – Operating Systems

Homework Assignment 4
Spring 2017 – Prof. Sventek

Due at 5:00pm on Tuesday, 6 June 2017

All questions must be answered by you without outside assistance. **Submission is via Canvas.** You may submit either a plain text (.txt) or a PDF (.pdf) file. Succinct, concise answers to the questions are preferable to long, rambling ones.

Textbook Questions (50 points)

1. OSC 10.11: [18 points]
   Suppose that a disk drive has 5,000 cylinders, numbered 0 to 4999. The drive is currently serving a request at cylinder 2150, and the previous request was at cylinder 1805. The queue of pending requests, in FIFO order, is:

   2069, 1212, 2296, 2800, 544, 1618, 356, 1523, 4965, 3681

   Starting from the current head position, what is the total distance (in cylinders) that the disk arm moves to satisfy all the pending requests for each of the following disk-scheduling algorithms?
   a. FCFS
   b. SSTF
   c. SCAN
   d. LOOK
   e. C-SCAN
   f. C-LOOK

2. Consider a file system that uses inodes to represent files. Disk blocks are 1 kB in size, and a pointer to a disk block requires 4 bytes. Each inode has 8 direct block pointers, as well as one each of single, double, and triple indirect block pointers.

n	2	3	5	10	20	30	40
2^n	4	8	32	1,024	1,048,576	1,073,741,824	1,099,511,627,776
label				kB	MB	GB	TB

   a. What is the maximum size of a disk (in bytes) for which one can use this file system? [3 points]
   b. What is the maximum size of a file (in bytes) that can be stored in this file system? [9 points]

3. The processor for which you are designing your application as L1i and L1d virtual caches.
   a. What type of data does each cache hold? [2 points]

b. Describe in detail the activities of the cache + memory system when executing the instruction [3 points]

LOAD virtual address, register

c. Assume that the above instruction is executed many times in a loop, and that the instruction itself is in the cache. Also assume that memory access costs τ μs, and cache access costs $\tau/15$ μs. What cache hit rate ρ for "virtual address" is required for the memory system to run 5 times faster than with no caching at all? Show your work. [7 points]

d. Suppose we have a memory system that has a main memory, a single-level cache, and demand paging virtual memory. The three levels of the memory system have the following access times:

Cache	2ns
Main memory	100ns
Paging disk	10ms

i. The cache has a 95% hit rate. What is the effective memory access time if we consider only the cache and main memory and ignore page faults and disk access times? [3 points]

ii. Now recalculate the effective memory access time assuming the same cache hit rate (95%) plus a page fault rate of 0.001% (i.e., 99.999% of the memory accesses succeed without producing a page fault). [5 points]

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