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B.Tech. Second Assessment – Oct/Nov. 2016

Third Semester

15ECE202 Digital Circuits and Systems

(Common to Computer Science and Engineering,
Electronics and Communication Engineering and Electrical and Electronics Engineering)

Time: Two hours Maximum: 50 Marks

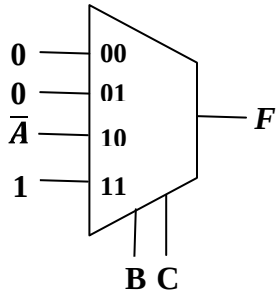
Answer all questions

1. (a) Implement the following truth table using a *single* MUX of appropriate size

$$F(A,B,C,D,E) = \sum m(0,1,5,11,16,19,21,23,29,31)$$

(6 Marks)

(b) Write the Boolean equation of the Boolean function *F* implemented by the following multiplexercircuit. **(4 Marks)**



2. (a) Implement a full adder circuit using a single decoder and additional gates **(6 Marks)**

(b)You are given a *4 to 2priority encoder* and a *4:1* MUX. There are four data lines coming from the following personnel in an office (mentioned in decreasing order of privilege)*(i)Manager (ii)Supervisor (iii)Operator (iv)Intern*.
Show a block diagram describing how the given building blocks can be connected to provide privilege based access to a single outgoing data line for data from all the above sources. **(4 Marks)**

3. (a) Draw the circuit of a comparator for comparing two 3-bit binary numbers $A_2A_1A_0$ and $B_2B_1B_0$ having separate outputs for *greater than*, *less than* and *equal to* conditions. **(6 Marks)**

(b)A 3-bit data is received from a sensor. If it exceeds 6 a letter "*H"* has to be displayed. If it falls below 3, a letter *"L"* has to be displayed. Draw a block diagram depicting how this can be accomplished using two 3-bit comparators, Multiplexers and a seven segment display. **(4 Marks)**

4. (a) Draw the circuit of an SR Latch using only NAND gates. Explain why the input combination S = R = 1 is undesirable **(4 Marks)**

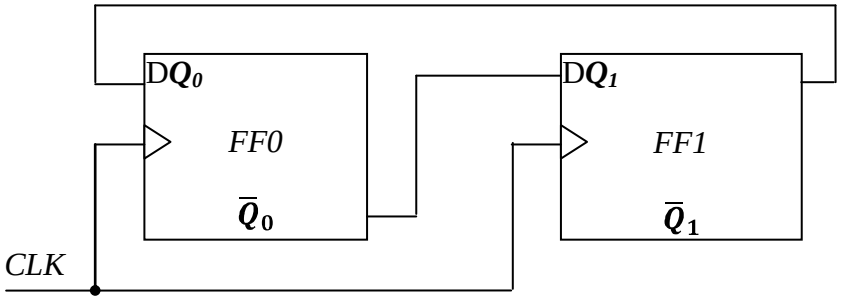
(b) A flip-flop having two inputs A and B has the truth table (characteristic table) given below. Design the flip-flop using a D Flip-flop and additional gates as building blocks.

A	B	Q(t+1)
0	*0*	*1*
0	*1*	$Q(t)$
1	*0*	$\overline{Q(t)}$
1	*1*	*0*

(6 Marks)

5. (a) Draw the circuit of a 3-bit synchronous Up counter using D flip-flops and additional gates **(4 Marks)**

(b)Determine the sequence generated byQ_1Q_0in the following circuit when a continuous clock signal is applied to the CLK line. Assume that both flip-flops are initially preset to $Q_1 = Q_0 = 1$ **(6 Marks)**



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