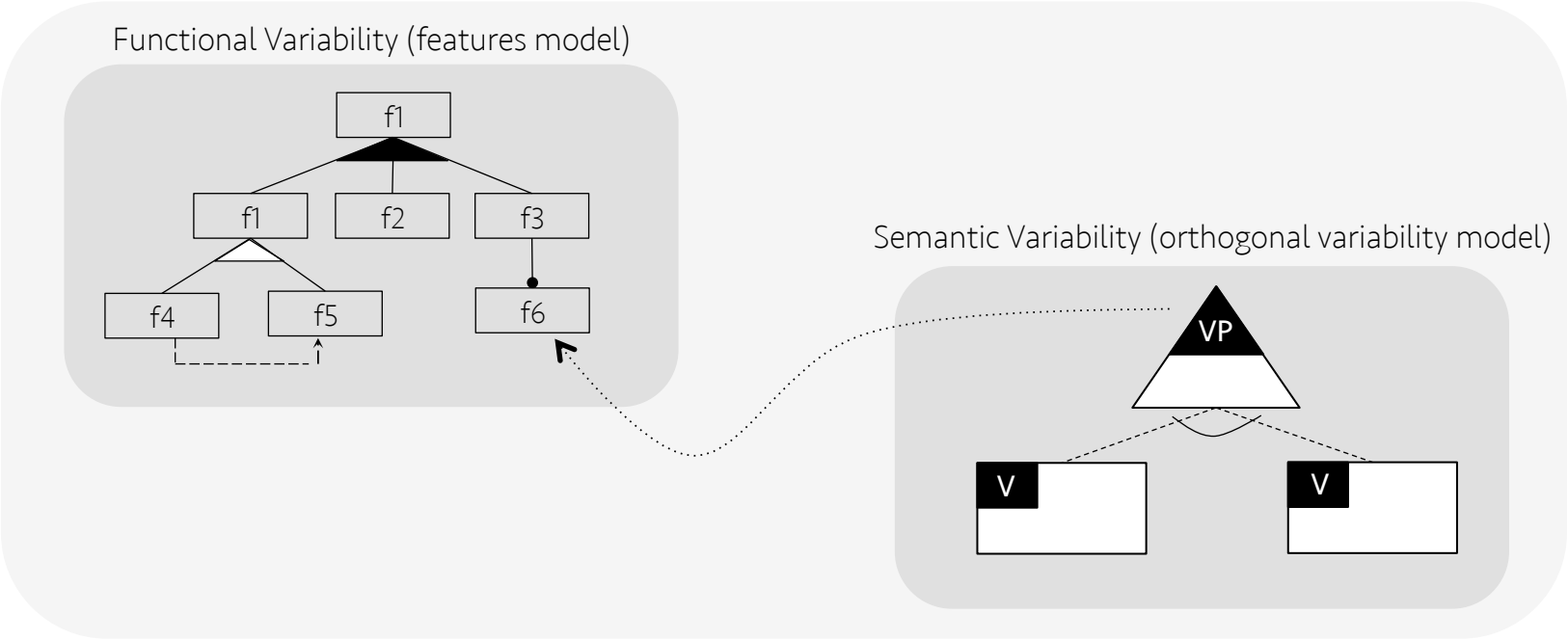
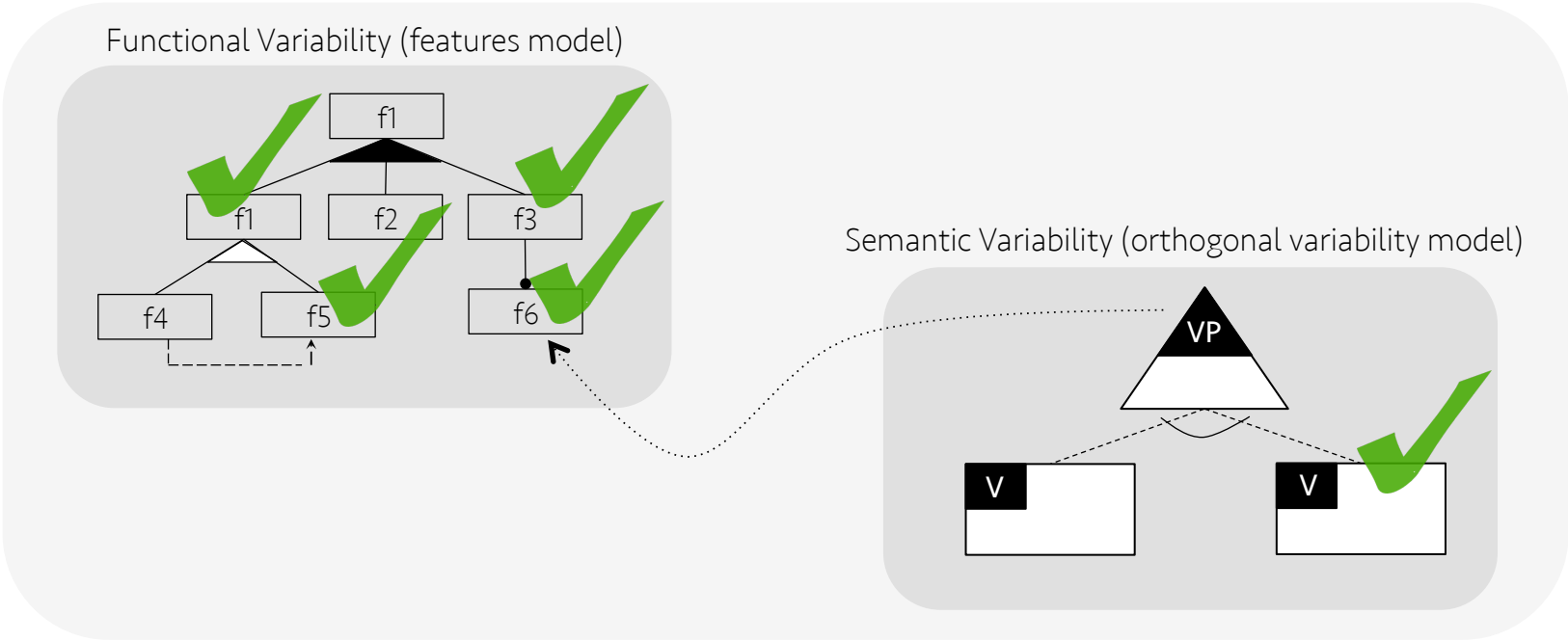
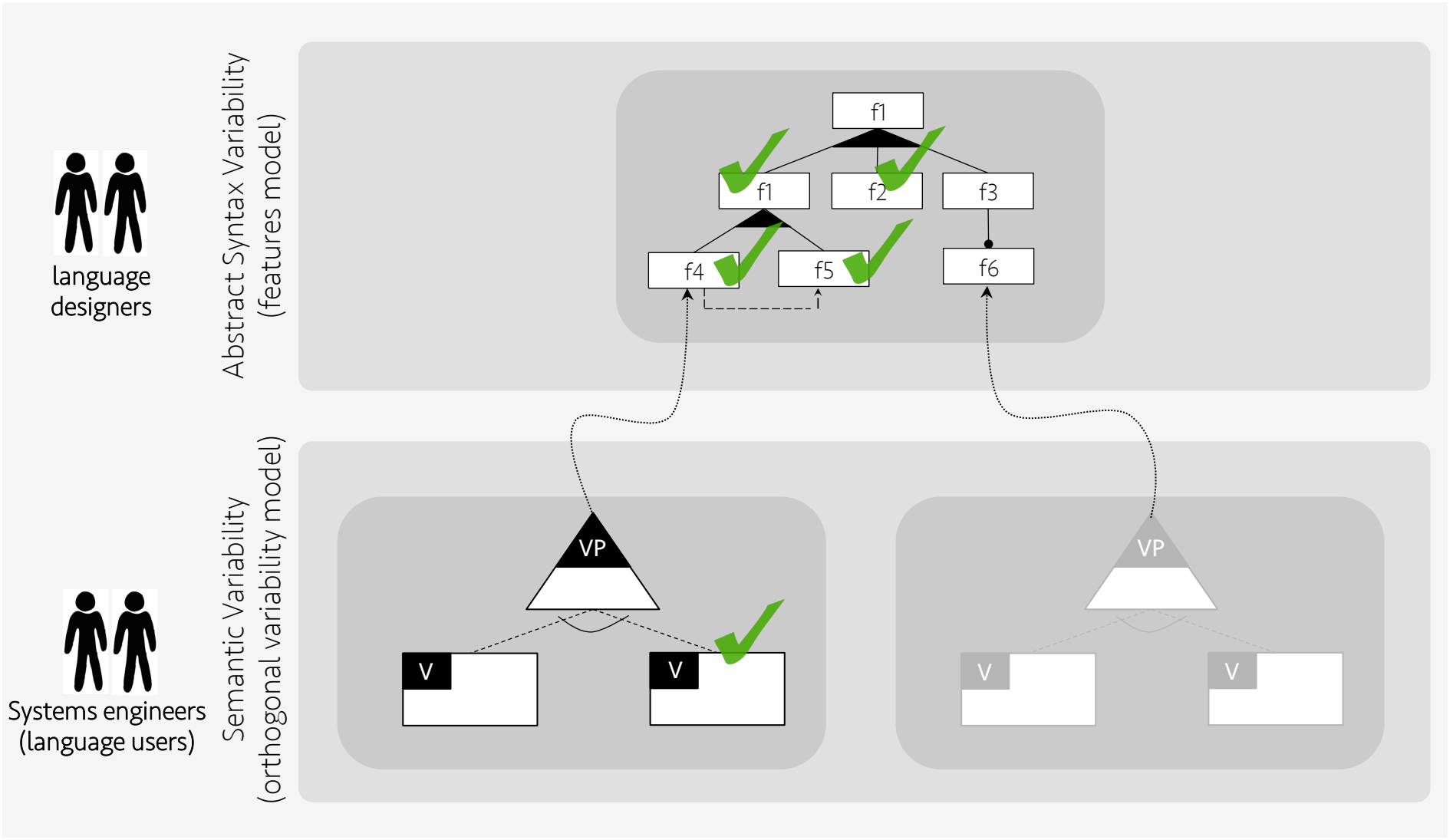
Step 2: Reverse-engineering **variability models**



Abstract Syntax Variability
(features model)
f1
f1
f2
f3
f4
f5
f6
Semantic Variability
(orthogonal variability model)
VP
V
V
VP
V
V

Step 3: Configuring and deriving DSLs




language designers
Systems engineers (language users)
Abstract Syntax Variability (features model)
Semantic Variability (orthogonal variability model)
f1
f1
f2
f3
f4
f5
f6
VP
V
V
VP
V
V

Abstract Syntax Variability
(features model)
State Machines
Pseudostates
TimedTransitions
Core
HierarchicalStates
Initial
Fork
Join
Junction
History
Condition
Deep
Shallow
Semantic Variability
(orthogonal variability model)
VP
Events
attending
policy
V
Simultaneous
events
V
Run to
completion
VP
Conflicting
transitions
treatment
V
Higher
Transition
V
Lower
Transition