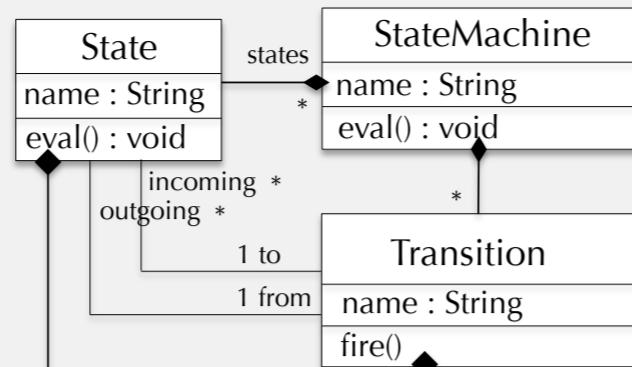
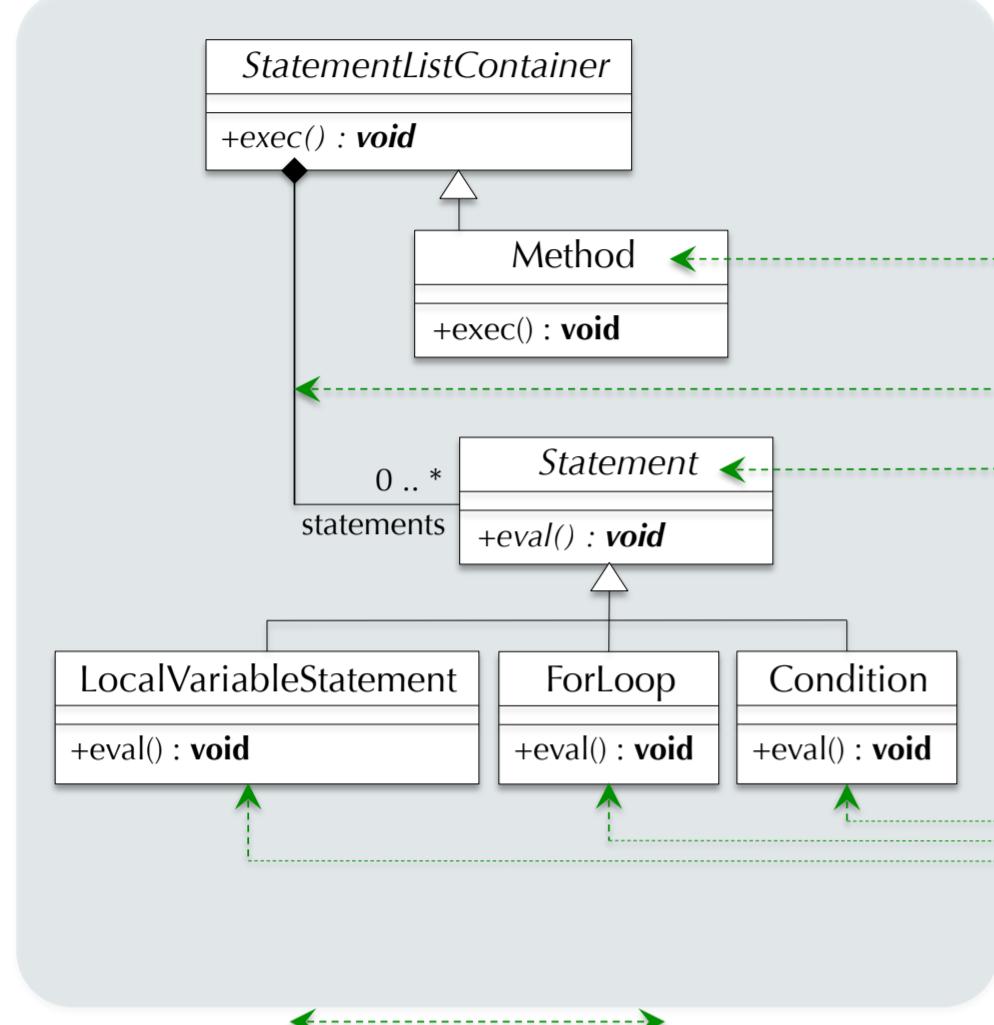


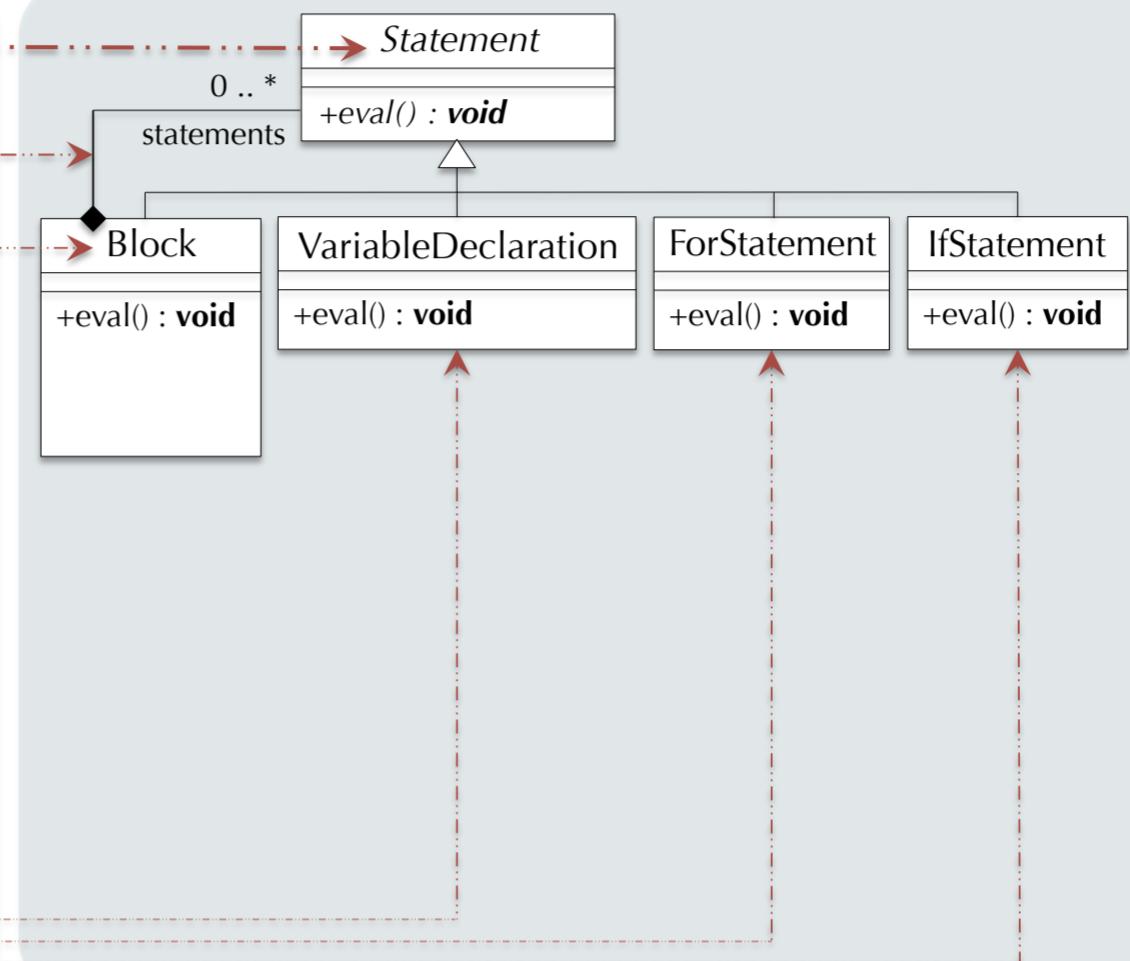
Finite State Machines



Provided Interface: Java



Provided Interface: C#

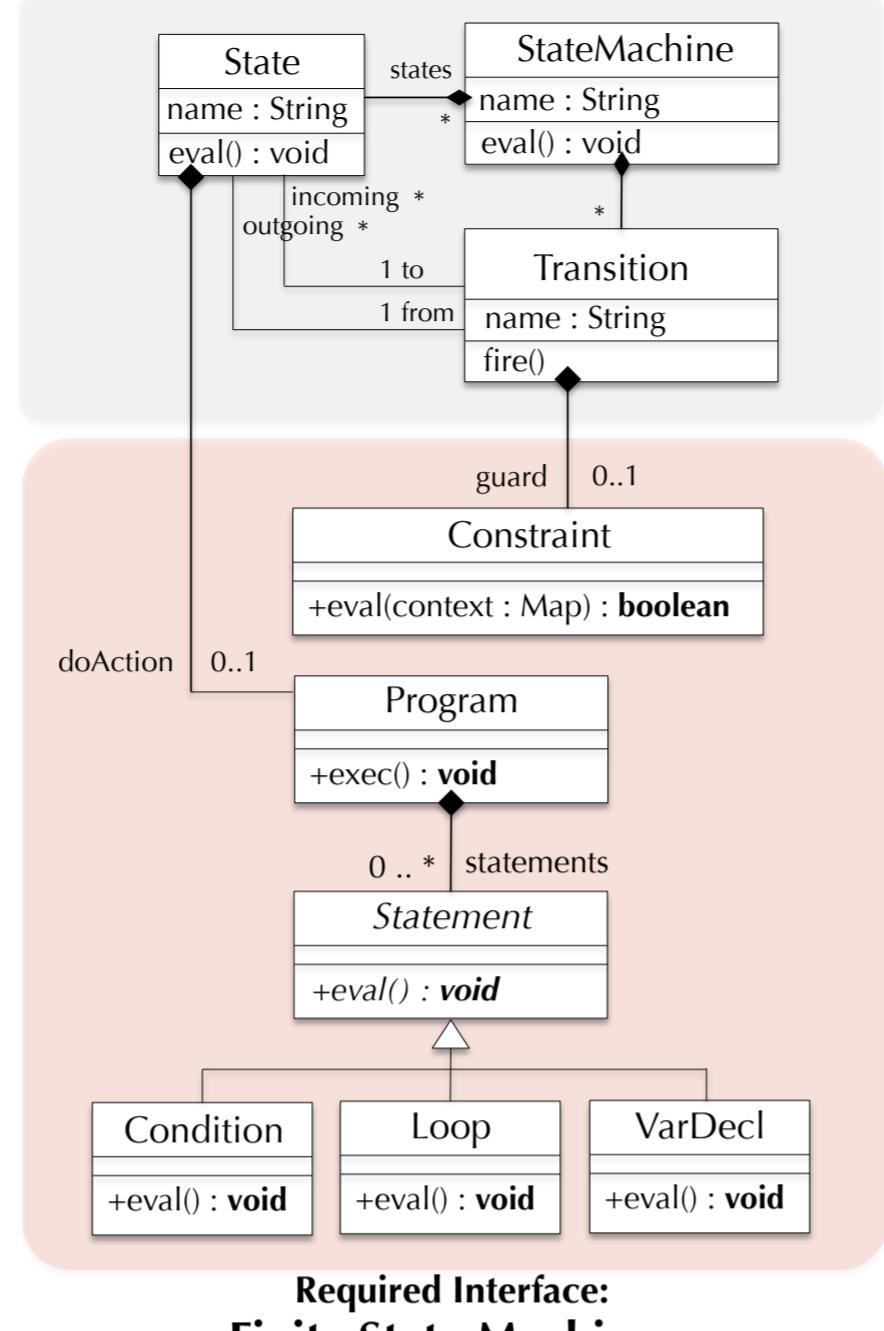


Binding
Java <-> FiniteStateMachines

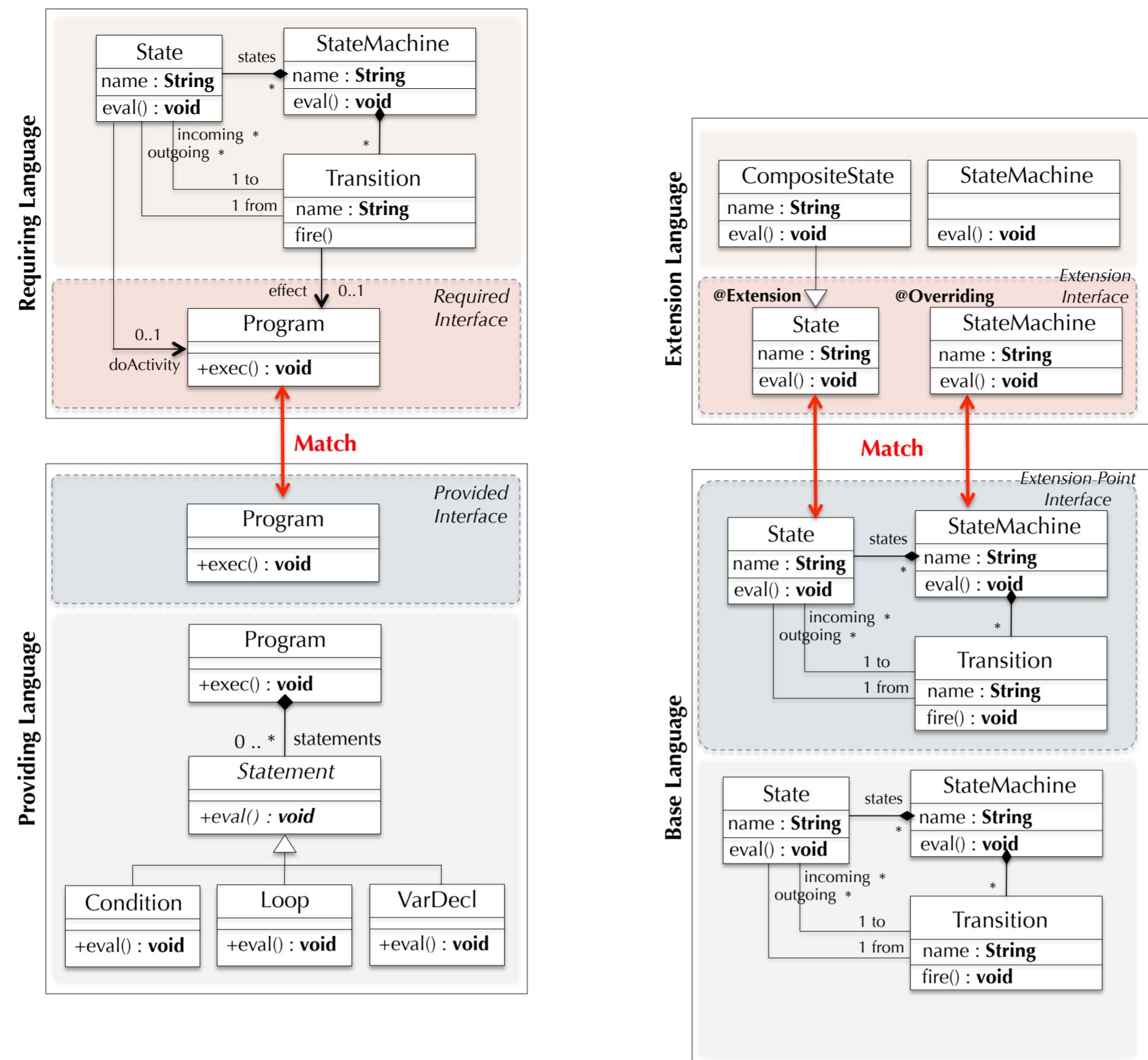
Required Interface:
Finite State Machines

Binding
C# <-> FiniteStateMachines

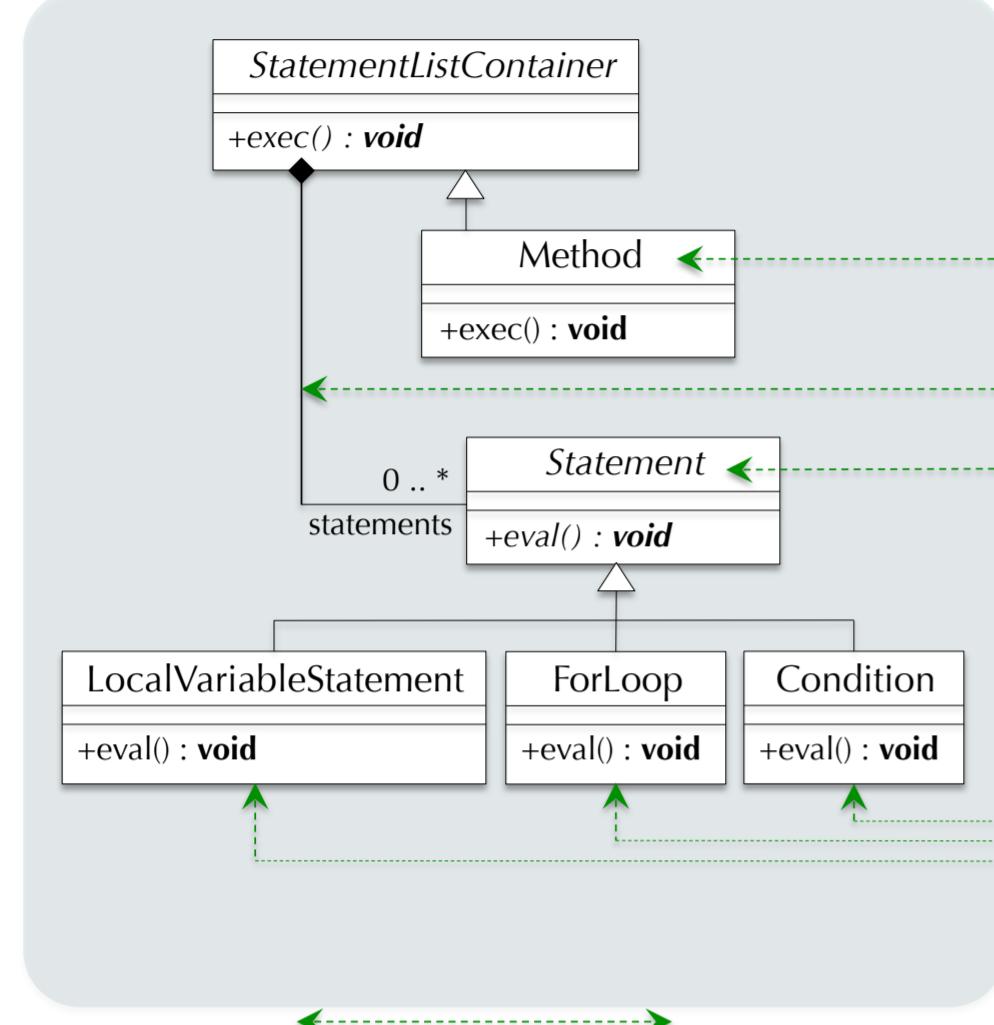
Finite State Machines



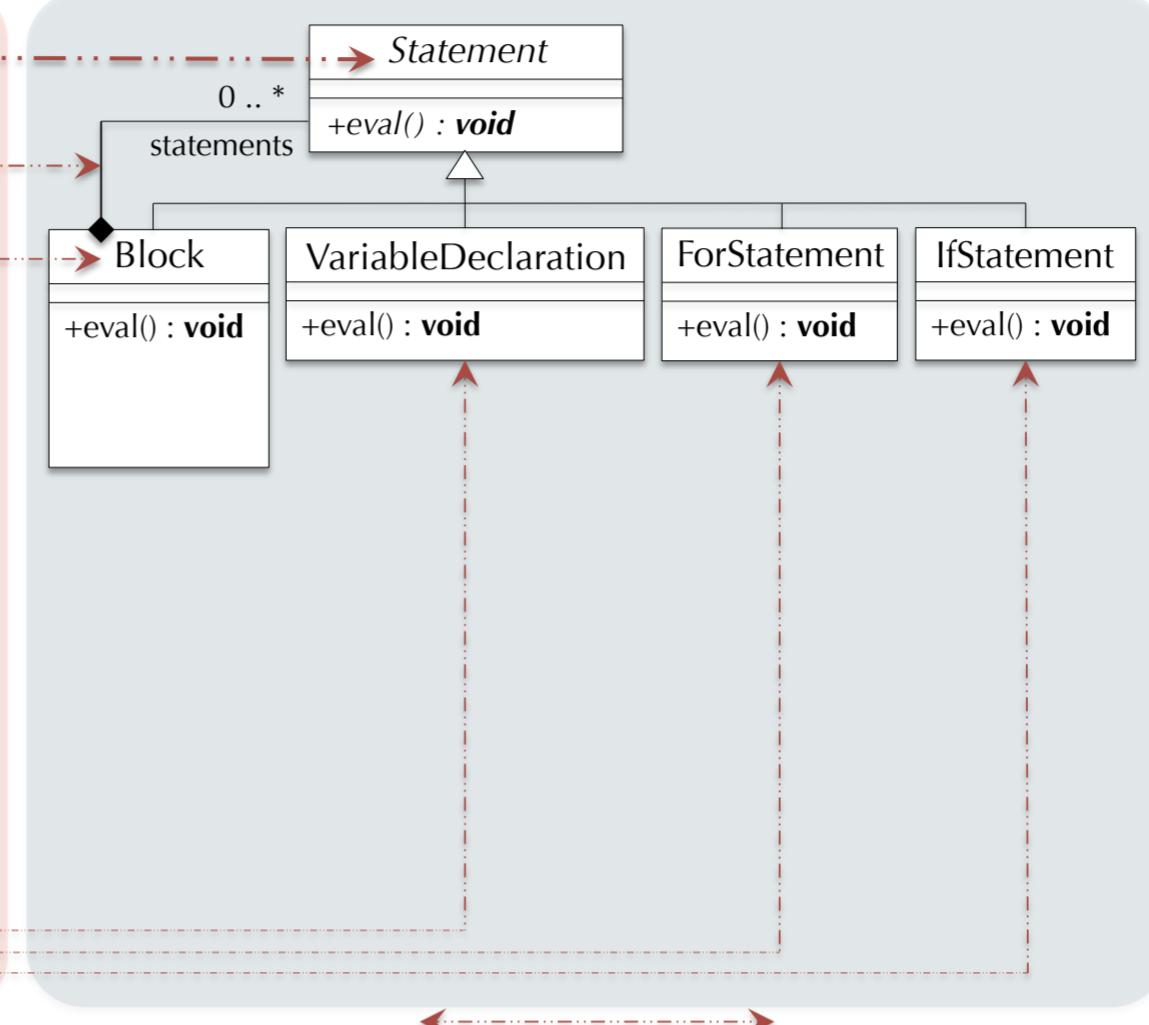
**Required Interface:
Finite State Machines**



Provided Interface: Java



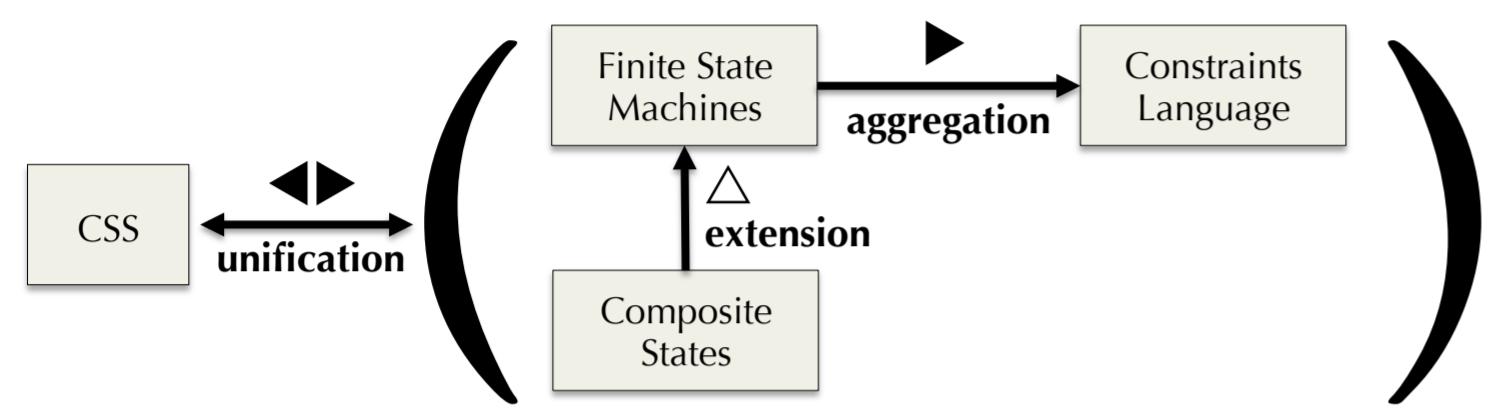
Provided Interface: C#

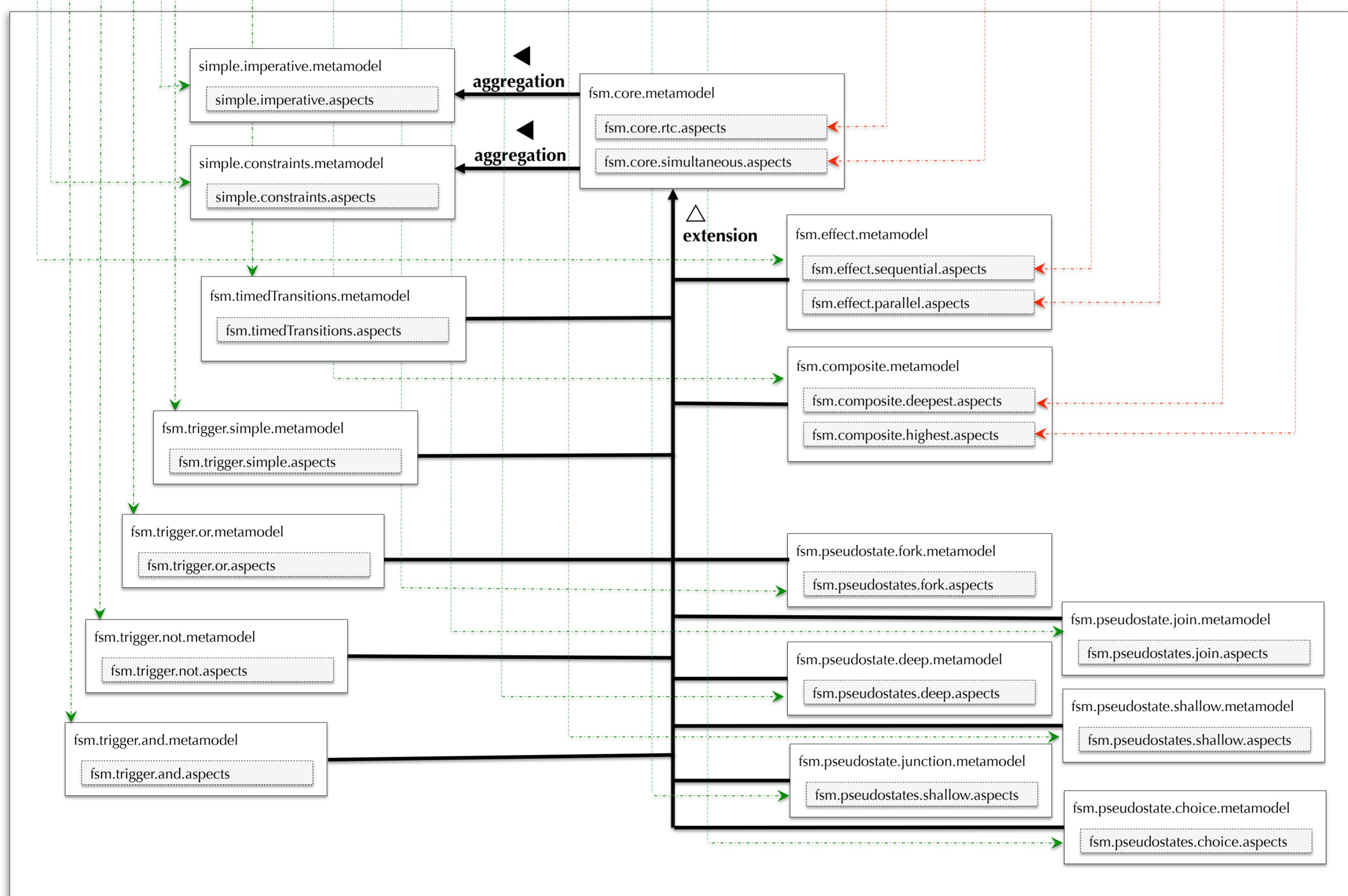
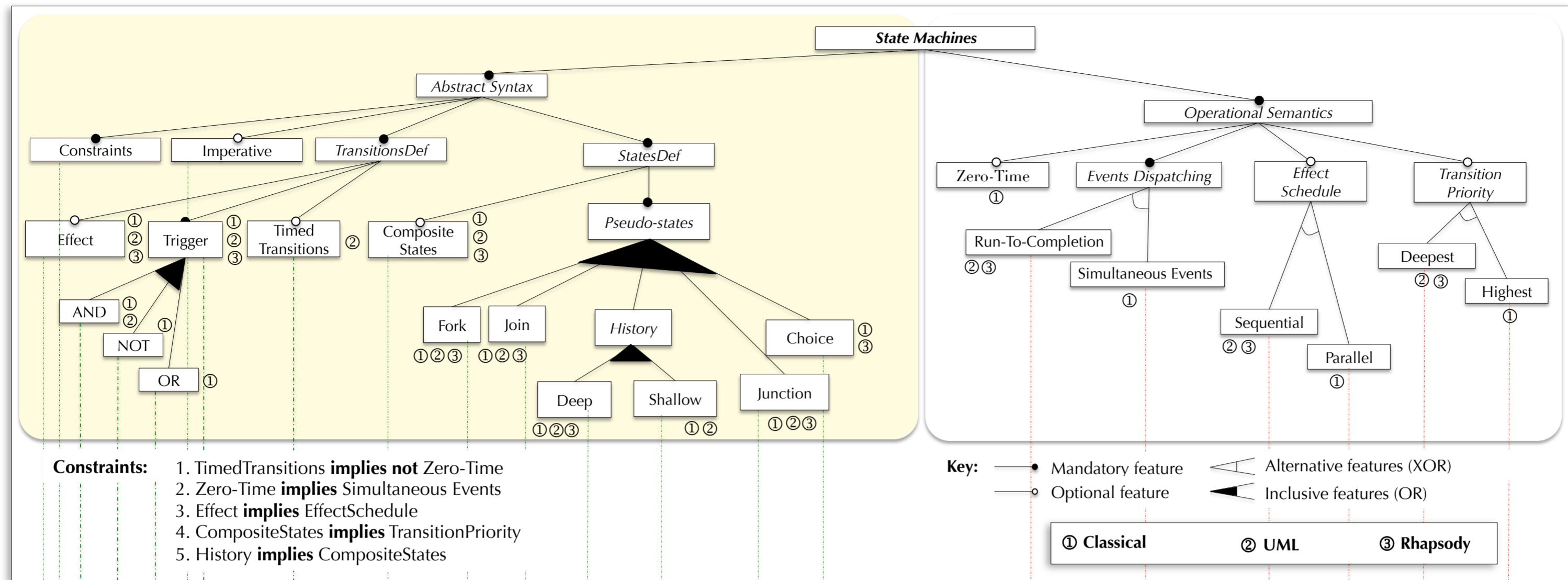


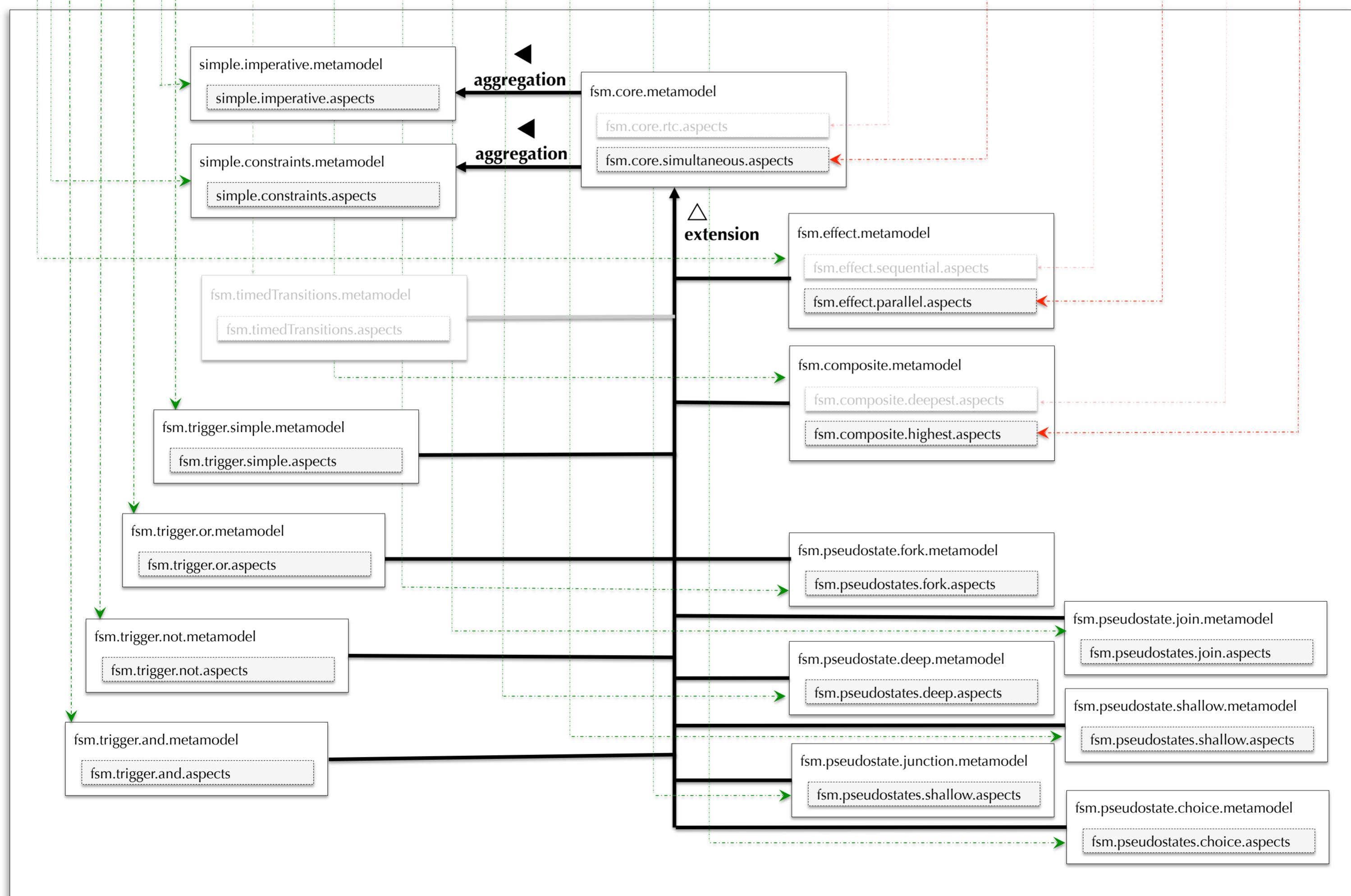
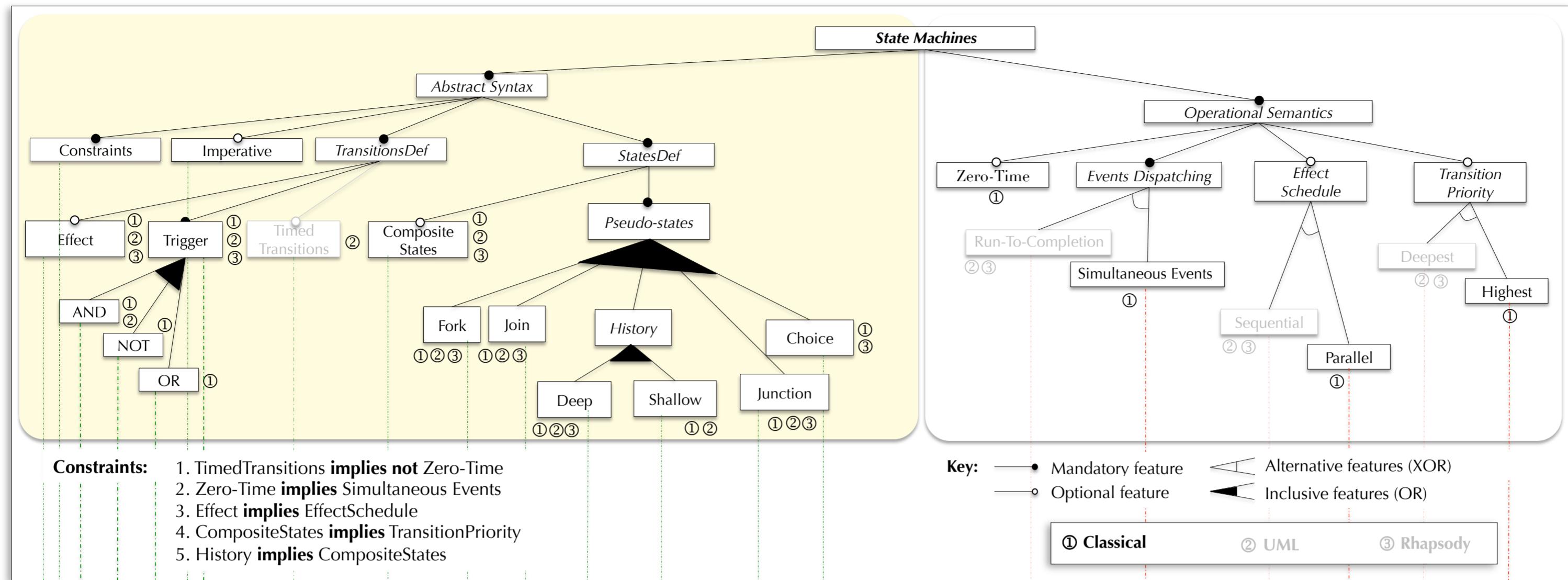
Required Interface: Finite State Machines

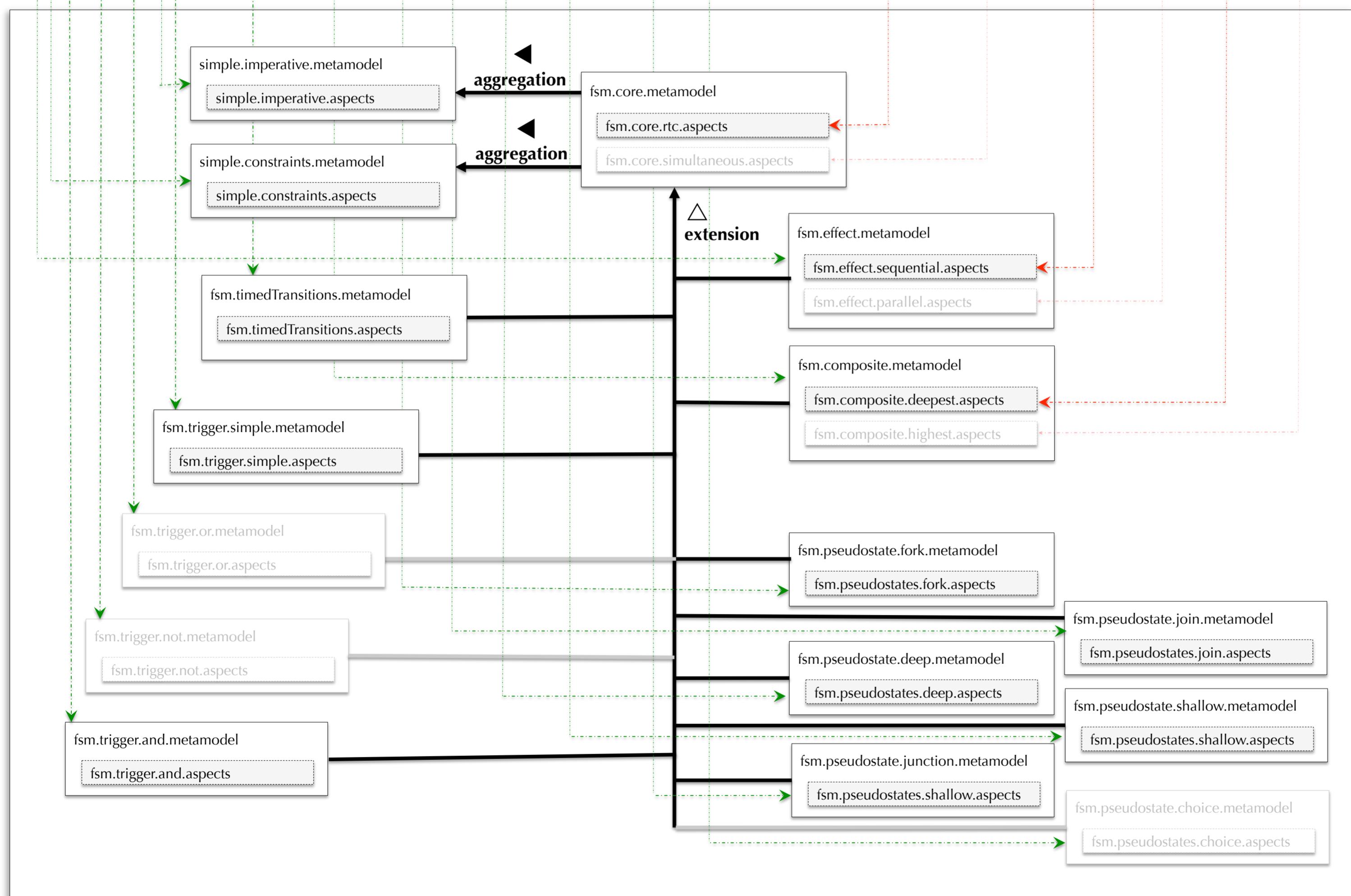
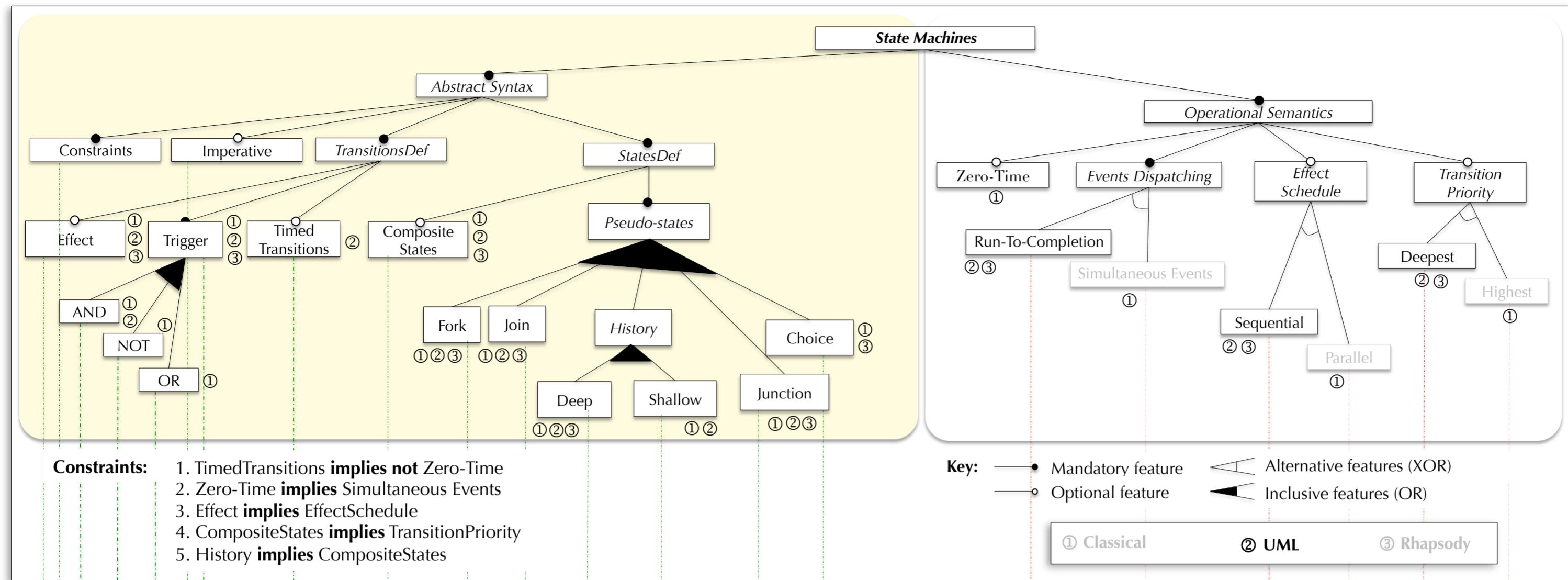
Binding
Java <-> FiniteStateMachines

Binding
C# <-> FiniteStateMachines

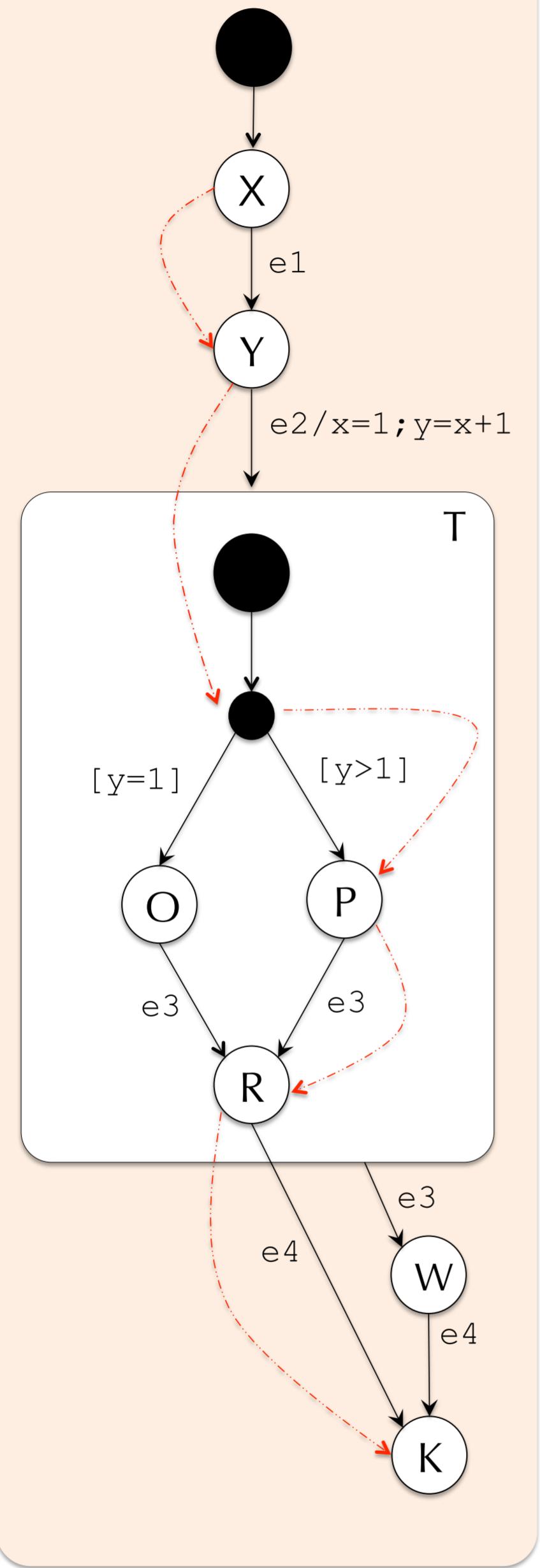




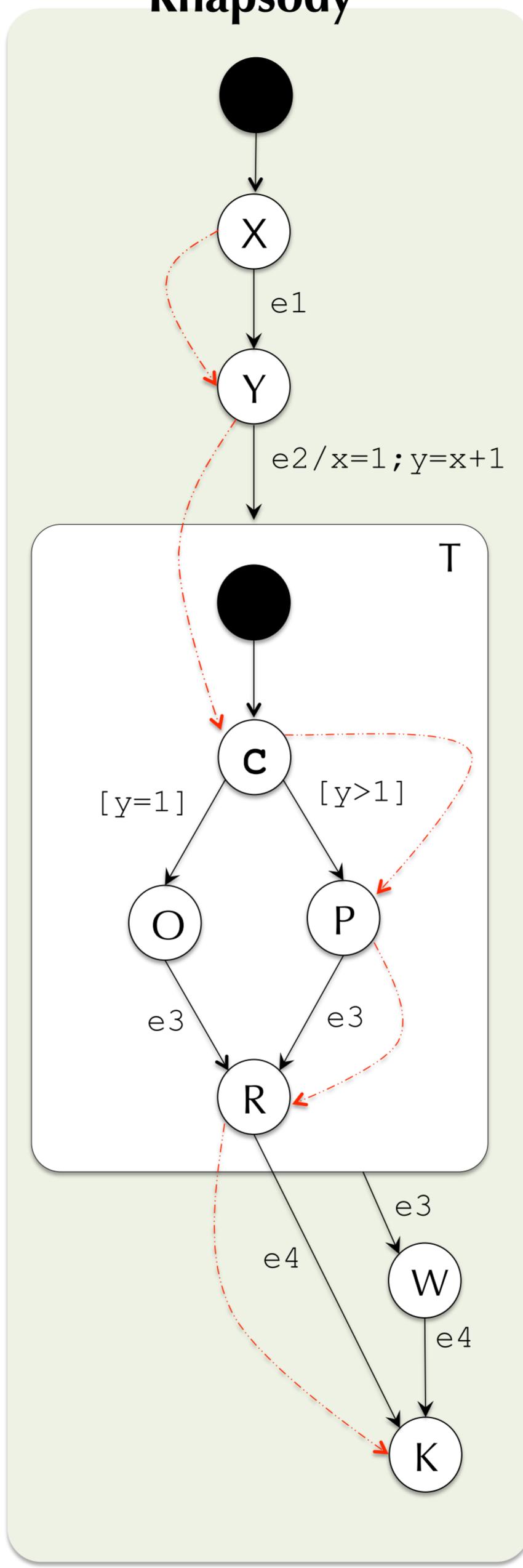




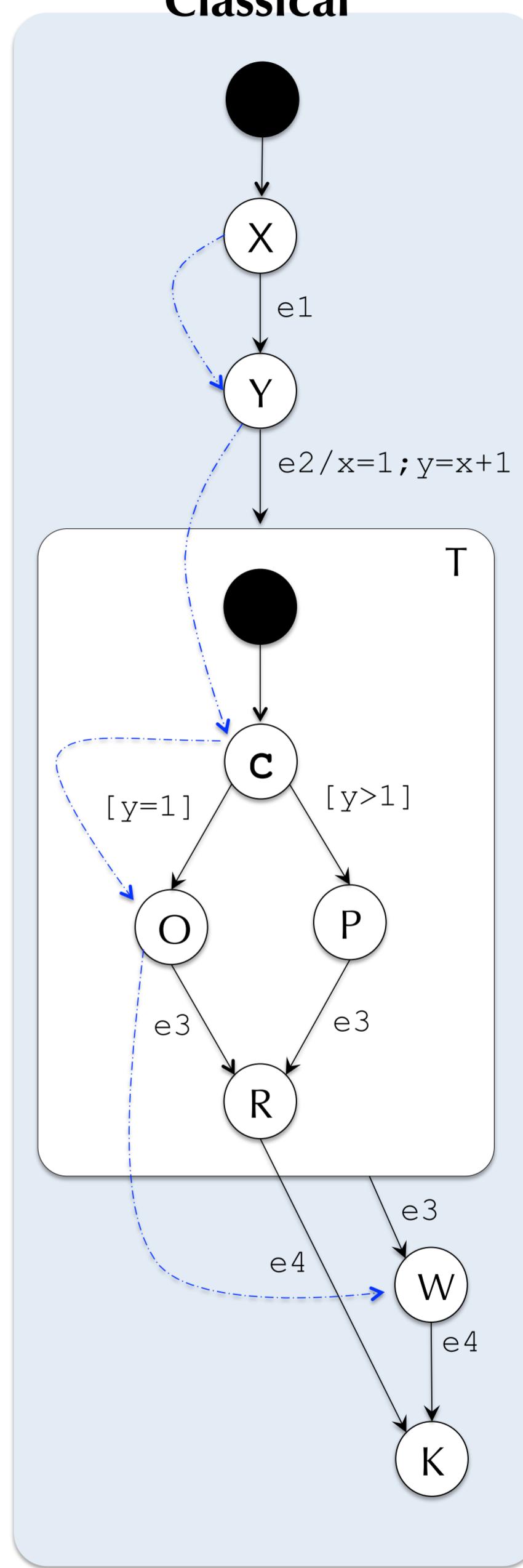
UML: State Machines

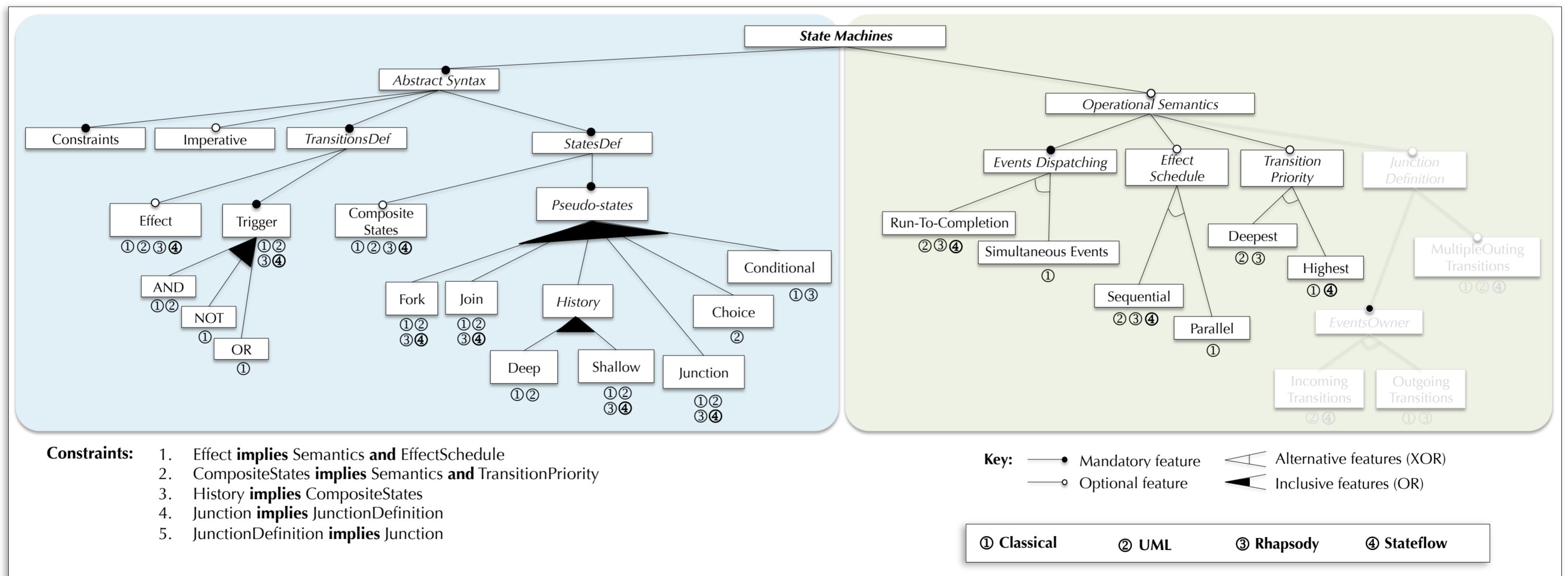
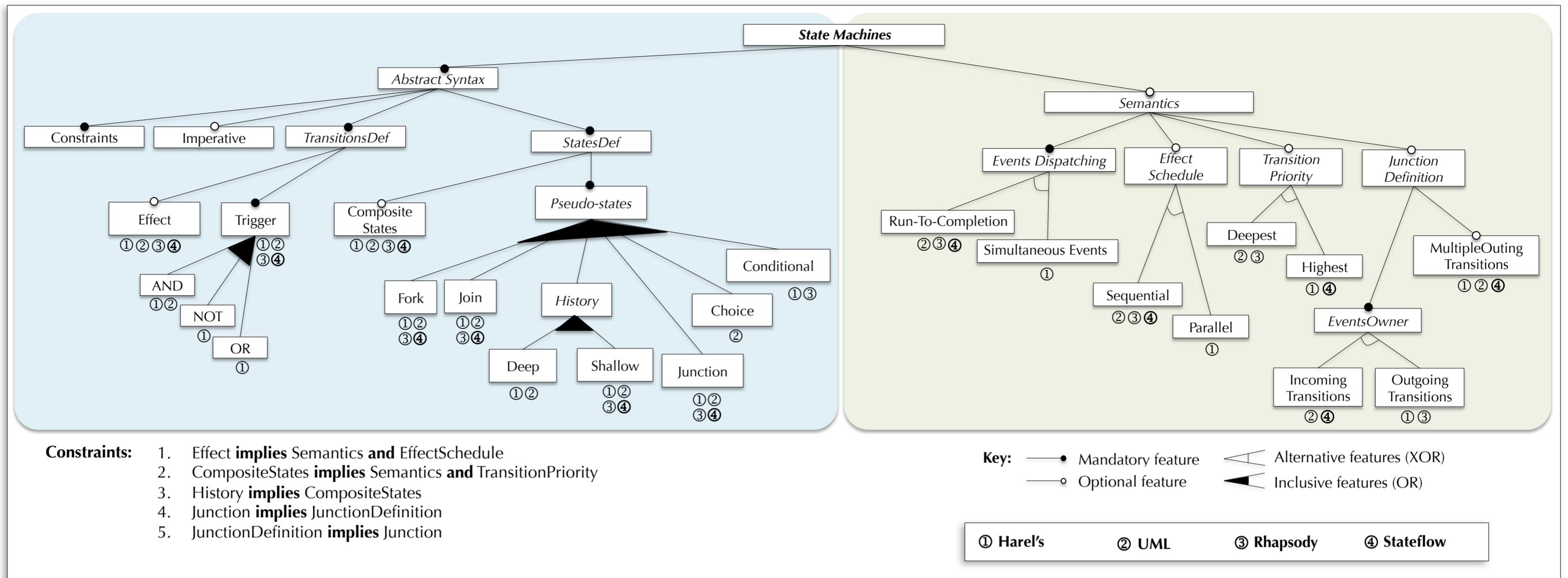


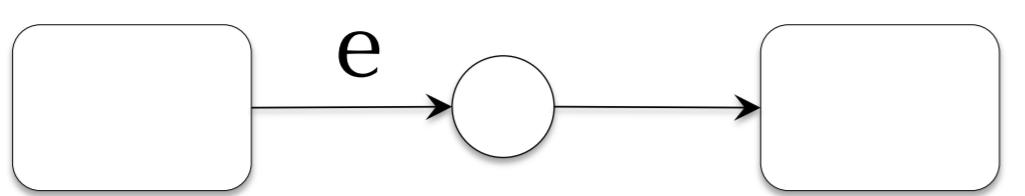
Rhapsody



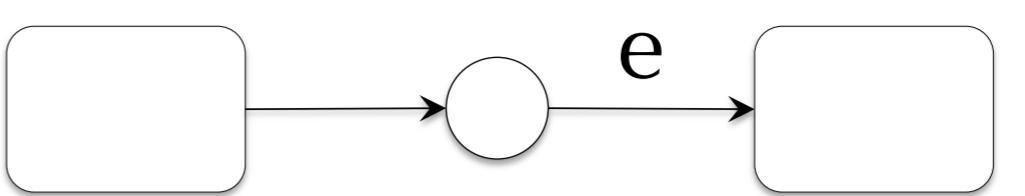
Classical



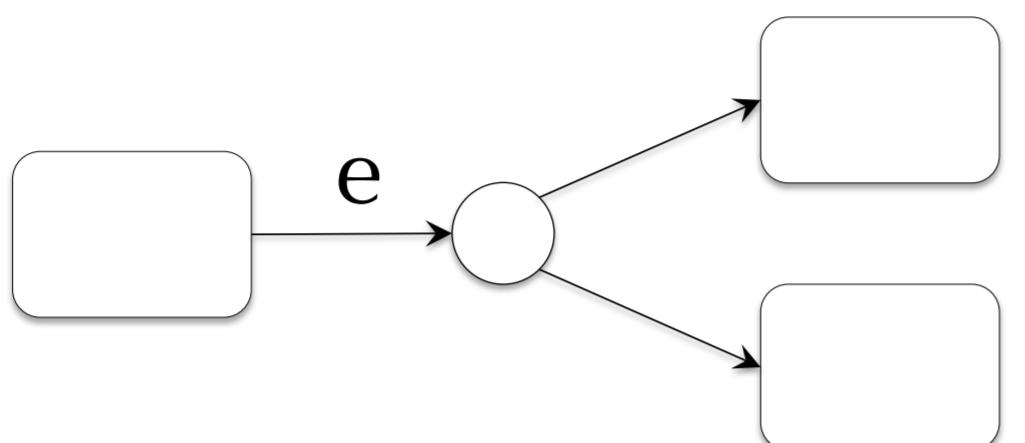




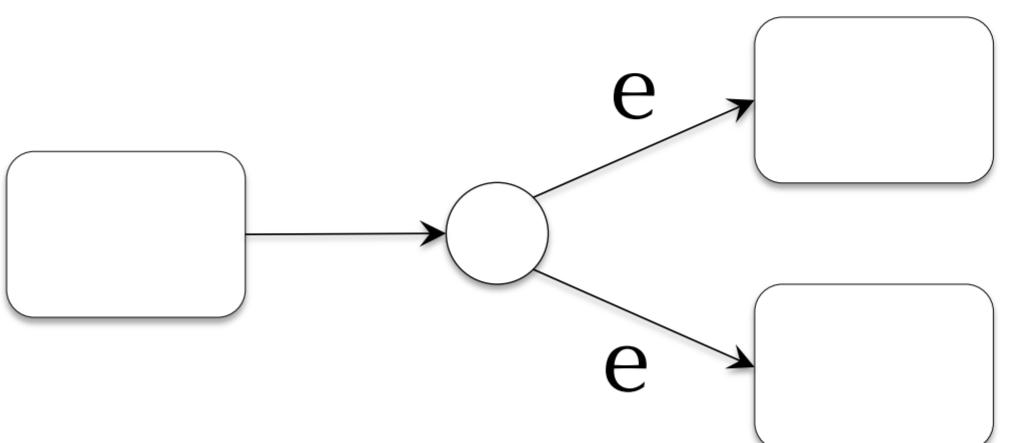
(a)



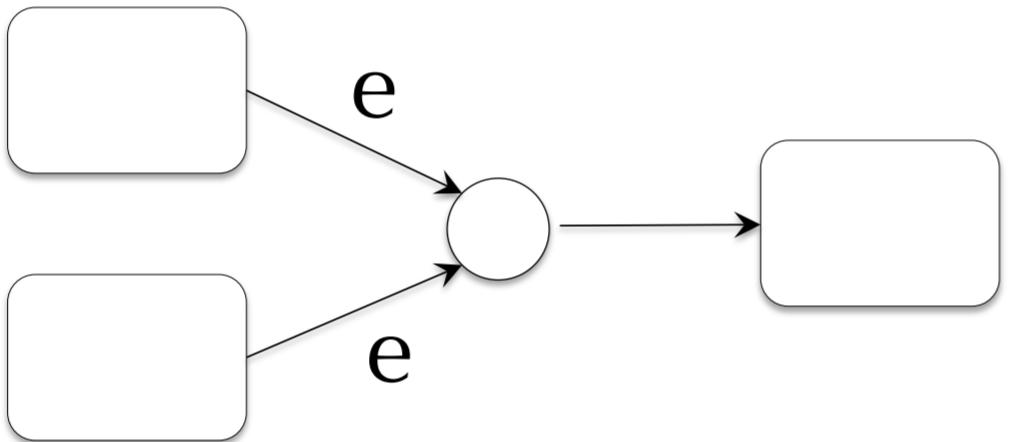
(b)



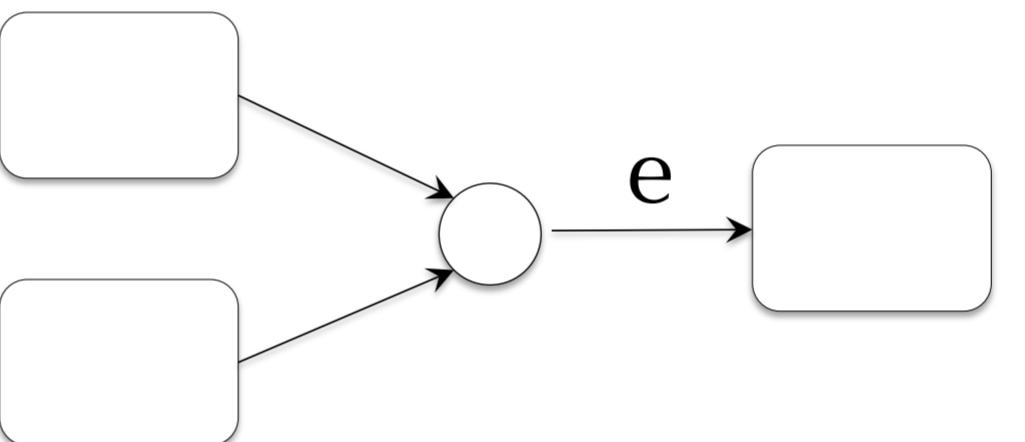
(a)



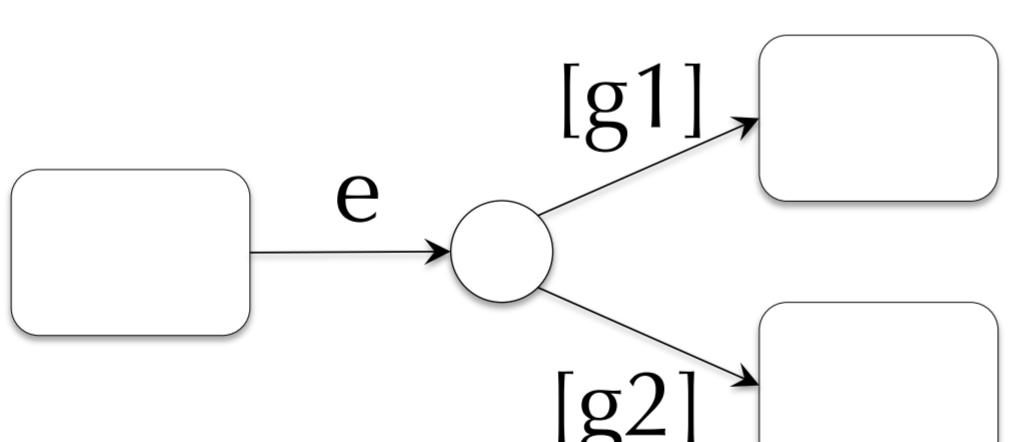
(b)



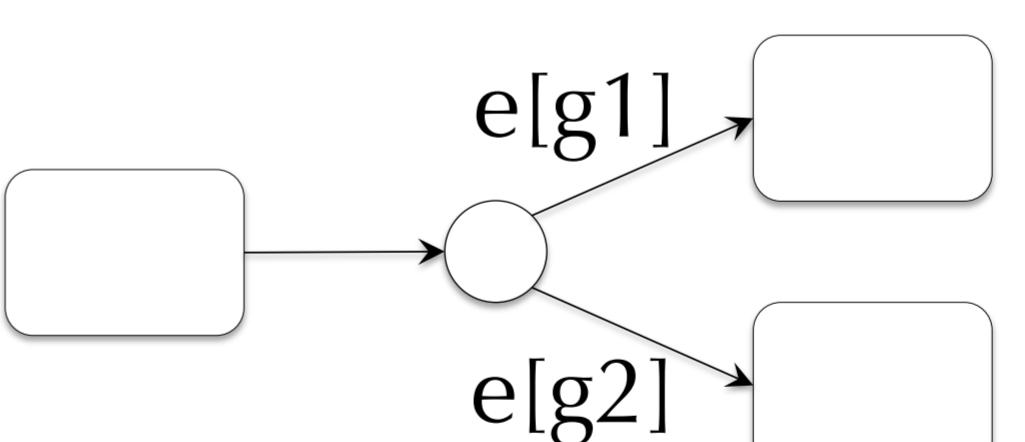
(c)



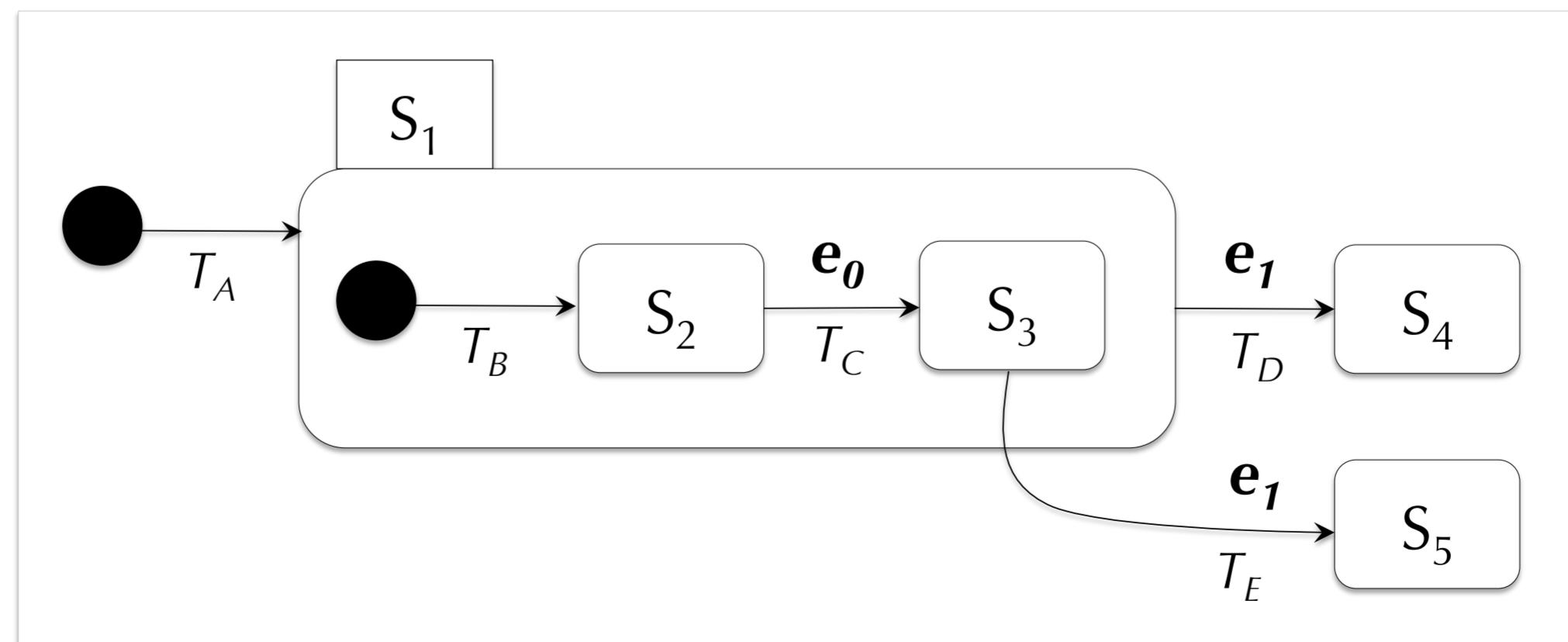
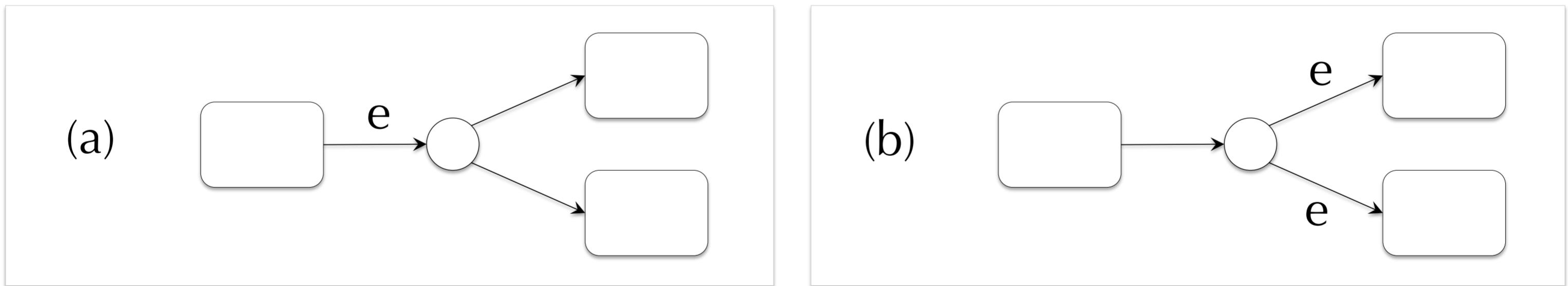
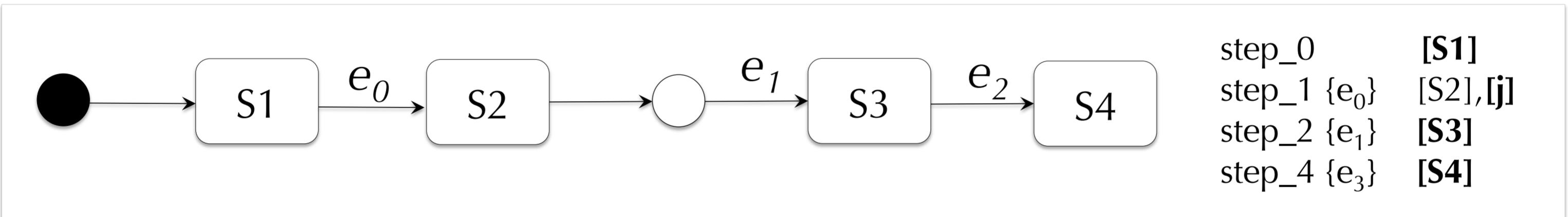
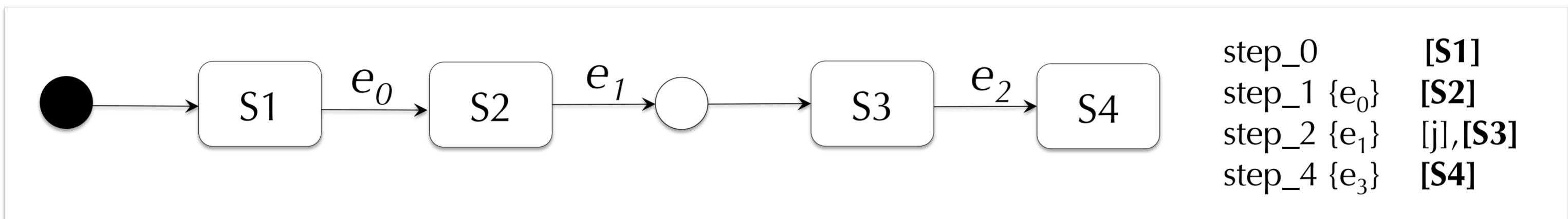
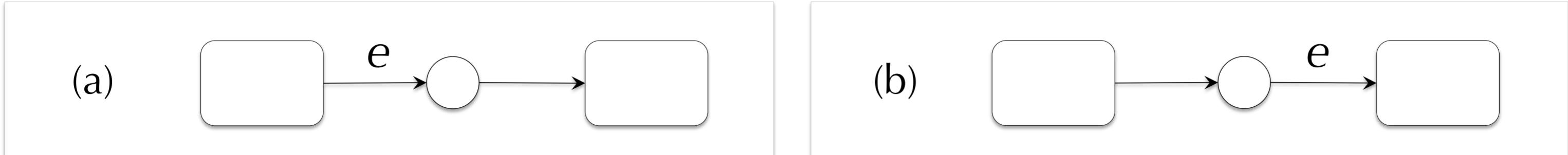
(d)

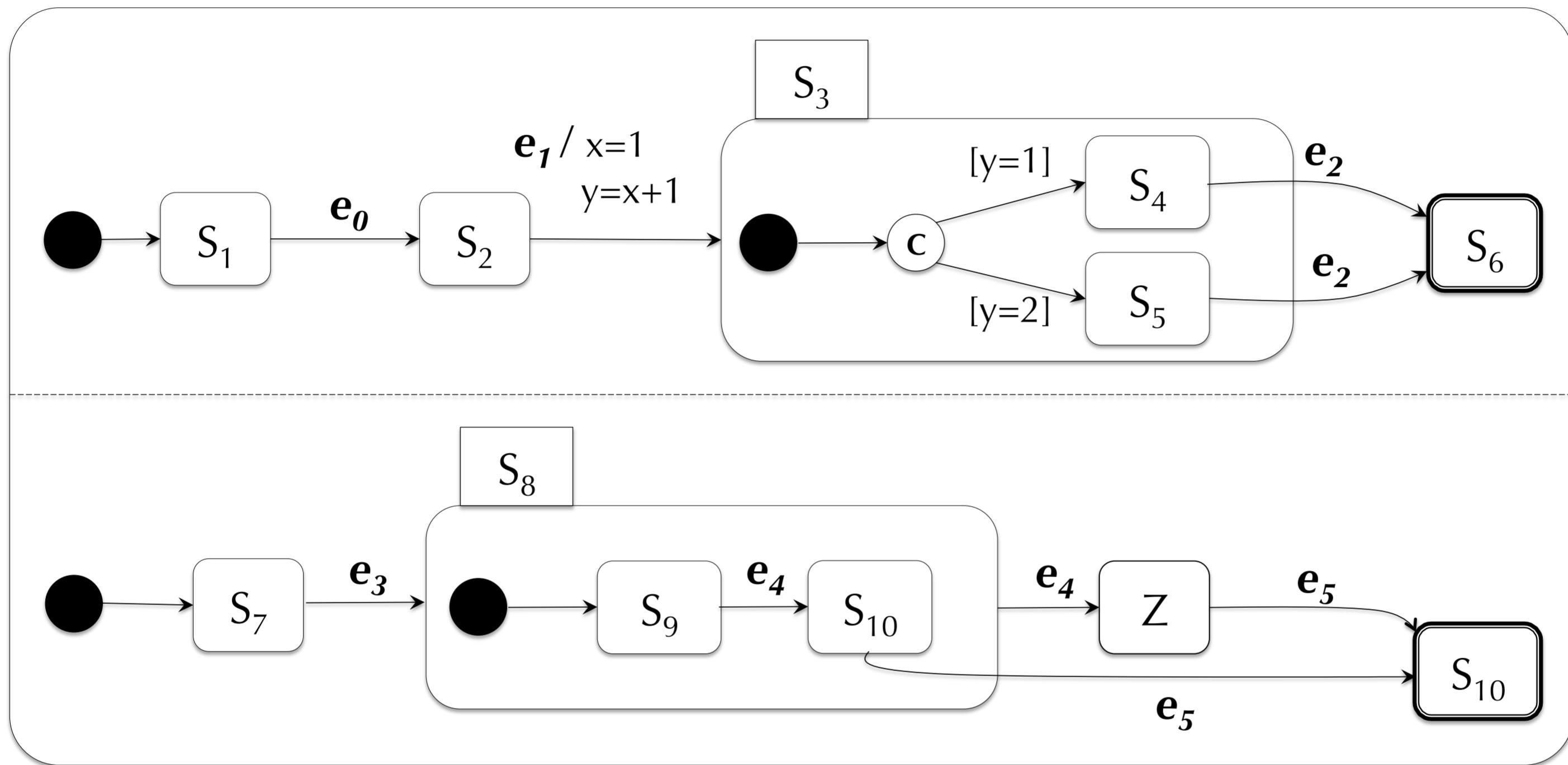
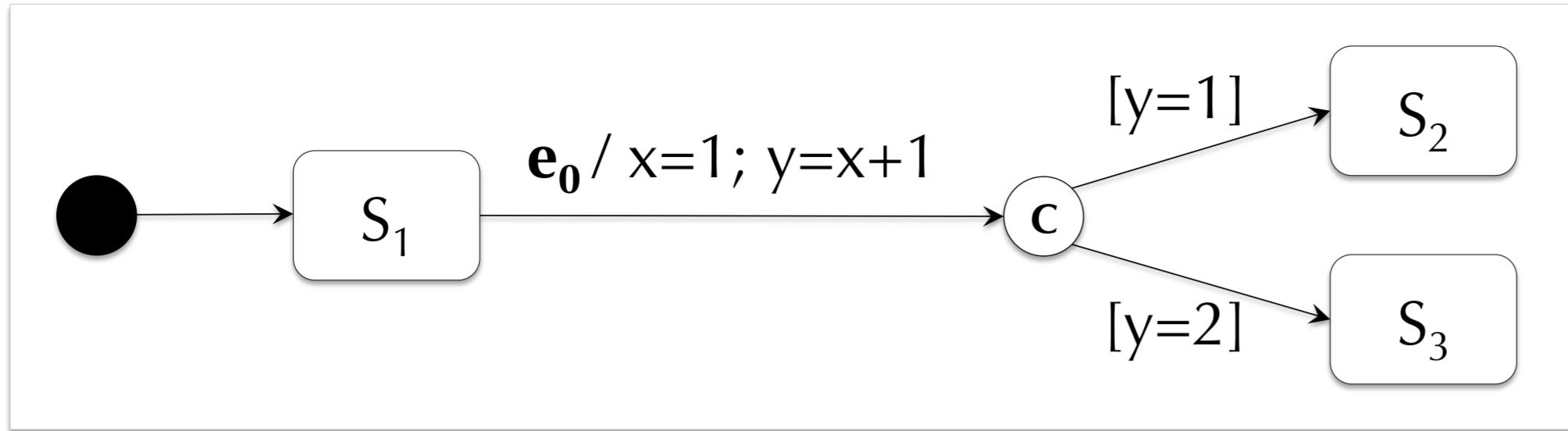


(e)



(f)





Execution traces

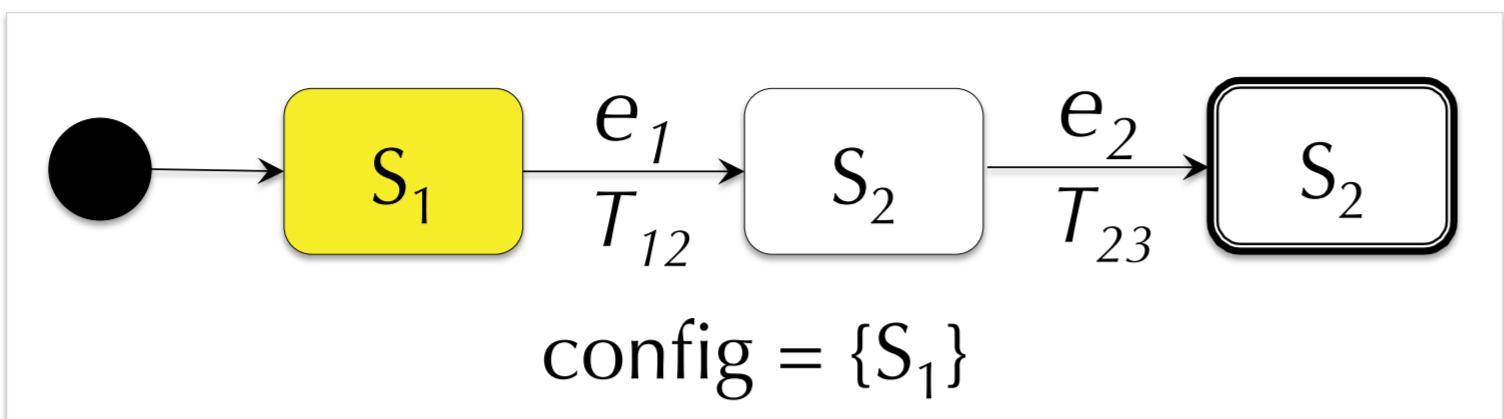
step_0	$[S_1 \ S_2 \ S_{10}]$
step_1 {e ₀ , e ₄ }	$[S_1 \ S_3 \ S_{11}]$
step_2 {e ₁ }	$[S_1 \ S_5 \ S_{11}]$
step_3 {e ₂ , e ₅ }	$[S_1 \ S_8 \ S_{12}]$
step_4 {e ₃ }	$[S_1 \ S_9 \ S_{12}]$

step_0	$[S_1 \ S_2 \ S_{10}]$
step_1 {e ₀ , e ₄ }	$[S_1 \ S_3 \ S_{10}]$
step_2 {e ₁ }	$[S_1 \ S_6 \ S_{11}]$
step_3 {e ₂ , e ₅ }	$[S_1 \ S_7 \ S_{11}]$
step_4 {e ₃ }	$[S_1 \ S_9 \ S_{12}]$

step_0	$[S_1 \ S_2 \ S_{10}]$
step_1 {e ₀ , e ₄ }	$[S_1 \ S_3 \ S_{10}]$
step_2 {e ₁ }	$[S_1 \ S_6 \ S_{11}]$
step_3 {e ₂ , e ₅ }	$[S_1 \ S_7 \ S_{11}]$
step_4 {e ₃ }	$[S_1 \ S_9 \ S_{12}]$

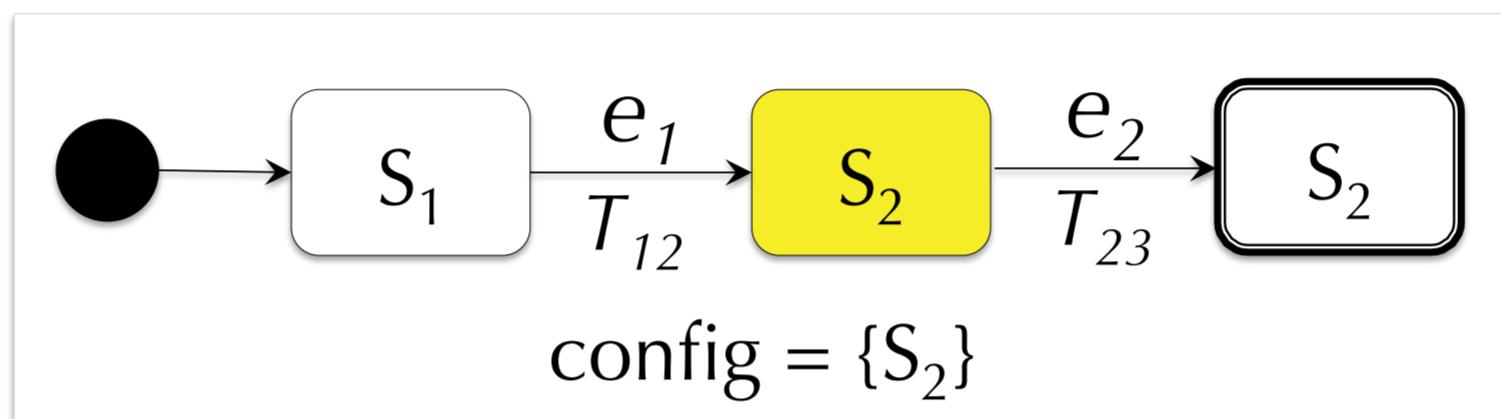
step_0	$[S_1 \ S_2 \ S_{10}]$
step_1 {e ₀ , e ₄ }	$[S_1 \ S_3 \ S_{10}]$
step_2 {e ₁ }	$[S_1 \ S_6 \ S_{11}]$
step_3 {e ₂ , e ₅ }	$[S_1 \ S_8 \ S_{11}]$
step_4 {e ₃ }	$[S_1 \ S_9 \ S_{12}]$

Step 0
(Initialization)



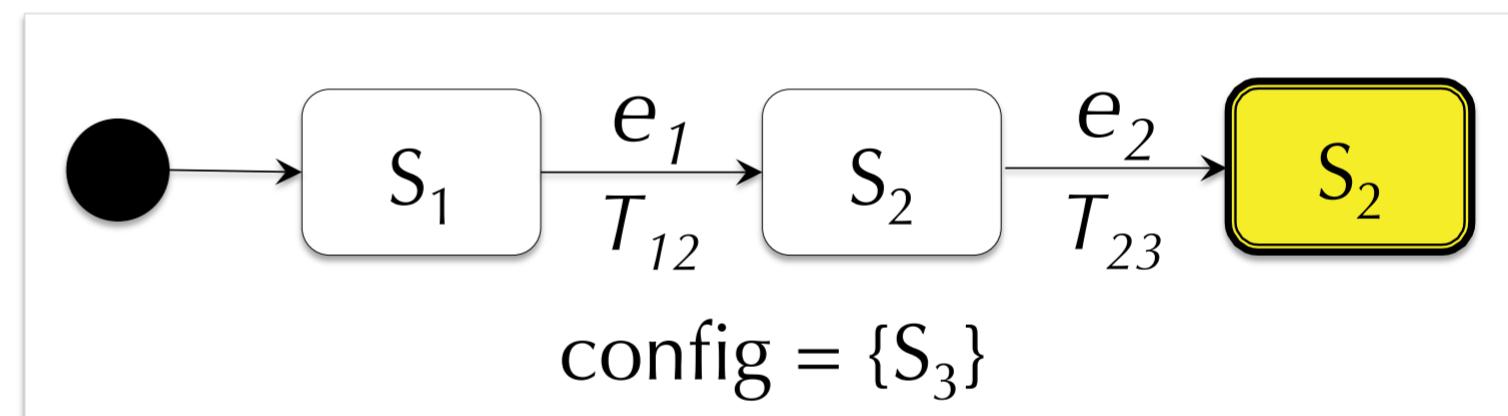
Current configuration (t_0)

Step 1 $\{e_1\}$

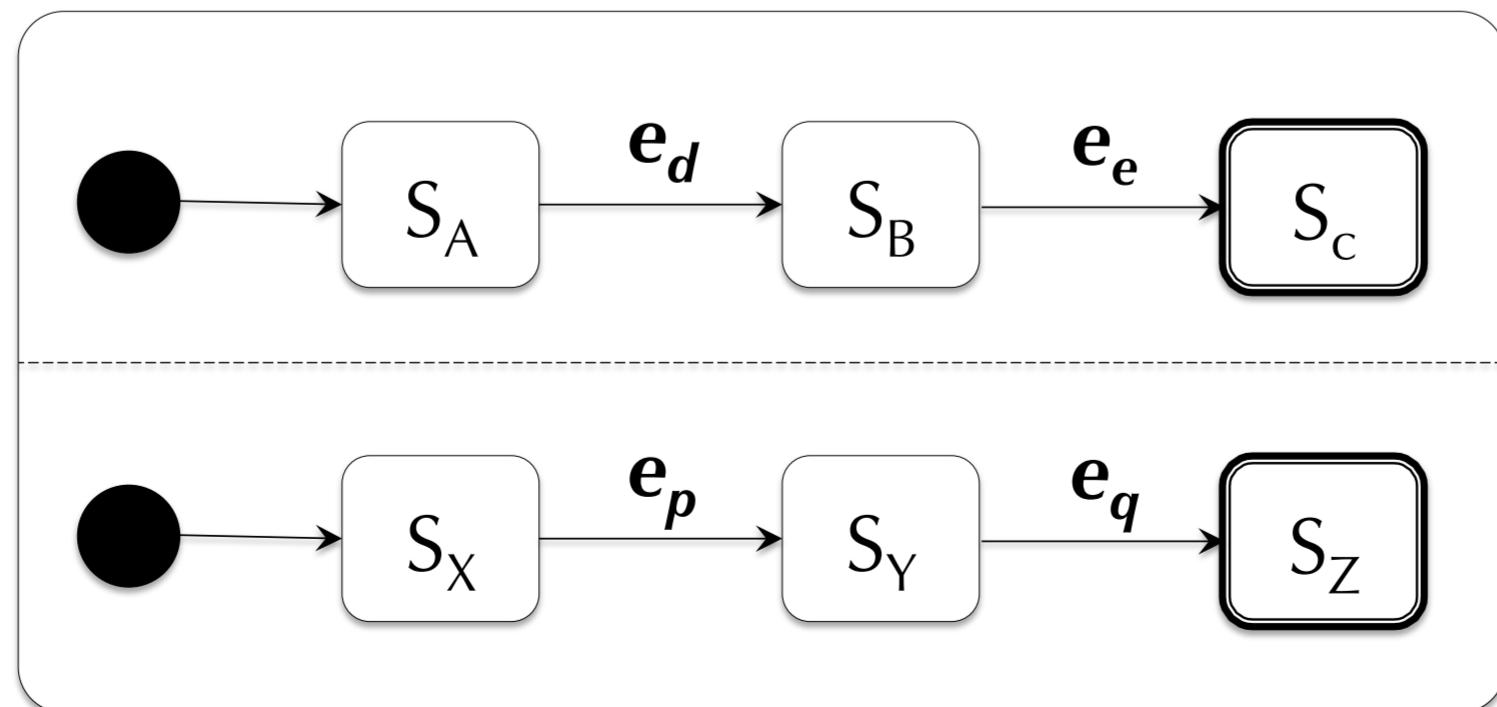


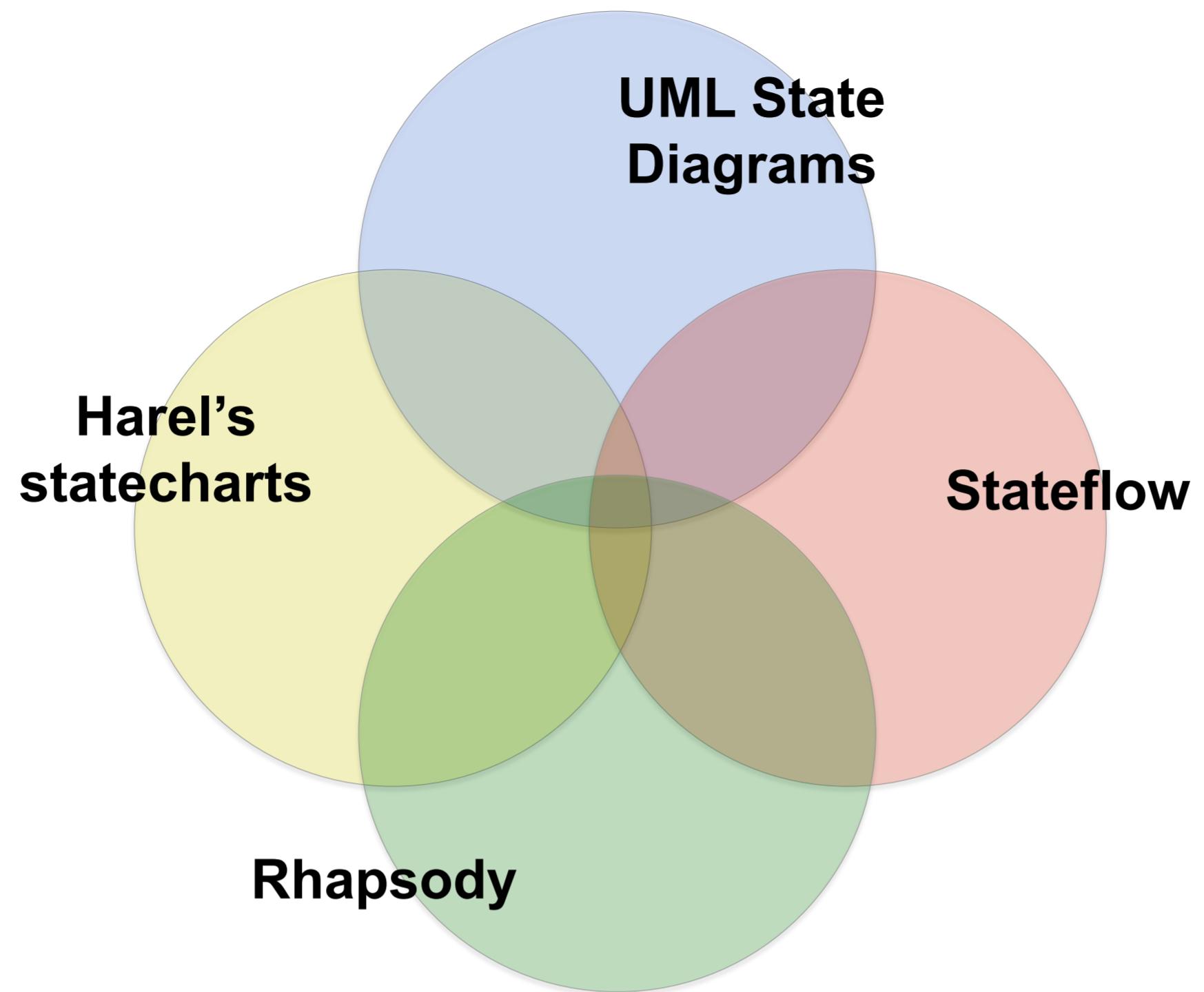
Current configuration (t_1)

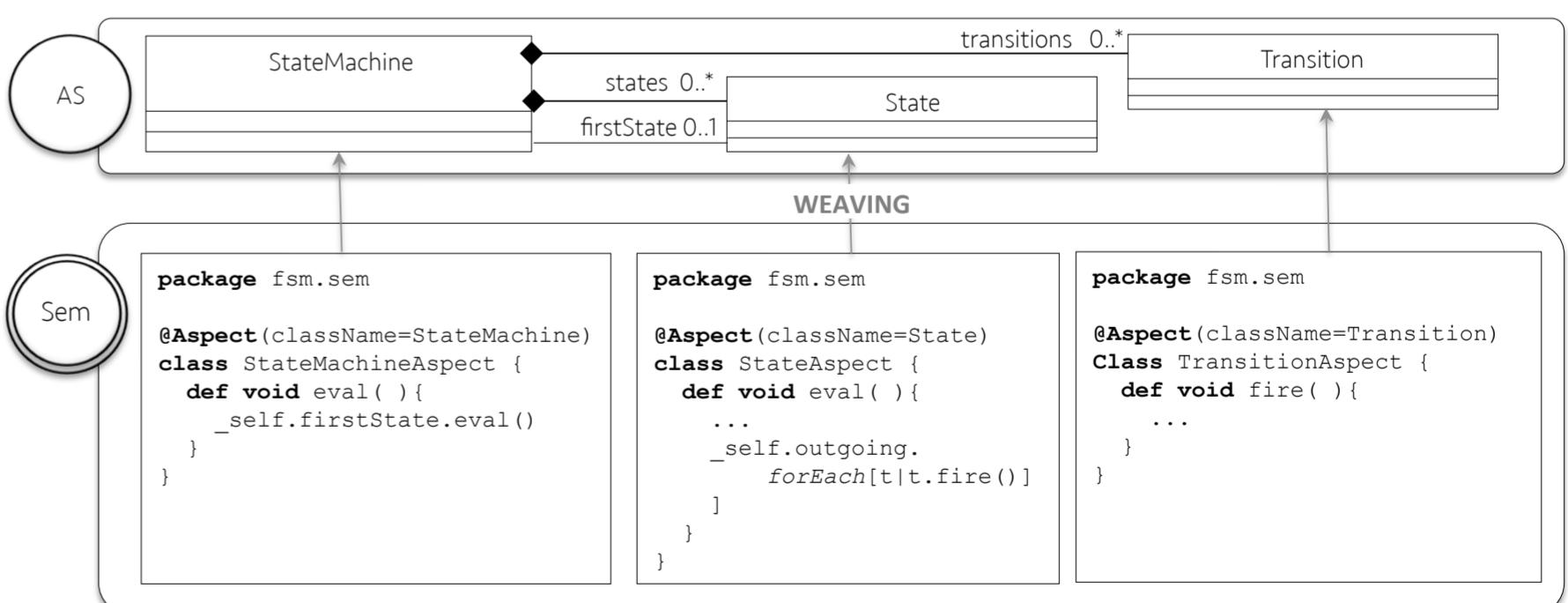
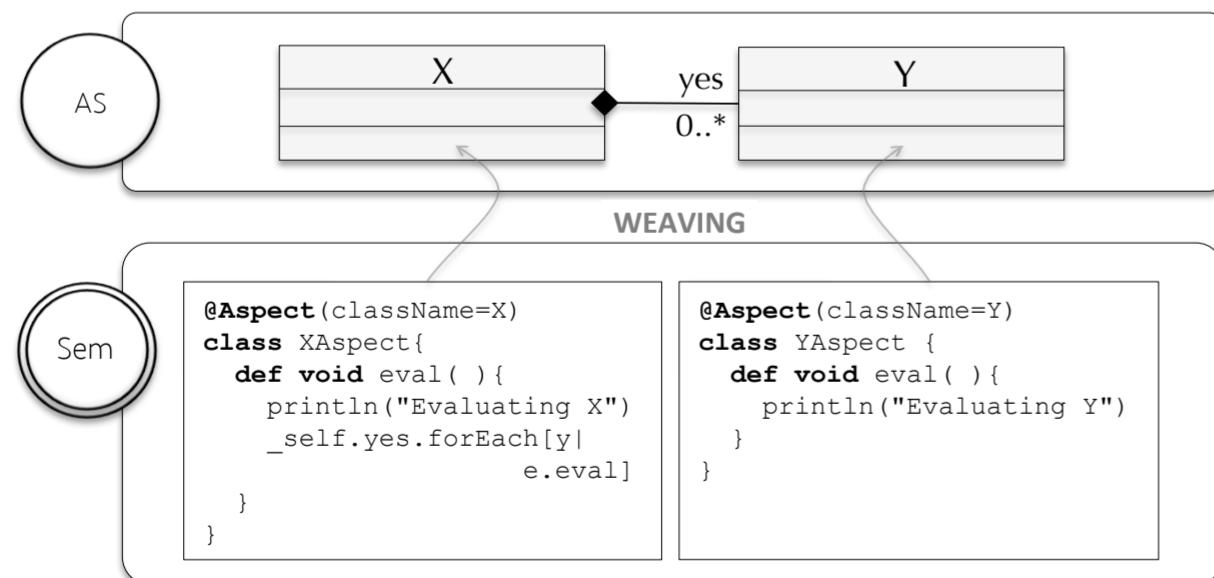
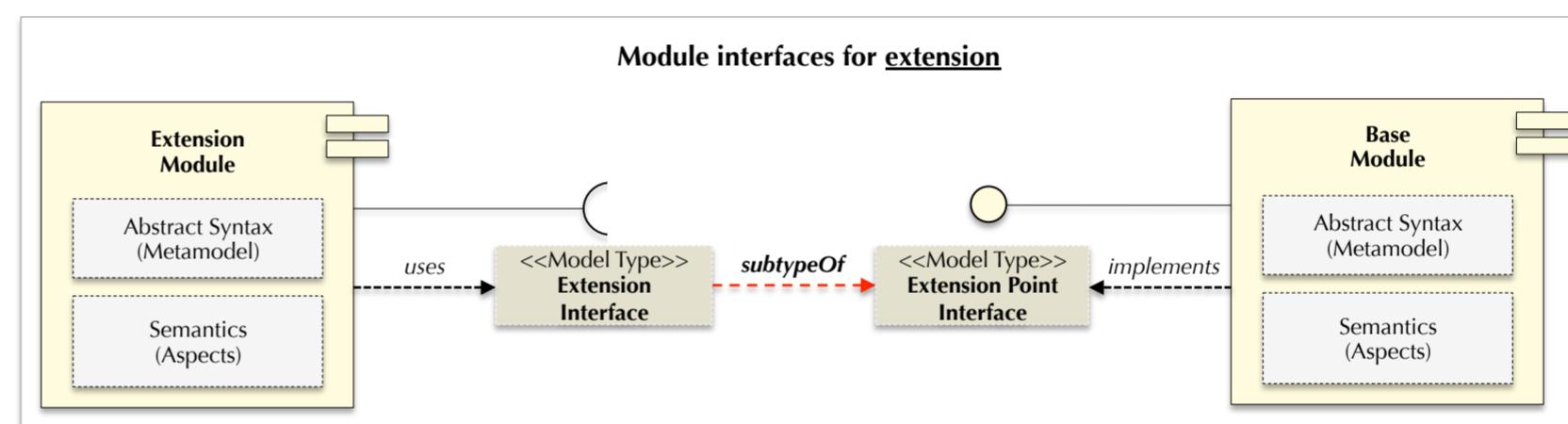
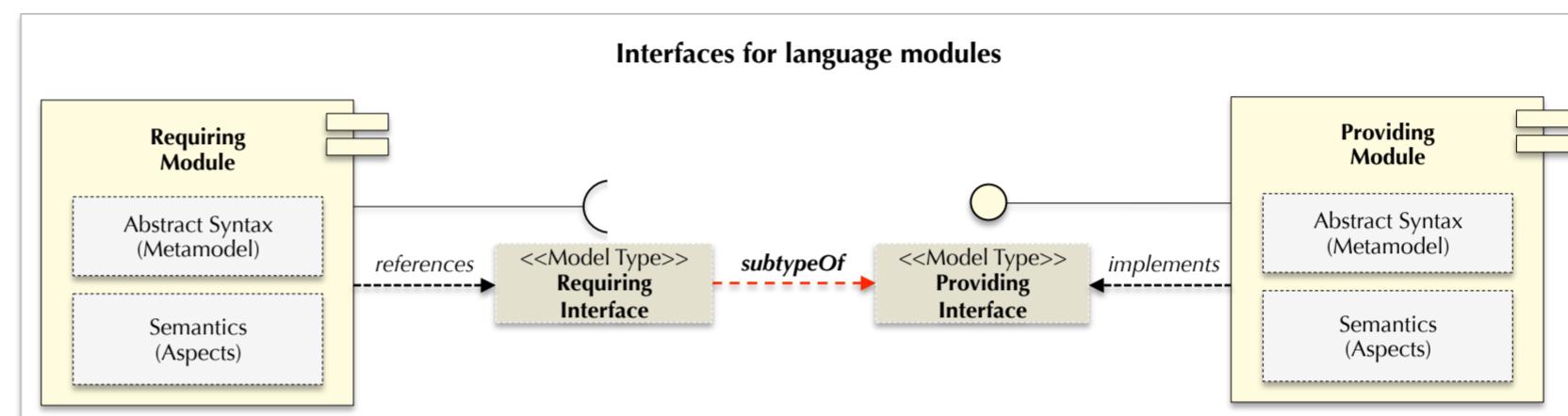
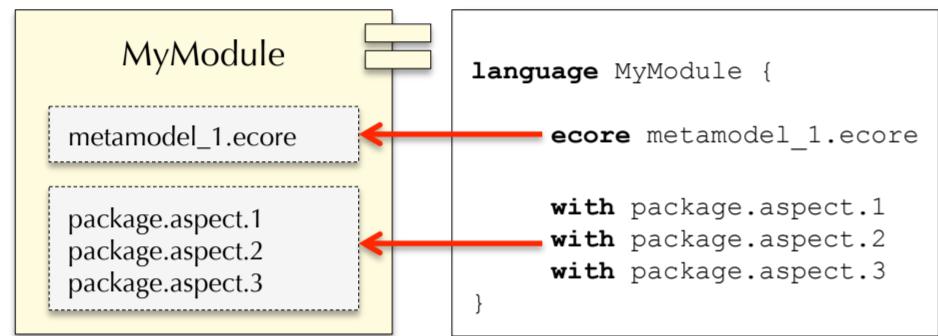
Step 2 $\{e_2\}$
(Final step)

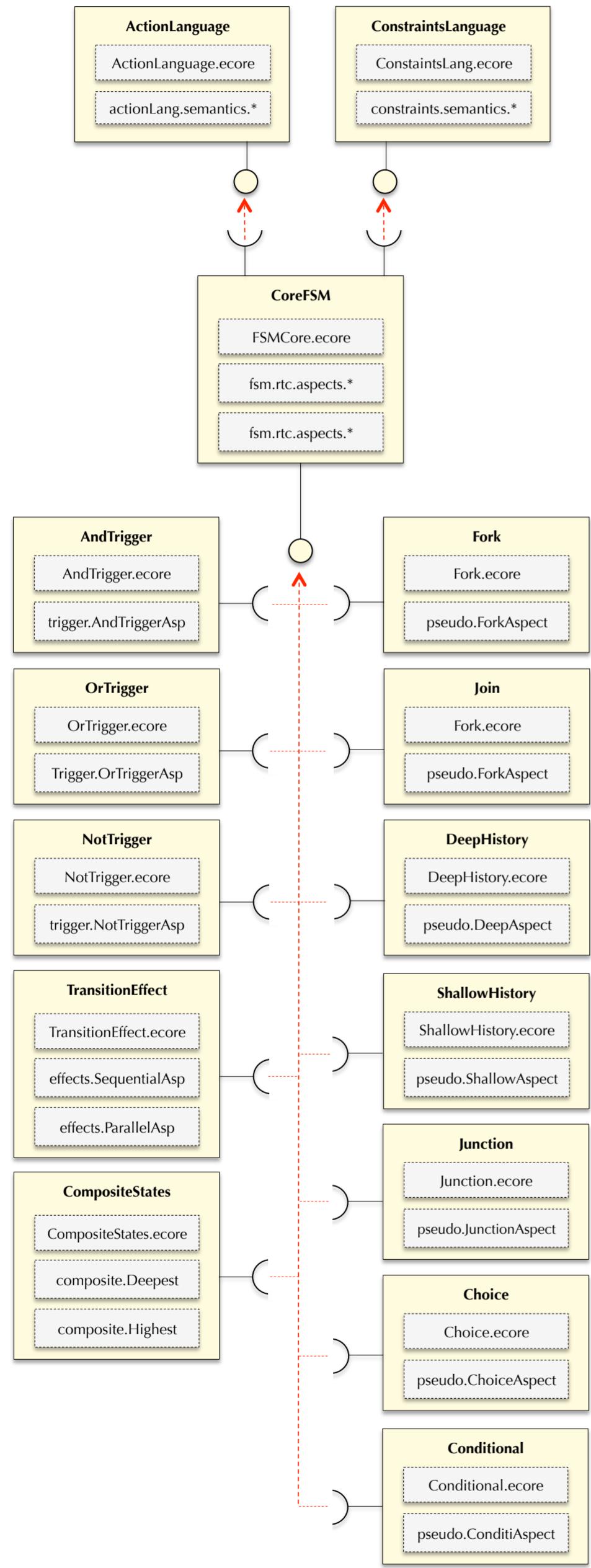


Current configuration (t_2)



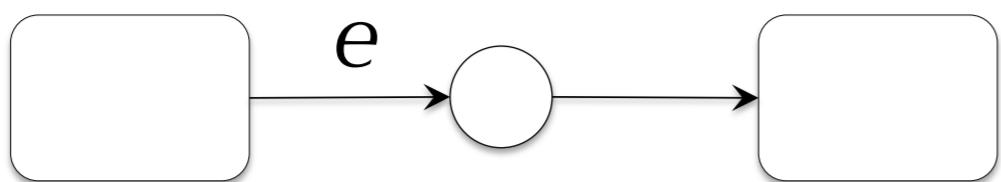




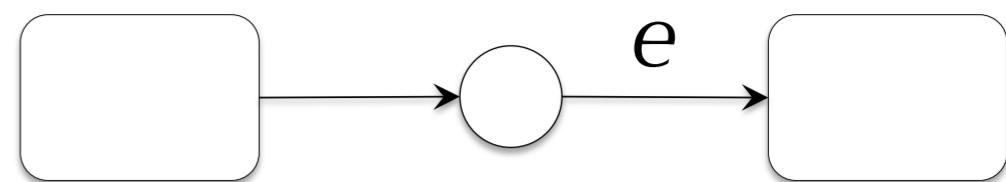


1

(a)

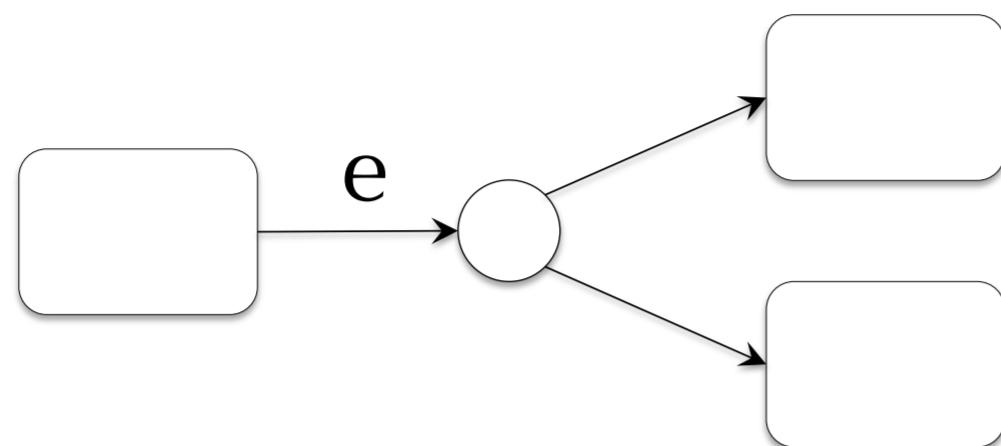


(b)

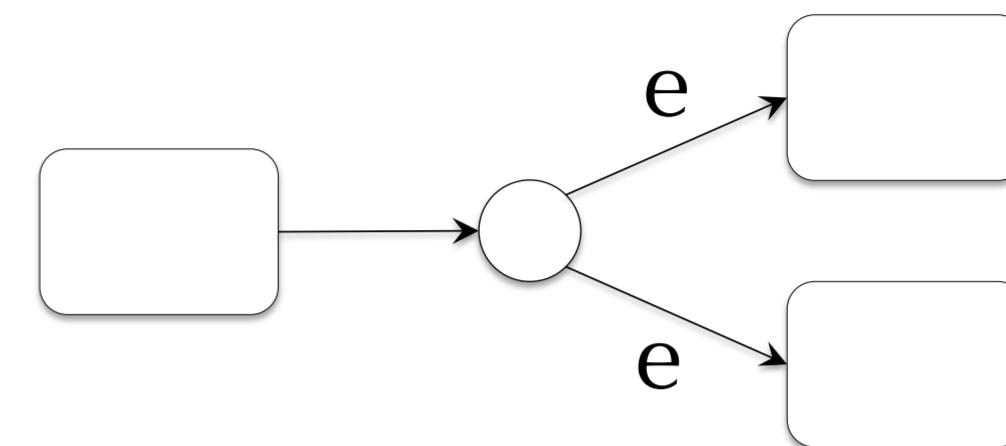


2

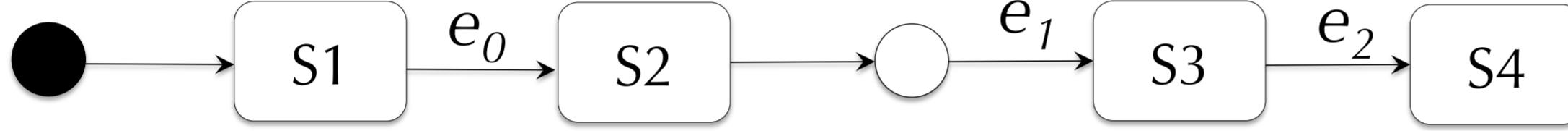
(a)



(b)

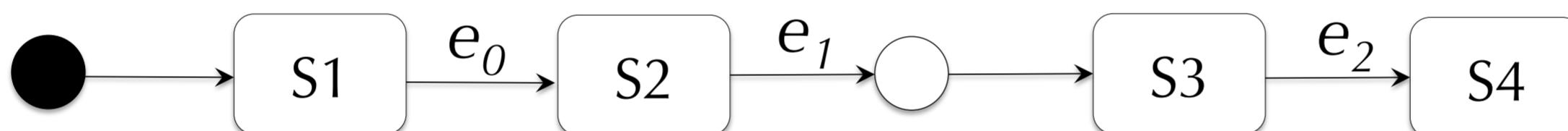


3



step_0	[S1]
step_1 {e ₀ }	[S2], [j]
step_2 {e ₁ }	[S3]
step_4 {e ₃ }	[S4]

4



step_0	[S1]
step_1 {e ₀ }	[S2]
step_2 {e ₁ }	[j], [S3]
step_4 {e ₃ }	[S4]