CS4223 - Examples of Out-of-Order Execution Techniques

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(Slides from Tulika Mitra)

Scoreboard in Action

Scoreboard Data Structures

- Instruction Status: stage instr is in (issue, Read, Ex, WB)
- Functional Unit Status:
 - Busy: whether this FU is busy
 - Op: Operation to perform in this FU (e.g., add or subtract)
 - Fi: Destination register
 - Fj, Fk: Source registers
 - Qj, Qk: Functional units producing source registers Fj,Fk
 - Rj, Rk: Flags indicating when Fj, Fk are ready and not yet read.
- Register result status: Which FU will write each register if an active instr has the register as destination; blank if no pending instr has this register as destination

Dynamic SchedulingScoreboard Example

LD	F6, 34(R2)
LD	F2, 45(R3)
MULT	F0, F2, F4
SUBD	F8, F6, F2
DIVD	F10, F0, F6
ADDD	F6, F8, F2

Execution clock cycles:

LD 1

MULT 10

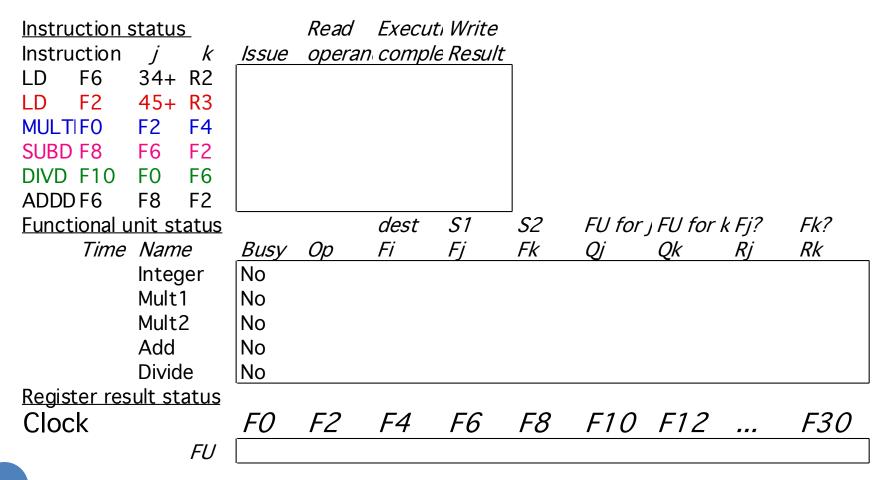
SUBD 2

DIVD 40

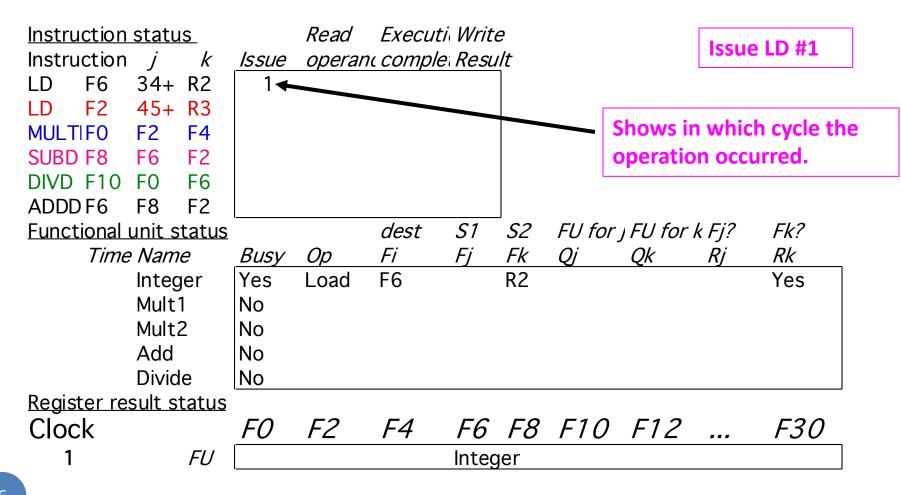
ADDD 2

What are the hazards in this code?

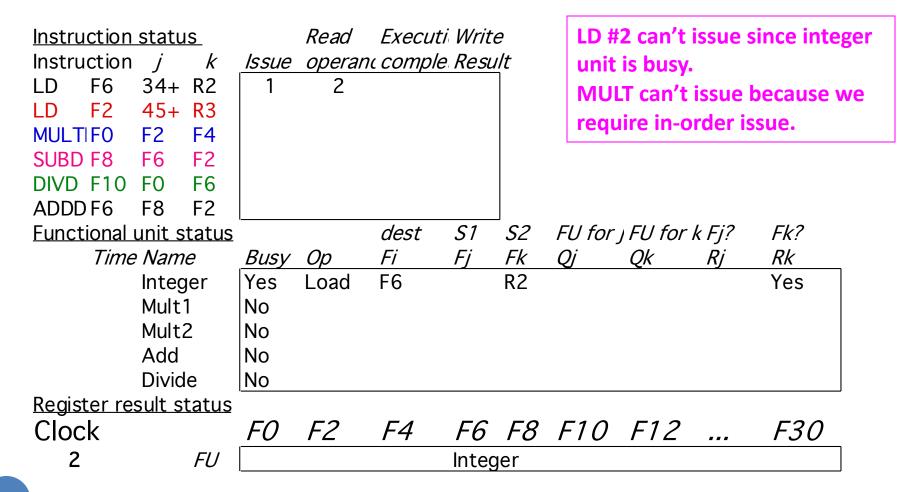
Dynamic Scheduling Scoreboard Example



Dynamic Scheduling



Dynamic Scheduling



Dynamic Scheduling

Instruction status Instruction j k LD F6 34+ R2 LD F2 45+ R3	Read Issue operari 1 2	Executi Wri o <u>ccomple Res</u> 3		addre	ne LD ca ss gene ory acce	ration	and
MULTIFO F2 F4							
SUBD F8 F6 F2							
DIVD F10 F0 F6							
ADDD F6 F8 F2							
Functional unit status		dest S1	 S2	FU for	FU for I	k Fj?	Fk?
Time Name	Busy Op	Fi Fj	Fk	Qj	Qk	Ŕj	Rk
Integer	Yes Load	F6	R2				Yes
Mult1	No						
Mult2	No						
Add	No						
Divide	No						
Register result status	•						
Clock	F0 F2	F4 F6	F8	F10	F12		F30
CIOCK	· · · · · ·						

Dynamic Scheduling

Instruction status Instruction j k LD F6 34+ R2	<i>Issue</i>	Read operari 2	Execut o <u>ccomple</u> 3		_				
LD F2 45+ R3									
MULTIFO F2 F4									
SUBD F8 F6 F2									
DIVD F10 F0 F6									
ADDD F6 F8 F2									
Functional unit status			dest	<i>S1</i>	<i>S2</i>	FU for	FU for	k Fj?	Fk?
Time Name	Busy	Ор	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Integer	Yes	Load	F6		R2				Yes
Mult1	No								
Mult2	No								
Add	No								
Divide	No								
Register result status									
Clock	F0	F2	F4	<i>F6</i>	F8	F10	F12		F30
4 <i>FU</i>				Integ	ger				

Dynamic Scheduling

Instruction status Instruction j k		Executi Writ	_	Issue L now fr		nce int	eger unit is
LD F6 34+ R2	1 2	3 4					
LD F2 45+ R3	5						
MULTIFO F2 F4							
SUBD F8 F6 F2							
DIVD F10 F0 F6							
ADDDF6 F8 F2							
Functional unit status		dest S1	<i>S2</i>	FU for J	FU for k	k Fj?	Fk?
Time Name	Busy Op	Fi Fj	Fk	Qj	Qk	Rj	Rk
Integer	Yes Load	F2	R3				Yes
Mult1	No						
Mult2	No						
Add	No						
Divide	No						
Register result status							
Clock	F0 F2	F4 F6	F8	F10	F12		F30
5 <i>FU</i>	Intege	r					

Dynamic Scheduling

Instruction status	,	Read	Executi				Issue N	IULT.	
Instruction <i>j k</i>	<u>Issue</u>	operan	comple	Kesu	/t				
LD F6 34+ R2	1	2	3	4					
LD F2 45+ R3	5	6							
MULTIFO F2 F4	6								
SUBD F8 F6 F2									
DIVD F10 F0 F6									
ADDD F6 F8 F2									
Functional unit status			dest	<i>S1</i>	<i>S2</i>	FU for J	FU for k	Fj?	Fk?
Time Name	Busy	Ор	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Integer	Yes	Load	F2		R3				Yes
Mult 1	Yes	Mult	F0	F2	F4	Integer		No	Yes
Mult2	No								
Add	No								
Divide	No								
Register result status	•								
Clock	FO	F2	F4	<i>F6</i>	F8	F10	F12		F30
6 FU	Mult1	Integer							

Dynamic Scheduling

Scoreboard Example Cycle 7

<u>Instru</u>	ction	<u>statu</u>	<u>S</u>		Read	Executi	Write	,
Instru	ction	j	k	Issue	operand	comple	Resul	lt
LD	F6	34+	R2	1	2	3	4	
LD	F2	45+	R3	5	6	7		
MULT	F0	F2	F4	6				
SUBD	F8	F6	F2	7				
DIVD	F10	FO	F6					
ADDD	F6	F8	F2					
	_	_				_		_

MULT can't read its operands (F2) because LD #2 hasn't finished.

Functional unit status

Time Name
Integer
Mult1
Mult2
Add
Divide

		dest	51	52	FU for ,	i FU for k	(FJ?	FK?
Busy	Ор	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Yes	Load	F2		R3				Yes
Yes	Mult	FO	F2	F4	Integer		No	Yes
No								
Yes	Sub	F8	F6	F2		Integer	Yes	No
No						J		

Register result status

Clock

FU

FO	F2	<i>F4</i>	F6 I	F8 F10	F12	 F30
Mult1	Integer		A	Add		

Dynamic Scheduling

Scoreboard Example Cycle 8a

<u>Instru</u>	<u>ction</u>	<u>statu</u>	<u>S</u>		Read	Executi	Write
Instru	ction	j	K	Issue	operand	comple	Result
LD	F6	34+	R2	1	2	3	4
LD	F2	45+	R3	5	6	7	
MULT	FO	F2	F4	6			
SUBD	F8	F6	F2	7			
DIVD	F10	F0	F6	8			
ADDD	F6	F8	F2				
	_	_					_

DIVD issues. MULT and SUBD both waiting for F2.

Functional unit status
Time Name
Integer
Mult1
Mult2
Add
Divide

<u> </u>		dest	<i>S1</i>	<i>S2</i>	FU for J FU for	r k Fj?	Fk?
Busy	Ор	Fi	Fj	Fk	Qj Qk	Rj	Rk
Yes	Load	F2		R3			Yes
Yes	Mult	FO	F2	F4	Integer	No	Yes
No					_		
Yes	Sub	F8	F6	F2	Intege	r Yes	No
Yes	Div	F10	FO	F6	Mult1	No	Yes

Register result status

Clock 8 FU

F0	<i>F2</i>	F4	F6	F8	F10	F12	 F30
Mult1	Integer			Add	Divide		

Dynamic Scheduling

Instruction status	Read	' Execut	ti Write	e	LD #2	writes	F2.	
Instruction j k	Issue opera	anc comple	e Resu	<u>/</u> t				
LD F6 34+ R2	1 2	3	4					
LD F2 45+ R3	5 6	7	8					
MULTIFO F2 F4	6							
SUBD F8 F6 F2	7							
DIVD F10 F0 F6	8							
ADDD F6 F8 F2								
Functional unit status		dest	<i>S1</i>	<i>S2</i>	FU for	FU for I	k Fj?	Fk?
Time Name	Busy Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Integer	No							
Mult1	Yes Mult	FO	F2	F4			Yes	Yes
Mult2	No							
Add	Yes Sub	F8	F6	F2			Yes	Yes
Divide	Yes Div	F10	FO	F6	Mult1		No	Yes
Register result status							·	
Clock	F0 F2	F4	F6	F8	F10	F12		F30
8 <i>FU</i>	Mult1			Add	Divide			

Dynamic Scheduling

Instruction status		Read	Execut	ti Write	e				
Instruction <i>j k</i>	Issue	operar	າເ compl	e Resu	<u>ı</u> /t	Now M	IIIT and	CLIDE	Can both
LD F6 34+ R2	1	2	3	4				1 3UBL	J can both
LD F2 45+ R3	5	6	7	8		read F2	•		
MULTIFO F2 F4	6	9				How ca	n both i	nstru	ctions do
SUBD F8 F6 F2	7	9				this at t	he sam	e time	e??
DIVD F10 F0 F6	8								
ADDD F6 F8 F2									
Functional unit status			dest	<i>S1</i>	<i>S2</i>	FU for J	FU for k	k Fj?	Fk?
Time Name	Busy	Ор	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Integer	No								
10 Mult1	Yes	Mult	FO	F2	F4			Yes	Yes
Mult2	No								
2 Add	Yes	Sub	F8	F6	F2			Yes	Yes
Divide	Yes	Div	F10	FO	F6	Mult1		No	Yes
Register result status									
Clock	FO	F2	F4	<i>F6</i>	F8	F10	F12		F30
9 <i>FU</i>	Mult1				Add	Divide			

Dynamic Scheduling

Instruction status	Read	Executi Wr	ite	ADDD can't i	ssue b	ecause add
Instruction j k	Issue opera	nccomple Re	<u>sul</u> t	unit is busy.		
LD F6 34+ R2	1 2	3 4				
LD F2 45+ R3	5 6	7 8				
MULTIFO F2 F4	6 9					
SUBD F8 F6 F2	7 9	11				
DIVD F10 F0 F6	8					
ADDD F6 F8 F2						
Functional unit status	<u></u>	dest S1	<i>S2</i>	FU for J FU for	k Fj?	Fk?
Time Name	Busy Op	Fi Fj	Fk	Qj Qk	Ŕj	<i>Rk</i>
Integer	No					
8 Mult1	Yes Mult	F0 F2	F4		Yes	Yes
Mult2	No					
0 Add	Yes Sub	F8 F6	F2		Yes	Yes
Divide	Yes Div	F10 F0	F6	Mult1	No	Yes
Register result status	<u> </u>					
Clock	F0 F2	F4 F6	6 F8	F10 F12		F30
11 <i>FU</i>	Mult1		Add	Divide		

SHRD finishes

Dynamic Scheduling

Instruction j k Issue operant comple Result	Instruction status	Re	ead Executi	Write	SUBD linishes.	50
LD F2 45+ R3 5 6 7 8 MULTIFO F2 F4 6 9 SUBD F8 F6 F2 7 9 11 12 DIVD F10 F0 F6 8 ADDD F6 F8 F2 Functional unit status Time Name Busy Op Fi Fj Fk Qj Qk Rj Rk Integer 7 Mult1 Yes Mult F0 F2 F4 Yes Yes Mult2 Add No Divide Yes Div F10 F0 F6 Mult1 No Yes Register result status Clock F0 F2 F4 F6 F8 F10 F12 F30	Instruction j k	Issue op	perant comple	Result	DIVD waiting to	or FU.
MULTIFO F2 F4 6 9 SUBD F8 F6 F2 7 9 11 12 DIVD F10 F0 F6 8 ADDD F6 F8 F2 Functional unit status dest S1 S2 FU for j FU for k Fj? Fk? Find Name Busy Op Fi Fj Fk Qj Qk Rj Rk Integer No Yes Mult F0 F2 F4 Yes Yes Yes Mult2 No No No No No No Yes No No Yes No No Yes No Yes No No Yes F0 F2 F4 F6 F8 F10 F12 F30	LD F6 34+ R2	1	2 3	4		
SUBD F8 F6 F2 7 9 11 12 DIVD F10 F0 F6 8 ADDD F6 F8 F2 Functional unit status dest S1 S2 FU for J FU for k Fj? Fk? Time Name Busy Op Fi Fj Fk Qj Qk Rj Rk Integer No Yes Mult F0 F2 F4 Yes Yes Yes Mult2 No No No No No Yes Div F10 F0 F6 Mult1 No Yes Register result status F0 F2 F4 F6 F8 F10 F12 F30	LD F2 45+ R3	5	6 7	8		
DIVD F10 F0 F6 8 ADDD F6 F8 F2 Functional unit status Time Name Busy Op Fi Fj Fk Qj Qk Rj Rk Integer No 7 Mult1 Yes Mult F0 F2 F4 Yes Yes Mult2 Add Divide Yes Div F10 F0 F6 Mult1 No Yes Register result status Clock F0 F2 F4 F6 F8 F10 F12 F30	MULTIFO F2 F4	6	9			
ADDD F6 F8 F2 Functional unit status	SUBD F8 F6 F2	7	9 11	12		
Functional unit status Time Name Busy Op Fi Fj Fk Qj Qk Rj Rk Integer 7 Mult1 No Yes Mult2 Add No Divide Pes Div F10 F2 F4 F6 F8 F10	DIVD F10 F0 F6	8				
Time Name Busy Op Fi Fj Fk Qj Qk Rj Rk Integer No No Yes Mult Po F2 F4 Yes Yes Yes Mult Po No No No No No No Yes No Yes Register result status Clock F0 F2 F4 F6 F8 F10 F12 F30	ADDD F6 F8 F2					
Integer 7 Mult1 Yes Mult F0 F2 F4 Yes Yes No No Divide Per Div F10 F0 F6 Mult1 No Yes Register result status Clock F0 F2 F4 F6 F8 F10 F12 F30	Functional unit status		dest	S1 S2	FU for J FU for k	Fj? Fk?
7 Mult1	Time Name	Busy Op	o Fi	Fj Fk	Qj Qk	Rj Rk
Mult2 Add No Divide Ves Div F10 F0 F6 Mult1 No Yes Register result status Clock F0 F2 F4 F6 F8 F10 F12 F30	Integer	No				
Add Divide Yes Div F10 F0 F6 Mult1 No Yes Register result status Clock F0 F2 F4 F6 F8 F10 F12 F30	7 Mult1	Yes Mu	ılt FO I	F2 F4		Yes Yes
Divide Yes Div F10 F0 F6 Mult1 No Yes Register result status Clock F0 F2 F4 F6 F8 F10 F12 F30	Mult2	No				
Register result status Clock F0 F2 F4 F6 F8 F10 F12 F30	Add	No				
Clock F0 F2 F4 F6 F8 F10 F12 F30	Divide	Yes Div	v F10 l	F0 F6	Mult1	No Yes
	Register result status					
12 FU Mult1 Divide	Clock	FO FZ	2 F4	F6 F8	F10 F12	F30
	12 <i>FU</i>	Mult1			Divide	

Dynamic Scheduling

Instruction status		Read	Execut	i Write	e		ADD	D issue	es.
Instruction $j = k$	Issue	operan	c comple	Resu	ı/t				
LD F6 34+ R2	1	2	3	4					
LD F2 45+ R3	5	6	7	8					
MULTIFO F2 F4	6	9							
SUBD F8 F6 F2	7	9	11	12					
DIVD F10 F0 F6	8								
ADDD F6 F8 F2	13								
Functional unit status			dest	<i>S1</i>	<i>S2</i>	FU for	FU for I	k Fj?	Fk?
Time Name	Busy	Ор	Fi	Fj	Fk	Qj	Qk	Ŕj	Rk
Integer	No								
6 Mult1	Yes	Mult	FO	F2	F4			Yes	Yes
Mult2	No								
Add	Yes	Add	F6	F8	F2			Yes	Yes
Divide	Yes	Div	F10	FO	F6	Mult1		No	Yes
Register result status									
Clock	FO	F2	F4	<i>F6</i>	F8	F10	F12		F30
13 <i>FU</i>	Mult1			Add		Divide			

Dynamic Scheduling

Instruction status		Read	Executi	i Write	e				
Instruction <i>j k</i>	Issue	operari	ι comple	Resu	<u>/</u> t				
LD F6 34+ R2	1	2	3	4					
LD F2 45+ R3	5	6	7	8					
MULTIFO F2 F4	6	9							
SUBD F8 F6 F2	7	9	11	12					
DIVD F10 F0 F6	8								
ADDD F6 F8 F2	13	14							
Functional unit status			dest	<i>S1</i>	<i>S2</i>	FU for	FU for	k Fj?	Fk?
Time Name	Busy	Ор	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Integer	No								
5 Mult1	Yes	Mult	F0	F2	F4			Yes	Yes
Mult2	No								
2 Add	Yes	Add	F6	F8	F2			Yes	Yes
Divide	Yes	Div	F10	FO	F6	Mult1		No	Yes
Register result status	-								
Clock	FO	F2	F4	<i>F6</i>	F8	F10	F12		F30
14 <i>FU</i>	Mult1			Add		Divide			

Dynamic Scheduling

Instruction status		Read	Executi	i Write	9				
Instruction <i>j k</i>	Issue	operan	c comple	Resu	<u>/</u> t				
LD F6 34+ R2	1	2	3	4					
LD F2 45+ R3	5	6	7	8					
MULTIFO F2 F4	6	9							
SUBD F8 F6 F2	7	9	11	12					
DIVD F10 F0 F6	8								
ADDD F6 F8 F2	13	14							
Functional unit status			dest	<i>S1</i>	<i>S2</i>	FU for	FU for k	k Fj?	Fk?
Time Name	Busy	Ор	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Integer	No								
4 Mult1	Yes	Mult	F0	F2	F4			Yes	Yes
Mult2	No								
1 Add	Yes	Add	F6	F8	F2			Yes	Yes
Divide	Yes	Div	F10	F0	F6	Mult1		No	Yes
Register result status	,								
Clock	F0	<i>F2</i>	F4	<i>F6</i>	F8	F10	F12		<i>F30</i>
15 <i>FU</i>	Mult1			Add		Divide			

Dynamic Scheduling

Instruction status		Read	Executi	Write	è				
Instruction <i>j k</i>	Issue	operan	c comple	Resu	/t				
LD F6 34+ R2	1	2	3	4					
LD F2 45+ R3	5	6	7	8					
MULTIFO F2 F4	6	9							
SUBD F8 F6 F2	7	9	11	12					
DIVD F10 F0 F6	8								
ADDDF6 F8 F2	13	14	16						
Functional unit status	-		dest	<i>S1</i>	<i>S2</i>	FU for J	FU for k	Fj?	Fk?
Time Name	Busy	Ор	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Integer	No								
3 Mult1	Yes	Mult	F0	F2	F4			Yes	Yes
Mult2	No								
0 Add	Yes	Add	F6	F8	F2			Yes	Yes
Divide	Yes	Div	F10	F0	F6	Mult1		No	Yes
Register result status									
Clock	F0	F2	F4	<i>F6</i>	<i>F8</i>	F10	F12		<i>F30</i>
16 <i>FU</i>	Mult1			Add		Divide			

Dynamic Scheduling

Instruction status Instruction <i>j k</i>	lecuo	Read	Execut			ADDD DIVD.	_		ecause of
,	<i>Issue</i>		<u>ı compl</u>		<i>71</i>]				
LD F6 34+ R2	1	2	3	4					
LD F2 45+ R3	5	6	7	8					
MULTIFO F2 F4	6	9							
SUBD F8 F6 F2	7	9	11	12					
DIVD F10 F0 F6	8								
ADDD F6 F8 F2	13	14	16						
Functional unit status			dest	<i>S1</i>	<i>S2</i>	FU for J	FU for k	k Fj?	Fk?
Time Name	Busy	Ор	Fi	Fj	Fk	Qj	Qk	Ŕj	Rk
Integer	No								
2 Mult1	Yes	Mult	FO	F2	F4			Yes	Yes
Mult2	No								
Add	Yes	Add	F6	F8	F2			Yes	Yes
Divide	Yes	Div	F10	FO	F6	Mult1		No	Yes
Register result status	-								
Clock	FO	F2	F4	F6	F8	F10	F12		F30
17 <i>FU</i>	Mult1			Add		Divide			

Dynamic Scheduling

Instruction status	Read	Execut	ti Writ	e	N	lothing	Нарр	ens!!
Instruction <i>j k</i>	Issue opera	nι compl	e Resu	<u>ı/t</u>				
LD F6 34+ R2	1 2	3	4					
LD F2 45+ R3	5 6	7	8					
MULTIFO F2 F4	6 9							
SUBD F8 F6 F2	7 9	11	12					
DIVD F10 F0 F6	8							
ADDD F6 F8 F2	13 14	16						
Functional unit status	<u>. </u>	dest	<i>S1</i>	<i>S2</i>	FU for J	FU for k	Fj?	Fk?
Time Name	Busy Op	Fi	Fj	Fk	Qj	Qk	Řj	Rk
Integer	No		_					
1 Mult1	Yes Mult	FO	F2	F4			Yes	Yes
Mult2	No							
Add	Yes Add	F6	F8	F2			Yes	Yes
Divide	Yes Div	F10	FO	F6	Mult1		No	Yes
Register result status								
Clock	F0 F2	F4	<i>F6</i>	F8	F10	F12		F30
18 <i>FU</i>	Mult1		Add		Divide			

Dynamic Scheduling

Instruction status		Read	Execut	ti Writ	e	MULT co	omplete	s exec	ution.
Instruction j k	Issue	operan	ic comple	e Resu	<u>ı</u> /t				
LD F6 34+ R2	1	2	3	4					
LD F2 45+ R3	5	6	7	8					
MULTIFO F2 F4	6	9	19						
SUBD F8 F6 F2	7	9	11	12					
DIVD F10 F0 F6	8								
ADDD F6 F8 F2	13	14	16						
Functional unit status			dest	<i>S1</i>	<i>S2</i>	FU for	FU for F	k Fj?	Fk?
Time Name	Busy	Ор	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Integer	No								
O Mult1	Yes	Mult	FO	F2	F4			Yes	Yes
Mult2	No								
Add	Yes	Add	F6	F8	F2			Yes	Yes
Divide	Yes	Div	F10	FO	F6	Mult1		No	Yes
Register result status									
Clock	F0	F2	F4	<i>F6</i>	F8	F10	F12		F30
19 <i>FU</i>	Mult1			Add		Divide			

Dynamic Scheduling

Instruction status	Rea	d Execu	iti Write	ė		MUL	T writ	es.
Instruction j k	Issue ope	ranc comp	le Resu	<u>/</u> t				
LD F6 34+ R2	1 2	3	4					
LD F2 45+ R3	5 6	7	8					
MULTIFO F2 F4	6 9	19	20					
SUBD F8 F6 F2	7 9	11	12					
DIVD F10 F0 F6	8							
ADDDF6 F8 F2	13 1	4 16						
Functional unit status		dest	<i>S1</i>	<i>S2</i>	FU for	FU for	k Fj?	Fk?
Time Name	Busy Op	Fi	Fj	Fk	Qj	Qk	Ŕj	Rk
Integer	No							
Mult1	No							
Mult2	No							
Add	Yes Add	F6	F8	F2			Yes	Yes
Divide	Yes Div	F10	FO	F6			Yes	Yes
Register result status								
Clock	F0 F2	F4	<i>F6</i>	F8	F10	F12		F30
20 <i>FU</i>			Add		Divide			

Dynamic Scheduling

Instruction status	. Reac		iti Write	_	D	IVD loa	ds ope	erands
Instruction <i>j k</i>	Issue oper	ant comp	le Resu	<u>//</u> t				
LD F6 34+ R2	1 2	3	4					
LD F2 45+ R3	5 6	7	8					
MULTIFO F2 F4	6 9	19	20					
SUBD F8 F6 F2	7 9	11	12					
DIVD F10 F0 F6	8 21							
ADDDF6 F8 F2	13 14	16						
Functional unit status		dest	<i>S1</i>	<i>S2</i>	FU for	JFU for	k Fj?	Fk?
Time Name	Busy Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Integer	No							
Mult1	No							
Mult2	No							
Add	Yes Add	F6	F8	F2			Yes	Yes
Divide	Yes Div	F10	FO	F6			Yes	Yes
Register result status								
Clock	F0 F2	F4	<i>F6</i>	F8	F10	F12		F30
21 <i>FU</i>			Add		Divide			

Dynamic Scheduling

Instruction status Instruction j k	Issue	Read operan	Executi ι comple		-		DDD car emoved		e since
LD F6 34+ R2	1	2	3	4]				
LD F2 45+ R3	5	6	7	8					
MULTIFO F2 F4	6	9	19	20					
SUBD F8 F6 F2	7	9	11	12					
DIVD F10 F0 F6	8	21							
ADDD F6 F8 F2	13	14	16	22					
Functional unit status			dest	<i>S1</i>	<i>S2</i>	FU for J	FU for k	Fj?	Fk?
Time Name	Busy	Ор	Fi	Fj	Fk	Qj	Qk	Ŕj	Rk
Integer	No								
Mult 1	No								
Mult2	No								
Add	No								
40 Divide	Yes	Div	F10	FO	F6			Yes	Yes
Register result status									
Clock	FO	F2	F4	<i>F6</i>	F8	F10	F12		F30
22 <i>FU</i>						Divide			

Dynamic Scheduling

Instruction status	Re	ad Execu	ıti Write		DIVD o	complet	es exe	cution
Instruction <i>j k</i>	Issue op	eranı comp	<u>le Resu</u> lt					
LD F6 34+ R2	1	2 3	4					
LD F2 45+ R3	5	6 7	8					
MULTIFO F2 F4	6	9 19	20					
SUBD F8 F6 F2	7	9 11	12					
DIVD F10 F0 F6	8	21 61						
ADDDF6 F8 F2	13	14 16	22					
Functional unit status		dest	<u>S1</u> S	<i>S2</i>	FU for	FU for F	k Fj?	Fk?
Time Name	Busy Op) Fi	Fj F	Fk	Qj	Qk	Řj	Rk
Integer	No		-			-		
Mult1	No							
Mult2	No							
Add	No							
0 Divide	Yes Div	/ F10	FO F	6			Yes	Yes
Register result status								
Clock	FO F	2 F4	F6 I	F8	F10	F12		F30
61 <i>FU</i>					Divide			

Dynamic Scheduling

Instruction status		Read	Execut	ti Write	e		DO	ONE!!	
Instruction <i>j k</i>	Issue	operari	ic comple	e Resu	<u>/</u> /t				
LD F6 34+ R2	1	2	3	4					
LD F2 45+ R3	5	6	7	8					
MULTIFO F2 F4	6	9	19	20					
SUBD F8 F6 F2	7	9	11	12					
DIVD F10 F0 F6	8	21	61	62					
ADDDF6 F8 F2	13	14	16	22					
Functional unit status			dest	<i>S1</i>	<i>S2</i>	FU for	JFU for	k Fj?	Fk?
Time Name	Busy	Ор	Fi	Fj	Fk	Qj	Qk	Ŕj	Rk
Integer	No								
Mult1	No								
Mult2	No								
Add	No								
0 Divide	No								
Register result status									
Clock	F0	F2	F4	F6	F8	F10	F12		F30
62 <i>FU</i>		_	<u> </u>			<u> </u>	- · -		

Tomasulo's Algorthm in Action

7 Components of Reservation Station

Op: Operation to perform in the unit (e.g., + or –)

Qj, Qk: Reservation stations producing the corresponding source operand

- Note: Qj,Qk=0 => ready or unnessary
- Store buffers only have Qi for RS producing result

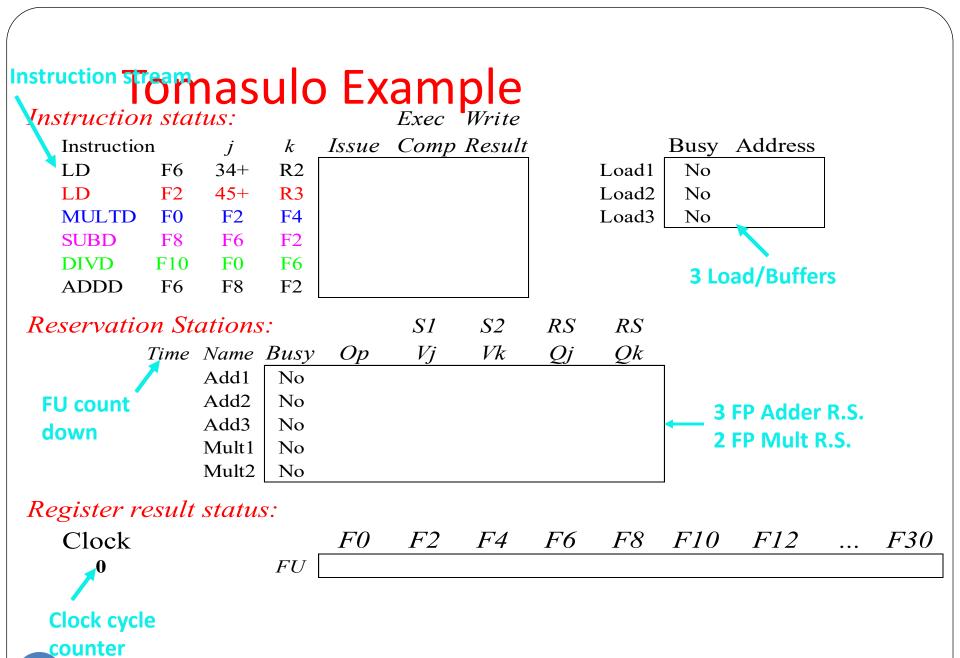
Vj, Vk: Value of Source operands

- Only one of V field or the Q field is valid
- Store buffers has V field, result to be stored

A: used to hold information for the memory address calculation for a load or a store

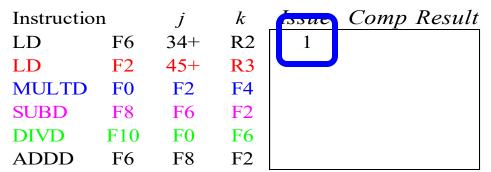
Busy: Indicates reservation station or FU is busy

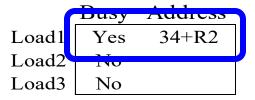
Register result status Qi—Indicates which functional unit will write each register, if one exists. Blank when no pending instructions that will write that register.



cution clock cycles: 2 cycle LOAD, 2 cycle for FP +,-; 10 for *; 40 clks for /







Reservation Stations:

Time		Busy	Op	Vj	Vk	Qj	Qk
	Add1 Add2 Add3 Mult1	No					
	Add2	No					
	Add3	No					
	Mult1	No					
	Mult2	No					

SI

Register result status:

Clock F0F2F4F8F10F12 F30 FULoad1

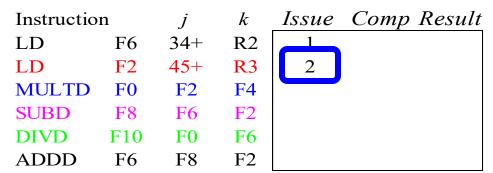
S2

RS

RS

Instruction status:





	Busy	Address
Load1	Yes	34+R2
Load2	Yes	45+R3
Load3	No	

Reservation Stations:

Time		Busy	Op	Vj	Vk	Qj	Qk
	Add1 Add2 Add3 Mult1	No					
	Add2	No					
	Add3	No					
	Mult1	No					
	Mult2	No					

SI

S2

Register result status:

Clock

FU

Load2

F4 *F*6 F8 Load₁

RS

RS

F10 F12 F30

Note: Can have multiple loads outstanding

Instruction status:

Instructio	n	\dot{J}	k	Issue	Comp	Result
LD	F6	34+	R2	1	3	
LD	F2	45+	R3	2		
MULTD	$\mathbf{F0}$	F2	F4	3		
SUBD	F8	F6	F2			
DIVD	F10	F0	F6			
ADDD	F6	F8	F2			

Busy Address Load1 Yes 34 + R2Load2 Yes 45+R3 Load3 No

Reservation Stations:

 V_i VkOkTime Name Busy Op*Oi* Add1 No Add2 No Add3 Mult 1 Yes MULTD R(F4) Load2 Mult2

SI

S2

RS

RS

Register result status:

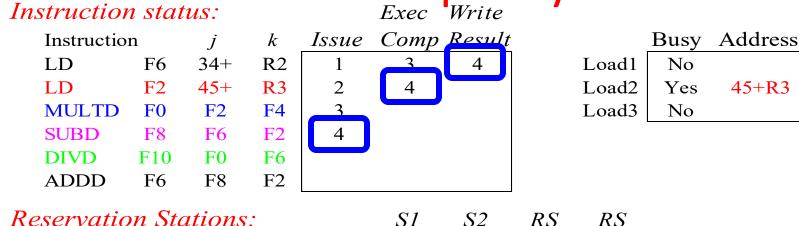
Clock

35

F2F4F6 F8 *F10* F12 F30 Load2 Load₁

Note: registers names are removed ("renamed") in Reservation Stations: MULT issued

Load1 completing; what is waiting for Load1?



Time Name	Rusv	On	V_i	Vk	Oi	Ok
Add1	Yes	SUBD	M(A1)			Load2
Add2	No					
Add3	No					
Mult1	Yes	MULTE)	R(F4)	Load2	
Mult2	No					

Register result status:

Clock F0F2F4*F6* F8 F10 F12 F30 FUMult1 Load2 M(A1)Add1

Load2 completing; what is waiting for Load2?

Tomasulo Example Cycle 5 Exec Write

Instruction status:

Instruction		\dot{J}	\boldsymbol{k}	Issue	Comp	Result
LD	F6	34+	R2	1	3	4
LD	F2	45+	R3	2	4	5
MULTD	FO	F2	F4	3		
SUBD	F8	F6	F2	4		
DIVD	F10	F0	F6	5		
ADDD	F6	F8	F2			

Address Busy Load1 No Load2 No Load3 No

Reservation Stations:

Time Name Busy OpOk**SUBD** Add1 Add2 No Add3 No Mult 1 Yes MULTE M(A2) R(F4) M(A1) Mult1 Mult2 Yes **DIVD**

SI

Register result status:

Clock F0*F2* F4*F6* F8 *F10* F12 F30 Mult1 M(A2)M(A1)Add1 Mult2

S2

RS

RS

Timer starts down for Add1, Mult1

Instruction status:

Instructio	n	j	\boldsymbol{k}	Issue	Comp	Result
LD	F6	34+	R2	1	3	4
LD	F2	45+	R3	2	4	5
MULTD	$\mathbf{F0}$	F2	F4	3		
SUBD	F8	F6	F2	4		
DIVD	F10	F0	F6	5		
ADDD	F6	F8	F2	6		

Yes

DIVD

Busy Address No Load1 Load2 No Load3 No

F10

Mult2

F12

F30

Reservation Stations:

SI S2RSRSVkTime Name Busy Op Ok

1 Add1 Yes SUBD M(A1) M(A2) Add2 Yes ADDD M(A2) Add1 Add3 No 9 Mult1 Yes MULTD M(A2) R(F4)

Mult2

Register result status:

Clock 6

F0*F2* F4*F6* F8 FUMult1 M(A2)Add2 Add1

M(A1) Mult1

Issue ADDD here despite name dependency on F6?

Instruction status:

Instruction	n	\dot{J}	k	Issue	Comp	Result
LD	F6	34+	R2	1	3	4
LD	F2	45+	R3	2	4	5
MULTD	F0	F2	F4	3		
SUBD	F8	F6	F2	4	7	
DIVD	F10	F0	F6	5		
ADDD	F6	F8	F2	6		

	Busy	Address
Load1	No	
Load2	No	
Load3	No	

Reservation Stations:

VkOkTime Name Busy Op *Oj* 0 Add 1Yes SUBD M(A1) M(A2)Add2 Yes ADDD M(A2) Add1 Add3 No 8 Mult1 Yes MULTD M(A2) R(F4)Mult2 Yes DIVD M(A1) Mult1

SI

Register result status:

F0*F2* F4*F6* F8 *F10* F12 F30 Clock Mult1 M(A2)Add2 Add1 Mult2

S2

RS

RS

Add1 (SUBD) completing; what is waiting for it?

Tomasulo Example Cycle 8 tion status: Exec Write

Instruction status:

Instructio	n	\dot{J}	k	Issue	Comp	Result
LD	F6	34+	R2	1	3	4
LD	F2	45+	R3	2	4	5
MULTD	$\mathbf{F0}$	F2	F4	3		
SUBD	F8	F6	F2	4	7	8
DIVD	F10	F0	F6	5		
ADDD	F6	F8	F2	6		

	Busy	Address
Load1	No	
Load2	No	
Load3	No	

Reservation Stations:

```
Time Name Busy
                              Vk
                                    Oj
                                          Ok
                 Op
     Add1
           No
           Yes ADDD (M-M
   2 Add2
     Add3
           No
           Yes MULTD M(A2) R(F4)
   7 Mult1
     Mult2 | Yes
                DIVD
                            M(A1) Mult1
```

SI

Register result status:

Clock F0F2F4*F6* F8 F10 F12 F30 FUMult1 M(A2)Add2 Mult2

S2

RS

Instruction status:

Instructio	n	j	k	Issue	Comp	Result
LD	F6	34+	R2	1	3	4
LD	F2	45+	R3	2	4	5
MULTD	F0	F2	F4	3		
SUBD	F8	F6	F2	4	7	8
DIVD	F10	F0	F6	5		
ADDD	F6	F8	F2	6		

	Busy	Address
Load1	No	
Load2	No	
Load3	No	

Reservation Stations:

```
S2
                                     RS
                                           RS
Time Name Busy
                         V_{j}
                               Vk
                                     Oj
                                           Ok
                Op
     Add1
            No
   1 Add2
           Yes ADDD (M-M) M(A2)
     Add3
            No
           Yes MULTD M(A2) R(F4)
   6 Mult1
     Mult2 | Yes
                DIVD
                             M(A1) Mult1
```

SI

Register result status:

Clock F0F2F4*F6* F8 F10*F12* F30 9 FUMult1 M(A2)Add2 (M-M) Mult2

Instruction status:

Instructio	n	\dot{J}	k	Issue	Comp	Result
LD	F6	34+	R2	1	3	4
LD	F2	45+	R3	2	4	5
MULTD	F0	F2	F4	3		
SUBD	F8	F6	F2	4	7	8
DIVD	F10	F0	F6	5		
ADDD	F6	F8	F2	6	10	

	Busy	Address
Load1	No	
Load2	No	
Load3	No	

Reservation Stations:

```
Vk
                                          Ok
Time Name Busy
                 Op
                                    Oi
    Add1
           No
   0 Add2
           Yes ADDD (M-M) M(A2)
    Add3
           No
   5 Mult1
           Yes MULTD M(A2) R(F4)
    Mult2
          Yes
                DIVD
                            M(A1) Mult1
```

SI

Register result status:

F0*F2* F4*F6* F8 F10 F12 F30 Clock 10 Mult1 M(A2)Add2 (M-M)Mult2

S2

RS

RS

Add2 (ADDD) completing; what is waiting for it?

	nstri	ıcti	on	stat	us:
-					

Instructio	n	\dot{J}	k	Issue	Comp	Result
LD	F6	34+	R2	1	3	4
LD	F2	45+	R3	2	4	5
MULTD	F0	F2	F4	3		
SUBD	F8	F6	F2	4	7	8
DIVD	F10	F0	F6	5		
ADDD	F6	F8	F2	6	10	11

	Busy	Address
Load1	No	
Load2	No	
Load3	No	

Reservation Stations:

SI

Register result status:

F0F2F8 *F10* F12 F30 Clock F4 F6 11 Mult1 M(A2)Mult2

S2

RS

- Write result of ADDD here?
- All quick instructions complete in this cycle!

Instruction status:

Instructio	n	\dot{J}	k	Issue	Comp	Result
LD	F6	34+	R2	1	3	4
LD	F2	45+	R3	2	4	5
MULTD	F0	F2	F4	3		
SUBD	F8	F6	F2	4	7	8
DIVD	F10	F0	F6	5		
ADDD	F6	F8	F2	6	10	11

	Busy	Address
Load1	No	
Load2	No	
Load3	No	

Reservation Stations:

```
Time Name Busy
                         V_{j}
                                Vk
                                            Ok
                  Op
                                      Oj
     Add1
            No
     Add2
            No
     Add3
            No
            Yes MULTD M(A2) R(F4)
   3 Mult1
     Mult2 | Yes
                 DIVD
                              M(A1) Mult1
```

SI

Register result status:

Clock F0F2F4*F6* F8F10*F12* F30 12 FUMult1 M(A2)(M-M+N(M-M) Mult2

S2

RS

Instruction status:

Instructio	n	\dot{J}	k	Issue	Comp	Result
LD	F6	34+	R2	1	3	4
LD	F2	45+	R3	2	4	5
MULTD	$\mathbf{F0}$	F2	F4	3		
SUBD	F8	F6	F2	4	7	8
DIVD	F10	F0	F6	5		
ADDD	F6	F8	F2	6	10	11

Busy Address No Load1 Load2 No Load3 No

Reservation Stations:

```
Time Name Busy
                         V_{j}
                               Vk
                                            Ok
                  Op
                                      Qi
     Add1
            No
     Add2
            No
     Add3
            No
   2 Mult1
           Yes MULTD M(A2) R(F4)
     Mult2
           Yes
                 DIVD
                             M(A1) Mult1
```

SI

Register result status:

Clock F0F2F4*F6* F8 F10F12 F30 13 FUMult1 M(A2)(M-M+N(M-M) Mult2

S2

RS

Instruction status:

Instructio	n	\dot{J}	k	Issue	Comp	Result
LD	F6	34+	R2	1	3	4
LD	F2	45+	R3	2	4	5
MULTD	$\mathbf{F0}$	F2	F4	3		
SUBD	F8	F6	F2	4	7	8
DIVD	F10	F0	F6	5		
ADDD	F6	F8	F2	6	10	11

	Busy	Address
Load1	No	
Load2	No	
Load3	No	

Reservation Stations:

```
Time Name Busy
                         V_{j}
                                Vk
                                            Ok
                  Op
                                      Oj
     Add1
            No
     Add2
            No
     Add3
            No
   1 Mult1
            Yes MULTD M(A2) R(F4)
     Mult2 | Yes
                 DIVD
                              M(A1) Mult1
```

SI

Register result status:

Clock F0F2F4*F6* F8F10*F12* F30 14 FUMult1 M(A2)(M-M+M(M-M) Mult2

S2

RS

Instruction status:

Instructio	n	\dot{J}	k	Issue	Comp	Result
LD	F6	34+	R2	1	3	4
LD	F2	45+	R3	2	4	5
MULTD	F0	F2	F4	3	15	
SUBD	F8	F6	F2	4	7	8
DIVD	F10	F0	F6	5		
ADDD	F6	F8	F2	6	10	11

Address Busy No Load1 Load2 No Load3 No

Reservation Stations:

Time Name Busy V_{j} VkOkOp*Qi* Add1 No Add2 No Add3 No 0 Mult1 Yes MULTD M(A2) R(F4)Mult2 Yes DIVD M(A1) Mult1

SI

Register result status:

Clock 15

F0*F2* F4

S2

F6

RS

F10

F12

F30

Mult1 M(A2)

(M-M+N.(M-M))Mult2

F8

RS

Mult1 (MULTD) completing; what is waiting for it?

Instruction status:

Instructio	n	\dot{J}	k	Issue	Comp	Result
LD	F6	34+	R2	1	3	4
LD	F2	45+	R3	2	4	5
MULTD	$\mathbf{F0}$	F2	F4	3	15	16
SUBD	F8	F6	F2	4	7	8
DIVD	F10	F0	F6	5		
ADDD	F6	F8	F2	6	10	11

Address Busy No Load1 Load2 No Load3 No

Reservation Stations:

Time Name Busy V_{j} VkOkOp*Qi* Add1 No Add2 No Add3 No Mult1 No 40 Mult2 | Yes **DIVD** M(A1)

SI

Register result status:

F2F4*F6* F8 *F10* F12 F30 Clock 16 M(A2)(M-M+N.(M-M))Mult2

S2

RS

RS

Just waiting for Mult2 (DIVD) to complete

Instruction status:

Instructio	n	\dot{J}	k	Issue	Comp	Result
LD	F6	34+	R2	1	3	4
LD	F2	45+	R3	2	4	5
MULTD	F0	F2	F4	3	15	16
SUBD	F8	F6	F2	4	7	8
DIVD	F10	F0	F6	5		
ADDD	F6	F8	F2	6	10	11

Busy Address Load1 No Load2 No Load3 No

Reservation Stations:

```
Time Name Busy
                         V_{j}
                                Vk
                                      Oj
                                             Ok
                  Op
     Add1
            No
     Add2
            No
     Add3
            No
     Mult1
            No
                 DIVD M*F4 M(A1)
   1 Mult2 | Yes
```

SI

Register result status:

Clock 55

FU

F0F2 F4

S2

F6

RS

F8

RS

F10

F12

F30

M*F4 M(A2)

(M-M+M(M-M))Mult2

Instruction status:

Instructio	n	\dot{J}	k	Issue	Comp	Result
LD	F6	34+	R2	1	3	4
LD	F2	45+	R3	2	4	5
MULTD	FO	F2	F4	3	15	16
SUBD	F8	F6	F2	4	7	8
DIVD	F10	F0	F6	5	56	
ADDD	F6	F8	F2	6	10	11

Address Busy No Load1 Load2 No Load3 No

Reservation Stations:

Time Name Busy V_{j} VkOkOp*Qi* Add1 No Add2 No Add3 No Mult1 No 0 Mult2 | Yes M*F4 M(A1) DIVD

SI

Register result status:

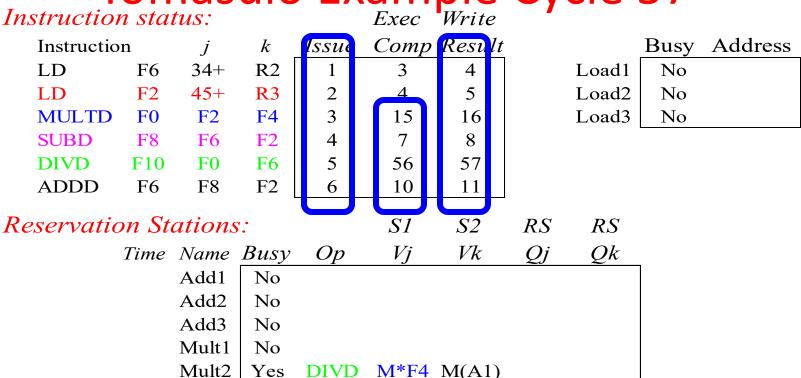
F0*F2* F4*F6* F8 F10 F12 F30 Clock 56 M*F4 M(A2)(M-M+N.(M-M))Mult2

S2

RS

RS

Mult2 (DIVD) is completing; what is waiting for it?



Register result status:

Clock F0 F2 F4 F6 F8 F10 F12 ... F30 FU M*F4 M(A2) (M-M+N(M-M) Result

Once again: In-order issue, out-of-order execution and out-of-order completion.

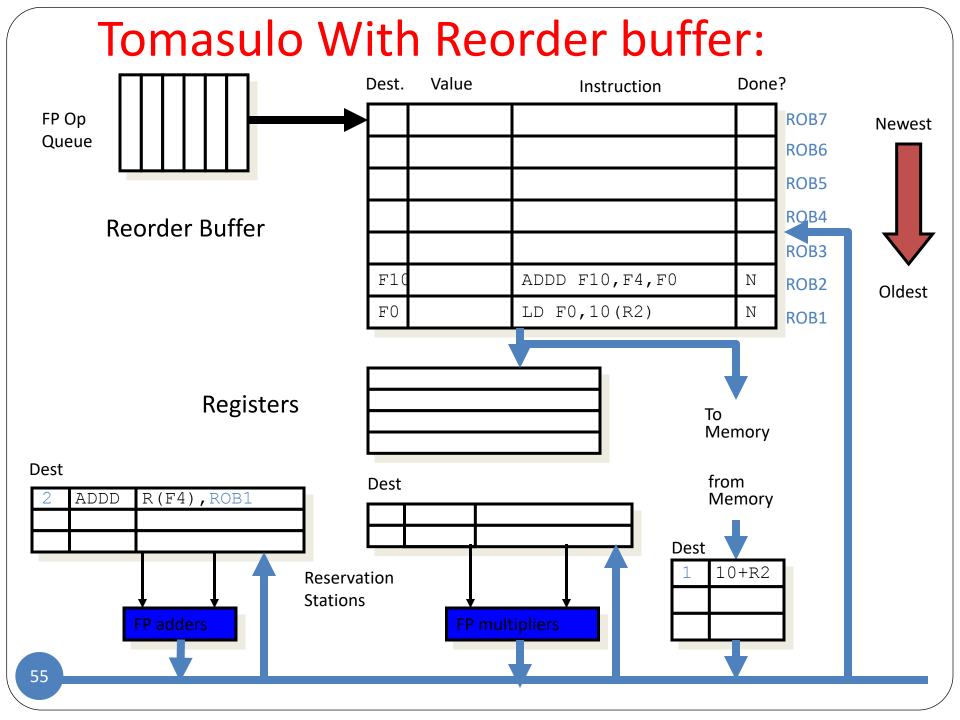
Tomasulo + Speculation in Action

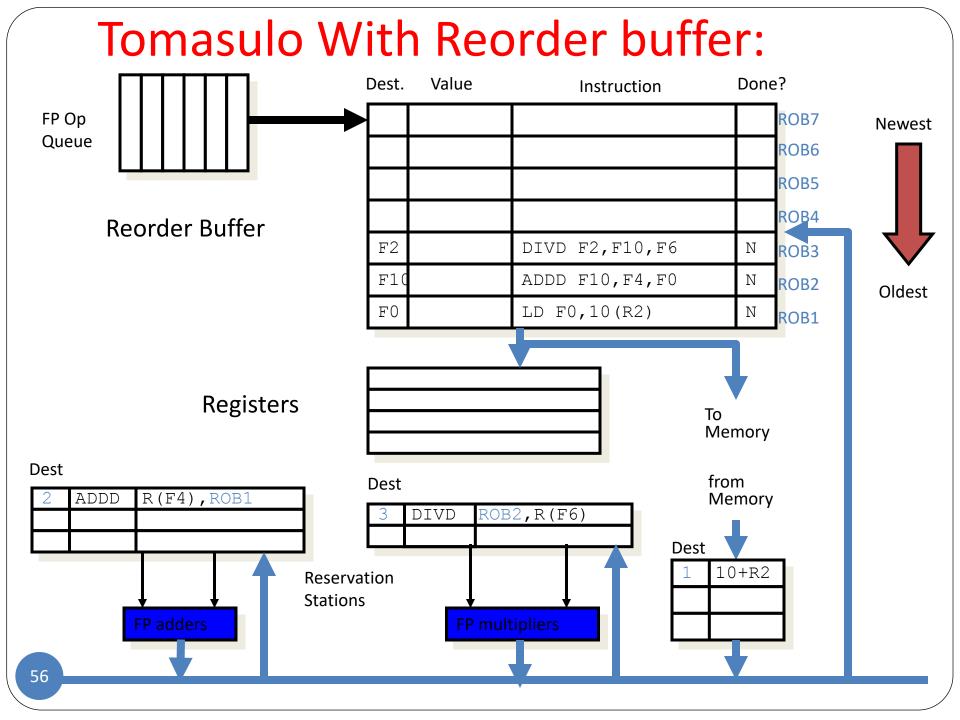
Speculative Tomasulo Example

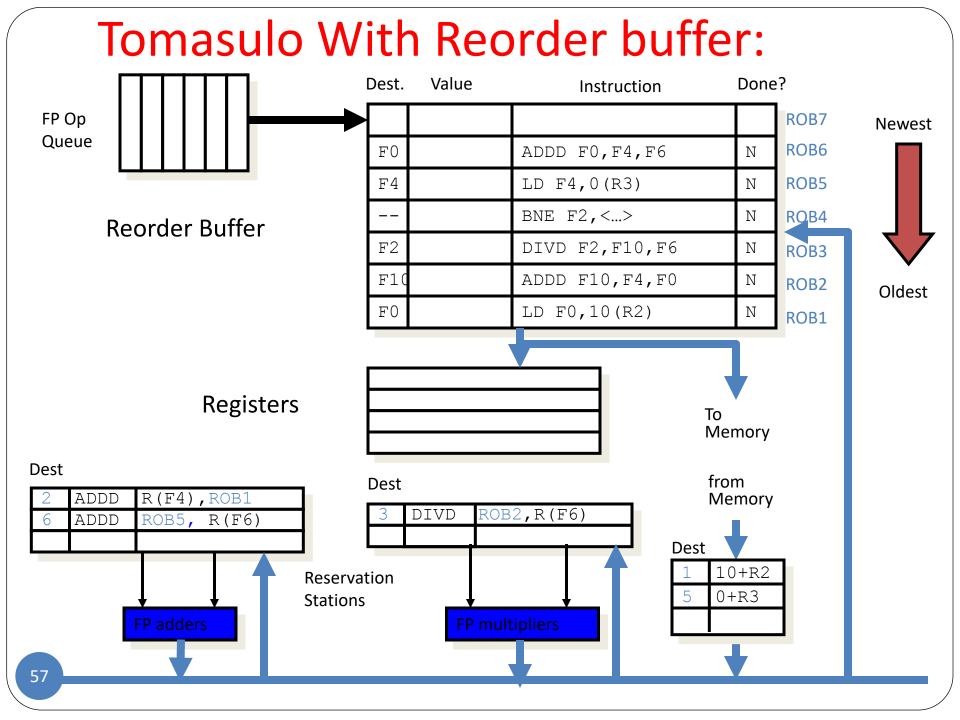
```
10
                   R2
LD
         FO
              F4 F0
         F10
ADDD
         F2 F10 F6
DIVD
         F2
              Exit
BNEZ
         F4
                   R3
LD
              0
                   F9
              F4
         FO
ADDD
                   R3
              0
SD
         F4
```

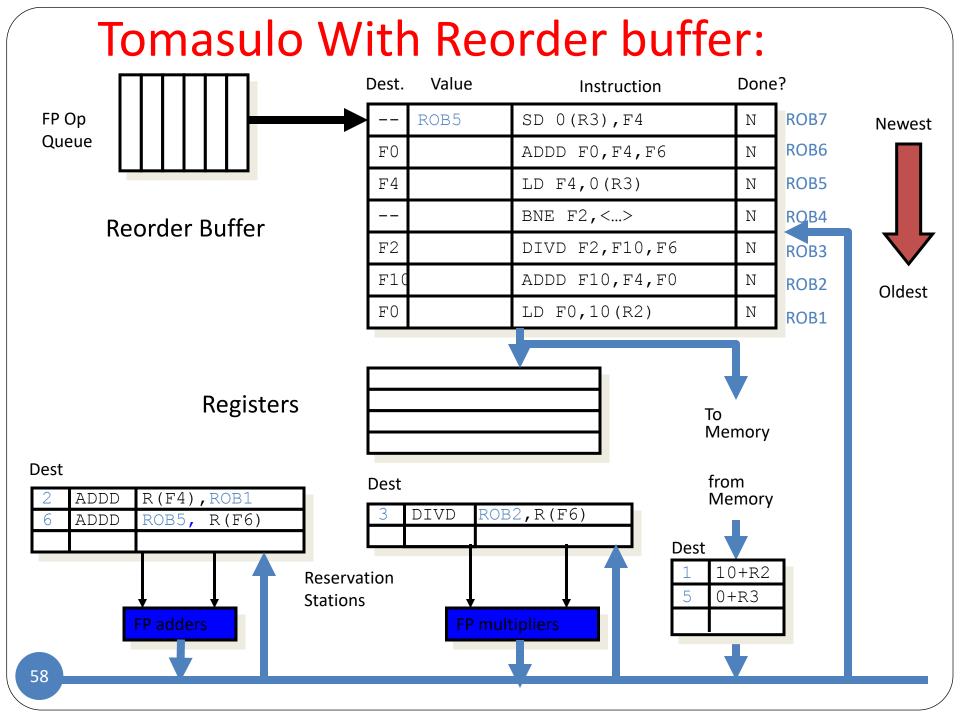
Exit:

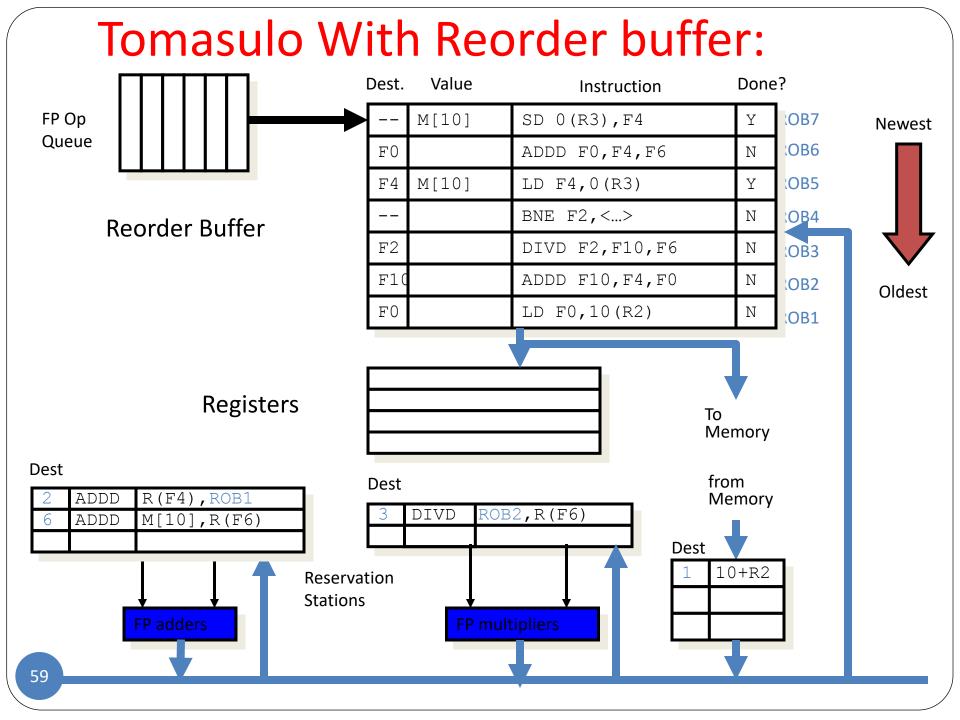
Tomasulo With Reorder buffer: Dest. Value Instruction Done? FP Op ROB7 Newest Queue ROB6 ROB5 RQB4 Reorder Buffer ROB3 ROB2 Oldest FΟ LD F0,10(R2) Ν ROB1 Registers То Memory Dest from Dest Memory Dest 10+R2 Reservation **Stations** 54

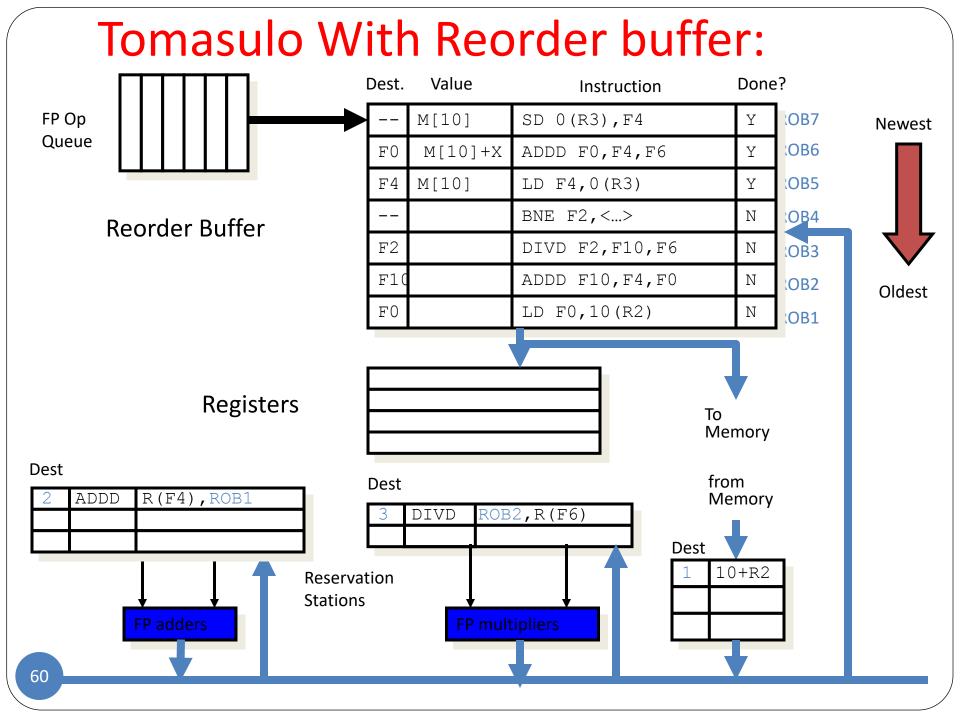












Notes

- If a branch is mispredicted, recovery is done by flushing the ROB of all entries that appear after the mispredicted branch
 - entries before the branch are allowed to continue
 - restart the fetch at the correct branch successor
- When an instruction commits or is flushed from the ROB then the corresponding slots become available for subsequent instructions