CS4223 – Test 1 Review

Below are a number of questions from previous exams and tests. These are examples of the types of questions that you could receive on the upcoming Test 1. Not that any material from the ILP and cache sections can be on this test, and that the questions listed here are non-exhaustive.

QUESTION: Instruction-Level Parallelism [19 marks]

Consider the following code fragment:

```
I1: LD     F0, 32(R0)
I2: LD     F2, 40(R0)
I3: DIVD   F4, F0, F2
I4: MULTD  F4, F4, F0
I5: ADDD   F0, F0, F2
```

(A) Clearly write down all true data dependence, output dependence, and anti-dependence in the code fragment. [3 marks]

(B) Assume a hypothetical 5-stage simple processor pipeline (fetch, decode, execute, memory, write-back) **without bypassing** discussed in class where each instruction (LD, DIVD, ADDD, and MULTD) spends only 1 clock cycle in the execute stage. How many cycles will it take to execute the code fragment? Assume there is no structural hazard. Explain your answer. [2 marks]

(C) Assume a hypothetical 5-stage simple processor pipeline (fetch, decode, execute, memory, write-back) **with bypassing** discussed in class where each instruction (LD, DIVD, ADDD, and MULTD) spends only 1 clock cycle in the execute stage. How many cycles will it take to execute the code fragment. Assume there is no structural hazard. Explain your answer. [2 marks]

(D) Consider **dynamic scheduling** for the code fragment in Q1(A). Assume that load executes for 1 cycle, DIVD executes for 20 cycles, MULTD executes for 10 cycles, and ADDD executes for 4 cycles. Further assume the presence of 1 load unit, 1 adder unit, 1 multiplier unit, and 1 divider unit. *These assumptions about instruction latency and number of execution units will be valid for Q1(E) as well.*

Consider now **dynamic scheduling with scoreboard** for the code fragment. Present the cycles in which the instructions will be issued, start execution, and write results into registers with detailed explanation of the stalls due to hazards. State your assumptions clearly. [5 marks]

(E) Consider now dynamic scheduling with **Tomasulo's algorithm but no speculation** for the code fragment in Q1(A). The instruction latency and number of execution units remain the same as Q1(D). Assume the presence of sufficient reservation station entries. Present the cycles in which the instructions will be issued, start execution, and write results into registers with detailed explanation of how the hazards are handled. State your assumptions clearly. [5 marks]

(F) Why do architects put more attention on the accuracy of branch predictors in a superscalar out-of-order processor than in a 5-stage in-order processor pipeline? [2 marks]

QUESTION 3: PIPELINE [8 marks]

Consider the following code fragment

```
DIV.D   F0, F2, F4
ADD.D   F6, F0, F2
SUB.D   F0, F2, F4
ADD.D   F2, F0, F4
```

The registers F* correspond to floating point registers. Assume that floating point add/sub executes for 2 cycles, floating point multiply/divide executes for 20 cycles. Further assume the presence of 3 floating-point add units and 1 floating-point multiply unit.

(A) Show all the data dependences in the code fragment including true data dependence, anti-dependence, and output dependence. [2 marks]

(B) Explain the hazards that will be experienced by this code fragment on an out-of-order processor employing Scoreboard and which of these hazards will be overcome by scoreboarding. [3 marks]

(C) Assuming the presence of enough reservation stations, explain how an out-of-order processor employing Tomasulo's algorithm will overcome the hazards in the code fragment. [3 marks]

QUESTION 2: Performance Analysis [11 marks]

Assume that the "go" program is executing on a multi-cycle datapath as discussed in class. The instruction mix and CPI for each instruction type is given in the table.

Instruction Class	CPI	% of dynamic instructions
ALU	4	40%
Branch	3	20%
Load	5	20%
Store	4	20%

(A) What is the CPI of the whole "go" program? [2 marks]

(B) If the total execution time for the "go" program is found to be 2 seconds and the program executes 2 million dynamic instructions altogether, what is the clock cycle time of the processor on which it was run? [2 marks]

(C) Assume that 25% of the load instructions in the "go" program are immediately followed by an ALU instruction that uses the data that was just loaded. To improve the performance, the processor designer is contemplating to add a new ALU instruction (MALU) where one of the source operands is a value from memory. MALU replaces the previous 2-instruction sequence (load followed by ALU) and takes 7 clock cycles to execute. What would be the CPI of the whole "go" program for this new design. Is there any benefit?
[3 marks]

QUESTION 1 PERFORMANCE [7 marks]

(A) For an application, Processor A has IPC = 2.1 while processor B has IPC = 1.5. Both the processors are running at the same frequency. Is Processor A faster than Processor B for the application? Explain your reasoning. [1 mark]

(C) A designer wants to improve the overall performance of a given processor and is considering an enhancement X that applies to 50% of the original dynamically-executed instructions, and speeds each of them up by a factor of 3. The designer's manager has some concerns about the complexity and the cost-effectiveness of X and suggests that the designer should consider an alternative enhancement Y. Enhancement Y, if applied only to some (as yet unknown) fraction of the original dynamically-executed instructions, would make them 75% faster. Determine what percentage of all dynamically-executed instructions should be optimized using enhancement Y in order to achieve the same overall speedup as obtained using enhancement X. [2 marks]

(D) A processor can run at 500 MHz and 1 GHz. An application developer measures the execution time of an application with the same data input running at 500 MHz and 1GHz. The developer observes that (unlike the expectation) the execution time at 1 GHz is more than half the execution time at 500 MHz. The developer suspects that the less than linear speedup with double the frequency has to do with the memory. Can you provide justifications for the developer's suspicion? [2 marks]

QUESTION 1 CPU Performance [5 marks]

(A) Processor A has a CPI of 1.3 and 600MHz clock frequency. Processor B has a CPI of 2.5 and 750 MHz clock frequency. The processors have different instruction-set architectures (ISA). A program P when compiled and run on processor A generates 100,000 dynamic instructions during execution. What should be the number of dynamic instructions for program P on processor B so as to have the exactly same execution time for this program on both processors? [2 marks]

(B) Two teams of CS4223 students are optimizing a program for single-cycle processor implementation. Team A discovers that by unrolling the loops, the static instruction count increases by 20%; but the dynamic instruction count reduces to 90% of the original value. Team B instead focuses on optimizing two functions func1( ) and func2( ) that account

for 60% and 30% of the running time of the program, respectively. After optimizations, the team manages to run func1( ) 1.5 times faster but func2( ) now runs 1.2 times slower. Which team has performed better optimization?
[3 marks]