CS4223 Tutorial 6: Memory Consistency Models

Question 1:

In a shared memory system with 3 processors (P1, P2, and P3) that implements Sequential Consistency, what are the legal combination of final values for A, B, and C for the code below? (Assume A, B, and C are initialized to 0)

P1	**P2**	**P3**
A = 1	C = 2	if (A = = 1)
if (B = = 0)	if (B = = 2)	B = 2
C = 1	C = 3	

ANS:

A B C

1 2 3

1 2 1

1 2 2

1 0 2

1 0 1

Question 2:

Consider the following snippet of code to be executed on 2 processors. X is a shared variable and the system uses sequential consistency.

P1	P2
X = 1;	X = 2;
X = X + 2;	X = X + 1;

Show how this code can produce a sequence of memory reads and writes such that X can end up with a value of 2.

ANS:

P2: X = 2

P1: X =1

P1: read X = 1 into R1

P2: read X = 1 into R2

P1: add 2 to R1

P1: write X = 3

P2: add 1 to R2 = 2

P2: write X = 2

Question 3:

Two threads are running in parallel on dual-core architecture. Assume that the shared memory location M is initialized to 0.

Processor P1	Processor P2
(X1) WRITE M ← 1	(Y1) WRITE M ← 3
(X2) READ M	(Y2) READ M
(X3) WRITE M ← 2	(Y3) WRITE M ← 4
(X4) READ M	(Y4) READ M

(i) List all the possible values of M at Y2 under the sequential consistency model.

ANS: M can be 1, 2, or 3

(ii) List all the possible values of M at Y2 under the release consistency model.

ANS: As it is about single memory location M, it can still only be 1, 2, or 3

Question 4:

Consider the following three threads running in parallel on three processors. Assume that the shared memory locations X, Y, Z are all initialized to 0.

Processor P1	Processor 2	Processor P3
WRITE X ← 1	WRITE Y ← 2	WRITE Z ← 3
READ Z	READ X	READ Y

(i) Write down all the possible combination of values that can be returned by the three reads under sequential consistency model.

ANS:

X Y Z

0 0 0 Not possible

0 2 0 Possible

0 2 3 Possible

0 0 3 Possible

1 0 0 Possible

1 2 0 Possible

1 2 3 Possible

1 0 3 Possible

(ii) Write down all the possible combination of values that can be returned by the three reads under TSO model.

ANS: All combinations are possible under TSO model.

Question 5:

Consider the following code fragment running on 2-core shared memory cache-coherent architecture. Initially A = 0, B = 0.

Core 0	Core 1

read A	read B
A = 1	B = 2
B = 1	A = 2

(i) What are the possible combination of values returned by read A and read B under SC memory model?

ANS: A = 0 B = 0

A = 0 B = 1

A = 2 B = 0

(ii) What are the possible combination of values returned by read A and read B under PSO memory model?

ANS: A = 0 B = 0

A = 0 B = 1

A = 2 B = 0

Write->Write reordering does not change anything. Note that there is dependency between read A and A=1; similarly between read B and B=2. These cannot be reordered.

(iii) What are the possible combination of values returned by read A and read B under RC memory model?

ANS: A = 0 B = 0

A = 0 B = 1

A = 2 B = 0

A = 2 B = 1

(iv) Show how you can produce the same results as SC execution when running on RC memory model by adding minimum number of fence instructions.

ANS:

Core 0	Core 1
read A	read B
fence	fence
A = 1	B = 2
B = 1	A = 2

The fence can also be after A=1 and B=2. The result is still the same.