The MiniS08 project (including the FPU) is used as an ABET Senior Design Project. As such its report will be judged on the following items:

1. Were the project scope and goals clearly presented?
2. Was it evident that the project analysis was based on mathematical/scientific/engineering principles?
3. Were various design alternatives considered? (Hint: which HDL to use)
4. Were multiple realistic constraints considered? (I must list them – so you must address them.)
5. Were appropriate engineering standards addressed? (Hint: IEEE 754 (Floating Point), what sections? Not to mention IEEE 1364 (Verilog))
6. Overall assessment of quality.

I would expect these reports to be 4-12 pages with 2-5 of the pages being diagrams – listings would be additional pages.

If you need help with anything like how to express the data flow or the controller state machine, I will be glad to help.

I suggest the following sections and content:

1.Introduction – describe the scope and goals of the project. This basically says we are implementing a subset of the Freescale S08 microcontroller with a memory-mapped Floating-point Unit on an Altera DE2 FPGA development board.
   Design constrains you were given were to implement the project on the DE2 using AHDL or Verilog. Also, you were assigned to use the 7-segment display.
2. For the IEEE 754 standards, discuss the format of the numbers you were using. Discuss the round to even or odd standard.
3. Data Flow – Design alternatives can be discussed in this section (without showing details of each alternative). At one point we discussed the possibility of a single multiplexed address/data bus.
4. Control Units – I would like to see the state diagrams that were used and an explanation of them. There was one for the S08, the multiply operation, and divide operation.
5. Conclusion or Summary – include what could be done to improve the project.