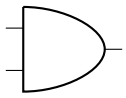
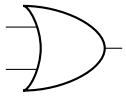
1 Logic gates

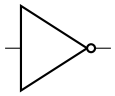
1.1 AND



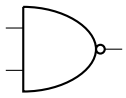
1.2 OR



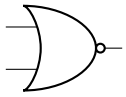
1.3 NOT



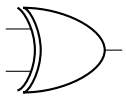
1.4 NAND



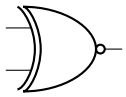
1.5 NOR



1.6 XOR



1.7 XNOR

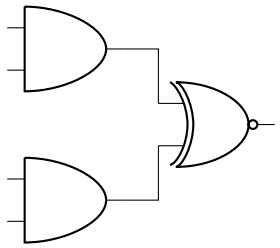


1.8 Basics

Nodes must have curly brackets at the end, even when empty. An optional anchor (#3) can be defined within round brackets to be addressed again later on.

```
\draw (x1,y1) to[<circuit element like, R,L,C>, i=<value>,v=<value>,l=<label>,color=<color>]
      (x2,y2) to[same as above]
      (x3,y3) to[same as above]
      ...
      (xn,yn);
```

1.9 Example 1



1.10 Example 2

Use .in and .out to refer to the inputs and outputs of gates.