Modeling and Analysis of Time-Aware Shaper on Half-Duplex Ethernet PLCA Multidrop

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***Abstract*—Recently, there has been an interest from the automotive industry in a novel single-pair, half-duplex Ethernet multidrop provision (i.e., 10BASE-T1S), which relies on a coordinated channel access method provided by Physical Layer Collision Avoidance (PLCA). PLCA avoids frame collisions and provides bounded latency, while guaranteeing fairness among nodes and optimal bandwidth utilization. However, despite these advantageous features, PLCA is not aware of flow priorities and, consequently, does not provide priority-based Quality of Service (QoS). Thus, there is an opportunity for integrating QoS-aware schemes, such as the Time-Sensitive Networking (TSN)-based Time-Aware Shaper (TAS) algorithm, into PLCA. In this paper, we present modeling and analysis strategies using Network Calculus for integrating TAS with PLCA to support scheduled traffic, and we compare our modeling and analysis with a baseline work which previously modeled TAS for full-duplex point-to-point Ethernet only. We show that replacing full-duplex point-to-point links with half-duplex PLCA multidrop links still complies with end-to-end delay deadlines, while leading to a reduction of system costs due to the fewer number of Ethernet transceivers in a PLCA multidrop. Moreover, we also show that our results for TAS, when applied only on full-duplex point-to-point links, outperform the results of the baseline work in most use cases.**

***Index Terms*—IEEE 802.1Qbv, Network Calculus, Physical Layer Collision Avoidance, Time-Aware Shaper, Time-Sensitive Networking.**

I. Introduction

ETHERNET is a very popular long-standing technology for commercial and industrial applications. In its early stages, Ethernet consisted of a half-duplex multidrop shared channel with CSMA/CD (Carrier Sense Multiple Access with Collision Detection) as the random access protocol. Due to possible frame collisions and the fact that nodes need to enter a random exponential backoff before retrying transmission, it is well known that in a traditional CSMA/CD multridop the overall throughput is (much) lower than the nominal rate of the channel and that latencies are random and unbounded [1]. These facts motivated the development of full-duplex, dedicated point-to-point Ethernet links, which comprise virtually almost all Ethernet implementations today [1].

However, despite their vast success, full-duplex point-to-point Ethernet links may be costly for some use cases. For instance, in automobiles, where Ethernet was not widely adopted until the advent of 100BASE-T1, over 90% of the current internal communication links need less than 10 Mbps [2]. Since the automobile is very cost-sensitive, and a full-duplex switched Ethernet system requires a pair of Ethernet transceivers for each link, the unrestricted use of 100BASE-T1 Ethernet links for use cases that demand low bandwidth in cars is not cost-efficient, especially because legacy technologies such as CAN (Controller Area Network) or CAN-FD (CAN with Flexible Data Rate) satisfy low-bandwidth demands in a timely manner with competitive costs.

Nevertheless, the trend in automobiles towards an all-Ethernet car, mostly motivated by the emergence of service-oriented and zonal-based architectures [3], [4], raised the need of a low-cost, lower-speed Ethernet solution that is compliant with the requirements of automotive systems. The recently standardized 10BASE-T1S Ethernet, which was a result of a revamped interest in a half-duplex, low-cost, and single-pair Ethernet multidrop, was the missing element for a complete suite of Ethernet speeds to be efficiently used in current and future automotive applications [5]. With 10BASE-T1S replacing legacy low-rate technologies in cars, Ethernet would connect all the way edge sensors and actuators, leveraging the flexibility of a homogeneous in-vehicle network and preventing the use of gateways, which add cost, complexity and latency [3], [4].

Unlike the early generations of Ethernet which are based on a random access protocol on a half-duplex multidrop, 10BASE-T1S relies on a coordinated channel access method provided by PLCA (Physical Layer Collision Avoidance). PLCA can be described as a generic Reconciliation Sublayer, which indeed reconciles Media-Independent Interface (MII) signals to the Medium Access Control (MAC) [6]–[8]. In contrast to the protocol of the original CSMA/CD, PLCA avoids frame collisions and provides bounded latency and optimal bandwidth utilization, while guaranteeing fairness among nodes [2], [7], [9]. Fig. 1 depicts Ethernet in the IEEE and highlights where PLCA acts in the layering model.

PLCA avoids physical collisions on the medium by signaling logical collisions to the MAC layer so that the MAC layer will not perform a new transmission attempt while the channel is busy (i.e., the Carrier Sense signal is asserted). After reporting a logical collision, the MAC layer applies the backoff algorithm for a random short time, while PLCA waits for a new transmit opportunity before deasserting the Carrier Sense signal. In this way, the MAC layer will always be ready to perform a new transmission attempt before the next transmit opportunity is met [8].

In spite of the aforementioned benefits, a major limitation of PLCA is the lack of support to flow priorities, i.e., the absence of priority-based QoS. In an all-Ethernet car, different

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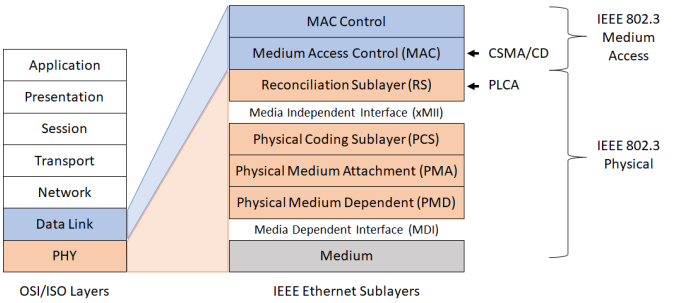

Fig. 1. Ethernet in the IEEE and where PLCA acts in the layered model (adapted from [2]).

types of traffic such as diagnostics, audio streaming, video and highly reliable control data coexist on the same in-vehicle network technology and need different levels of QoS [10]. So, an integration of PLCA with a QoS-aware scheme would provide the sought-after traffic prioritization on half-duplex multidrops in an all-Ethernet car.

A. Related Work

Time-Sensitive Networking (TSN), a set of standards specified by IEEE 802, has the goal of enabling IEEE 802 networks to support novel applications that need precise clock synchronization among nodes, deterministic latencies, and stringent QoS requirements [11]. As one of the most prominent TSN standards for QoS, the protocol IEEE 802.1Qbv is managed by the Time-Aware Shaper (TAS) algorithm, which provides a configurable periodic transmission scheduling using time-based gates for priority queues on the Ethernet interface. TAS enables a network to provide fully-deterministic, end-to-end communication with very low latency and jitter for critical, scheduled flows over point-to-point links [12].

An all-Ethernet car will contain many safety-critical systems that rely on real-time critical flows. The failure of these systems could lead to loss of life, serious property damage or harm to the environment [13]. Thus, the worst-case timing condition of safety-critical, time-sensitive systems must be verified to guarantee their safety compliance. Among the techniques commonly used for this verification, Network Calculus stands out as a powerful system theory for the worst-case timing analysis of critical flows, and it has been extensively used in the literature for this purpose as described as follows.

Modeling and analysis using Network Calculus for the Time-Aware Shaper algorithm in full-duplex Ethernet links are presented in [12], where the authors model class-based TAS scheduling and show how the overlapping among priority queue time slots can impact on the latency of scheduled, critical flows. In [14], the authors use Network Calculus to model and analyze the latency of mixed-criticality traffic in an integration of TAS with the Credit-Based Shaper (CBS) from IEEE 802.1Qav, where TAS is used to control critical, scheduled traffic, and CBS is used to control multimedia streams.

Modeling and analysis for combinations of TAS, CBS, and preemption are proposed in [15]. The authors use Network Calculus to investigate the scenario with and without preemption, and compare such results. In [16], the authors present modeling and analysis with the use of Network Calculus for two traffic shapers for critical traffic: TAS and the Asynchronous Traffic Shaper (ATS) protocol from IEEE 802.1Qcr. The authors also combine such protocols with CBS and Strict Priority (SP).

An enhanced Network Calculus modeling for stream-based TAS scheduling is provided in [17], where the authors propose a modeling that relies on the relative offset of transmission time slots in the path of flows. However, the model is not suitable to be directly applied in class-based TAS scheduling because the overlapping of time slots is not supported in that model. In [18], the authors present a Network Calculus theory to compute delay bounds for flows with packet-level arrival-curve for a First-In-First-Out (FIFO) system with a TSN scheduler (e.g., CBS), which leads to delay improvements. However, such a work does not cover the TAS protocol. A survey about modeling and analysis for several TSN protocols using Network Calculus is provided in [19]. There are also proposals for modeling TAS using the mathematical framework Compositional Performance Analysis (CPA) [20], [21].

Despite the aforementioned works provide modeling and analysis for TSN protocols, none of them have considered the integration of TSN protocols with a half-duplex PLCA multidrop. In [9], the author discusses the benefits and drawbacks of integrating TSN with PLCA, but he does not provide neither modeling nor timing analysis. In [22], [23], the author sheds light about using priorities in PLCA.

B. Contributions

In this paper, we present modeling and analysis strategies for integrating the TAS algorithm with PLCA using Network Calculus to determine the worst-case delay of scheduled traffic by TAS on a half-duplex PLCA multidrop. While TAS was originally designed for full-duplex point-to-point Ethernet links, an appropriate integration of TAS with PLCA has the potential to enable stringent deterministic latency with very low jitter in half-duplex multidrop provisions. The integration of TAS with PLCA is a major challenge as it must consider that both TAS on the link layer and PLCA on the physical layer are cyclic, but not synchronized. TAS has a clock-based, static cycle length, whereas PLCA has a dynamic cycle length based on frame sizes on the half-duplex multidrop. That is, there is a synchronization issue between TAS and PLCA, such that a wrong choice on the TAS or PLCA planning can make critical flows not meet deadlines or even cause frame starvation due to a synchronization mismatch between TAS and PLCA. Thereby, a model to compute the deterministic latencies for scheduled traffic on a half-duplex PLCA multidrop is required. In this paper, we address these issues as well as its aftereffects, and propose a solution to verify a TSN network regarding both TAS scheduling and its compatibility to the half-duplex PLCA multidrops.

The worst-case timing analysis to verify guarantees that critical flows meet the stringent deadlines in a scenario where TSN is combined with PLCA on half-duplex multidrop is an open research problem. To the best of our knowledge, this paper presents the first modeling and analysis for the

integration of TAS with PLCA on half-duplex multidrop, either using Network Calculus or another framework.

In a nutshell, the main contributions of this paper are:

- A Network Calculus modeling using simple curves and enhanced analyses as an alternative solution in contrast to other works that rely on accurate curves and archaic analyses;
- The proposal of a modeling for integrating PLCA with TAS on a half-duplex multidrop;
- Comparison of our solution with a baseline work as a trade-off between modeling and analysis on TAS-based full-duplex Ethernet networks. We show that our alternative solution provides lower worst-case end-to-end delay bounds compared to a baseline work in most use cases;
- Comparison of half-duplex multidrop using PLCA with full-duplex point-to-point links in terms of delay bounds. We show that for all scheduling cases, a single-hop half-duplex PLCA multidrop with four nodes provides a lower delay bound than two hops of full-duplex point-to-point links of the same speed;
- An open-source Network Calculus tool for calculating bounds on TAS-based TSN networks with full-duplex point-to-point links and half-duplex PLCA multidrop links.

C. Organization

The remainder of this paper is organized as follows. Section II presents the background on PLCA, TAS and Network Calculus for the subsequent sections. Section III presents the details on our Network Calculus system modeling and analysis for an integrated TAS and PLCA networked system. In Section IV, we numerically evaluate our model before Section V concludes the paper.

II. Background

In this section, we briefly present the three basics that we bring together on our work: PLCA on the physical layer, TAS on the link layer and the Network Calculus that we use to provide an integrated modeling and analysis of such a system (see Section III).

A. Physical Layer Collision Avoidance

The IEEE 802.3cg Ethernet PHY standard defines Physical Layer Collision Avoidance (PLCA) as a generic Reconciliation Sublayer for 10BASE-T1S, allowing for multidrop functionality [2], [8], [24]. In-vehicle networks are a use case for 10BASE-T1S. Fig. 2 shows a network where the 10BASE-T1S multidrop link connects Electronic Control Units (ECUs) to an Ethernet TSN switch.

A node can send a frame in a transmission slot called Transmit Opportunity (TO). Each node has a single TO within a PLCA cycle (called beacon cycle). Each node attached to the multidrop has a unique ID, and there is one head node (called coordinator) with ID $= 0$. PLCA cycles are defined as follows. First, the coordinator sends a beacon for synchronization of

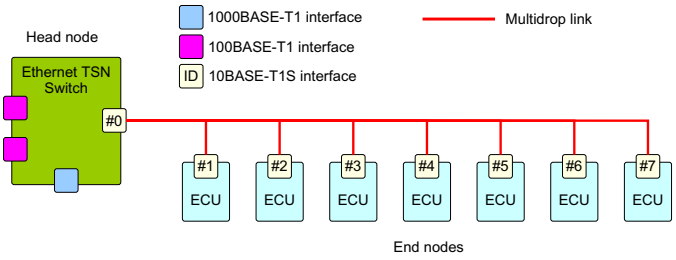

Fig. 2. Example of an in-vehicle network composed of an Ethernet TSN switch and seven ECUs connected through a 10BASE-T1S multidrop link.

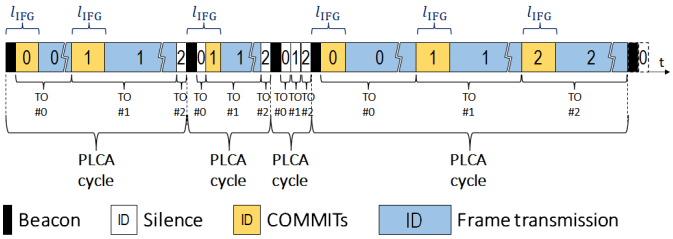

Fig. 3. Example of TOs and PLCA cycles in a multidrop with three nodes.

nodes. Then, the head node has its TO, followed by the end nodes (called drop nodes) according to their ID ordering [2, Section 5.4.3.2]. Overall, PLCA enables for a coordinated half-duplex medium access avoiding frame collisions. In case collisions occur nonetheless, CSMA/CD is applied with a time shorter than its next TO [8].

Fig. 3 shows a detailed example with three nodes. Numbers inside rectangles denote node IDs. TOs are represented by blue or white rectangles, showing frame transmissions (i.e., used TOs) or silences (i.e., unused TOs). Fig. 3 shows that PCLA cycles can therefore be of different length. COMMIT symbols, represented by yellow rectangles, are sent to signal that the current node has a frame to transmit. They are sent during the so-called Interframe Gap (IFG) before a frame transmission from the current TO owner. If the elapsed time after the last transmission is smaller than the IFG length, denoted by l_{IFG}, then those COMMIT symbols are repeated during the length of an IFG [2, Section 5]. The third PLCA cycle in Fig. 3 shows the shortest possible PLCA cycle length and the fourth PLCA cycle shows the longest one.

It is important to note the difference to Time-Division Multiple Access (TDMA). In TDMA, transmission slots are of fixed size and at fixed positions in the cycle. PLCA aims to minimize the unused transmission slot length dynamically. Fig. 4 compares TDMA and PLCA.

Last, note that PLCA has two transmission modes that are required to consider: *normal mode* and *burst mode*. In the normal mode, a node can transmit only a single frame within a TO, whereas in the burst mode more than one frame can be transmitted by a node whithin a TO.

B. The Time-Aware Shaper algorithm

On the link layer, IEEE Time-Sensitive Networking (TSN) emerged as a promising technology. One of the most widely

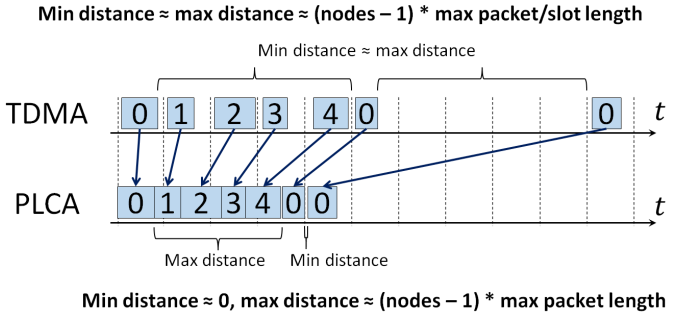

Fig. 4. Comparison of TDMA and PLCA regarding minimum and maximum distance between transmissions from node 0 in a shared medium with five nodes (adapted from [2]).

used algorithms of this standardization suite is the Time-Aware Shaper (TAS) specified in the TSN protocol IEEE 802.1Qbv. It was designed to deal with Scheduled Traffic (ST) transmissions with different priorities [12]. TAS defines a gate for each priority queue. A frame can be sent when the corresponding priority queue's gate is scheduled to be open. Overall, gate scheduling is managed by a Gate Control List (GCL) configuration. The GCL scheduling describes the gate states within a cycle, the GCL hyperperiod.

Two main objectives are known for defining GCLs within a network: stream-based scheduling and (entirely) class-based scheduling. In stream-based scheduling, the GCLs are defined to achieve complete temporal isolation of data flows (the streams), i.e., by configuration, there will be no queuing delay. Unfortunately, the provision of a network scheduling that is able to accommodate all the scheduled flows is, in general, an NP-hard problem [25]. Some papers have addressed the TSN scheduling and have pointed solutions [26]–[28]. To avoid this, class-based scheduling allows GCL configurations to open multiple gates simultaneously such that the data with the highest priority will be transmitted [12]. Although TAS can be configured using either class-based or stream-based scheduling, the class-based scheduling is predominant as it is easier to implement. Yet, it requires a subsequent, more complex performance evaluation. This paper relies on a class-based scheduling dataset as in [12]. We are interested in analyzing GCL configurations when implemented on top of PLCA on the physical layer. Our contribution is in Section III.

C. Network Calculus

Network Calculus (NC) is a system theory dedicated to worst-case queuing and forwarding of data. In a first step, the worst-case behavior of input to the network as well as data forwarding within the network need to be modeled. Then, a (min,+)-algebraic analysis can be applied to compute a deterministic bound on the worst-case end-to-end delay of a flow as well as servers' buffer requirements [29]. In this section, we provide the background to use NC for modeling the interaction of a system that runs TSN TAS on top of a PLCA PHY.

In NC, data flows are represented as cumulative function $R(t)$ counting the flow's data in the time interval $[0, t]$, i.e., $R(t) = 0, \forall t \leq 0$. The function $R(t)$ is thus positive and wide-sense increasing. Servers are forwarding incoming data, i.e., they generate data output that is described with the cumulative function $R^*(t)$. Servers can implement, for example, simple queues or complex scheduling mechanisms such as TAS, PLCA or their combination.

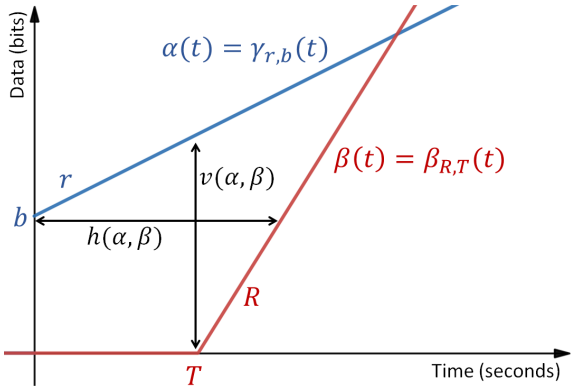

Fig. 5. Examples of token-bucket arrival curve $\gamma_{r,b}(t)$ and rate-latency service curve $\beta_{R,T}(t)$.

NC modeling is based on functions bounding $R(t)$ and $R^*(t)$, the so-called Arrival Curves. Their relation is captured by the bounding function describing a server's forwarding capabilities, the so-called Service Curves. Curves are cumulative and wide-sense, a set of functions denoted as $\mathcal{F}$.

Definition 1 (Arrival Curve)**.** *[29, Section 1.2.1] Given a wide-sense increasing function α defined for $t \geq 0$, we say that a flow R is constrained by α if and only if for all $s \leq t$:*

$$R(t) - R(s) \leq \alpha(t - s).$$

Definition 2 (Service Curve)**.** *[29, Section 1.3.1] Consider a system $\mathcal{S}$ and a flow through $\mathcal{S}$ with input and output functions equal to R and R^*, respectively. We say that $\mathcal{S}$ offers the flow a service curve β if and only if β is wide-sense increasing with $\beta(0) = 0$ and for all $t > 0$:*

$$R^*(t) \geq \inf_{0 \leq s \leq t} \{R(s) + \beta(t - s)\}.$$

A commonly found arrival curve shape is the token-bucket curve. It is denoted by $\gamma_{r,b}(t) = \{r \cdot t + b, \text{if } t > 0; 0, \text{otherwise}\}$, where r upper-bounds the flow rate and b is the burst size of the flow, for $t > 0$. In addition, a commonly found service curve shape is the rate-latency curve. It is denoted by $\beta_{R,T}(t) = R[t - T]^+$, where R lower-bounds the rate the system can offer the flow, T is the latency the flow will experience when crossing the system, and $[x]^+ := \max\{0, x\}$. See Fig. 5 for illustrations. More complex data arrival and forwarding patterns may yield more complex curves. Yet, token buckets and rate latencies can still be used to bound these patterns while simultaneously allow for application of more advanced NC analyses.

Classical Network Calculus analysis builds on (min,+)-algebraic operations. The following set of operations is used to reduce the network to a single service curve β for the analyzed flow's (the flow of interest's) end-to-end service guarantee. This service curve and the flow of interest's arrival curve are used to bound performance worst-case characteristics.

Definition 3 ((min,+) convolution)**.** *[29, Section 3.1.6] Let f and g be two functions or sequences from the set of functions $\mathcal{F}$. The (min,+) convolution of f and g is the function*

$$(f \otimes g)(t) = \inf_{0 \le s \le t} \{f(t-s) + g(s)\}.$$

If $t < 0$, $(f \otimes g)(t) = 0$.

Definition 4 ((min,+) deconvolution)**.** *[29, Section 3.1.9] Let f and g be two functions or sequences of $\mathcal{F}$. The (min,+) deconvolution of f by g is the function*

$$(f \oslash g)(t) = \sup_{u \ge 0} \{f(t+u) + g(u)\}.$$

Theorem 1 (FIFO Left-over Service Curve)**.** *[29, Section 6.2.2] Consider that a flow shares a server with service curve β with some cross-traffic with α_{xtx}. If the server implements the First-In-First-Out policy, then the remaining service is*

$$\beta^{l.o.}(t) = [\beta(t) - \alpha_{xtx}(t-\theta)]^{+} \cdot 1_{\{t>\theta\}}$$

with $[x]^{+} := \max\{0, x\}$ and the indicator function $1_{\{condition\}}$.

Note that the optimal value for the θ parameter needs to be found depending on the overall analysis. We will use a classical result for approximation of this parameter: $\theta = T + \frac{b_{\text{xtx}}}{R}$, where b_{xtx} denotes the burst term of α_{xtx} [30].

Theorem 2 (Delay Bound)**.** *[29, Section 3.1.11] Consider a server s that offers a service curve β. Assume that a flow f with arrival curve α traverses the server. We bound the delay of f with the maximum horizontal deviation between α and β:*

$$\forall t \in \mathbb{R}^{+}: \; D(t) \le \inf\{d \ge 0 \,|\, (\alpha \oslash \beta)(-d) \le 0\}.$$

Applying Network Calculus to an application requires the derivation of the above curves. We present models for a combination of TSN TAS and half-duplex PLCA multidrop (Section III). For the analysis of an entire network, we then use existing NC tool support [31].

TABLE I
LIST OF SYMBOLS AND THEIR DEFINITION.

Term	Description
$\alpha_{P_m}^{ST}(t)$	Leaky-bucket arrival curve for an ST flow of priority P_m.
$\beta_{\text{PLCA}}^{h}(t)$	Service curve for PLCA service of interface h.
$\beta_{P_m}^{h}(t)$	Service curve of interface h for priority traffic P_m.
$\beta_{P_m}^{h,j,i}(t)$	Service curve of interface h in the j-th guaranteed window by taking the i-th guaranteed window as reference.
$\beta_{T,L}(t)$	Classic TDMA staircase shape service curve.
$\beta_{T,L}^{\text{rate-latency}}(t)$	TDMA rate-latency shape service curve.
$D_{P_m}^{h}$	Delay bound on interface h regarding TAS service.
D_{PLCA}^{h}	Delay bound on interface h regarding PLCA service.
$D_{\text{q\&t}}^{dev,h}$	Delay bound on interface h of an Ethernet device ($dev \in \{ES, SW\}$).
D_{proc}	Delay bound on a switch regarding input interface and switching-fabric.
$L_{W,P_m}^{h,i}$	Length of the i-th window of interface h for priority queue P_m.
$L_{GW,P_m}^{h,i}$	Length of the i-th guaranteed window of interface h for priority queue P_m.
$L_{\text{Tx},P_m}^{\max}$	Maximum transmission length of a frame from priority P_m.
$l^{h,\min}$	Minimum frame size from interface h regardless of priority.
$l^{h,\max}$	Maximum frame size from interface h regardless of priority.
$l_{P_m}^{\max}$	Maximum frame size from an ST flow with priority P_m.
l_{IFG}	Length of the Interframe Gap.
l_{beacon}	Length of the beacon.
N_{W,P_m}^{h}	Number of windows in schedule in interface h for priority queue P_m.
P_m	Priority of a frame with $m \in [0..7]$.
PQ_{P_m}	Priority queue for frames with priority P_m.
q_{beacon}	Quantum of PLCA service for the beacon transmission.
$q^{h,\min}$	Minimum quantum of PLCA service for interface h.
$q^{h,\max}$	Maximum quantum of PLCA service for interface h.
$Q^{h,\max}$	Maximum cross-traffic quanta of PLCA service of interface h.
T_{GCL}^{h}	GCL hyperperiod of interface h.
T_{P_m}	Transmissions period of frames from an ST flow with priority P_m.
w^{h}	Number of frames interface h can transmit within its transmit opportunity.

III. Worst-Case Modeling and Analysis of TSN Time-Aware Shaper in conjunction with a half-duplex PLCA multidrop link

As mentioned before and already visualized in Fig. 2, we present strategies for integrated modeling and analysis of TAS shaped traffic sent via a PLCA multidrop link. In this section, we start by modeling the parts with Network Calculus, followed by integration of both models via proposed coordination of their design and configuration parameters.

A. Modeling the Time-Aware Shaper

Modeling and analysis for class-based TAS scheduling without preemption were proposed in [12], where the authors tackled a principal aspect of it: critical scheduled traffic may suffer interference from traffic of other priorities in each output interface. This happens because the class-based TAS scheduling may not produce exclusive windows among priorities, leading to overlapping windows. Thus, even if a priority queue gate is open, it may not have the whole window available for transmission. TAS applies the strict priority algorithm when more than one gate is open. For instance, without preemption, when a higher priority window is open during the transmission of a lower priority frame, the interface must wait for the conclusion of its current lower priority frame transmission before starting the transmission of the higher priority frame. Note that a stream-based scheduling is a special case of scheduling that does not have overlapping, thus a modeling for the class-based scheduling can be applied for both class-based and stream-based schedulings.

Due to overlapping situations, the guaranteed windows must be calculated. Within these guaranteed windows, data from a specific priority can receive minimum guaranteed service. There is a guaranteed window inside of each window; however, the position and length of the guaranteed window depend on its own window and the overlapping windows. Thus, the modeling of [12] relies on calculating guaranteed windows for all priority queues in all output interfaces of every network device, and this paper follows the same approach. Table I shows the list of symbols used in this paper along with their definition.

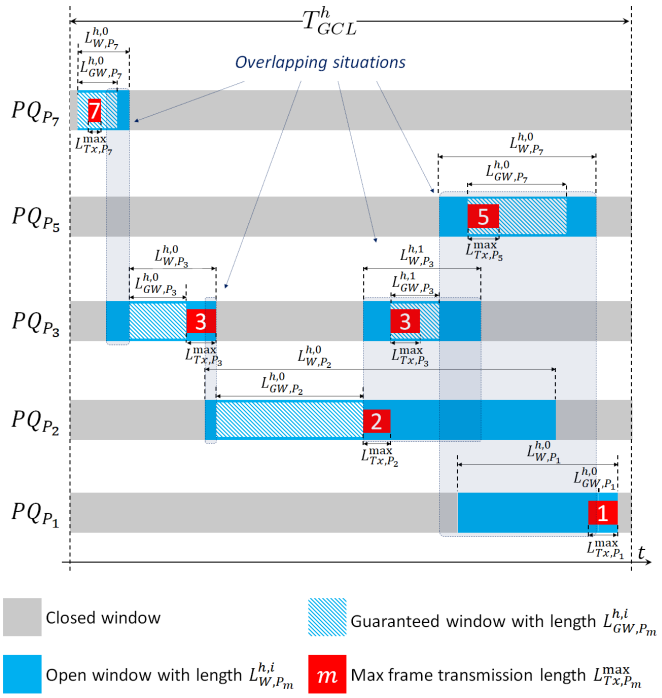

Fig. 6. Example of a TAS scheduling of an Ethernet interface h with five priority queues in descending order of priority, PQ_{P_7}, PQ_{P_5}, PQ_{P_3}, PQ_{P_2}, and PQ_{P_1}.

Fig. 6 depicts an example of TAS scheduling with overlapping windows among five priority queues in descending order of priority[1], PQ_{P_7}, PQ_{P_5}, PQ_{P_3}, PQ_{P_2}, and PQ_{P_1} for the Ethernet interface h. The lengths of all windows and guaranteed windows are denoted by $L^{h,i}_{W,P_m}$ and $L^{h,i}_{GW,P_m}$, respectively, where $i \in [0..N^h_{W,P_m} - 1]$ denotes the index of the window and its related guaranteed window, and N^h_{W,P_m} denotes the number of windows in the TAS scheduling of Ethernet interface h for priority queue $PQ_{P_m}, m \in [0..7]$. In the worst-case scenario, a frame with the maximum transmission length $L^{\max}_{\text{Tx},P_m}$ can start anytime within the guaranteed windows. For instance, in Fig. 6, the frame from PQ_{P_5} starts at the beginning of its guaranteed window, and the frame from PQ_{P_2} starts just before the ending of its guaranteed window. Also, frames from PQ_{P_1} could not be transmitted because the guaranteed window for PQ_{P_1} has length zero, i.e., $L^{h,0}_{GW,P_1} = 0$. This is an example of an invalid class-based scheduling.

A priority queue PQ_{P_m} in use of interface h can have one or more windows within the GCL hyperperiod (i.e., $N^h_{W,P_m} \geq 1$), as shown in the example of Fig. 6. In that figure, each priority P_m has the following number of windows: $N^h_{W,P_7} = 1$, $N^h_{W,P_5} = 1$, $N^h_{W,P_3} = 2$, $N^h_{W,P_2} = 1$, and $N^h_{W,P_1} = 1$. So, the resulting TAS guaranteed service for priority P_m is the sum of the guaranteed service in all guaranteed windows for P_m. However, since an ST frame of priority P_m can be transmitted within any window for P_m, it is required to assume that such frame can be transmitted in the i-th ($i \in [0..N^h_{W,P_m} - 1$]) guaranteed window for which the worst-case condition for transmission will be provided.

Thus, the service curve for traffic with priority P_m is the minimum guaranteed service for P_m by taking the i-th guaranteed window as reference,

$$\beta^h_{P_m}(t) = \min_{0 \leq i \leq N^h_{W,P_m}-1} \left\{ \sum_{j=i}^{i+N^h_{W,P_m}-1} \beta^{h,j,i}_{P_m}(t) \right\}, \quad (1)$$

where $\beta^{h,j,i}_{P_m}(t)$ denotes the guaranteed service of interface h in the j-th guaranteed window by taking the i-th guaranteed window as reference [12].

Guaranteed windows do not have overlapping, then one can model the guaranteed service for traffic with priority P_m in TAS based on the minimum TDMA (Time Division Multiple Access) service using the following equation as in [12], [14],

$$\beta_{T,L}(t) = C \cdot \max\left(\left\lfloor \frac{t}{T} \right\rfloor L, t - \left\lceil \frac{t}{T} \right\rceil (T - L) \right). \quad (2)$$

That is a classic TDMA staircase shape service curve with period T, time slot length L, and link speed C [33].

By applying

$$\beta^{h,j,i}_{P_m}(t) = \beta_{T^h_{GCL}, L^{h,i}_{GW,P_m}}(t + t_0),$$

where $T = T^h_{GCL}$ is the GCL hyperperiod of interface h, $L = L^{h,i}_{GW,P_m}$ is the length of the i-th guaranteed window, and t_0 is the proper offset for the i-th guaranteed window within the GCL hyperperiod due to the overlapping situations [12]. Then one can compute the guaranteed service for the i-th guaranteed window of interface h.

However, $\beta_{T^h_{GCL}, L^{h,i}_{GW,P_m}}(t + t_0)$ proposed by [12] relies on $\beta_{T,L}(t)$, which is a staircase shape TDMA equation. For simplicity of depiction and improved analysis performance [34], [35], we replace that staircase TDMA service curve with a rate-latency TDMA service curve

$$\beta^{\text{rate-latency}}_{T,L}(t) = \beta_{R,\tau}(t) = \frac{L}{T} \cdot C \cdot [t - (T - L)]^+, \quad (3)$$

where rate $R = \frac{L}{T} \cdot C$, latency $\tau = (T - L)$, C denotes the link speed, T denotes the period, and L denotes the time slot length [35]. That is, in this paper we propose to apply

$$\beta^{h,j,i}_{P_m}(t) = \beta^{\text{rate-latency}}_{T^h_{GCL}, L^{h,i}_{GW,P_m}}(t + t_0).$$

As a consequence, we get $\forall t : \beta^{\text{rate-latency}}_{T,L}(t) \leq \beta_{T,L}(t)$, as shown in Fig. 7 (a).

Hence, $\beta^h_{P_m}(t)$ from [12] is composed of a sum of $\beta^{h,j,i}_{P_m}(t)$ terms, which are staircase curves, resulting in a complex shape curve, as shown in the red dashed curve of Fig. 7 (b). However, even using rate-latency service curves for $\beta^{h,j,i}_{P_m}(t)$, the $\beta^h_{P_m}(t)$ is composed of a sum of many curves. Then it results in a piece-wise linear shape curve, as shown in the blue solid line curve in Fig. 7 (b).

While this approximation decreases the model's accuracy by giving less service capacity than a queue actually gets, many analysis results in Network Calculus are currently not applicable to more complex curve shapes, for instance, staircase. Prime examples are the Pay Multiplexing Only Once

[1]We used the priority levels as defined by IEEE 802.1Q [32], which specifies a priority level between 0 (lowest) to 7 (highest). However, the baseline work [12] uses an inverted order of priorities.

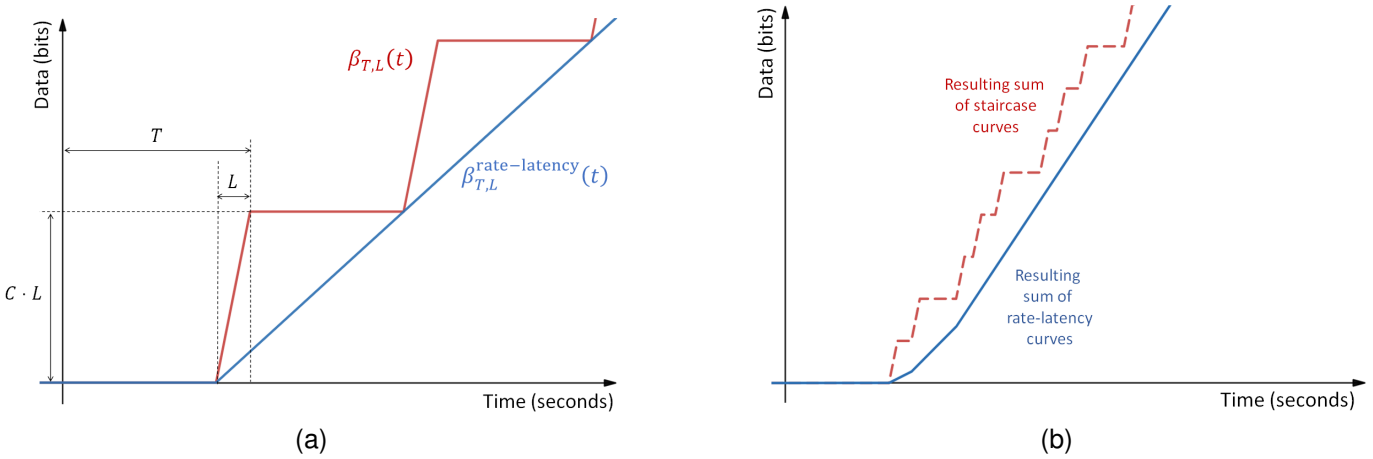

Fig. 7. Curve examples and comparison: (a) staircase- and rate-latency-based TDMA service curves. The red curve, denoted by $\beta_{T,L}(t)$, is a staircase shape curve, and the blue curve, denoted by $\beta_{T,L}^{\text{rate-latency}}(t)$, is a rate-latency shape curve; and (b) resulting curve shapes for $\beta_{P_m}^{h}(t)$ with three guaranteed windows (i.e., $N_{W,P_m}^{h} = 3$). The red dashed line is a result from the sum of staircase curves (i.e., when $\beta_{P_m}^{h,j,i}(t)$ relies on $\beta_{T,L}(t)$), and the blue solid line is a result from the sum of rate-latency curves (i.e., when $\beta_{P_m}^{h,j,i}(t)$ relies on $\beta_{T,L}^{\text{rate-latency}}(t)$).

(PMOO) analysis and the Tandem Matching Analysis (TMA) provided by the DNC tool [31] or the Least Upper Delay Bound (LUDB) analysis [36]. Thus, we choose to apply simple curves with enhanced analysis techniques rather than complex, accurate curves with an archaic analysis.

B. Modeling PLCA and its integration with TAS

Whereas TAS is a TDMA-based scheme, PLCA is a Round Robin (RR) one. Various RR scheduling variants have already been modeled with NC. Among them, Weighted Round Robin (WRR) [37, Section 8.2.4] best matches the PLCA behavior, since the weights in WRR can represent the number of frame transmissions within a PLCA's Transmit Opportunity (TO), independent of the actual frames' sizes [9], [38]. WRR can model both PLCA normal mode and burst mode by using, respectively, weights $w^h = 1$ and $w^h > 1$, where an interface h can transmit up to w^h frames in one TO. Moreover, unused credits by the weight are lost between rounds, matching the TO behavior.

Deficit RR [37, Section 8.2.3] allows to carry over unused credit into the subsequent round, which is incompatible with the PLCA behavior. Interleaved WRR [39] is an adaptation of WRR that does not grant scheduled interfaces with a weight larger than 1 to send all frames in one burst. Instead, the transmissions from the interfaces are interleaved with one another within an RR cycle. IWRR is also incompatible with the PLCA behavior.

The TAS service in each priority queue relies on the guaranteed window lengths. However, guaranteed windows in TAS are clock-based, and TOs in PLCA are round-robin-based. TAS and PLCA are cyclic, but not synchronized. PLCA has a dynamic cycle length based on frame sizes on the half-duplex multidrop (i.e., PLCA cycle) and TAS has a clock-based, static cycle length (i.e., GCL hyperperiod). So a wrong choice on the TAS or PLCA planning can make a synchronization mismatch between TAS and PLCA. As a result, the modeling for TAS with PLCA on the half-duplex multidrop must consider both timing cycles. Therefore, a model to compute the deterministic latencies for scheduled traffic over a half-duplex PLCA multidrop must be provided.

The baseline on TAS modeling [12] covers the medium access control (MAC) layer behavior, which deals with packet queuing of different priorities and transmission in full-duplex point-to-point interfaces. When the half-duplex PLCA multidrop is used in the physical layer, the interface speed and the additional latency for the channel access are used in the WRR-based PLCA modeling.

In this section, we further develop the Network Calculus model, assuming a hierarchical scheduler in two independent locations: one on the MAC layer that shares TAS service among priority queues relying on TDMA and another on the PHY layer that shares PLCA service among multidrop nodes relying on WRR.

Since the PLCA scheme is based on WRR [9], [38], we investigate the straightforward solution of putting a single PLCA server in each Ethernet interface of the multidrop for sharing service among devices in a WRR manner. By adapting the WRR modeling from [40], we propose a PLCA modeling strategy, which we name Single PLCA WRR Server modeling. So, in an output Ethernet interface, the servers of the TAS priority queue of the MAC layer are connected to a single PLCA server in the PHY layer, acting like a hierarchical scheduler, as depicted in Fig. 8.

In default WRR, the service is shared among queues accordingly to their weight and frame size. Weight denotes the number of frames a queue can transmit in a WRR round. However, for this modeling, WRR is applied for sharing service among interfaces of a multidrop rather than queues of an interface. So, an Ethernet interface h can transmit up to w^h frames in a PLCA cycle. When all weights $w^h = 1$, then all devices are using PLCA in normal mode. When some devices are using $w^h > 1$, then they are using PLCA burst mode. The maximum number of frames transmitted from interface h within a TO, denoted here as w^h, is a PLCA parameter [24,

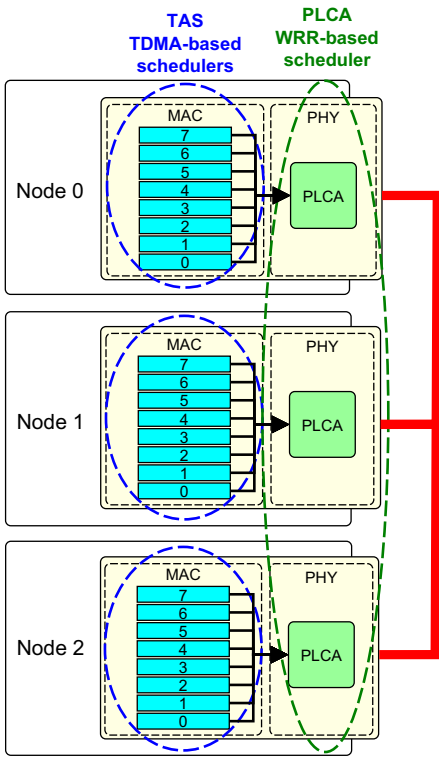

Fig. 8. Example of an Ethernet half-duplex PLCA multidrop network with three nodes running TAS. Blue rectangles in the MAC layer depict TSN queues, green rectangles in the PHY layer depict the PLCA, and the red line the multidrop link.

Section 30.16.1.1.6].

Theorem 3. *A PLCA service curve for interface h regarding the multidrop access can be given by*

$$\beta^{h}_{PLCA}(t) = \frac{q^{h,\min}}{q^{h,\min} + Q^{h,\max}} \cdot C \cdot \left[t - \frac{Q^{h,\max}}{C} \right]^{+}, \quad (4)$$

where C denotes the speed of the Ethernet multidrop, $q^{h,\min}$ denotes the minimum quantum of PLCA service for interface h, and $Q^{h,\max}$ denotes maximum cross-traffic quanta of PLCA service.

Proof. Relying on the WRR modeling concept from [40], our PLCA modeling assumes that an Ethernet interface $h \in I$ will share the PLCA service among a set of interfaces I that compose multidrop in each PLCA cycle. Since the link rate is shared among queues in WRR modeling [40], similarly, in this modeling the multidrop rate is shared among interfaces. Thus, h will have proportional rate and relative latency accordingly to its multidrop access for frame transmissions.

In a PLCA cycle, firstly there is the beacon transmission from the head-node's interface (i.e., $h = 0$), whose service is given by

$$q_{\text{beacon}} = w^{0}_{\text{beacon}} \cdot l_{\text{beacon}}, \quad (5)$$

with $w^{0}_{\text{beacon}} = 1$, and $l_{\text{beacon}} = 20$ bits [24, Section 148.4.4.4].

Subsequently, all interfaces may use their TOs for transmitting frames such that any interface $h \in I$ can have, respectively, minimal and maximal PLCA service given by

$$q^{h,\min} = w^{h} \cdot (l_{\text{IFG}} + l^{h,\min}), \quad (6)$$

and

$$q^{h,\max} = w^{h} \cdot (l_{\text{IFG}} + l^{h,\max}). \quad (7)$$

That is, within its TO, interface h is able to transmit w^{h} frames with minimum length $l^{h,\min}$ and maximum length $l^{h,\max}$, preceded by COMMIT symbols. Such symbols are transmitted in the whole IFG with length $l_{\text{IFG}} = 32$ bits and are used for signaling when there is a frame ready to be transmitted in the TO [2, Section 5.4.3.2].

By considering the integration of TAS and PLCA for interface h with proper TAS scheduling in which none ST frame will miss its window for transmission, in the worst case scenario an ST frame from any priority queue of interface h may be ready to be transmitted just after the end of the TO of interface h. That is, such frame must wait to be transmitted in the TO of interface h in the next PLCA cycle, but still in its current window from TAS scheduling.

Thus, a minimum quantum of PLCA service, denoted by $q^{h,\min}$, may be given to an interface h after the maximum quanta of service was given to all other transmissions: the service for the beacon transmission, denoted by q_{beacon}, and the maximum quantum of PLCA service for transmissions from all other interfaces $\hat{h} \in I \setminus \{h\}$, denoted by $q^{\hat{h},\max}$. That is, the maximum cross-traffic quanta of PLCA service, denoted by $Q^{h,\max}$, is given by

$$Q^{h,\max} = q_{\text{beacon}} + \sum_{\hat{h} \in I \setminus \{h\}} q^{\hat{h},\max}. \quad (8)$$

Given that h is an interface of a multidrop, in the worst-case scenario, the latency to access the multidrop for transmission is upper bounded by

$$T^{h} = \frac{Q^{h,\max}}{C}. \quad (9)$$

Also, since the multidrop speed C is shared among all interfaces, then interface h has the proportional rate

$$R^{h} = \frac{q^{h,\min}}{q^{h,\min} + Q^{h,\max}} \cdot C. \quad (10)$$

Thereby, by replacing terms accordingly, the PLCA rate-latency service curve is given by

$$\beta^{h}_{\text{PLCA}}(t) = \beta_{R^{h},T^{h}}(t) = \frac{q^{h,\min}}{q^{h,\min} + Q^{h,\max}} \cdot C \cdot \left[t - \frac{Q^{h,\max}}{C} \right]^{+}.$$

□

We provide a Network Calculus modeling for deriving a valid yet conservative performance bound given all data flows competing for the half-duplex PLCA multidrop access, i.e., for service curve $\beta^{h}_{\text{PLCA}}(t)$.

Higher cross-traffic PLCA service in the multidrop and shorter guaranteed windows in TAS can lead to an ST frame to miss its window. In the worst-case, an ST frame may be sent in its TO of the next PLCA cycle. So such ST frame

may wait all the cross-traffic frames be sent first for then be transmitted in still current guaranteed window. Thus, for a proper integration of TAS with PLCA, the transmissions of cross-traffic (regardless of their priorities) and transmission of the ST frame from P_m in the multidrop must be fit into any guaranteed window for P_m. That is, the following condition must be true

$$\frac{Q^{h,\max} + q^{h,\max}}{C} \leq \min_{0 \leq i \leq N^h_{W,P_m}-1} \left\{ L^{h,i}_{GW,P_m} \right\},$$

otherwise, an ST frame can miss its window.

In addition to the issue of transmissions length, the model reveals the main problem of the current lack of proper integration with TAS and PLCA: PLCA is not aware of TSN priorities. So, while TAS provides traffic prioritization in an Ethernet interface, such prioritization is not used for the multidrop access. That is, PLCA enables fair access among interfaces, but allows that the transmissions of lower priority traffic from other interfaces occur before the transmission of higher priority traffic from the current interface.

C. End-to-end Worst-Case Delay

An ST flow, denoted as $\tau^{ST}_{P_m}$, with periodic transmission of frames with maximum length $l^{\max}_{P_m}$ in periods with length T_{P_m} is constrained by a leaky-bucket arrival curve

$$\alpha^{ST}_{P_m}(t) = \begin{cases} \frac{l^{\max}_{P_m}}{T_{P_m}} \cdot t + l^{\max}_{P_m}, & t > 0 \\ 0, & t \leq 0. \end{cases}$$

An ST flow $\tau^{ST}_{P_m}$, which originates from an end system (ES), may traverse some switches (SW), and finally is destined to another ES. The end-to-end delay for such flow is the sum of the delays in all devices in the flow route path. So the delays in the source ES and in all switches in the route path must be computed.

The end-to-end delay a frame suffers when it crosses an Ethernet switch is formed by the following components [41]:

- d_{proc}: caused by processing such as storing the receiving frame, checksum verification, and forwarding to the output interface by the switching fabric;
- $d_{\text{q\&t}}$: caused by the queuing and transmission processes in an output interface.

Besides these components, there is the d_{prop} delay caused by bit propagation on the wire. For instance, a 10-meter in-vehicle Ethernet cable has a delay of 50 ns due to the propagation speed of $2 \cdot 10^8$ m/s.

The delay $d_{\text{q\&t}}$ is the most relevant delay component to be taken into account. Input and switching fabric features have a known, small delay d_{proc}, and previous modelings assume the d_{prop} delay as negligible [12], [17], [42]. The upper bound value for d_{proc} delay is denoted by D_{proc}. Fig. 9 shows an Ethernet switch with two interfaces and the delay components suffered by a frame.

Fig. 10 depicts an Ethernet network with mixed link types and shows Network Calculus servers' locations and connections according to technologies chosen. In the figure, all flows are originated from end system ES1 and destined to ES4. All

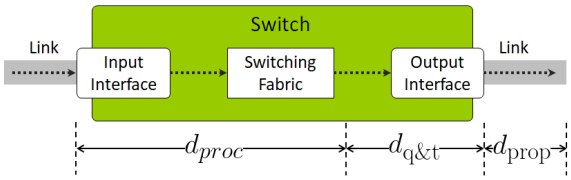

Fig. 9. Example of a basic Ethernet switch model with two interfaces and its delay components.

servers are connected accordingly to the output interface in the flow route path in a multi-hop switched network.

Depending on the Ethernet technology chosen (i.e., TAS only or both TAS and PLCA), the delay in an output interface can occur in two modes, which are shown in Fig. 10. For instance, in that figure, interface eth1 (blue rectangle) of SW1 runs TAS only, and interface eth0 (yellow rectangle) of ES1 runs both TAS and PLCA. There is a server for each priority queue and one server for PLCA, where $\beta^h_{P_m}$ denotes the servers for the priority queues $P_m, m \in [0..7]$ in the MAC layer regarding TAS, and β^h_{PLCA} denotes the server in the PHY layer regarding PLCA.

For an ST flow $\tau^{ST}_{P_m}$ constrained by its arrival curve $\alpha^{ST}_{P_m}$, the delay components in the output interface of all devices in the flow path are:

$$D^h_{P_m} = h(\alpha^{ST}_{P_m}, \beta^h_{P_m}),$$
$$D^h_{\text{PLCA}} = h(\alpha^{ST}_{P_m}, \beta^h_{\text{PLCA}}),$$

where $h(\alpha, \beta)$ denotes the maximum horizontal deviation between α and β computed as shown in Theorem 2, $D^h_{P_m}$ denotes the delay bound for priority P_m regarding the TAS of interface h, and D^h_{PLCA} denotes the delay bound regarding the half-duplex PLCA multidrop access from interface h.

Thus, the delay for an ST flow $\tau^{ST}_{P_m}$ of priority P_m in an output interface h that runs TAS is given by

$$D^h_{\text{q\&t}} = \begin{cases} D^h_{P_m} & \text{if } h \text{ runs TAS only} \\ D^h_{P_m} + D^h_{\text{PLCA}} & \text{if } h \text{ runs both TAS and PLCA,} \end{cases}$$

where $D^h_{\text{q\&t}}$ denotes the delay bound on output interface h of an Ethernet device. When the device is an ES, such delay is denoted by $D^{ES,h}_{\text{q\&t}}$, whereas when it is a SW, such delay is denoted by $D^{SW,h}_{\text{q\&t}}$.

An ordinary solution for calculating the worst-case end-to-end delay for the i-th ST flow $\tau^{ST}_{P_m,i}$ is to apply the Total Flow Analysis, where the delay bound is computed as the sum of the delay in each hop in its path, i.e., delays in the source ES and all switches in its path:

$$D_i = D^{ES,h}_{\text{q\&t}} + \sum_{SW \in r(\tau^{ST}_{P_m,i})} \left(D^{SW,h}_{\text{q\&t}} + D_{proc} \right), \qquad (11)$$

where $r(\tau)$ returns the set of switches in the route path of flow τ [17].

As shown in Fig. 10, D_{proc} is represented by a Network Calculus server modeled by a Pure Delay function $\delta_{D_{proc}}(t)$. Then there is a $\delta_{D_{proc}}$ for all flow paths inside the switch to indicate that, independently, of the internal path, all flows will suffer a delay bound of D_{proc} before they arrive at the output interface.

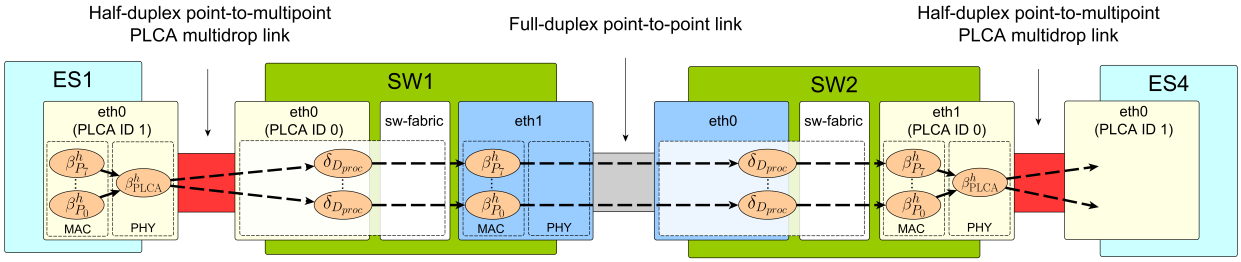

Fig. 10. Example of an Ethernet TSN network using both Ethernet TSN full-duplex point-to-point link and Ethernet TSN half-duplex PLCA multidrop links. All servers are depicted as ellipses and dashed arrows depict all the possible paths for the flows from end systems ES1 to ES4 by crossing both switches SW1 and SW2.

However, as one can see in Fig. 10, from SW1 to SW2 there are servers connected in tandem in separated paths. That is, flows of different priorities traverse different servers in their paths. Thus, in a multi-hop network with point-to-point links, the enhanced analysis techniques can take advantage of server in tandem to achieve lower end-to-end delay bounds compared to an archaic analysis such as Total Flow Analysis.

D. Choosing a Network Calculus Analysis

The modeling alternative can enable various Network Calculus analyses. In particular, the decision to approximate staircase curves with rate-latency curves further allows the model to fast and accurate Network Calculus analyses implemented in the DNC tool [31].

The baseline work [12], which focuses solely on TSN, applies the Total Flow Analysis (TFA). TFA derives, however, overly pessimistic delay bounds when analyzing sequences of servers as it never applies the beneficial (min,+)-convolution.

In a multi-hop Ethernet TSN network, we naturally may obtain multiple Network Calculus server locations in sequence per device. Therefore, we provide results from the so-called Separate Flow Analysis (SFA). Our modeled systems rely on the FIFO multiplexing with a fixed choice for θ, for which we compute the left-over service curve as described in Definition 1. Then, as described in Definition 3, the left-over service curves along the analyzed flow path are convolved to an end-to-end service curve, which is used for delay bounding. Our bounds outperform most of those of the baseline work, showing the benefit of using an advanced Network Calculus analysis. This is shown in the following section.

IV. Setup and Numerical Results

For the modeling strategy of TAS, we use a TDMA-based linear shape (rate-latency) curve instead of the staircase shape curve used in [12], and a new model for the half-duplex PLCA multidrop: the Single PLCA WRR Server. For the analysis, we use SFA, and FIFO multiplexing instead of TFA as the baseline [12]. The critical ST flows and class-based scheduling dataset used in this paper are the same as the baseline work [12], as well as the simple (token-bucket-based) arrival curves. Such a dataset contains windows overlappings. For assuring a base for comparison, in this paper we use the same class-based scheduling without modifications. Since a stream-based scheduling is a window scheduling with no overlappings, so a class-based modeling can be applied in both stream-based or class-based schedulings.

There are four experiments with distinct GCL scheduling cases, which result in a total of 13 GCL scheduling dataset cases, as shown in Table II. Those dataset cases cover several scenarios of guaranteed windows. They are the same as baseline [12, Section VI-A]. All dataset cases have 13 ST flows. The source, destination, and deadlines of the flows are equal for all dataset cases, and they are shown in Table III.

TABLE II
Description of the Scheduling Cases.

Experiment	Description	Number of scheduling cases
1	Different overlapping scenarios	4
2	Different lengths of open window	3
3	Different open-close cycles	3
4	Different priority assign	3

TABLE III
Source, destination and frame size (in bytes) of flows, transmission cycle (in μs), and deadline (in μs). For the sake of comparison, the flows are the same as in [12] for all scheduling cases. End-System (ES) device positions are shown in Fig. 11. The highlighted flow tt11 is the flow of interest which is named as τ_{TT_1} in the baseline work [12]. Depending on the experiment, the transmission cycle of the flow of interest can be 100, 250, or 350 μs.

Flow	Source	Dest.	Frame size (bytes)	Transm. cycle (μs)	Deadline (μs)
tt1	ES1	ES4	400	250	58972
tt2	ES2	ES5	400	250	114419
tt3	ES3	ES6	400	250	56935
tt4	ES1	ES2	400	250	170198
tt5	ES2	ES3	400	250	34481
tt6	ES3	ES1	400	250	11709
tt7	ES2	ES3	400	250	352023
tt8	ES3	ES5	400	250	23165
tt9	ES2	ES6	400	250	35879
tt10	ES1	ES5	400	250	8908
tt11	**ES2**	**ES6**	**400**	**100, 250, or 350**	**8908**
tt12	ES1	ES2	400	250	8908
tt13	ES3	ES6	400	250	8908

We provide two different combinations of modeling and analysis, named MA1 and MA2, and compare them to the results of the baseline work [12]. Flow tt11 is the flow

TABLE IV
NETWORK SETUP FOR MA1 AND MA2.

	MA1	MA2
ES link type	Full-duplex point-to-point links only as in the baseline work. It is shown in Fig. 11 (a).	Half-duplex PLCA multidrop, as shown in Fig. 11 (b), using the modeling strategy Single PLCA WRR Server for multidrop with all WRR weights equal to 1 (i.e., PLCA normal mode).
ST flows	Same as in the baseline work.	Same as in the baseline work.
GCL config.	Same GCL configuration as the baseline work.	A GCL configuration for the half-duplex interface, which resulted from a merge of three GCL configurations of full-duplex interfaces.

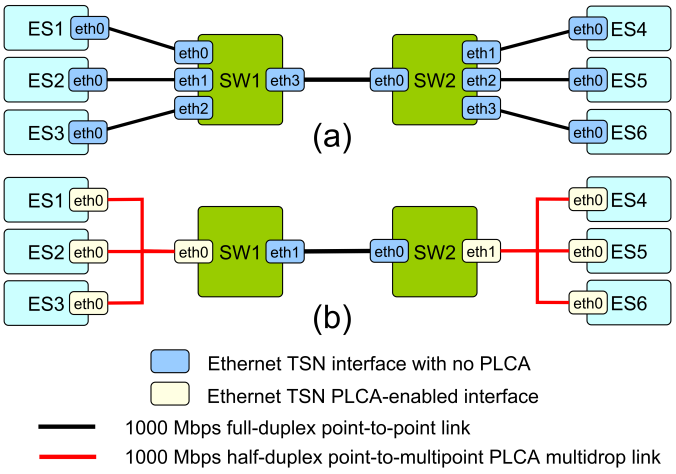

Fig. 11. (a) Ethernet network using 1000 Mbps full-duplex point-to-point links only for connecting all devices as in [12, Fig. 12]. (b) Ethernet TSN network with a 1000 Mbps full-duplex point-to-point link to connect switches SW1 and SW2 and hypothetical 1000 Mbps half-duplex point-to-multipoint PLCA multidrop links to connect the end systems.

of interest of the baseline work, then the results named as Baseline, MA1, and MA2 concern such flow. Both MA1 and MA2 analyses were done in an Ethernet-TSN performance analysis tool developed by us[2], which is an extension of DNC [31]. MA1 and MA2 are explained in Table IV.

For enabling half-duplex PLCA multidrop analysis MA2, we created two multidrop links, as indicated in Fig. 11 (b). These two hypothetical 1000 Mbps half-duplex PLCA multidrop links resulted from the merge of the 1000 Mbps full-duplex point-to-point links between the switch (SW) and the end systems (ES) from Fig. 11 (a). The full-duplex links ES1-SW1, ES2-SW1, and ES3-SW1 become a half-duplex multidrop link composed of ES1, ES2, ES3, and SW1. Similarly, the full-duplex links SW2-ES4, SW2-ES5, and SW2-ES6 become a half-duplex multidrop link composed of SW2, ES4, ES5, and ES6.

Since in both switches of Fig. 11 (b) three of their Ethernet interfaces become a single Ethernet interface connected to the multidrop, the three independent GCL configurations of the switch interfaces were also merged, resulting in a single GCL configuration containing all windows from these three Ethernet interfaces. Also, flows tt4 (ES1 to ES2), tt5 (ES2 to ES3), tt6 (ES3 to ES1), tt7 (ES2 to ES3), and tt12 (ES1 to ES2), which had to traverse two point-to-point links in the network shown in Fig. 11 (a), now have to traverse a single multidrop link in the network shown in Fig. 11 (b). That is, the path for those flows becomes a single-hop path because the source ES and destination ES are now linked in the same multidrop.

The sum of flows bandwidth exceeds 10 Mbps. As shown in Table III, all flows have the burst length of 400 bytes with the transmission cycle of 250 μs (in most cases), which results in an individual flow bandwidth of 1.6 Mbps. Thus, the sum of bandwidth of all 13 flows is 20.8 Mbps. So, we assume a hypothetical "1000BASE-T1S", i.e., 1000 Mbps half-duplex PLCA multidrop links instead of using 10BASE-T1S links. We also calculate the delay change that happens when full-duplex point-to-point links of same speed (i.e., 1000 Mbps) are replaced with the hypothetical half-duplex multidrop links.

Both MA1 and MA2 use SFA and FIFO multiplexing, as well as rate-latency service curves and token-bucket arrival curves. As in [12], D_{proc} is neglected.

TABLE V
COMPARISON OF MA2 AND MA1 REGARDING THE FLOW OF INTEREST (I.E., TT11). VALUES ARE IN μS.

Experiment	Case	MA1	MA2	MA2 - MA1	$\frac{\text{MA2}-\text{MA1}}{\text{MA1}}$
1	1	1004.4	1215.2	210.7	21.0%
	2	1096.1	1315.5	219.4	20.0%
	3	1055.5	1316.1	260.6	24.7%
	4	1630.3	∞	-	-
2	1	1389.8	1636.6	246.8	17.8%
	2	1096.1	1315.5	219.4	20.0%
	3	888.9	1090.5	201.5	22.7%
3	1	3469.9	3842.1	372.2	10.7%
	2	1096.1	1315.5	219.4	20.0%
	3	839.3	1065.0	225.6	26.9%
4	1	1116.9	1334.9	217.9	19.5%
	2	1096.1	1315.5	219.4	20.0%
	3	1551.6	1979.7	428.1	27.6%

TABLE VI
COMPARISON OF MA1 AND BASELINE REGARDING THE FLOW OF INTEREST (I.E., TT11). VALUES ARE IN μS.

Experiment	Case	Baseline (BL)	MA1	MA1 − BL	$\frac{\text{MA1}-\text{BL}}{\text{BL}}$
1	1	1036.6	1004.4	-32.2	**-3.1%**
	2	1287.8	1096.1	-191.7	**-14.9%**
	3	1173.0	1055.5	-117.5	**-10.0%**
	4	2309.6	1630.3	-679.3	**-29.4%**
2	1	1791.1	1389.8	-401.3	**-22.4%**
	2	1287.8	1096.1	-191.7	**-14.9%**
	3	744.7	888.9	144.2	19.4%
3	1	2527.8	3469.9	942.1	37.3%
	2	1287.8	1096.1	-191.7	**-14.9%**
	3	474.0	839.3	365.3	77.1%
4	1	1177.9	1116.9	-61.0	**-5.2%**
	2	1287.8	1096.1	-191.7	**-14.9%**
	3	2014.0	1551.6	-462.4	**-23.0%**

[2]Our extension of [31] is available on https://github.com/davidalain/DNC-EthernetTSN_IEEE_TCOM_code

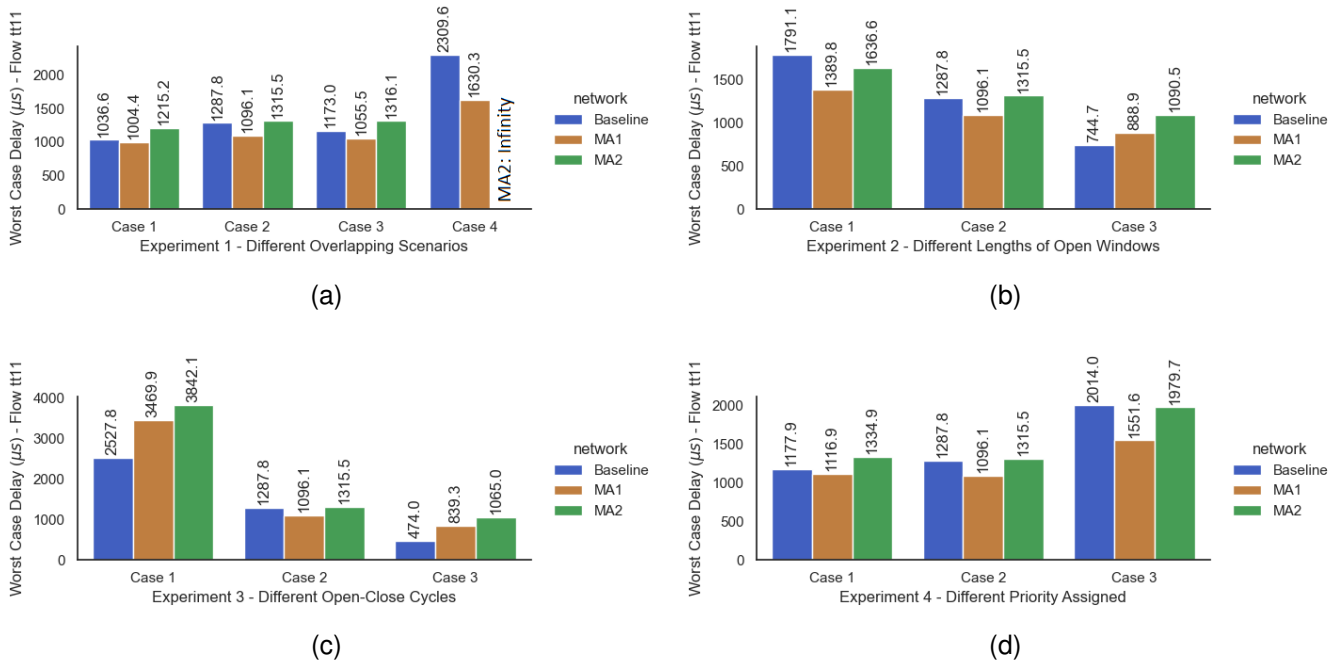

Fig. 12. Comparison of Baseline, MA1, and MA2 for the worst-case delay of the flow of interest in the four experiments with their different scheduling cases: (a) Experiment 1, (b) Experiment 2, (c) Experiment 3, and (d) Experiment 4.

Fig. 12, and Tables V and VI show the worst-case delay bounds and comparison of our solutions MA1 and MA2 with the baseline work [12, Table 2] regarding the flow of interest (i.e., tt11). As shown in Table V, by taking MA1 as a reference and comparing MA1 to MA2, i.e., by replacing two full-duplex point-to-point links with two half-duplex PLCA multidrop links in the path of the flow of interest, we show that the increase in the worst-case delay ranges from 10.7% to 27.6%, which is still below the deadline. Also, as shown in Table VI, by taking Baseline as reference and comparing MA1 to Baseline, i.e., by applying our alternative modeling and analysis solutions for the flow of interest in the same network scenarios, we reduced the worst-case delay bound in 10 of 13 scheduling cases (highlighted in bold), showing the benefits of using a better Network Calculus analysis. For those with lower delay bounds, such reduction reaches up to 29.4%. However, for those with higher delay bounds, such increasing reaches up to 77.1%, yet with all delay bounds under the deadline. As it can be seen in Fig. 12, the modeling and analysis of MA1 outperform the Baseline in 10 of 13 GCL scheduling cases.

Results for worst-case delays for all flows regarding MA1 and MA2 in all scheduling cases of Experiments 1 to 4 are shown in Figs. 13 (a) to 13 (d), respectively. Flows tt4, tt5, tt6, tt7, and tt12 have a lower worst-case delay in all scheduling cases for MA2 than for MA1. By calculating the worst-case delay decrease for these flows (i.e., $\frac{\text{MA2}-\text{MA1}}{\text{MA1}}$), the decrease ranges from 16.7% to 33.2%. Such flows traverse a single-hop multidrop only in the multidrop network scenario (i.e., MA2), rather than two hops of point-to-point links in the point-to-point network scenario (i.e., MA1). That is, a single-hop PLCA multidrop link provides a lower delay bound than two hops of full-duplex point-to-point links.

Also, all flows of all cases in MA1 and MA2 meet their deadlines, except those with infinity delay bound. Table III show the deadline of all flows. As shown in Fig. 13 (a), there are flows with an infinity delay bound, which is explained as follows. In MA1 Case 4, flows tt7 and tt8 do not have bounded delays, denoted by infinity. That occurs because such flows have a frame length of 400 bytes, requiring at least a guaranteed window with a length of 3.2 μs in their respective priority queues in the flow path. However, the GCL scheduling for MA1 Case 4 has hops in the flow path with windows that result in zero-length guaranteed windows. Therefore, it is impossible to provide end-to-end data communication for those flows.

Nevertheless, most worst-case delay results of the MA2 Case 4, including the flow of interest (i.e., tt11), have unbounded delay. There is no available service for the flow to enable it to traverse the half-duplex PLCA multidrop. That is, the GCL scheduling of this case is not compatible with being used on a half-duplex PLCA multidrop with such cross-traffic. That scheduling cases confirm the importance of choosing a proper GCL scheduling to achieve a compliant integration of TAS and PLCA.

V. Conclusion

Previous works on modeling and analysis of Time-Sensitive Networking just considered full-duplex point-to-point links in the whole network. However, a revamped interest in single-pair half-duplex Ethernet multidrop, especially in the automotive and industrial domains (i.e., 10BASE-T1S), raised the need to include TSN and hence the worst-case timing analysis for frame delivery in such half-duplex PLCA multidrop networks.

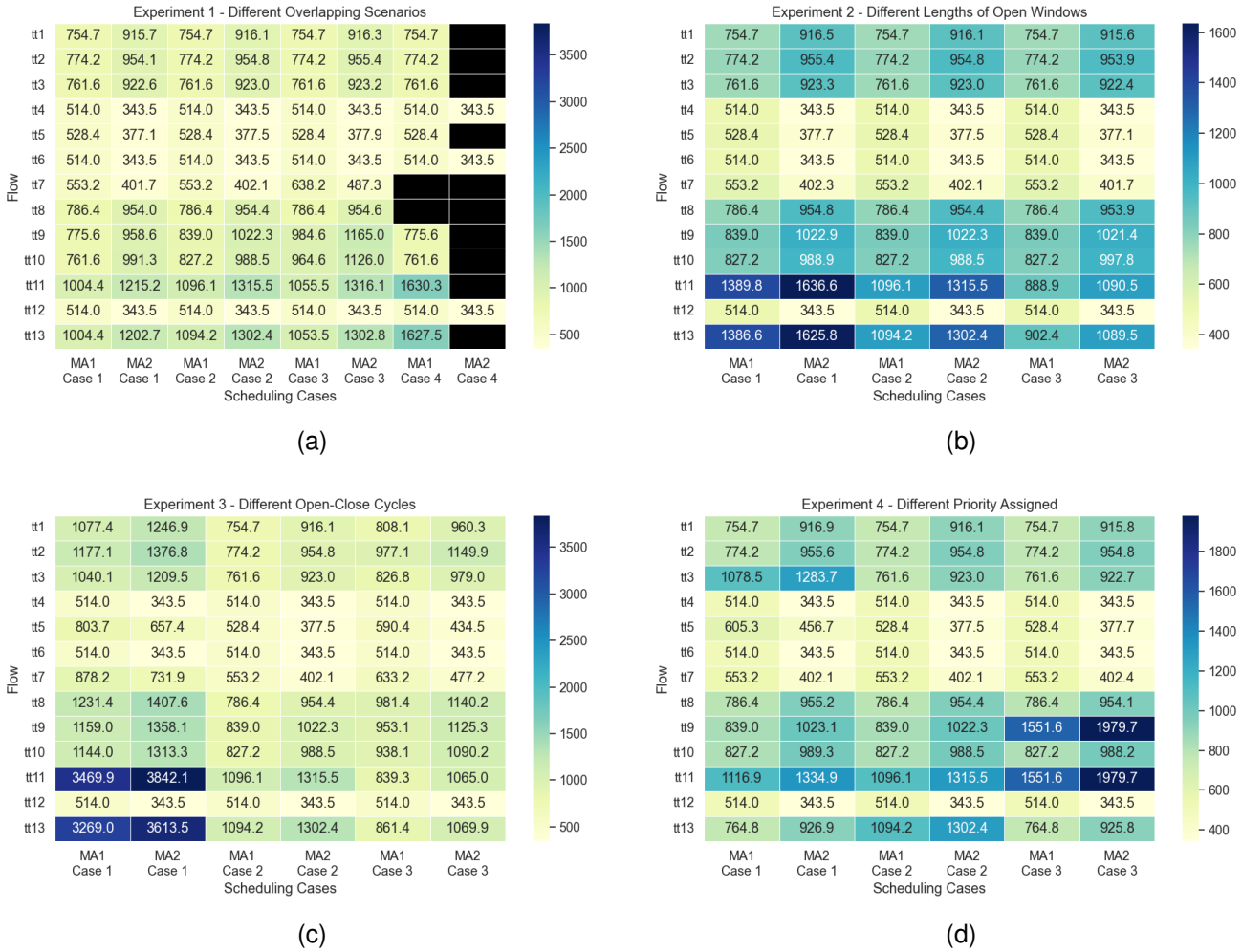

Fig. 13. Results of worst-case delay for all flows regarding MA1 and MA2 for: (a) Experiment 1, (b) Experiment 2, (c) Experiment 3, and (d) Experiment 4. All values are in μs. Unbounded values are denoted by black boxes.

This paper provides modeling and analysis using Network Calculus for the Time-Aware Shaper (TAS) protocol over an Ethernet multidrop network with Physical Layer Collision Avoidance (PLCA). For the modeling strategy, we propose a linear shape (rate-latency) curve for TAS, and a new model for the integration of TAS with the half-duplex PLCA multidrop: the Single PLCA WRR Server modeling. We use Separate Flow Analysis (SFA) and First-In-First-Out (FIFO) multiplexing for the analysis. The modeling and analysis presented in this paper can help networking engineers to provide a proper integration of TAS and PLCA.

We show through numerical calculations that the increase in the worst-case delay bound of the flow of interest ranges from 10.8% to 27.8%, which still meeting its deadlines, in a network scenario where the flow of interest traverses two half-duplex PLCA multidrop links and a single full-duplex link when compared to a network scenario where the flow of interest traverses three point-to-point Ethernet links. However, we show that a single-hop half-duplex PLCA multidrop link provides a lower delay bound than two hops of full-duplex point-to-point links for all flows in that scenario. The reduction in the worst-case delay for these flows ranges from 16.7% to 33.2%.

Nevertheless, our solution that makes use of more advanced Network Calculus reduces the worst-case delay bound in 10 of 13 GCL scheduling cases in full-duplex point-to-point network scenario, i.e, the same network of the baseline work. However, in contrast to the baseline work, we provide alternative modeling and analysis, in which we can reduce delay bounds by using simple curves with accurate analysis rather than accurate curves with an archaic analysis.

With modeling using WRR presented in this paper, the Interleaved WRR constitutes a potential future work direction for QoS in a possible PLCA extension [43]. Future works include: a) The proposal of an alternative Network Calculus modeling for the integration of 10BASE-T1S with TAS covering both guaranteed service from TAS and PLCA without assuming an additional server for the PLCA service; b) Apply improved analysis such as Least Upper Delay Bound (LUDB) [36] to reach less pessimistic bounds; c) Provide both end-to-end delay and jitter bounds; and d) Provide a comparison analysis of 10BASE-T1S with the recent 10 Mbps CAN XL (Controller Area Network Extra Long) [44].

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