Diamond Standard 108Mini Controller

A Small, Low-Power, Cache-less RISC CPU

Product Brief

FEATURES

- Small, low power 32-bit RISC controller core
- Cache-less processor with memory protection unit
- 5-stage pipeline
- Dhrystone 2.1: 1.34 DMIPS/MHz
- 24/16-bit ISA with modeless switching
- Iterative 32x32 multiplier and 32-bit integer divider
- Separate instruction and data memory interfaces
- Dual local data RAMs
- 2x32-wire GPIO ports for direct control and monitoring of peripherals
- Integrated interrupt controller with 22 interrupts and 6 priority levels
- Three integrated timers
- On-chip debugging hardware
- Embedded trace support
- Comprehensive software development environment
- AHB-lite and AXI bridges

BENEFITS

- Low die area due to small core area and high code density
- Deterministic real-time operation through optional single-cycle local instruction and data SRAMs
- Achieve high frequency: >900 MHz in 45gs process
- High arithmetic and DSP performance
- No memory contention between instructions and data
- Dual data RAMs allow ping-pong access —read/write one, DMA into other
- Fast and flexible interrupt handling
- Drop into existing AMBA™-based SOCs

A Solid, Low-Power Performer

The Diamond Standard 108Micro controller gives you the performance you need at very low power. It requires just 0.019 mW/MHz in a 45gs low-power process.

Achieves Performance Levels of Much Larger CPUs

The Diamond Standard 108Mini CPU is a small, fully synthesizable, cache-less 32-bit RISC core with tightly coupled local instruction and data memories, a rich interrupt architecture, and high arithmetic and DSP performance. It enables SOC architects to quickly integrate an efficient CPU into their designs. The Diamond 108Mini features class-leading low-power consumption for portable applications.

Although the Diamond 108Mini is smaller in die area than comparable 32-bit CPUs, its performance is extremely high: >700 MHz in a 65gp and >900 MHz in 45gs process technology while achieving 1.34 Dhrystone MIPS/MHz. By modelessly switching between 24– and 16-bit narrow instructions, it achieves much higher code density than other 32/16-bit architectures. It also achieves high performance on DSP applications and engine and motor control applications because of the built-in 32x32 multiplier and 32-bit integer divider.

The Diamond 108Mini features innovative I/O that allows data to be directly streamed in and out of the processor without going over the main data bus. The two 32-wire GPIO (general-purpose I/O) ports allow direct control and monitoring of peripherals via simple instructions built into the CPU.

The Diamond Standard 108Mini delivers fast and flexible interrupt handling with low latency and a rich interrupt architecture. The processor has deterministic behavior for applications with hard real-time constraints. 32 base registers are windowed 16 at a time, which enables much faster context switching due to reduced stack operations. Local single-cycle SRAM allows time-critical code to be placed near the CPU. Dual local data SRAMs enable processor access to one bank of RAM while an external DMA operation can operate on the other bank. Separate instruction and data memory interfaces lead to lower contention than unified interface architectures.

While small and low power, the Diamond 108Mini achieves the performance levels of much larger CPUs.

Instruction Set Architecture

The Diamond Standard Series implements the Xtensa® Instruction Set Architecture (ISA) a 32-bit RISC architecture featuring a compact instruction set optimized for embedded designs.

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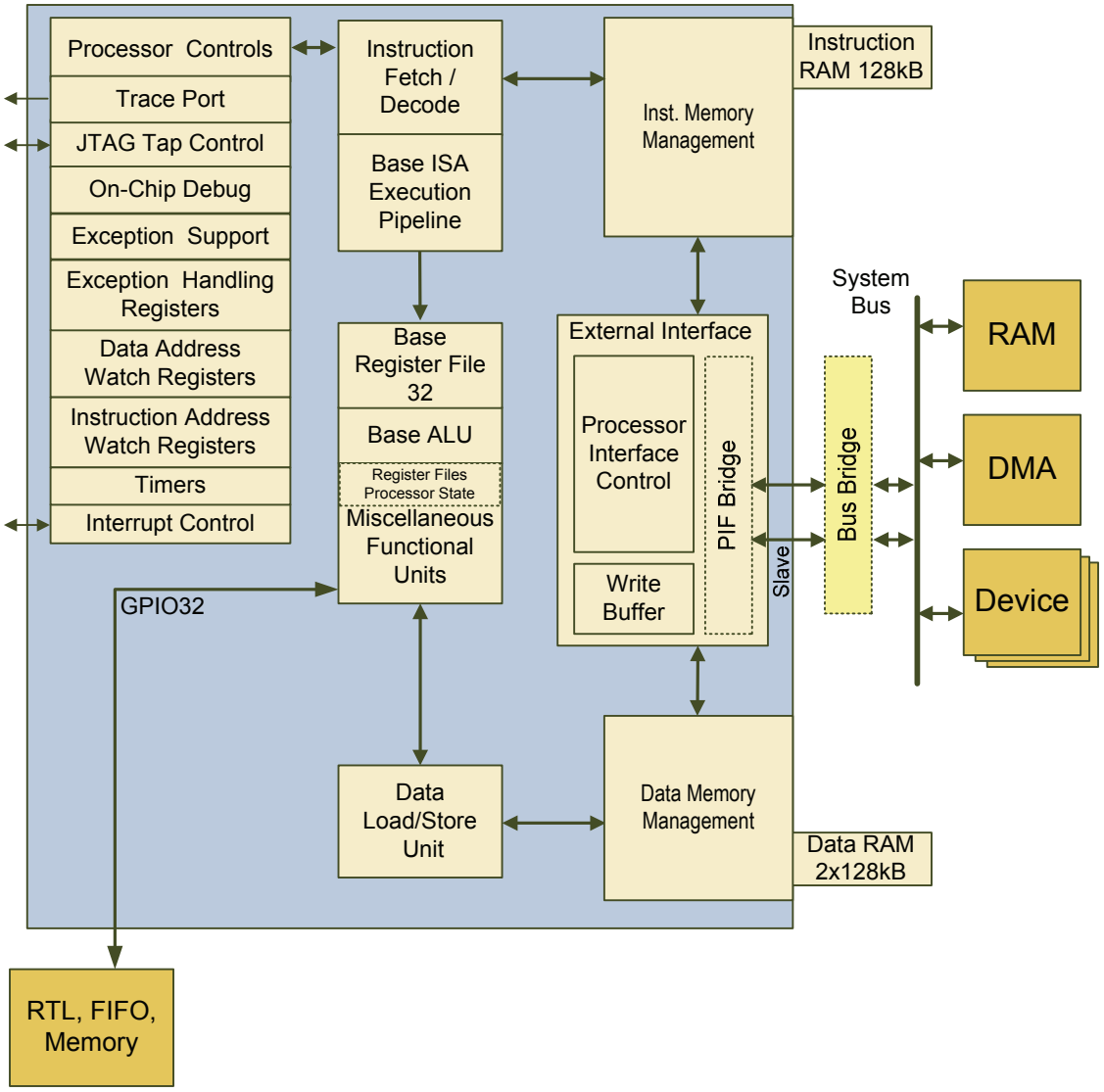

The Diamond Standard 108Mini

Instruction Set Architecture (cont.)

The Xtensa ISA employs 24-bit instructions with 16-bit narrow encodings for the most common instructions. These 16-and 24-bit instruction words are freely intermixed to achieve higher code density without compromising application performance. The Xtensa ISA thus optimizes the size of the program instructions by minimizing both the static number of instructions (the instructions that constitute the application program) and the average number of bits per instruction.

The use of 24- and 16-bit instruction words and compound instructions, the richness of the comparison and bit-testing instructions, zero-overhead-loop instructions, register windowing, and the use of encoded immediate values all contribute to the Diamond processors' small code size. The 24-/16-bit Diamond processor ISA enables designers to achieve 25% to 50% lower code size compared to conventional 32-/16- bit ISA-based RISC cores.

Reducing code size results in smaller memory sizes and lower power dissipation – key parameters in cost-sensitive, highly integrated SOC designs.

The Xtensa ISA also provides powerful compare-and-branch instructions, zero-overhead loops, and bit manipulations including funnel shifts and field-extract operations.

Comprehensive Software Tool Support

A full-featured development environment – the Xtensa Xplorer™ – provides a graphical user interface (GUI) to all code development tools. The compiler toolchain and instruction set simulator (ISS) are available through the GUI in addition to performance modeling tools. Based on the Eclipse framework, Xtensa Xplorer allows developers to quickly evaluate code on the pipeline-accurate ISS and interface to emulation and hardware development boards. Xtensa Xplorer serves as the cockpit for the entire development .

Tensilica's XCC C/C++ compiler is an optimizing compiler that employs sophisticated multi-level optimizations to increase code execution performance and reduce code size. Also included in the Xtensa Xplorer environment are a software project manager, code profiling tools, source code editor, debugger, performance-modeling tool, the Xenergy™ energy estimation tool, the cache performance explorer, and a number of graphical visualization tools. Tensilica also provides both a C-based modeling environment called XTMP, as well as SystemC models of the Diamond processors. For fast-functional simulation, Tensilica offers TurboXim for a 40-80x faster simulation than the ISS. See Tensilica's Software Developer's Toolkit product brief for more information.

Specifications

	65gp		65lp		45gs		40lp	
Flows:	**High-Speed**	**Low-Power**	**High-Speed**	**Low-Power**	**High-Speed**	**Low-Power**	**High-Speed**	**Low-Power**
Post-route cell area (mm^2)	0.226	0.131	0.220	0.126	.139	0.082	0.152	0.0845
Speed (MHz) post Prime Time	727	58	442	57	923	58	608	58
Post-Route Power (mW/MHz)	0.052	0.033	0.062	0.041	0.029	0.019	0.043	0.026

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