IQ Modulator and Practical Considerations

EE 340: Prelab Reading Material for Experiment 4
August 17, 2015

Any arbitrary passband signal $s_p(t)$ with center frequency f_c can be written as

$$s_{\rm p}(t) = s_I(t)\cos(2\pi f_c t) - s_Q(t)\sin(2\pi f_c t) = {\rm Re}\left\{s(t)e^{j2\pi f_c t}\right\},$$

where $s(t) = s_I(t) + js_Q(t)$ is a complex baseband signal consisting of the two independent real baseband signals $s_I(t)$ and $s_Q(t)$. The signal $s(t)$ is also called the complex envelope of $s_p(t)$. Therefore, an IQ modulator is typically used for upconverting a complex baseband signal to a passband IF (intermediate frequency) or RF (radio frequency) signal, as shown in Fig. 1a. In a similar way, an IQ demodulator is used for downconverting a passband RF or IF signal to the complex baseband signal, as shown in Fig. 1b.

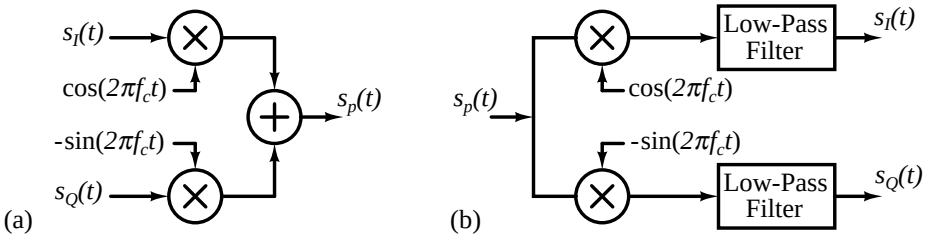

Figure 1: Flowgraph of (a) an IQ modulator, and (b) an IQ demodulator.

Among the hardware used in your experiments, the RTL-SDR dongle basically implements an IQ demodulator, which finally gives out the digitized versions (obtained using analog-to-digital converters) of the baseband signals to the computer through the USB port. For implementing the IQ modulator, the printed circuit board shown in Fig. 2 has been developed in-house (i.e. in the Wadhwani Electronics Lab). In this experiment, you will be using this board for carrying out complex multiplication in hardware to obtain arbitrary passband signals.

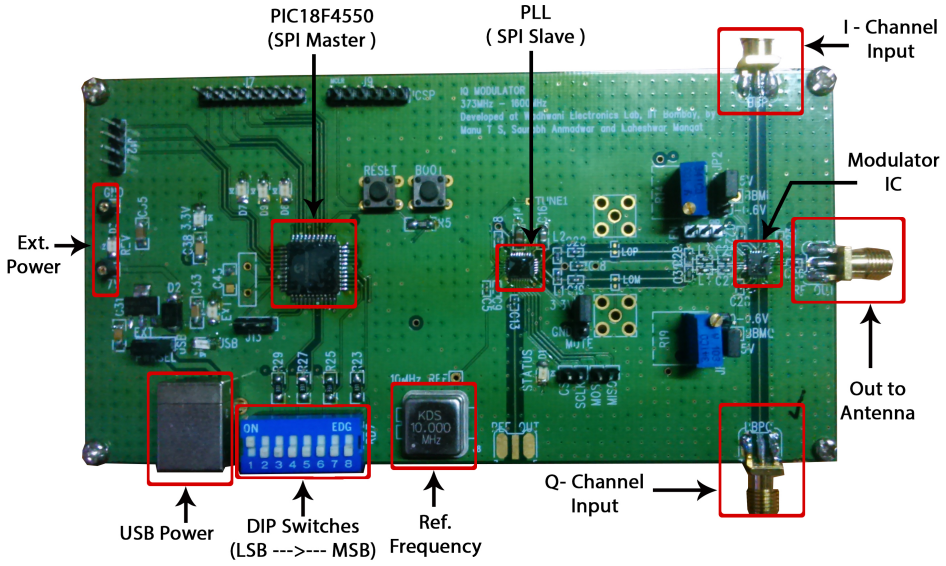

Figure 2: The IQ modulator board developed at the Wadhwani Electronics Lab.

1 The IQ Modulator Board

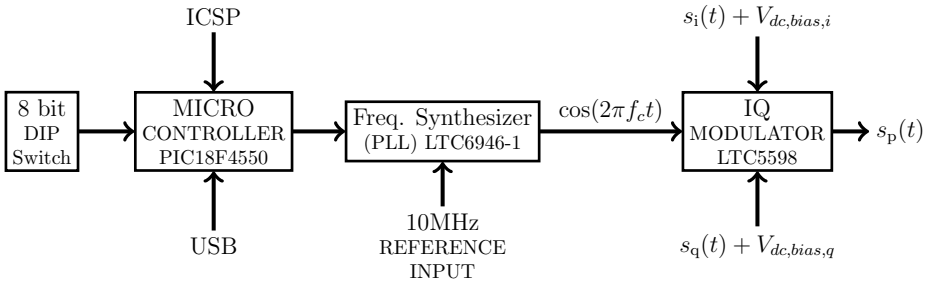

Figure 3: The block diagram of the IQ modulator board.

The block diagram of the IQ modulator board is shown in Fig. 3. It consists of several components, among which, the following ones are worth mentioning:

a. **The IQ Modulator IC**: In these experiments, the role of this IC is to upconvert the analog baseband I and Q signals to the RF carrier frequency. The local oscillator (LO) signal going to the IQ modulator, i.e. the carrier frequency signal here, is generated by an on-board frequency synthesizer (i.e. a phase locked loop). Internally in the IQ modulator IC, a poly-phase filter uses the LO signal to generate its 0° and 90° phases. These two phases are multiplied by the analog baseband I and Q signals (which are provided by an external source), respectively, and the resulting signals are combined to obtain the desired passband signal $s_p(t)$ at the output port, as shown in Fig. 3.
Caution: For proper biasing of the internal IQ modulator circuitry, the baseband I and Q signals also have to include DC biases, which should NOT exceed 0.6 V (the nominal DC bias voltage is around 0.45 V).

b. **The Phase Locked Loop (PLL) for Frequency Synthesis**: The main function of the PLL on this board is to generate the LO signal for modulation or upconversion of the baseband signals. The input to the PLL is a fixed 10 MHz clock signal (also called the reference frequency f_{ref}) coming from an on-board crystal oscillator. The PLL IC has a voltage controlled oscillator (VCO) followed by a configurable frequency divider of division ratio N, as shown in Fig. 4. The feedback loop in the PLL ensures that the frequency divider output phase (and hence frequency) exactly matches the reference clock phase (and frequency). The phase error is basically determined by the time difference between the rising edges of the reference clock and the frequency divider output, and should be practically zero when the PLL is locked. For a given f_{ref} and N, the VCO output frequency in a locked PLL is $f_{out} = N f_{ref}$ (prove it yourself). The frequency division factor N is always > 1, but it is possible to achieve effectively a non-integer value of N using some tricks (discussion on these tricks is beyond the scope of this material).

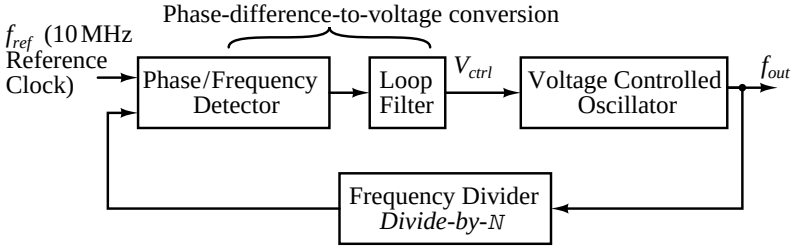

Figure 4: The block diagram of a PLL used as a frequency synthesizer.

Various parameters of the PLL, such as the loop bandwidth, the loop settling behaviour and frequency divider ratios are decided by configuration register bits, which are programmed by an on-board micro-controller. There is also a lock-bit in the PLL. The red "STATUS" LED on the board glows when this lock-bit is "HIGH", which means that the PLL is locked.

c. **The Micro-Controller**: The micro-controller (PIC18F) on the board configures the twelve 8-bit registers of the PLL at the start-up or when the controller is reset. All the 96 bits corresponding to these twelve registers have to be set individually for setting various parameters of the PLL on the board. The controller talks with the PLL through an SPI link, in which, the PLL is the slave and the micro-controller is the master (you will be studying the SPI interface in EE337).

d. **The DIP Switch**: The role of this switch is to set the PLL register bits so as to change the carrier frequency going to the IQ modulator IC. Each group has to use a distinct DIP switch setting so that different groups are using different frequency channels. The DIP switch sets various frequency divider ratios in the PLL, which decides the PLL output frequency. For your group, you will be using the following setting:

$$\texttt{DIP-switch-value} = 2 \times \texttt{<Your Group No.>},$$

which gives the carrier frequency in the form: $f_c = f_{c0} + f_{step} \times$ `<DIP-switch-value>`.

2 Non-Idealities in a Practical IQ Modulator

a. **Carrier Feedthrough:** The multipliers shown in Fig. 1 are implemented using double-balanced mixers (recall Experiment 3). Recall that a single-balanced mixer always has the carrier frequency component at the output, but ideally it is zero in case of a double-balanced mixer, i.e. when the carrier frequency outputs from the two switching pairs perfectly cancel each other. However, DC offsets or device mismatches lead to improper cancellation and the appearance of the carrier frequency component at the double-balanced mixer output as well, as shown in Fig. 5a. This is called LO or carrier feed-through.

In our experiments, the DC bias voltages of the I and the Q channel inputs have to be individually adjusted on the board (manually), to minimize the LO feed-through to the output. This is adjustment is iterative as the feed-through from each channel has to be individually suppressed (feed-through from one channel generally dominates the feed-through from the other channel).

b. **I-Q Imbalance Resulting in Finite Image Rejection Ratio**: If our message signal is $\cos(2\pi f_m t)$ and we wish to carry out single sideband (SSB) modulation, we can use the signals $s_I(t) = \cos 2\pi f_m t$ and $s_Q(t) = \sin 2\pi f_m t$, for the I and the Q channels of the IQ modulator, respectively. This should ideally generate the signal $s_p(t) = \cos 2\pi(f_m + f_c)t$ at the output of the modulator.

However, due to mismatches (or imbalances), the phase and the amplitude of the I and Q channel inputs (or that of the two carrier phases) may not match perfectly. For example, because of mismatches, Q channel input can actually be written as $s_Q(t) = (1+\delta)\sin(2\pi f_m t + \Delta\phi)$, if $s_I(t)$ is unchanged. Because of this mismatch, the output is non-zero at the frequency $f_c - f_m$ in addition to the desired signal at the frequency $f_c + f_m$ as shown in Fig. 5b. The component at $f_c - f_m$ is called the image component. The ratio of power in the desired signal component to the power in the image component is called the Image Rejection Ratio (IRR). If $\delta \ll 1$, $\Delta\phi \ll 1$, and $\Delta\phi$ is expressed in radians, prove yourself that

$$\text{IRR} = \frac{4}{\delta^2 + (\Delta\phi)^2}.$$

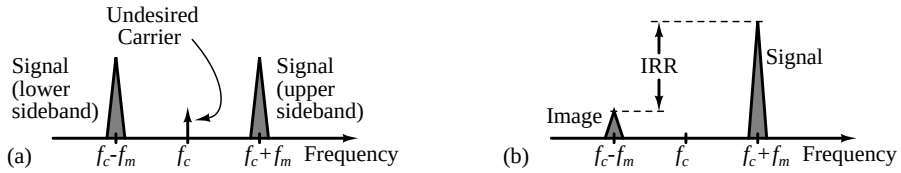

Figure 5: Non-idealities in IQ modulation: (a) Undesired carrier in DSB-SC modulation. (b) Undesired image in SSB modulation.