Clock Timing Synchronization for Data Recovery in Communication Links using Phase Locked Loops (PLLs)

EE 340: Prelab Reading Material for Experiment 8

Clock Synchronization

Systems that are based on digital electronics generally need a clock source, with respect to which all logic blocks operate and data flow takes place. However, when two such systems are connected via a digital communication link (be it wired, wireless or optical), their clocks are generally derived from physically different reference clock sources (such as crystal oscillators). Even if these reference clock sources are meant to generate the same frequency, there may be small offset between their oscillation frequencies (the frequencies can never be precisely same). For example, even if there is 1 Hz frequency offset between two 1 MHz clock sources, their cycles will slip with respect to each other, once in a second. If the data is generated using clock source A at a transmitter is sampled using clock source B, the cycle slips will result in sampling of data erroneously.

Clock synchronization is required to overcome this problem. The receiver knows the approximate clock frequency of the transmitter, but uses a Phase Locked Loop (PLL) to lock to it exactly, and generate a clock locally with exactly same frequency. In addition, clock synchronization may also be used for aligning the clock sampling edges to the centre of data symbol periods, so that data can be sampled with least probability of error. Also, recall the usage of 'Polyphase Clock Synchronization' block in Experiment 7 for the purpose of aligning sampling clock to the center of symbol periods (after applying pulse-shaping filter to the signals).

Phase Locked Loops (PLLs)

A phase locked loop is a feedback loop that adjusts the phase (and frequency) of the oscillator in it to lock to the phase of the incoming clock signal or clock-synchronous data signal. As a result, the oscillator output clock gets synchronized with the incoming data or clock.

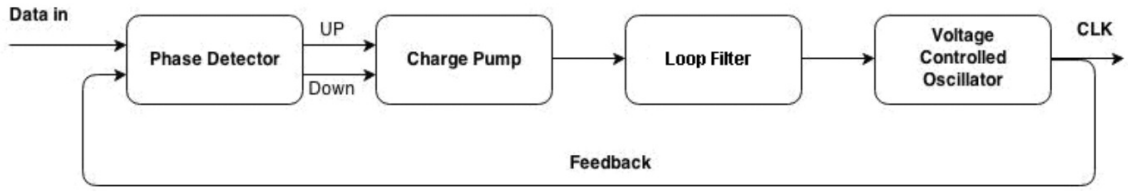

Figure 1: A Phase locked for clock recovery and synchronization

There are several types and uses of PLLs. For example, in addition to use in data symbol timing synchronization (as in the Polyphase Clock Synchronizer in your GNU radio experiments), a PLL can also be used for carrier frequency synchronization (for example in a Costas Loop, that is being used in our SDR dongle based experiments). PLLs can also by used for synthesis of a desired frequency from reference frequency source such as a crystal oscillator (for this a suitable frequency divider is used in the feedback path). For example, the IQ modulator boards you use in the lab, employs a PLL to generate the desired carrier frequency signal from a reference clock.

In a typical PLL, the phases corresponding to clock transitions at various nodes are considered as "phase signals" and the feedback loop tries to match the feedback phase to the incoming phase. The following modules are commonly used in a Phase Locked Loop:

A. *Phase Detector:* The "phase detector" gives an output which depends on the difference between the incoming signal phase (or reference phase) and the feedback signal phase. There can be several types of phase-detectors. Some of them work only for periodic signals, while others can work even for clock synchronous digital data signals.

The phase detector you will be using for synchronizing the clock signal to bit sequences is called the Hogge Phase Detector (PD), as shown in Fig.2. The Hogge Phase detector generates UP and DOWN pulses when and only when there are data transitions. In this PD, the the UP pulse begins with the data transition and the ends at the positive edge of the feedback clock. Therefore, the UP pulse width is dependent on the phase difference between the incoming signal and the clock generated by the VCO (Voltage Controlled Oscillator). On the other hand, the DOWN pulse is a fixed pulse of half-clock cycle pulse width (assuming that the VCO generates clock with 50% duty cycle).

The feedback loop tries make the UP pulse width equal to the DOWN pulse width (in equilibrium), by making their difference equal to zero. This condition ensures that the clock period is equal to the data bit period and the clock positive edges are aligned with the center of the data periods. Since the output duty cycle difference changes from -0.5 to +0.5 as the input phase of the clock shifts by 2π, the gain of a Hogge PD is $1/2\pi$. However, this happens only when there is a transition. Therefore, for random data, in which the probability of transitions is 50%, the Hogge PD gain will be $K_{PD} = 0.5 \times 1/(2\pi) = 1/(4\pi)$.

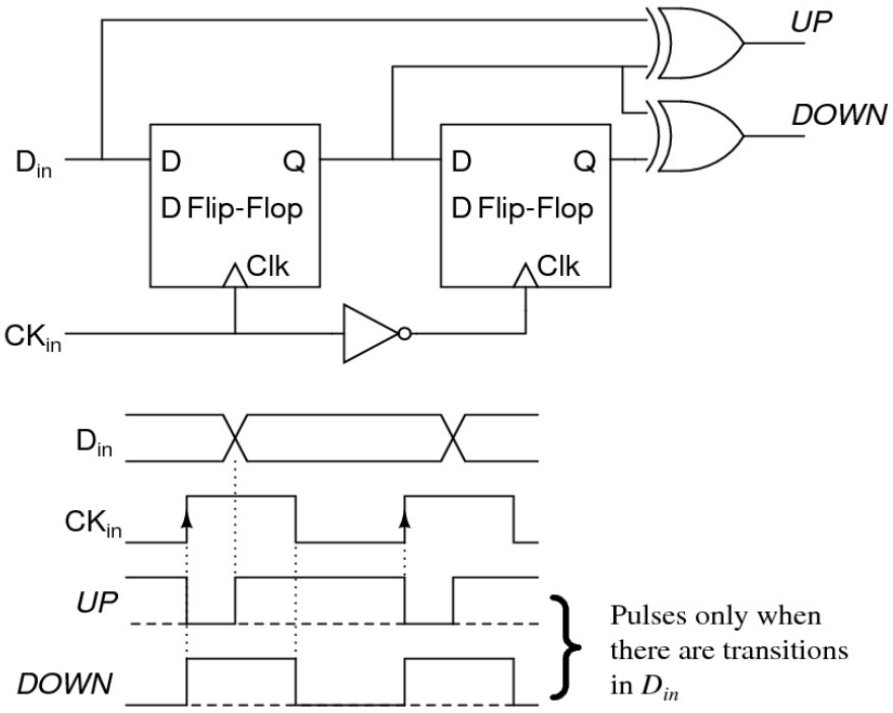

Figure 2: Hogge phase detector and its output waveforms.

B. *Charge Pump:* A charge pump is used when the phase detector produces two pulses (the UP pulse and the DOWN pulse). When the UP pulse is high the charge pump provides current equal to I_{CP} and when the DOWN pulse is high, it draws out current equal to I_{CP}. Therefore, in locked condition, when both the pulses are of equal width, there is no net charge (or average current) provided by the charge pump.

C. *Loop Filter:* The loop filter is meant for storing the charge provided by the charge pump, or for generating analog voltage corresponding to the duty cycle of the pulses provided by a phase detector if a charge pump is not used. The loop filter output voltage controls the frequency of the VCO (hence, it has to reduce ripples on this voltage cause by pulses as much as possible).

D. *Voltage Controlled Oscillator (VCO):* The VCO generates the clock whose frequency changes (roughly) linearly with the input voltage. Therefore, the resultant phase is an integration of

voltage applied at the input (as phase is an integration of frequency). Its gain K_{VCO} is defined as the change in output angular frequency per unit change in applied input voltage and the units are rad.s^{-1} V^{-1}. Therefore, output frequency should be first converted to angular frequency to obtain K_{VCO}, and the transfer function in frequency (or Laplace) domain is written as $K_{VCO}/s(rad.s^{-1}V^{-1})$.

Sometimes, in a PLL based frequency synthesizer, the feedback path also has a frequency divider, which also divides the phase by the frequency division ratio.

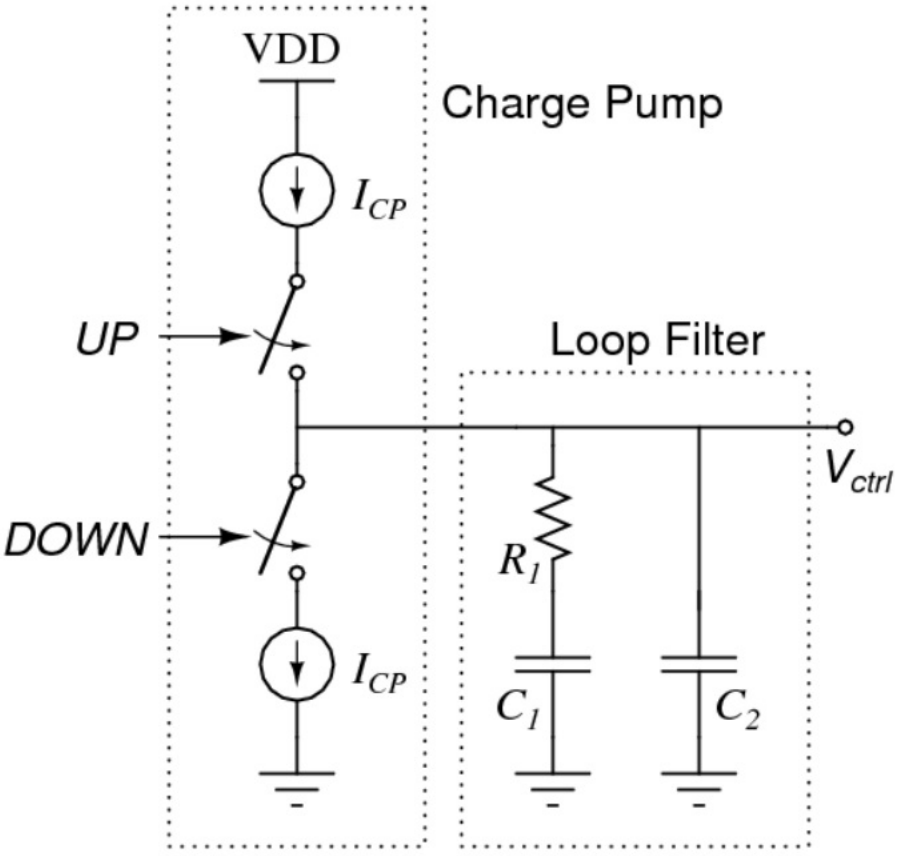

Figure 3: Charge pump and a typical loop filter used for charge pump based PLLs

Analysis of PLL Loop Dynamics:

Based on these parameters, the open loop gain becomes

$$H(s)G(s) = K_{PD} \times I_{CP} \times Z_{LF} \times \frac{K_{VCO}}{s},$$

where, Z_{LF} is the impedance of the Loop Filter, H(s) is the forward transfer function and G(s) is the feedback transfer function (which is 1 in this case, and the divider ratio when the frequency divider is present). The equation for calculating the output phase of the system becomes

$$\phi_{out}(s) = \big[\phi_{in}(s) - \phi_{out}(s)\big] K_{PD} \times I_{CP} \times Z_{LF} \times \frac{K_{VCO}}{s}$$

The loop is stable if the loop gain has sufficient gain and phase margins. In charge-pump based PLLs, if Z_{LF} is simply a capacitor, there are two poles at zero frequency and therefore stability cannot be ensured. Therefore, the resistor R_1 is added to obtain a zero at angular frequency R_1C_1. In addition, C_2, which is about one-tenth of C_1, is added to reduce ripples (though it doesn't significantly affect the gain and phase margins). The circuit parameters and loop filter parameters can be chosen keeping stability into consideration (arbitrary values generally don't work).