\* Freescale 83xx DMA Controller

Freescale PowerPC 83xx have on chip general purpose DMA controllers.

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Required properties:
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: compatible list, contains 2 entries, first is
- compatible
                     "fsl, CHIP-dma", where CHIP is the processor
                     (mpc8349, mpc8360, etc.) and the second is
                      'fsl,elo-dma"
                         : <registers mapping for DMA general status reg>
- reg
                              : Should be defined as specified in 1) to describe the
- ranges
                      DMA controller channels.
- cell-index
                         : controller index. 0 for controller @ 0x8100
- interrupts
                         : <interrupt mapping for DMA IRQ>
- interrupt-parent : optional, if needed for interrupt mapping
- DMA channel nodes:
                               : compatible list, contains 2 entries, first is "fsl, CHIP-dma-channel", where CHIP is the processor (mpc8349, mpc8350, etc.) and the second is "fsl, elo-dma-channel". However, see note below.
          - compatible
                                   : <registers mapping for channel>
          - reg
          - cell-index
                                   : dma channel index starts at 0.
Optional properties:

    interrupts

                                   : <interrupt mapping for DMA channel IRQ>
                                 (on 83xx this is expected to be identical to
                                  the interrupts property of the parent node)
          - interrupt-parent : optional, if needed for interrupt mapping
Example:
          dma@82a8 {
                    \#address-cells = \langle 1 \rangle:
                    #size-cells = <1>;
compatible = "fs1, mpc8349-dma", "fs1, elo-dma";
                    reg = \langle 0x82a8 \ 4 \rangle;
                    ranges = \langle 0 \ 0x8100 \ 0x1a4 \rangle:
                    interrupt-parent = <&ipic>;
                    interrupts = \langle 71 \rangle;
                    cell-index = \langle 0 \rangle;
                    dma-channel@0 {
                              compatible = "fsl, mpc8349-dma-channel".
"fsl, elo-dma-channel":
                              cell-index = \langle 0 \rangle:
                              reg = \langle 0 \ 0x80 \rangle:
                              interrupt-parent = <&ipic>;
                              interrupts = \langle 71 \ 8 \rangle;
                    dma-channel@80 {
                              compatible = "fs1, mpc8349-dma-channe1",
"fsl, elo-dma-channel";
                              cell-index = \langle 1 \rangle:
                              reg = \langle 0x80 \ 0x80 \rangle;
                              interrupt-parent = <&ipic>;
                                              第1页
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dma. txt
                               interrupts = \langle 71 \rangle;
                     };
                     dma-channel@100 {
                               compatible = "fsl, mpc8349-dma-channel",
"fsl, elo-dma-channel";
                               cell-index = \langle 2 \rangle;
                               reg = \langle 0x100 \ 0x80 \rangle;
                               interrupt-parent = <&ipic>;
                               interrupts = \langle 71 \ 8 \rangle;
                     dma-channel@180 {
                               compatible = "fs1, mpc8349-dma-channel",
"fsl, elo-dma-channel";
                               cell-index = \langle 3 \rangle;
                               reg = \langle 0x180 \ 0x80 \rangle;
                               interrupt-parent = <&ipic>;
                               interrupts = \langle 71 \ 8 \rangle;
                     };
          };
* Freescale 85xx/86xx DMA Controller
Freescale PowerPC 85xx/86xx have on chip general purpose DMA controllers.
Required properties:
                          : compatible list, contains 2 entries, first is
- compatible
                      "fsl, CHIP-dma", where CHIP is the processor (mpc8540, mpc8540, etc.) and the second is
                       "fsl,eloplus-dma"
                          : <registers mapping for DMA general status reg>
- reg
                          : controller index.
                                                     0 for controller @ 0x21000,
- cell-index
                                                      1 for controller @ 0xc000
                                : Should be defined as specified in 1) to describe the
- ranges
                       DMA controller channels.
- DMA channel nodes:
                                : compatible list, contains 2 entries, first is "fsl, CHIP-dma-channel", where CHIP is the processor (mpc8540, mpc8560, etc.) and the second is "fsl, eloplus-dma-channel". However, see note below.
          - compatible
                                    : dma channel index starts at 0.
          - cell-index
          - reg
                                     : <registers mapping for channel>
                                    : <interrupt mapping for DMA channel IRQ>
          - interrupts
          - interrupt-parent : optional, if needed for interrupt mapping
Example:
          dma@21300 {
                     \#address-cells = \langle 1 \rangle;
                     #size-cells = <1>;
compatible = "fs1, mpc8540-dma", "fs1, eloplus-dma";
                     reg = \langle 0x21300 \ 4 \rangle;
                     ranges = \langle 0 \ 0x21100 \ 0x200 \rangle;
                     cell-index = \langle 0 \rangle;
                     dma-channel@0 {
                               compatible = "fsl, mpc8540-dma-channel",
                                                第 2 页
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dma. txt
"fsl, eloplus-dma-channel";
                                reg = \langle 0 \ 0x80 \rangle;
                                cell-index = \langle 0 \rangle;
                                interrupt-parent = <&mpic>;
                                interrupts = \langle 20 \ 2 \rangle;
                     };
compatible = "fsl, mpc8540-dma-channel",
"fsl, eloplus-dma-channel";
                                reg = \langle 0x80 \ 0x80 \rangle;
                                cell-index = \langle 1 \rangle;
                                interrupt-parent = <&mpic>;
                                interrupts = \langle 21 \ 2 \rangle;
                     dma-channel@100 {
                                compatible = "fs1, mpc8540-dma-channel",
"fsl, eloplus-dma-channel";
                                reg = \langle 0x100 \ 0x80 \rangle;
                                cell-index = \langle 2 \rangle;
                                interrupt-parent = <&mpic>;
                                interrupts = \langle 22 2 \rangle;
                     };
                     dma-channel@180 {
                                compatible = "fs1, mpc8540-dma-channel",
"fsl, eloplus-dma-channel";
                                reg = \langle 0x180 \ 0x80 \rangle;
                                cell-index = \langle 3 \rangle;
                                interrupt-parent = <&mpic>;
                                interrupts = \langle 23 \ 2 \rangle;
                     };
          };
```

Note on DMA channel compatible properties: The compatible property must say "fsl, elo-dma-channel" or "fsl, eloplus-dma-channel" to be used by the Elo DMA driver (fsldma). Any DMA channel used by fsldma cannot be used by another DMA driver, such as the SSI sound drivers for the MPC8610. Therefore, any DMA channel that should be used for another driver should not use "fsl, elo-dma-channel" or "fsl, eloplus-dma-channel". For the SSI drivers, for example, the compatible property should be "fsl, ssi-dma-channel". See ssi.txt for more information.