esdhc. txt

* Freescale Enhanced Secure Digital Host Controller (eSDHC)

The Enhanced Secure Digital Host Controller provides an interface for MMC, SD, and SDIO types of memory cards.

```
Required properties:
   compatible: should be
    fsl, <chip>-esdhc", "fsl, esdhc"
  - reg : should contain eSDHC registers location and length.
  - interrupts : should contain eSDHC interrupt.
  - interrupt-parent : interrupt source phandle.
  - clock-frequency: specifies eSDHC base clock frequency.
  - sdhci, wp-inverted: (optional) specifies that eSDHC controller
    reports inverted write-protect state;
  - sdhci, 1-bit-only: (optional) specifies that a controller can
    only handle 1-bit data transfers.
Example:
```

```
sdhci@2e000 {
          compatible = "fsl, mpc8378-esdhc", "fsl, esdhc";
          reg = \langle 0x2e000 \ 0x1000 \rangle;
          interrupts = \langle 42 \ 0x8 \rangle;
          interrupt-parent = <&ipic>;
          /* Filled in by U-Boot */
          clock-frequency = \langle 0 \rangle;
};
```