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<book id="Generic-IRQ-Guide">
 <bookinfo>
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\langle toc \rangle \langle /toc \rangle
  <chapter id="intro">
    <title>Introduction</title>
    <para>
        The generic interrupt handling layer is designed to provide a
        complete abstraction of interrupt handling for device drivers.
        It is able to handle all the different types of interrupt controller
        hardware. Device drivers use generic API functions to request, enable,
        disable and free interrupts. The drivers do not have to know anything
        about interrupt hardware details, so they can be used on different
        platforms without code changes.
    </para>
    (para)
        This documentation is provided to developers who want to implement
        an interrupt subsystem based for their architecture, with the help
        of the generic IRQ handling layer.
    </para>
  </chapter>
  <chapter id="rationale">
    <title>Rationale</title>
        <para>
        The original implementation of interrupt handling in Linux is using
        the __do_IRQ() super-handler, which is able to deal with every
        type of interrupt logic.
        </para>
        para>
        Originally, Russell King identified different types of handlers to
        build a quite universal set for the ARM interrupt handler
        implementation in Linux 2.5/2.6. He distinguished between:
        <itemizedlist>
          <listitem><para>Level type</para></listitem>
          tistitem><para>Edge type</para></listitem>
          <listitem><para>Simple type</para></listitem>
        </itemizedlist>
        In the SMP world of the do IRQ() super-handler another type
        was identified:
        <itemizedlist>
          stitem><para>Per CPU type</para></listitem></para>
        </itemizedlist>
        </para>
        para>
        This split implementation of highlevel IRQ handlers allows us to
        optimize the flow of the interrupt handling for each specific
        interrupt type. This reduces complexity in that particular codepath
                                     第2页
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     and allows the optimized handling of a given type.
      </para>
      <para>
     The original general IRQ implementation used hw interrupt type
     structures and their ->ack(), ->end() [etc.] callbacks to
     differentiate the flow control in the super-handler. This leads to
     a mix of flow logic and lowlevel hardware logic, and it also leads
     to unnecessary code duplication: for example in i386, there is a
      ioapic level irq and a ioapic edge irq irq-type which share many
     of the lowlevel details but have different flow handling.
      </para>
     <para>
     A more natural abstraction is the clean separation of the
      irq flow' and the 'chip details'.
      </para>
      <para>
     Analysing a couple of architecture's IRQ subsystem implementations
     reveals that most of them can use a generic set of 'irq flow'
     methods and only need to add the chip level specific code.
     The separation is also valuable for (sub)architectures
     which need specific quirks in the irq flow itself but not in the
     chip-details - and thus provides a more transparent IRQ subsystem
     design.
     </para>
      <para>
     Each interrupt descriptor is assigned its own highlevel flow
     handler, which is normally one of the generic
     implementations. (This highlevel flow handler implementation also
     makes it simple to provide demultiplexing handlers which can be
     found in embedded platforms on various architectures.)
     </para>
      <para>
     The separation makes the generic interrupt handling layer more
     flexible and extensible. For example, an (sub)architecture can
     use a generic irq-flow implementation for 'level type' interrupts
     and add a (sub)architecture specific 'edge type' implementation.
     </para>
     ⟨para⟩
     To make the transition to the new model easier and prevent the
     breakage of existing implementations, the __do_IRQ() super-handler
     is still available. This leads to a kind of duality for the time
     being. Over time the new model should be used in more and more
     architectures, as it enables smaller and cleaner IRQ subsystems.
     </para>
</chapter>
<chapter id="bugs">
  <title>Known Bugs And Assumptions</title>
  <para>
     None (knock on wood).
  </para>
</chapter>
<chapter id="Abstraction">
  <title>Abstraction layers</title>
  ⟨para⟩
     There are three main levels of abstraction in the interrupt code:
                                   第3页
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<orderedlist>
      stitem><para>Highlevel driver API</para></listitem>
      <listitem><para>Highlevel IRQ flow handlers</para></listitem>
      <listitem><para>Chiplevel hardware encapsulation</para></listitem>
    </orderedlist>
</para>
<sect1 id="Interrupt_control_flow">
    <title>Interrupt control flow</title>
    <para>
   Each interrupt is described by an interrupt descriptor structure
   irq desc. The interrupt is referenced by an 'unsigned int' numeric
   value which selects the corresponding interrupt decription structure
    in the descriptor structures array.
   The descriptor structure contains status information and pointers
   to the interrupt flow method and the interrupt chip structure
   which are assigned to this interrupt.
   </para>
    <para>
   Whenever an interrupt triggers, the lowlevel arch code calls into
   the generic interrupt code by calling desc-handle irq().
   This highlevel IRQ handling function only uses desc->chip primitives
   referenced by the assigned chip descriptor structure.
   </para>
\langle /\text{sect1} \rangle
<sect1 id="Highlevel Driver API">
    <title>Highlevel Driver API</title>
    <para>
      The highlevel Driver API consists of following functions:
      <itemizedlist>
      <listitem><para>request irq()</para></listitem>
      <listitem><para>free irq()</para></listitem>
      <listitem><para>disable irq()</para></listitem>
      <listitem><para>enable_irq()</para></listitem>
      titem><para>disable irq nosync() (SMP only)</para></listitem>
      titem><para>synchronize_irq() (SMP only)</para></listitem>
      <listitem><para>set_irq_type()</para></listitem>
      tistitem><para>set_irq_wake()</para></listitem>
      <listitem><para>set_irq_data()</para></listitem>
      <listitem><para>set irq chip()</para></listitem>
      <listitem><para>set irq chip data()</para></listitem>
      </itemizedlist>
      See the autogenerated function documentation for details.
    </para>
\langle /\text{sect1} \rangle
<sect1 id="Highlevel IRQ flow handlers">
    <title>Highlevel IRQ flow handlers</title>
      The generic layer provides a set of pre-defined irq-flow methods:
      <itemizedlist>
      <listitem><para>handle_level_irq</para></listitem>
      <listitem><para>handle_edge_irq</para></listitem>
      <listitem><para>handle_simple_irq</para></listitem>
      <listitem><para>handle percpu irg</para></listitem>
      </itemizedlist>
     The interrupt flow handlers (either predefined or architecture
      specific) are assigned to specific interrupts by the architecture
                                 第4页
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         either during bootup or during device initialization.
        </para>
        <sect2 id="Default flow implementations">
        <title>Default flow implementations</title>
           <sect3 id="Helper_functions">
               <title>Helper functions</title>
               <para>
               The helper functions call the chip primitives and
               are used by the default flow implementations.
               The following helper functions are implemented (simplified
excerpt):
               programlisting>
default enable(irq)
       desc->chip->unmask(irq);
default disable(irg)
       if (!delay disable(irq))
               desc->chip->mask(irg);
default ack(irg)
       chip->ack(irg);
default mask ack(irg)
       if (chip->mask ack) {
               chip->mask ack(irq);
       } else {
               chip->mask(irq);
               chip->ack(irg):
noop(irq)
               gramlisting>
               </para>
           </sect3>
        </sect2>
        <sect2 id="Default_flow_handler_implementations">
       <title>Default flow handler implementations</title>
           handle_level_irq provides a generic implementation
               for level-triggered interrupts.
               </para>
               ⟨para⟩
               The following control flow is implemented (simplified excerpt):
                                   第 5 页
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genericing. tmpl. txt
                programlisting>
desc->chip->start();
handle IRQ event (desc->action);
desc->chip->end();
                gramlisting>
                </para>
            \langle sect 3 \rangle
            <sect3 id="Default Edge IRQ flow handler">
                <title>Default Edge IRQ flow handler</title>
                handle edge irq provides a generic implementation
                for edge-triggered interrupts.
                </para>
                <para>
                The following control flow is implemented (simplified excerpt):
                programlisting>
if (desc->status & running) {
        desc->chip->hold();
        desc->status |= pending | masked;
        return;
desc->chip->start();
desc->status |= running;
do {
        if (desc->status & amp; masked)
                desc->chip->enable();
        desc->status & = ~pending;
        handle IRQ event (desc->action);
} while (status & amp; pending);
desc->status & amp; = ~running;
desc->chip->end();
                gramlisting>
                </para>
            </sect3>
            <sect3 id="Default simple IRQ flow handler">
                <title>Default simple IRQ flow handler</title>
                ⟨para⟩
                handle simple irg provides a generic implementation
                for simple interrupts.
                </para>
                <para>
                Note: The simple flow handler does not call any
                handler/chip primitives.
                </para>
                para>
                The following control flow is implemented (simplified excerpt):
                programlisting>
handle_IRQ_event(desc->action);
                gramlisting>
                </para>
            \langle sect 3 \rangle
            <sect3 id="Default_per_CPU_flow_handler">
                <title>Default per CPU flow handler</title>
                handle percpu irq provides a generic implementation
                for per CPU interrupts.
                                      第 6 页
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                 </para>
                 <para>
                 Per CPU interrupts are only available on SMP and
                 the handler provides a simplified version without
                 locking.
                 </para>
                 <para>
                 The following control flow is implemented (simplified excerpt):
                 programlisting>
desc->chip->start();
handle IRQ event (desc->action);
desc->chip->end();

c/programlisting>
                 </para>
            \langle /\text{sect3} \rangle
        \langle \text{sect2} \rangle
        <sect2 id="Quirks and optimizations">
        <title>Quirks and optimizations</title>
        The generic functions are intended for 'clean' architectures and chips,
        which have no platform-specific IRQ handling quirks. If an architecture
        needs to implement quirks on the 'flow' level then it can do so by
        overriding the highlevel irq-flow handler.
        </para>
        \langle sect 2 \rangle
        <sect2 id="Delayed interrupt disable">
        <title>Delayed interrupt disable</title>
        This per interrupt selectable feature, which was introduced by Russell
        King in the ARM interrupt implementation, does not mask an interrupt
        at the hardware level when disable irq() is called. The interrupt is
        kept enabled and is masked in the flow handler when an interrupt event
        happens. This prevents losing edge interrupts on hardware which does
        not store an edge interrupt event while the interrupt is disabled at
        the hardware level. When an interrupt arrives while the IRQ DISABLED
        flag is set, then the interrupt is masked at the hardware level and
        the IRQ_PENDING bit is set. When the interrupt is re-enabled by
        enable irg() the pending bit is checked and if it is set, the
        interrupt is resent either via hardware or by a software resend
        mechanism. (It's necessary to enable CONFIG_HARDIRQS_SW_RESEND when
        you want to use the delayed interrupt disable feature and your
        hardware is not capable of retriggering an interrupt.)
        The delayed interrupt disable can be runtime enabled, per interrupt,
        by setting the IRQ DELAYED DISABLE flag in the irq desc status field.
        </para>
        \langle /\text{sect2} \rangle
    \langle sect 1 \rangle
    <sect1 id="Chiplevel hardware encapsulation">
        <title>Chiplevel hardware encapsulation</title>
        <para>
        The chip level hardware descriptor structure irq_chip
        contains all the direct chip relevant functions, which
        can be utilized by the irg flow implementations.
          <itemizedlist>
          titem><para>ack()</para></listitem>
          titem><para>mask ack() - Optional, recommended for
                                       第7页
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performance </para> </listitem>
          <listitem><para>mask()</para></listitem>
          <listitem><para>unmask()</para></listitem>
          titem><para>retrigger() - Optional</para></listitem>
          titem><para>set type() - Optional</para></listitem>
          titem><para>set_wake() - Optional</para></listitem>
          </itemizedlist>
        These primitives are strictly intended to mean what they say: ack means
        ACK, masking means masking of an IRQ line, etc. It is up to the flow
        handler(s) to use these basic units of lowlevel functionality.
        </para>
    \langle /\text{sect1} \rangle
  </chapter>
  <chapter id="doirg">
     <title> do IRQ entry point</title>
     <para>
        The original implementation do IRQ() is an alternative entry
        point for all types of interrupts.
     </para>
     <para>
        This handler turned out to be not suitable for all
        interrupt hardware and was therefore reimplemented with split
        functionality for egde/level/simple/percpu interrupts. This is not
        only a functional optimization. It also shortens code paths for
        interrupts.
      </para>
      <para>
        To make use of the split implementation, replace the call to
          do IRQ by a call to desc->handle irq() and associate
        the appropriate handler function to desc-handle irq().
        In most cases the generic handler implementations should
        be sufficient.
     </para>
  </chapter>
  <chapter id="locking">
     <title>Locking on SMP</title>
     <para>
        The locking of chip registers is up to the architecture that
        defines the chip primitives. There is a chip->lock field that can be
used
        for serialization, but the generic layer does not touch it. The per-irq
        structure is protected via desc->lock, by the generic layer.
     </para>
  </chapter>
  <chapter id="structs">
     <title>Structures</title>
     This chapter contains the autogenerated documentation of the structures
which are
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used in the generic IRQ layer.

</para>
!Iinclude/linux/irq.h

</chapter>

!Iinclude/linux/interrupt.h

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<chapter id="pubfunctions">
     <title>Public Functions Provided</title>
     <para>
     This chapter contains the autogenerated documentation of the kernel API
functions
      which are exported.
     </para>
!Ekernel/irq/manage.c
!Ekernel/irq/chip.c
  </chapter>
  <chapter id="intfunctions">
     <title>Internal Functions Provided</title>
     This chapter contains the autogenerated documentation of the internal
functions.
     </para>
!Ikernel/irq/handle.c
!Ikernel/irq/chip.c
  </chapter>
  <chapter id="credits">
     <title>Credits</title>
        <para>
                The following people have contributed to this document:
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                         titem><para>Thomas
Gleixner<email>tglx@linutronix.de</email></para></listitem>
                         <listitem><para>Ingo
Molnar < email > mingo@elte.hu < / email > < / / para > < / listitem >
                 </orderedlist>
        </para>
  </chapter>
</book>
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