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承　認　書

(Revision Note)

品名 (Part Number)	802.11b/g/n +BT 3.0+FM 3-in-1 NC024 SIP Module
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0. Revision History

REV Note	Date	Change Note
Draft Rev.00	Feb.,2, 2010	Initial
Rev.01	Mar.,30, 2010	Update Wi-Fi /BT RF Specifications
Rev.02	Apr.,20, 2010	Add host interface and power sequence timing
Rev.03	May.,20, 2010	Update the WLAN RF spec. based-on over temp./voltage. Add MSL condition.

1. Introduction

The NC024 SIP Module (802.11b/g/n + BT +FM) is based on IC Marvell 88W8787 with flip chip package.

This documentation describes the Engineering requirements specification of the WLAN (802.11b/g/n) +Bluetooth 3.0 +FM Module. It is a confidential document of CyberTAN.

1.1 RF module Overview

The general HW architecture for the module is shown in Figure 1. The module integrates Marvell® 88W8787, PA,SP3T RF switch and all required passive elements into a miniature 8.3mm x 8.6mm x 1.2mm(max. thickness) size package.

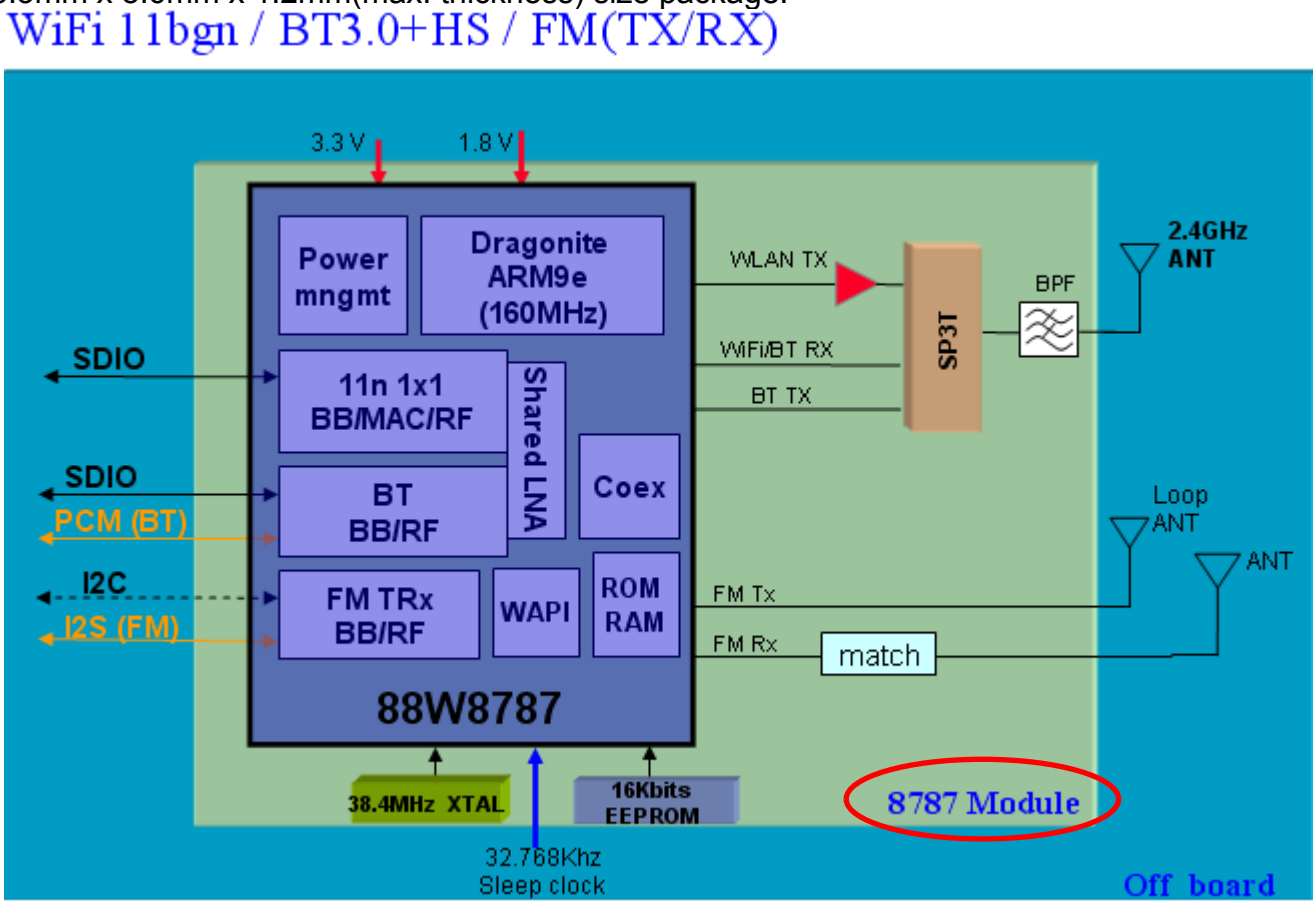


Figure1 8787 SIP Module Block Diagram

The Module is powered in the application from two regulated supply (3.3V and 1.8V). Host digital interfacing is compatible with SDIO interface for WLAN, PCM/I2S interfaces for Bluetooth and I2C/I2S interfaces for FMRXTX. Host analog audio interfaces are available for both FM RX and FM TX.

1.2 Specification reference

This specification is based on additional references listed below.

- IEEE Std. 802.11b
- IEEE Std. 802.11g
- IEEE Std. 802.11n draft
- Bluetooth 3.0 + High Speed (HS) (also compliant with Bluetooth 2.1 + EDR)

1.3 System Functions

- Multi-Radio coexistence: WLAN 11bgn (1x1)+ BT3.0/HS + FM Tx/Rx
  a, 55nm CMOS single-chip with all CPU/MAC/BB/RF integrated
  b, Independent and simultaneous radio operation
  c, Support 802.11 AMP operation
- Host Interface: WLAN-- SDIO (1 and 4 bit, up to 75MHz)
  BT--- SDIO and PCM for voice
  FM--- I2C and dedicated I2S for audio
- WLAN Modulation: DBPSK, DQPSK and CCK and DSSS with IEEE 802.11b mode.
  BPSK, QPSK, 16QAM, 64QAM and OFDM with IEEE 802.11g mode.
  MCS0~7 OFDM with IEEE802.11n (HT20/HT40) mode
- WLAN Date rates: 1, 2, 5.5 and 11Mbps with IEEE 802.11b mode.
  6, 9, 12, 18, 24, 36, 48 and 54 Mbps with IEEE 802.11g mode.
  MCS0~7 (up to 150Mbps) with IEEE802.11n (HT20/HT40) mode
- WLAN/BT share with single antenna,
- Two FM ANT design (one for TX, other for RX)
- Sharp Band Pass Filter inside to reduce interference
- Ultra low power design
- Lead Free design compliant with ROHS requirement

1.4 Structure

Table1: General Specification

Form factor	64 pin LGA
Host Interface	SDIO for Wi-Fi& BT
PCB	4-layer design
Dimension	8.3mmx8.6mmx1.2mm
Antenna	Wi-Fi &BT use the same ANT and FM use two ANT
Operation Temperature	-20℃ to +70℃
Storage Temperature	-40℃ to +85℃
Operation Voltage	3.3V+/-5%,1.8V+/-5%
Weight (Reference)	0.2 g typ.

2. Mechanical Specification

2.1 Package Type

This module is a surface mount device with a Land Grid Array footprint on the bottom side of a laminate substrate with a molding case attached on top.

2.2 Appearance

The module surface is marked with a Pin 1 indicator, P/N and Lot code.
The module surface appearance is illustrated in below Figure2.

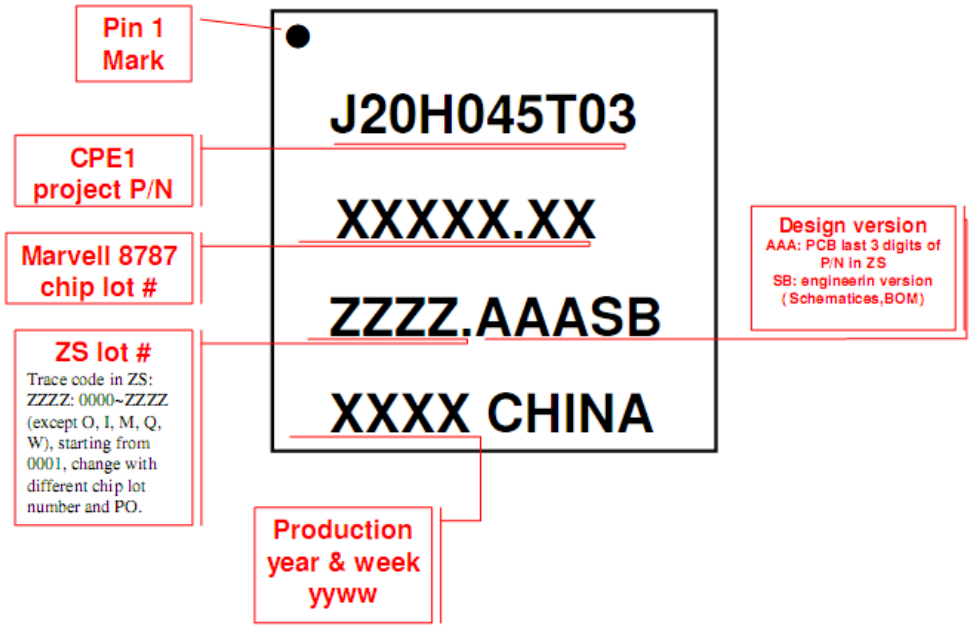
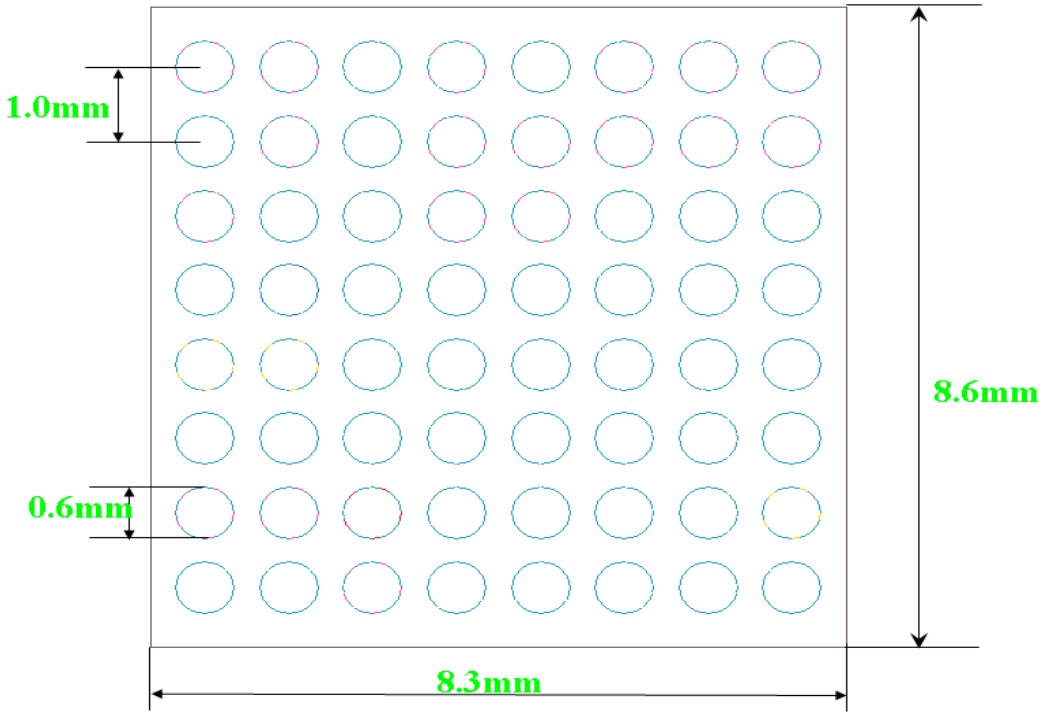


Figure2 8787 SIP Module Marking

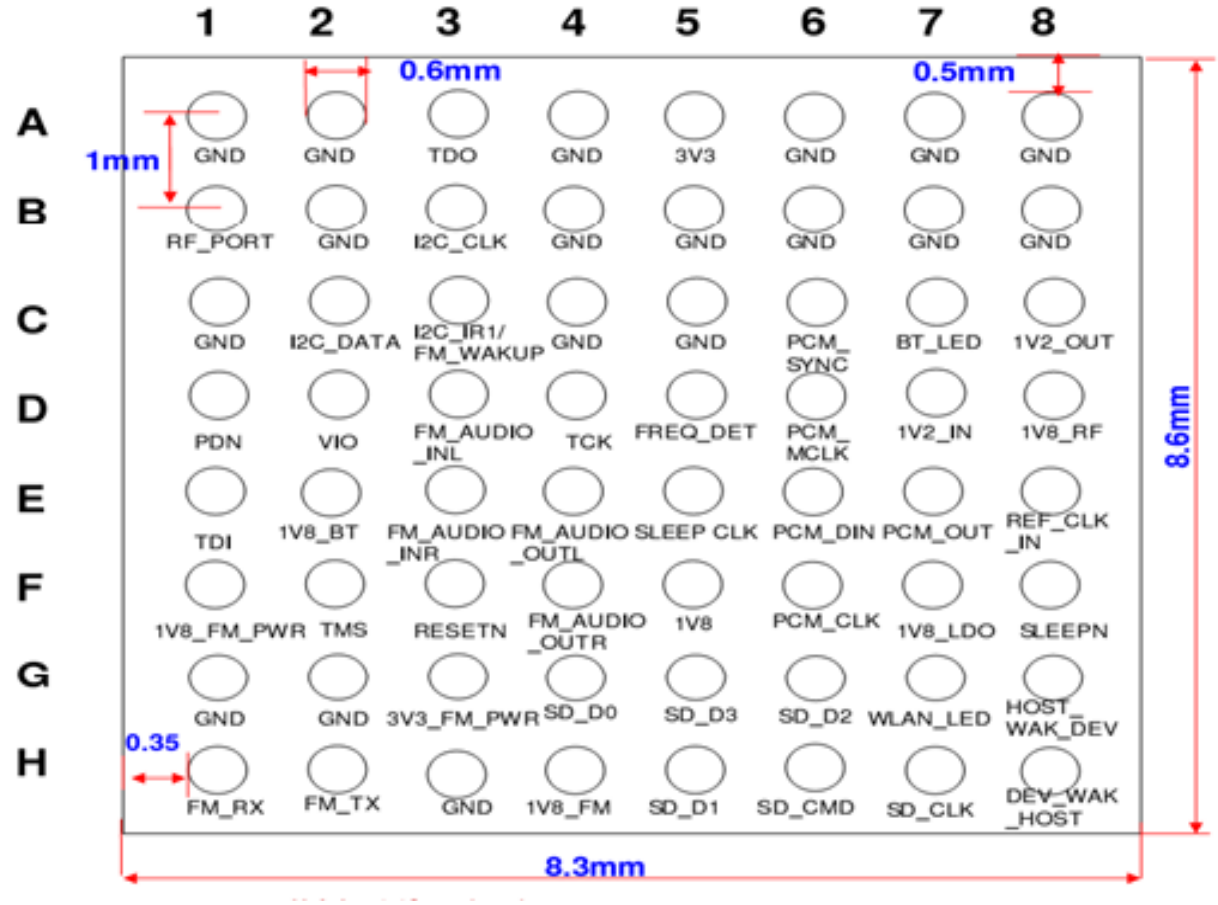
2.3 Mechanical Outline Drawing

The MARVELL 8787 NC024 SIP Module 802.11b/g/n module shall be 4-layer PCB design. Dimension (W x L x T): 8.3mm ×8.6mm ×1.2mm(max.).



2.4 Land Grid Array

2.4.1 LGA assignment and location



TOP View

2.4.2 Module Pin-out

Table2: Module Pin-Out

Pin Symbol	Pin No.	Type	Pin description
RF_PORT	B1	I/O	Wi-Fi&BT RF Port
FM_RX	H1	I	FM RF Signal input
FM_TX	H2	O	FM RF Signal output
TDO	A3	O	Debug Port
TCK	D4	I	Debug Port
TDI	E1	I	Debug Port
TMS	F2	I	Debug Port
I2C_CLK	B3	I/O	I2C interface Clock for FM function
I2C_DAT	C2	I/O	I2C interface Data for FM function
I2C_IR1/FM_WAKUP	C3	O	I2C interface IRQ Signal /FM WAKUP HOST Signal
PCM_SYNC	C6	I/O	PCM MODE:PCM Interface SYNC signal I2S MODE:I2S interface LRCLK signal
PCM_MCLK	D6	O	PCM MODE:PCM Interface MCLK signal I2S MODE:I2S interface CCLK signal
PCM_CLK	F6	I/O	PCM MODE:PCM Interface CLK signal I2S MODE:I2S interface BCLK signal
PCM_DIN	E6	I	PCM MODE:PCM Interface DIN signal I2S MODE:I2S interface DIN signal
PCM_OUT	E7	O	PCM MODE:PCM Interface DOUT signal I2S MODE:I2S interface DOUT signal
FM_AUDIO_INL	D3	I	FM AUDIO Stereo input
FM_AUDIO_INR	E3	I	FM AUDIO Stereo input
FM_AUDIO_OUTL	E4	O	FM AUDIO Stereo Output
FM_AUDIO_OUTR	F4	O	FM AUDIO Stereo Output
SD_CLK	H7	I	SDIO CLK
SD_CMD	H6	I/O	SDIO Command
SD_D0	G4	I/O	SDIO data interface
SD_D1	H5	I/O	SDIO data interface
SD_D2	G6	I/O	SDIO data interface
SD_D3	G5	I/O	SDIO data interface
HOST_WAK_DEV	G8	I/O	Host Wakeup: Bluetooth/WLAN/G-SPI host wakeup (output) ,configure by GPIO[4]
DEV_WAK_HOST	H8	I/O	Host Wakeup: WLAN host wakeup (output) configure by GPIO[16]
FREQ_DET	D5	O	Ref. clock auto detect /fix select, load a 100K to GND. NC: auto detect (sleep clk pin must input 32.768KHz square clock) Pull low: fix the clk to 38.4MHz
PDN	D1	I	Power down , need pull high to VIO
RESETN	F3	I	reset signal ,need pull high to VIO
SLEEPN	F8	I	inform Host that device is in sleeping mode
BT_LED	C7	I/O	GPIO[17] output for BT LED, low active

WLAN_LED	G7	I/O	GPIO[1] output for WLAN LED , low active
REF_CLK_IN	E8	I	Ref. clk input (internal contains crystal, NC it)
SLEEP CLK	E5	I	32.768KHz clock input (AVDD1.8V)
3V3	A5	I	3.3V power input
1V2_OUT	C8	O	1.2V LDO output
1V2_IN	D7	I	1.2V power input (if use internal 1.2V,must connect the pin D7[1V2_IN] to C8[1V2_OUT] externally，load 1uF)
1V8_BT	E2	I	1.8V power input
VIO	D2	I	1.8V/2.6V/3.3V input
1V8_FM_PWR	F1	I/O	1.8V power or FM (with internal LDO). FM TX mode / 3V3_FM_PWR / 1V8_FM_PWR High Power / Load / Floating Low Power / Floating / Load
1V8	F5	I	1.8V power input
1V8_LDO	F7	I	1.8V power input
3V3_FM_PWR	G3	I	3.3V power input for FM(if without FM, just NC it)
1V8_RF	D8	I	1.8V power input
1V8_FM	H4	I	1.8V power input for FM(if without FM, just NC it)
GND	A1 A2 A4 A6 A7 A8 B2 B4 B5 B6 B7 B8 C1 C4 C5 G1 G2 H3	Ground	GND

3. ELECTRICAL SPECIFICATIONS

This Specification is based upon the Marvell 88W8787 Data Sheet (MV-S106697-00, Rev.-February 19, 2010) and is subject to any subsequent changes in applicable Marvell documentation and software. Any parameter marked TBD indicates that this is yet to be determined by CyberTAN design/testing. Any parameter marked TBC indicates that this is yet to be determined in an update of Marvell documentation.

3.1 Common Specifications

3.1.1 Absolute Maximum Ratings

Table3: Absolute Maximum Ratings

Symbol	Description	Min.	Typ.	Max.	Unit
3V3	3.3V power supply	--	3.3	4.0	V
VIO	1.8V/2.6V/3.3V digital power supply	--	1.8	2.2	V
		--	2.6	3.1	V
		--	3.3	4.0	V
1V8 1V8_BT 1V8_LDO 1V8_RF 1V8_FM	1.8V analog power supply	--	1.8	1.89	V
1V2_IN 1V2_OUT	1.2V power supply	--	1.2	1.32	V

3.1.2 Recommended Operating Conditions

Table4: Recommended Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit
3V3	3.3V power supply	3.15	3.3	3.45	V
VIO	1.8V/2.6V/3.3V digital power supply	1.62	1.8	1.98	V
		2.5	2.6	2.7	V
		2.97	3.3	3.63	V
1V8 1V8_BT 1V8_LDO 1V8_RF 1V8_FM	1.8V analog power supply	1.71	1.8	1.89	V
1V2_IN 1V2_OUT	1.2V power supply	1.14	1.2	1.32	V
Ta	Normal Operating Temperature	-20	+25	+65	℃

3.1.3 Digital Interface—VIO

A, 1.8V Operation

Table 5: DC Electricals—General (UART, I2C-Compatible Slave, and FM host interface), 1.8V Operation (VIO)

Symbol	Description	Min.	Typ.	Max.	Unit
VIH	Input high voltage	0.7*V18	--	V18+0.3	V
VIL	Input low voltage	-0.3	--	0.3*V18	V
VHYS	Input hysteresis	200	--	--	V
VOH	Output high voltage	V18-0.2	--	--	V
VOL	Output low voltage	--	--	0.2	V

Table 6: DC Electricals—Host Interface (SDIO host interface), 1.8V Operation (VIO)

Symbol	Description	Min.	Typ.	Max.	Unit
VIH	Input high voltage	0.7*V18	--	V18+0.3	V
VIL	Input low voltage	-0.3	--	0.3*V18	V
VHYS	Input hysteresis	200	--	--	V
VOH	Output high voltage	V18-0.4	--	--	V
VOL	Output low voltage	--	--	0.4	V

B. 2.6V Operation

Table 7: DC Electricals—General (UART, I2C-Compatible Slave, and FM host interface), 2.6V Operation (VIO)

Symbol	Description	Min.	Typ.	Max.	Unit
VIH	Input high voltage	0.7*V26	--	V26+0.3	V
VIL	Input low voltage	-0.3	--	0.3*V26	V
VHYS	Input hysteresis	200	--	--	V
VOH	Output high voltage	V26-0.2	--	--	V
VOL	Output low voltage	--	--	0.4	V

Table 8: DC Electricals—Host Interface (SDIO host interface), 2.6V Operation (VIO)

Symbol	Description	Min.	Typ.	Max.	Unit
VIH	Input high voltage	0.7*V26	--	V26+0.3	V
VIL	Input low voltage	-0.3	--	0.3*V26	V
VHYS	Input hysteresis	200	--	--	V
VOH	Output high voltage	V26-0.4	--	--	V
VOL	Output low voltage	--	--	0.4	V

C.3.3V Operation

Table 9: DC Electricals—General (UART, I2C-Compatible Slave, and FM host interface), 3.3V Operation (VIO)

Symbol	Description	Min.	Typ.	Max.	Unit
VIH	Input high voltage	0.7*V33	--	V33+0.3	V
VIL	Input low voltage	-0.3	--	0.3*V33	V
VHYS	Input hysteresis	200	--	--	V
VOH	Output high voltage	V33-0.4	--	--	V
VOL	Output low voltage	--	--	0.4	V

Table 10: DC Electricals—Host Interface (SDIO host interface), 3.3V Operation (VIO)

Symbol	Description	Min.	Typ.	Max.	Unit
VIH	Input high voltage	0.7*V33	--	V33+0.3	V
VIL	Input low voltage	-0.3	--	0.3*V33	V
VHYS	Input hysteresis	200	--	--	V
VOH	Output high voltage	V33-0.4	--	--	V
VOL	Output low voltage	--	--	0.4	V

3.1.3 Sleep Clock Specifications

Table 11: External Sleep Clock Timing (Note: Limited to within 10℃ variance)

Symbol	Description	Min.	Typ.	Max.	Unit
CLK	CLK Clock frequency range/accuracy • CMOS input clock signal type • ±250 ppm (initial, aging, temperature)	--	32.768	--	KHz
VIH	Input levels	0.8	--	1.98	V
VIL		0.0	--	0.25	V
PN	Phase noise requirement (@ 100 KHz)	--	-125	--	dBc/Hz
Jc	Cycle Jitter	--	1.5	--	ns(RMS)
SR	Slew rate limit (10-90%)	--	--	100	ns
DC	Duty cycle tolerance	20	--	80	%

3.2 RF Specifications

3.2.1 WLAN Specifications

Wireless LAN Standards	IEEE 802.11g standard ,IEEE 802.11b, IEEE 802.11n
Operating Frequency	2.412~2.484GHz
Channel Numbers	11 channels for United States 13 channels for Europe Countries 14 channels for Japan
WLAN Data Rate	802.11n:MCS7 with fall back of MCS6,MCS5…MCS0 802.11g: 54Mbps with fall back of 48, 36, 24, 18, 12, 9, 6Mbps. 802.11b: 11Mbps with fall back rates of 5.5, 2, and 1Mbps
Modulation Schemes	802.11g: 64QAM (54Mbps, 48Mbps), 16QAM (36Mbps, 24Mbps), QPSK (18Mbps, 12Mbps), BPSK (9Mbps, 6Mbps) 802.11b: CCK (11 Mbps, 5.5Mbps), DQPSK (2 Mbps), DBPSK (1 Mbps) 802.11n: MCS0~7(BPSK,QPSK,16-QAM,64-QAM)
Transmitter Output Power	802.11b 11Mbps：18dBm+/-1.5dB
	802.11g 54Mbps：15dBm+/-1.5dB
	802.11n(HT20&HT40)：13dBm+/-1.5dB
Receiver Sensitivity (802.11n-HT40)	for MCS7 (HT40) 10%PER @ –65dBm,+/-2dB for MCS6 (HT40) 10%PER @ –66dBm,+/-2dB for MCS5 (HT40) 10%PER @ –68dBm,+/-2dB for MCS4 (HT40) 10%PER @ –72dBm,+/-2dB for MCS3 (HT40) 10%PER @ –75dBm,+/-2dB for MCS2 (HT40) 10%PER @ –78dBm,+/-2dB for MCS1 (HT40) 10%PER @ –80dBm,+/-2dB for MCS0 (HT40) 10%PER @ –83dBm,+/-2dB
Receiver Sensitivity (802.11n-HT20)	for MCS7 (HT20) 10%PER @ –67dBm,+/-2dB for MCS6 (HT20) 10%PER @ –69dBm,+/-2dB for MCS5 (HT20) 10%PER @ –70dBm,+/-2dB for MCS4 (HT20) 10%PER @ –74dBm,+/-2dB for MCS3 (HT20) 10%PER @ –78dBm,+/-2dB for MCS2 (HT20) 10%PER @ –80dBm,+/-2dB for MCS1 (HT20) 10%PER @ –83dBm,+/-2dB for MCS0 (HT20) 10%PER @ –86dBm,+/-2dB
Receiver Sensitivity (802.11g)	for 54Mbps 10% PER @ –70dBm,+/-2dB for 48Mbps 10% PER @ –72dBm,+/-2dB for 36Mbps 10% PER @ –76dBm,+/-2dB for 24Mbps 10% PER @ –79dBm,+/-2dB for 18Mbps 10% PER @ –82dBm,+/-2dB for 12Mbps 10% PER @ –84dBm,+/-2dB for 9Mbps 10% PER @ –87dBm,+/-2dB for 6Mbps 10% PER @ –87dBm,+/-2dB

Receiver Sensitivity (802.11b)	for 11Mbps 8% PER @ –85dBm,+/-2dB for 5.5Mbps 8% PER @ –90dBm,+/-2dB for 2Mbps 8% PER @ –92dBm,+/-2dB for 1Mbps 8% PER @ –94dBm,+/-2dB
WLAN power consumption (Transmit power at 100% duty cycle,25℃)	11b_11Mbps@18dBm: Typical 148mA@3.3V and 120mA@1.8V 11g_54Mbps@15dBm: Typical 119mA@3.3V and 125mA@1.8V HT20_MCS7@15dBm Typical 121mA@3.3V and 125mA@1.8V HT40_MCS7@15dBm Typical 119mA@3.3V and 132mA@1.8V
Encryption	AES(CCMP),AES(CMAC), WEP 64/128 (TKIP), WPA,WPA2 IEEE802.11i IEEE802.11w WAPI

3.2.2 Bluetooth Specifications

Radio Technology	FHSS
Operating Frequency	2402 ~ 2480MHz ISM band
Channel Numbers	79 channels with 1MHz BW(Except EDR mode)
Transmitter Output Power	4~10dBm output power for class1.5 operation
Receiver Sensitivity	GFSK 0.1% BER, 1Mbps@-84dBm,+/-2dB 8DPSK 0.1% BER, 3Mbps @ -79dBm,+/-2dB
Maximum Receiver Signal	-20dBm
Operating Voltage	1.8V/3.3V

3.2.3 FM (TBD)

Radio Technology	FM
Operating Frequency	76 ~ 108MHz
Transmitter Output Power	8dBm output power
Receiver Sensitivity	5 dBuV
Maximum Receiver Signal	105 dBuV

3.2.4 RDS (TBD)

Radio Technology	BPSK
Operating Frequency	76 ~ 108MHz
Transmitter Output Power	8dBm output power
Receiver Sensitivity	25 dBuV
Maximum Receiver Signal	105 dBuV

3.3 Host Interface Specifications

3.3.1 SDIO Interface Specifications

The 88W8787 SDIO host interface pins are powered from the VIO voltage supply.
The SDIO electrical specifications are identical for the 1-bit SDIO, 4-bit SDIO, and SPI modes.

Figure 3: SDIO Protocol Timing Diagram—Normal Mode

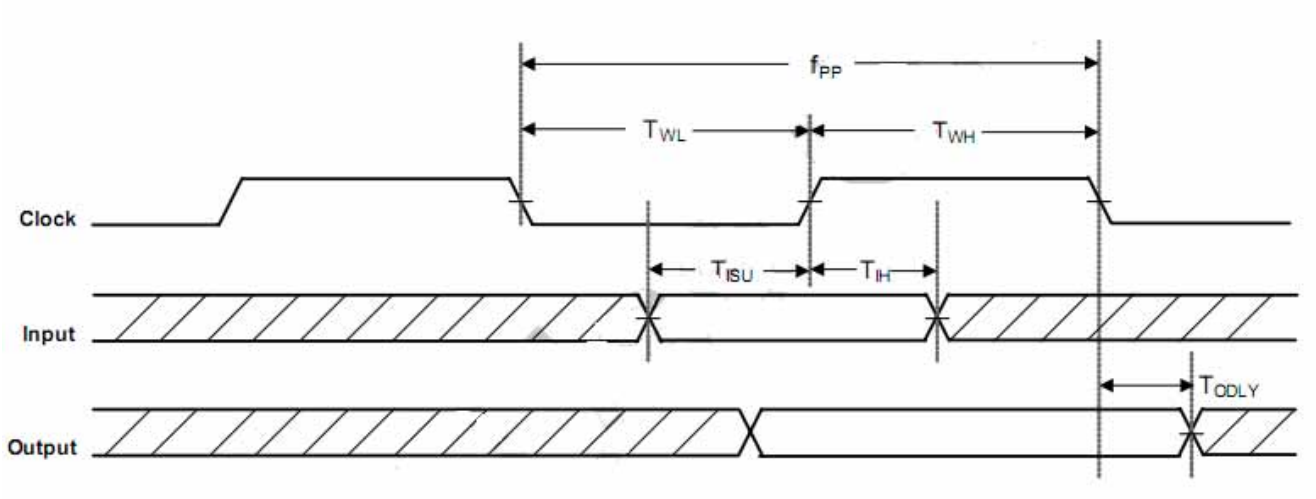


Figure 4: SDIO Protocol Timing Diagram—High Speed Mode

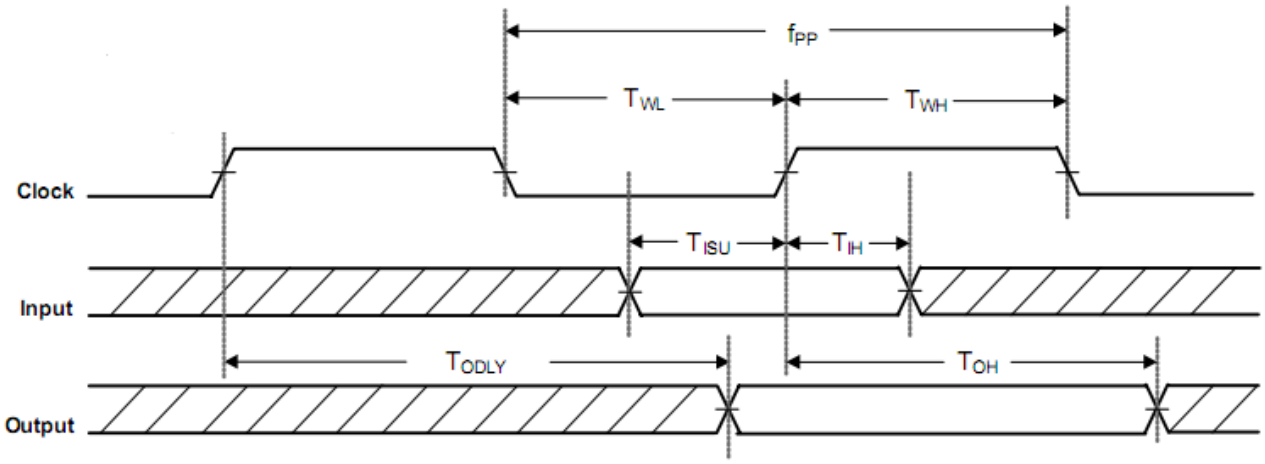


Table 12: SDIO Interface Timing Data

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
fPP	Clock Frequency	Normal	0	--	25	MHz
		High Speed	0	--	75	MHz
TWL	Clock Low Time	Normal	10	--	--	ns
		High Speed	7	--	--	ns
TWH	Clock High Time	Normal	10	--	--	ns
		High Speed	7	--	--	ns
TISU	Input Setup Time	Normal	5	--	--	ns
		High Speed	6	--	--	ns
TIH	Input Hold Time	Normal	5	--	--	ns
		High Speed	2	--		ns
TODLY	Output Delay Time	---	--	--	7.33	ns
TOH	Output Hold Time	High Speed	2.5	--	--	ns

3.3.2 I2C Interface Specifications

The 88W8787 I2C-compatible pins are powered from the VIO voltage supply.

Table 14: I2C Interface Timing Data

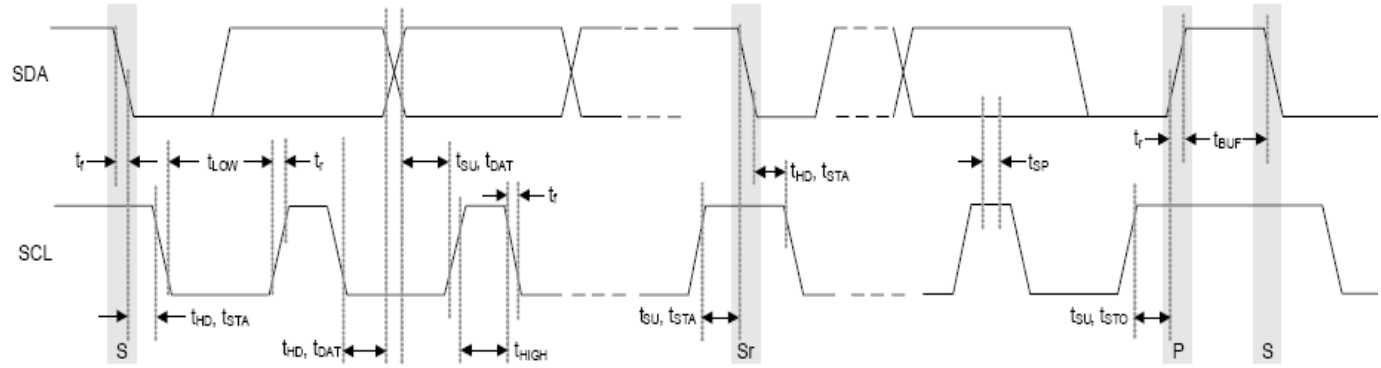
NOTE: For F/S-mode I2C-compatible bus devices[1].

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{HD, STA}$	Hold time (repeated) start condition. The first clock pulse is generated after this period.	4.0	--	-0.6	--	µs
t_{LOW}	SCL clock low period	4.7	--	1.3	--	µs
t_{HIGH}	SCL clock high period	4.0	--	0.6	--	µs
$t_{SU, STA}$	Setup time for repeated start condition	4.7	--	0.6	--	µs
$t_{HD, DAT}$	Data hold time (CBus-compatible masters)	5.0	--	--	--	µs
	Data hold time (I^2C-compatible devices)	0(2)	3.45(3)	0(2)	0.9(3)	µs
$t_{SU, DAT}$	Data setup time	250	--	100(4)	--	ns
t_r	Rise time of both SDA and SCL signals	--	1000	20+0.1Cb(5)	300	ns
t_f	Fall time of both SDA and SCL signals	--	300	20+0.1Cb(5)	300	ns
$t_{SU, STO}$	Setup time for stop condition	4.0	--	0.6	--	µs
t_{BUF}	Bus free time between a stop and start condition	4.7	--	1.3	--	µs
C_b	Capacitive load for each bus line	--	400	--	400	pF
V_{nL}	Noise margin at low level for each connected device (inlcuding hysteresis)	0.1Vdd	--	0.1Vdd	--	V
V_{nH}	Noise margin at high level for each connected device (inlcuding hysteresis)	0.2Vdd	--	0.2Vdd	--	V

1. All values refer to VIHmin and VILmax levels.
2. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum tHD, DAT must only be met if the device does not stretch the low period (tLOW) of the SCL signal.
4. A fast mode I2C-compatible bus device can be used in a standard mode I2C-compatible bus system, as long as the tSU;DAT ≥250 ns requirement is met. This will automatically be the case if the device does not stretch the low period of the SCL signal. If the device does stretch the low period, it must output the next data bit to the SDA line, tr max + tSU;DAT = 1000 + 250 = 1250 ns (per standard mode I2C-compatible bus specification) before the SCL line is released.
5. Cb = total capacitance of one bus line (pF). If mixed with Hs-mode devices, faster fall times are allowed.

Figure 7: I2C-Compatible Timing Data Protocol Timing Diagram



3.3.3 PCM Interface Specifications

Figure 8: PCM Timing Specification—Master Mode

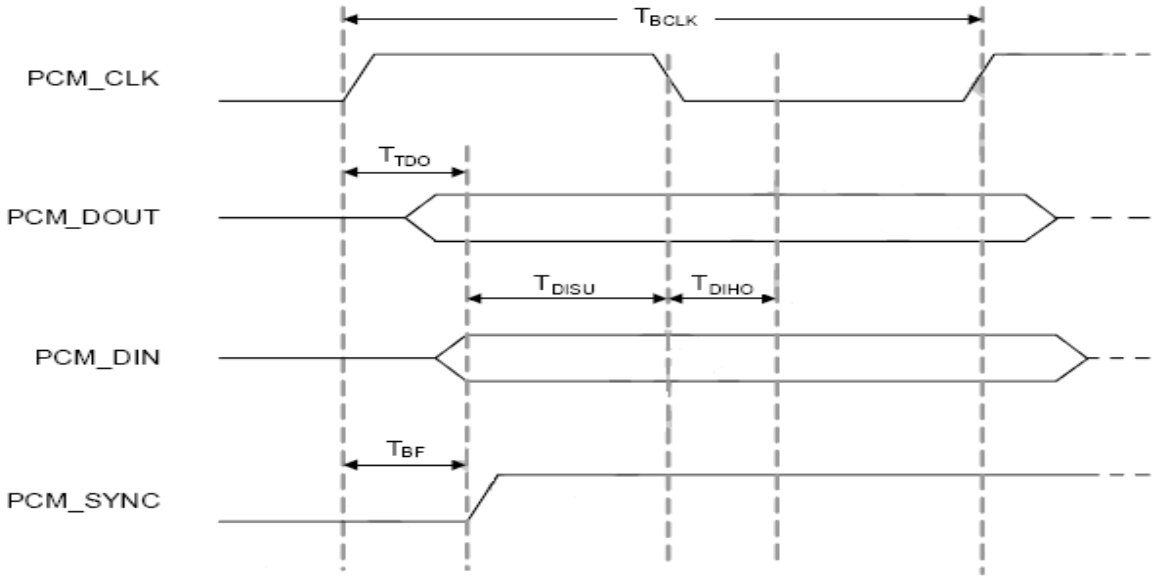


Table 15: PCM Timing Specification—Master Mode

Symbol	Condition	Min	Typ	Max	Units
F_{BCLK}	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	--	--	3	--	ns
T_{DO}	--	--	--	15	ns
T_{DISU}	--	20	--	--	ns
T_{DIHO}	--	15	--	--	ns
T_{BF}	--	--	--	15	ns

Figure 9: PCM Timing Specification—Slave Mode

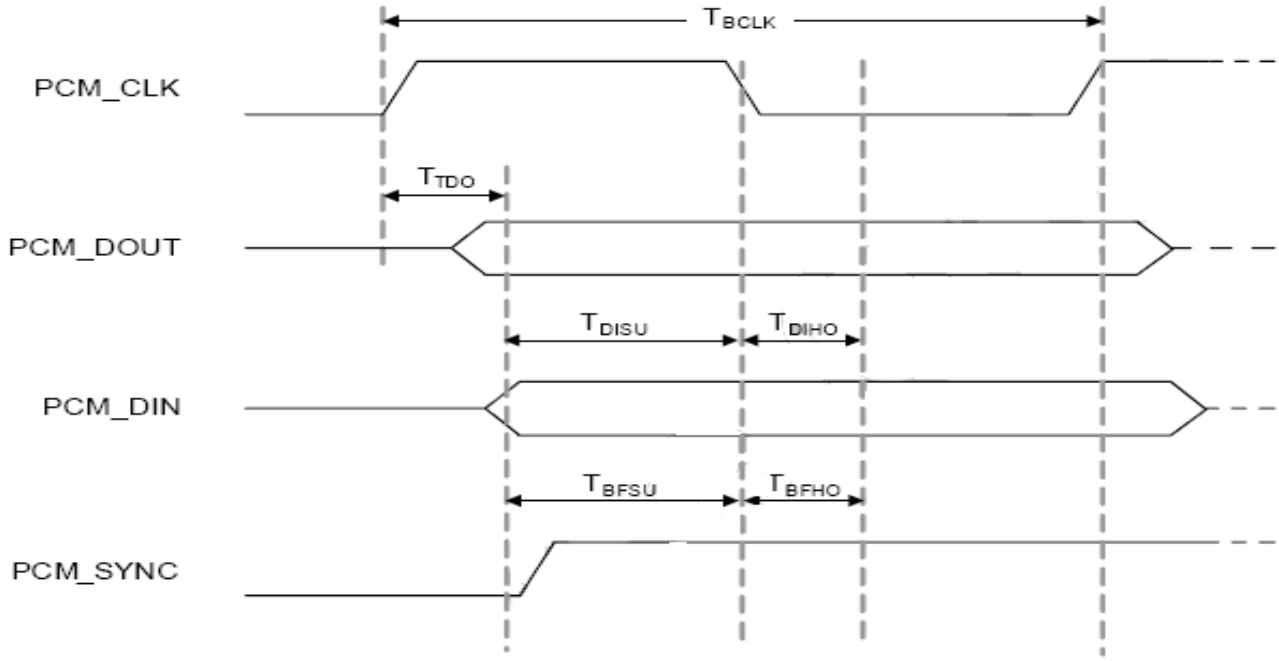


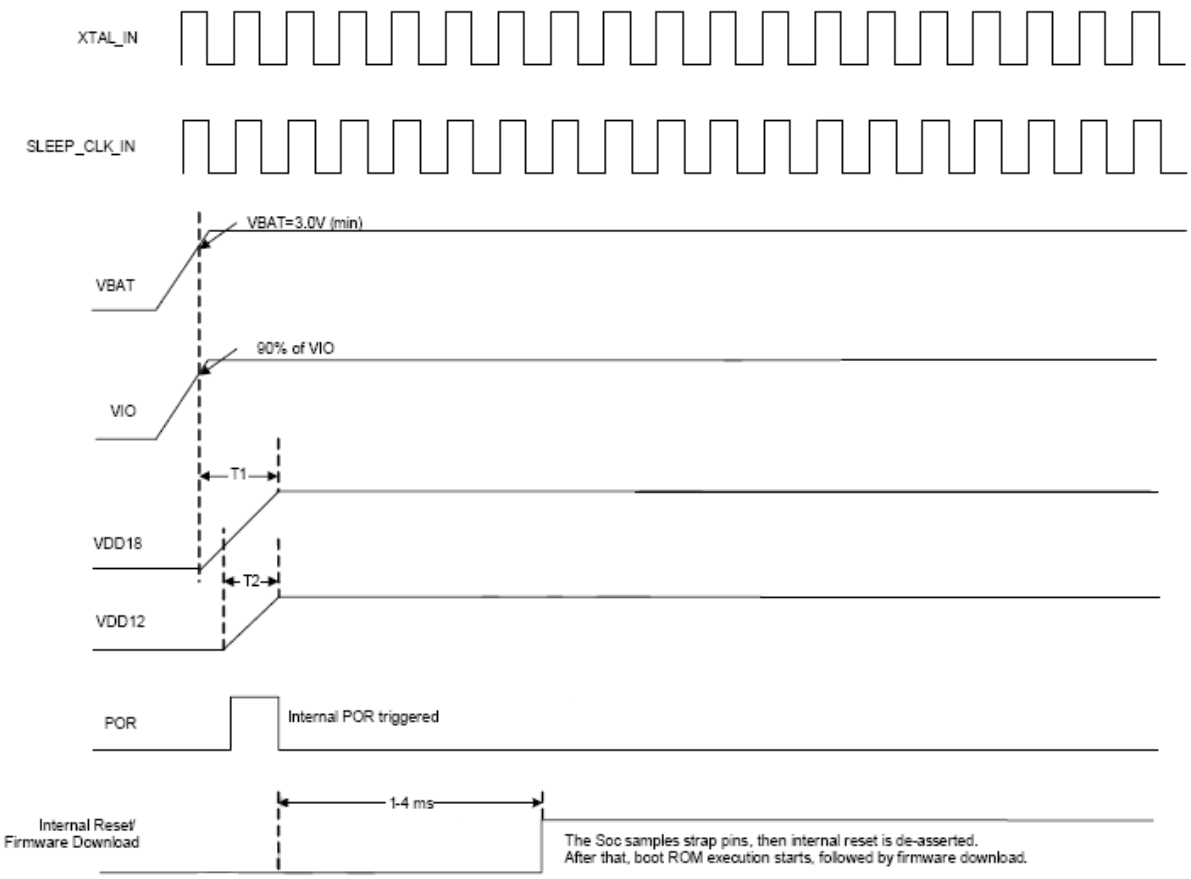
Table 16: PCM Timing Specification—Slave Mode

Symbol	Condition	Min	Typ	Max	Units
F_{BCLK}	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	--	--	3	--	ns
T_{DO}	--	--	--	30	ns
T_{DISU}	--	15	--	--	ns
T_{DIHO}	--	10	--	--	ns
T_{BFSU}	--	15	--	--	ns
T_{BFHO}	--	10	--	--	ns

3.4.Power up sequence

The following requirements must be met for for correct power up:

- VDD33/VIO must be stable before VDD18 ramp up
- VDD18 is used as input to LVLDO, which outputs VDD12
  - Ramp up time required for VDD18 is T1 < 240 µs
  - Output load on VDD12 should be 1 µF–10 µF
  - Ramp up time of VDD12 will be T2 = 100 µs (minimum) for this load condition
- Ensure XTAL_IN is stable before VDD12 ramp up
- For auto reference clock detection, SLEEP_CLK_IN (32.768 KHz) must be used and must be stable before VDD12 ramp up
- PDn and RESETn should be inactive values (asserted high)



In cases where above power up sequence cannot be met, the PDn signal can be used for “Alternate Power Up Sequence”. The following requirements must be met:

- PDn must be asserted low until VDD30, VIO, and VDD18 are stable
- SLEEP_CLK_IN and XTAL_IN must be stable, and then PDn should be de-asserted
- Ensure VDD12 ramp up time T > 20 µs for proper internal POR generation
- For auto reference clock detection, the sleep clock (32.768 KHz) must be used and must be
- stable before VDD12 ramp up for internal VDD12 (using LVLDO)
- RESETn should be inactive value (asserted high)
- Figure 10 shows the sequence when using an internal VDD12 supply (from LVLDO)
- Figure 11 shows the sequence when using all external supplies

Figure 10: Power Option—Alternate (PDn with internal VDD12)

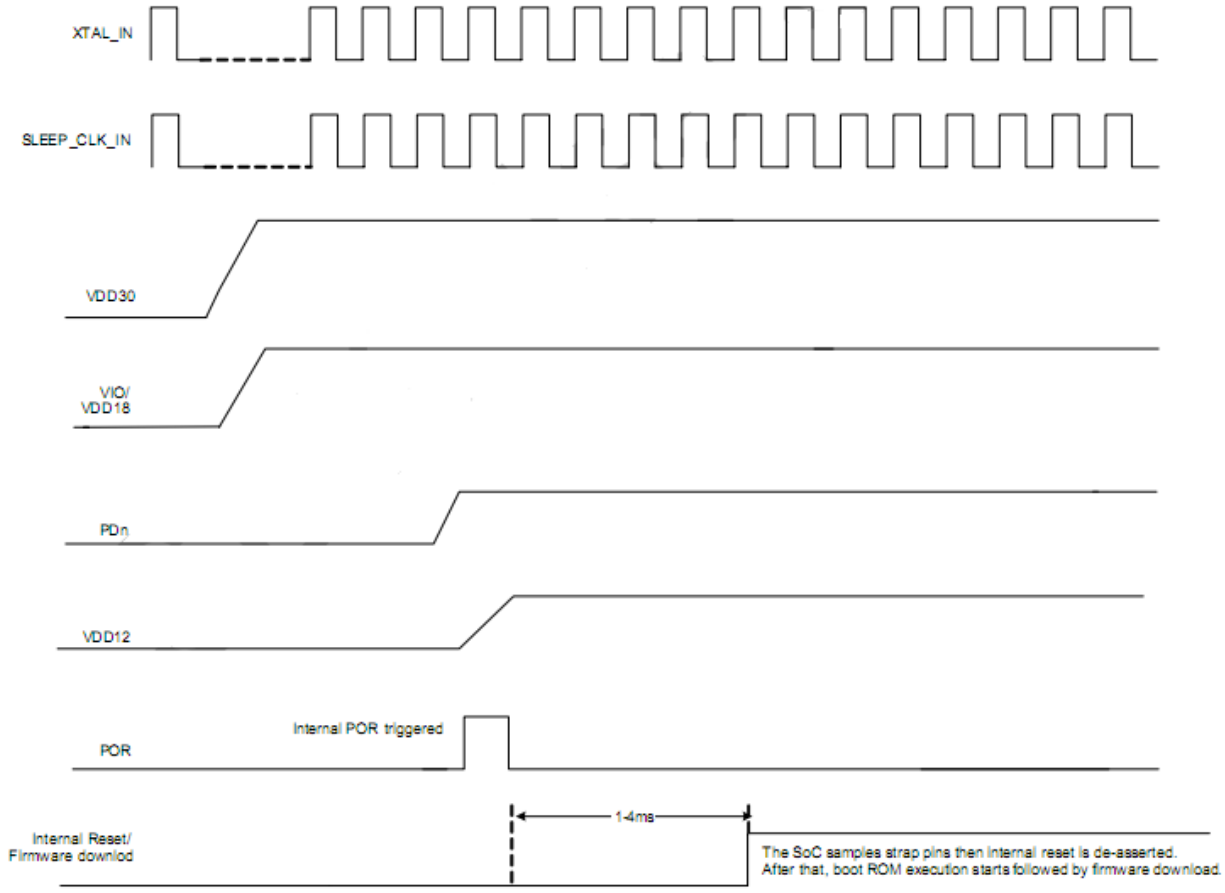
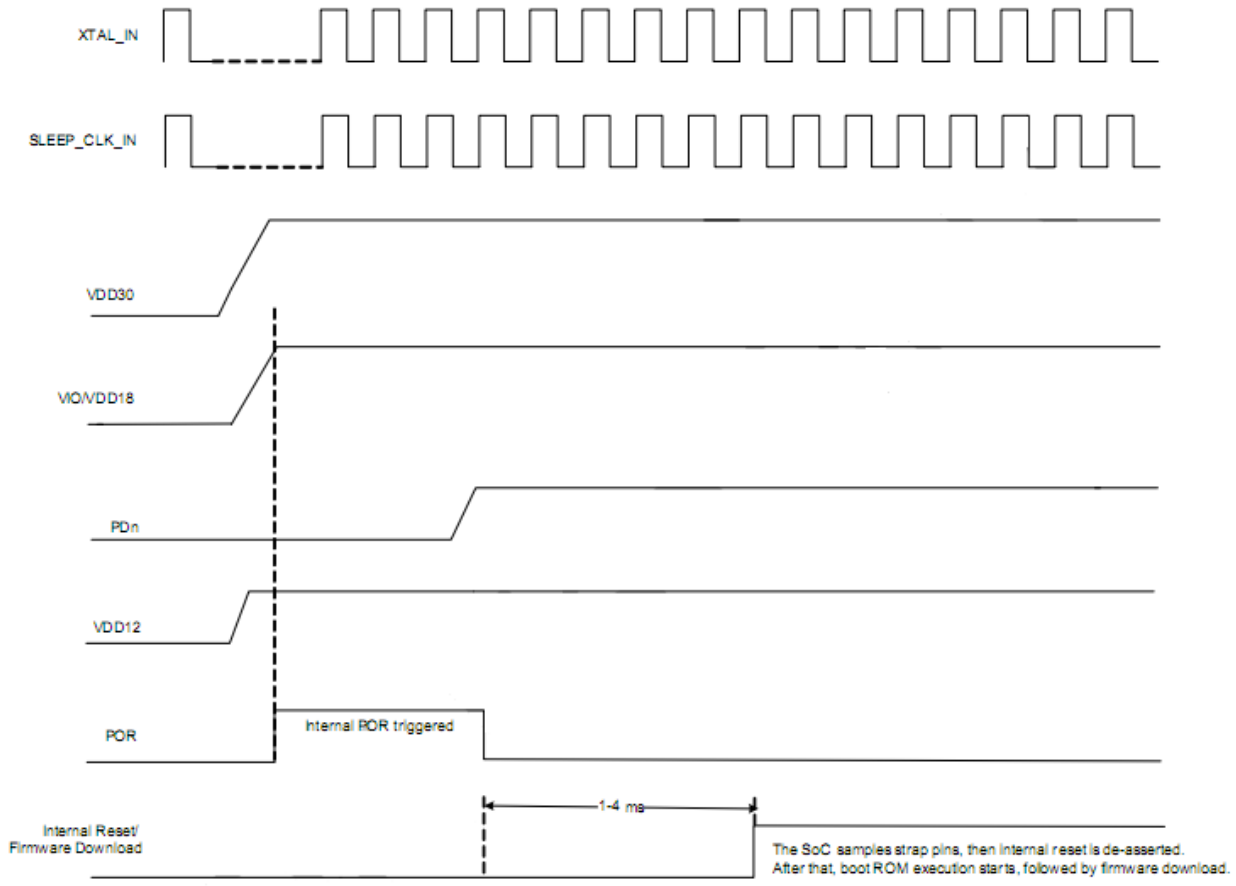


Figure 11: Power Option—Alternate (PDn with all external supplies)



4 Software Requirements

The software includes firmware, driver and configuration utility for Wireless WLAN 802.11 b/g/n + Bluetooth Module based on Marvell 88W8787-W16CBJ2-T chip

4.1 Software setup

The software components required for operations will be packed into one installation program, thus user and customer can setup and upgrade software simply by running the setup program (ex. Setup.exe) without any obstacles.

4.2 Operating System Support

All software components, including the installer will work on Microsoft Windows XP SP2. Driver for some common Linux systems is also supported, such as Fedora 5. Other Operate Systems (such as Android) will be supported if required by customer.

4.3 Software Functions

For WLAN part, the WLAN configuration utility will include the Link Statistics Software, thus customers can evaluate various PHY performance parameters independent of system performance. This utility can also be used to change various WLAN parameters, such as SSID, Band, channel, Data rate, etc. The firmware and driver will fully compliance to the 802.11 published PHY and MAC specifications. It can support the following functions:

- Scan for Wireless Networks
- Connect to a Wireless Network
- Change Profiles
- Support security standards such as, WEP, WPA, WPA2, WPA-PSK, and WPA2-PSK.
- Support WAPI
- Support Marvell Bluetooth coexistence

For Bluetooth part, a fully working Configuration Utility is supplied. It is:

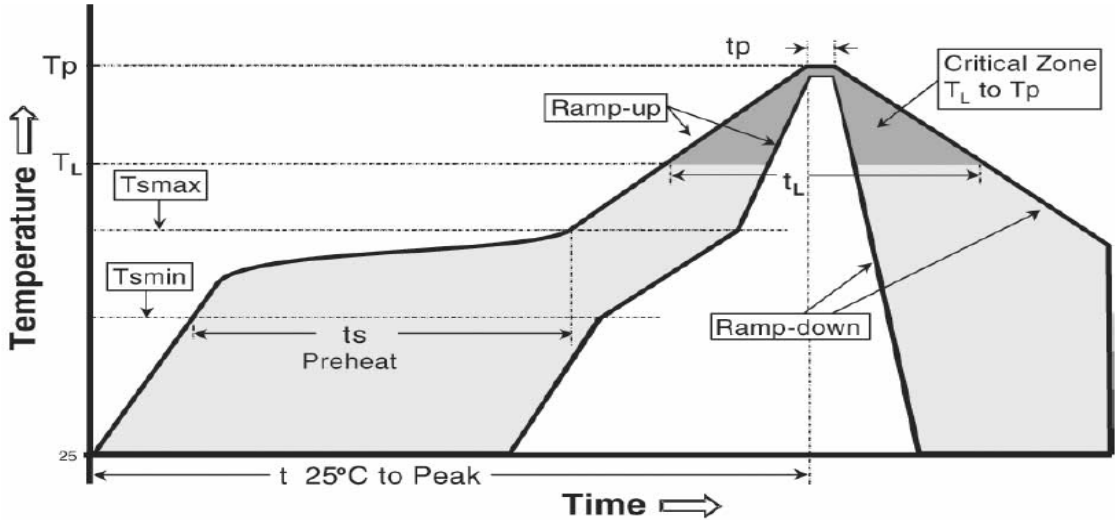
- Fully compliant with Bluetooth 3.0 + High Speed (HS) (also compliant with Bluetooth 2.1 + EDR) specifications up to HCI (Host Controller Interface) layer
- Support all standard operations: Inquiry scan, page scan, paring, authentication, link key, and encryption
- Support many approved features of Bluetooth 3.0+HS release (Link Supervision Timeout, Encryption Pause/Resume, Extended Inquiry Response, Sniff Sub Rating)
- Support all Bluetooth low power operation modes. (ie, hold, sniff, and park with configurable intervals).
- Support sleep and standby modes for ultra low-power operation.

For FM part, a fully working Configuration Utility is supplied. It is:

- Compatibility with Europe/US (87.5-108 MHz) and Japan (76-90 MHz) FM Bands
- integrated RDS/RDBS features

5. Recommend Reflow Profile

Referred to IPC/JEDEC standard.
Reflow times<= 2times.



Profile Feature	Pb-Free Assembly
Average ramp-up rate (Tsmax to Tp)	3° C/second max.
Preheat - Temperature Min (Ts_{min}) - Temperature Max (Ts_{max}) - Time (Ts_{min} to Ts_{max}) (ts)	 150 °C 200 °C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	 217 °C 60-150 seconds
Peak Temperature (Tp)	See Table 4.2
Time within 5°C of actual Peak Temperature $(tp)^2$	20-40 seconds
Ramp-down Rate	6 °C/second max.
Time 25°C to Peak Temperature	8 minutes max.

Table 4-2 Pb-free Process - Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 < 350	Volume mm^3 350 - 2000	Volume mm^3 > 2000
< 1.6 mm	260 °C *	260 °C *	260 °C *
1.6 mm - 2.5 mm	260 °C *	250 °C *	245 °C *
> 2.5 mm	250 °C *	245 °C *	245 °C *
* Tolerance: The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature at the rated MSL level			

6.MSL/Storage Condition

CAUTION
This bag contains
MOISTURE-SENSITIVE DEVICES

LEVEL **3**

If Blank, see adjacent bar code label

1. Calculated shelf life in sealed bag: 12 months at < 40°C and < 90% relative humidity (RH)
2. Peak package body temperature: 260 °C
   If Blank, see adjacent bar code label
3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must
   a) Mounted within: 168 hrs. of factory conditions
      If Blank, see adjacent bar code label
      ≤ 30°C/60%RH, OR
   b) Stored at <10% RH
4. Devices require bake, before mounting, if:
   a) Humidity Indicator Card is > 10% when read at 23 ± 5°C
   b) 3a or 3b not met.
5. If baking is required, devices may be baked for 48 hrs. at 125 ± 5°C

   Note: If device containers cannot be subjected to high temperature or shorter bake times are desired, reference IPC/JEDEC J-STD-033 for bake procedure

Bag Seal Date: _____
If Blank, see adjacent bar code label

Note: Level and body temperature defined by IPC/JEDEC J-STD-020

7.Packing Specifications (TBD)