* Freescale MSI interrupt controller

Required properties:
- compatible : compatible list, contains 2 entries,
  first is "fsl,CHIP-msi", where CHIP is the processor(mpc8610, mpc8572,
  etc.) and the second is "fsl,mpic-msi" or "fsl,ipic-msi" depending on
  the parent type.
- reg : should contain the address and the length of the shared message
  interrupt register set.
- msi-available-ranges: use <start count> style section to define which
  msi interrupt can be used in the 256 msi interrupts. This property is
  optional, without this, all the 256 MSI interrupts can be used.
- interrupts : each one of the interrupts here is one entry per 32 MSIs,
  and routed to the host interrupt controller. the interrupts should
  be set as edge sensitive.
- interrupt-parent: the phandle for the interrupt controller
  that services interrupts for this device. for 83xx cpu, the interrupts
  are routed to IPIC, and for 85xx/86xx cpu the interrupts are routed
  to MPIC.

Example:

```
        msi@41600 {
                compatible = "fsl,mpc8610-msi", "fsl,mpic-msi";
                reg = <0x41600 0x80>;
                msi-available-ranges = <0 0x100>;
                interrupts = <
                        0xe0 0
                        0xe1 0
                        0xe2 0
                        0xe3 0
                        0xe4 0
                        0xe5 0
                        0xe6 0
                        0xe7 0>;
                interrupt-parent = <&mpic>;
        };
```