

* OpenPIC and its interrupt numbers on Freescale's e500/e600 cores

The OpenPIC specification does not specify which interrupt source has to become which interrupt number. This is up to the software implementation of the interrupt controller. The only requirement is that every interrupt source has to have a unique interrupt number / vector number. To accomplish this the current implementation assigns the number zero to the first source, the number one to the second source and so on until all interrupt sources have their unique number.

Usually the assigned vector number equals the interrupt number mentioned in the documentation for a given core / CPU. This is however not true for the e500 cores (MPC85XX CPUs) where the documentation distinguishes between internal and external interrupt sources and starts counting at zero for both of them.

So what to write for external interrupt source X or internal interrupt source Y into the device tree? Here is an example:

The memory map for the interrupt controller in the MPC8544[0] shows, that the first interrupt source starts at 0x5_0000 (PIC Register Address Map-Interrupt Source Configuration Registers). This source becomes the number zero therefore:

External interrupt 0 = interrupt number 0
External interrupt 1 = interrupt number 1
External interrupt 2 = interrupt number 2

...

Every interrupt number allocates 0x20 bytes register space. So to get its number it is sufficient to shift the lower 16bits to right by five. So for the external interrupt 10 we have:

0x0140 >> 5 = 10

After the external sources, the internal sources follow. The in core I2C controller on the MPC8544 for instance has the internal source number 27. To obtain its interrupt number we take the lower 16bits of its memory address (0x5_0560) and shift it right:

0x0560 >> 5 = 43

Therefore the I2C device node for the MPC8544 CPU has to have the interrupt number 43 specified in the device tree.

[0] MPC8544E PowerQUICC™ III, Integrated Host Processor Family Reference Manual
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