MPC5200 Device Tree Bindings

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Naming conventions

For mpc5200 on-chip devices, the format for each compatible value is <chip>-<device>[-<mode>]. The OS should be able to match a device driver to the device based solely on the compatible value. If two drivers match on the compatible list; the 'most compatible' driver should be selected.

The split between the MPC5200 and the MPC5200B leaves a bit of a How should the compatible property be set up to provide conundrum. maximum compatibility information; but still accurately describe the chip? For the MPC5200; the answer is easy. Most of the SoC devices originally appeared on the MPC5200. Since they didn't exist anywhere else; the 5200 compatible properties will contain only one item; "fs1, mpc5200-<device>".

The 5200B is almost the same as the 5200, but not quite. It fixes silicon bugs and it adds a small number of enhancements. Most of the devices either provide exactly the same interface as on the 5200. devices have extra functions but still have a backwards compatible mode. To express this information as completely as possible, 5200B device trees should have two items in the compatible list: compatible = "fs1, mpc5200b-<device>", "fs1, mpc5200-<device>";

It is *strongly* recommended that 5200B device trees follow this convention (instead of only listing the base mpc5200 item).

ie. ethernet on mpc5200: compatible = "fsl, mpc5200-fec"; ethernet on mpc5200b: compatible = "fs1, mpc5200b-fec", "fs1, mpc5200-fec";

Modal devices, like PSCs, also append the configured function to the end of the compatible field. ie. A PSC in i2s mode would specify "fsl, mpc5200-psc-i2s", not "fsl, mpc5200-i2s". This convention is chosen to avoid naming conflicts with non-psc devices providing the same function. For example, "fsl, mpc5200-spi" and "fsl, mpc5200-psc-spi" describe the mpc5200 simple spi device and a PSC spi mode respectively.

At the time of writing, exact chip may be either 'fsl, mpc5200' or 'fsl, mpc5200b'.

The soc node

This node describes the on chip SOC peripherals. Every mpc5200 based board will have this node, and as such there is a common naming convention for SOC devices.

Required properties:

name description

Memory range of the internal memory mapped registers. ranges 第 1 页

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Should be <0 [baseaddr] 0xc000> Should be <[baseaddr] 0x100> reg mpc5200: "fs1, mpc5200-immr" compatible

mpc5200b: "fs1, mpc5200b-immr"

'fsystem' frequency in Hz; XLB, IPB, USB and PCI system-frequency

clocks are derived from the fsystem clock.

bus-frequency IPB bus frequency in Hz. Clock rate

used by most of the soc devices.

soc child nodes

Any on chip SOC devices available to Linux must appear as soc5200 child nodes.

Note: The tables below show the value for the mpc5200. A mpc5200b device tree should use the "fsl, mpc5200b- \langle device \rangle ", "fsl, mpc5200- \langle device \rangle " form.

Required soc5200 child nodes:

compatible Description name cdm@<addr> fs1, mpc5200-cdm Clock Distribution interrupt-controller@<addr> fsl, mpc5200-pic need an interrupt controller to boot bestcomm@<addr> fsl, mpc5200-bestcomm Bestcomm DMA controller

Recommended soc5200 child nodes; populate as needed for your board

gpio@ <addr> fsl, mpc5200-gpio-wkup rtc@<addr> fsl, mpc5200-rtc</addr></addr>	name	compatible	Description	
mscan@ <addr> fsl, mpc5200-mscan</addr>	<pre>gpio@<addr> gpio@<addr> rtc@<addr> mscan@<addr></addr></addr></addr></addr></pre>	fsl, mpc5200-gpio fsl, mpc5200-gpio-wkup fsl, mpc5200-rtc fsl, mpc5200-mscan	MPC5200 simple gpio controlle MPC5200 wakeup gpio controlle Real time clock CAN bus controller	
serial@ <addr> fsl,mpc5200-psc-uart PSC in serial mode</addr>	serial@ <addr></addr>	fs1, mpc5200-psc-uart	PSC in serial mode	
i2s@ <addr> fsl, mpc5200-psc-i2s PSC in i2s mode ac97@<addr> fsl, mpc5200-psc-ac97 PSC in ac97 mode</addr></addr>	$ac97@\langle addr \rangle$	fs1, mpc5200-psc-ac97	PSC in ac97 mode	
spi@ <addr> fsl, mpc5200-psc-spi PSC in spi mode irda@<addr> fsl, mpc5200-psc-irda PSC in IrDA mode</addr></addr>	irda@ <addr></addr>	fsl, mpc5200-psc-irda	PSC in IrDA mode	
spi@ <addr> fsl, mpc5200-spi MPC5200 spi device ethernet@<addr> fsl, mpc5200-fec MPC5200 ethernet device</addr></addr>	ethernet@ <addr></addr>	fsl, mpc5200-fec	MPC5200 ethernet device	
ata@ <addr> fsl, mpc5200-ata IDE ATA interface i2c@<addr> fsl, mpc5200-i2c I2C controller</addr></addr>	i2c@ <addr></addr>	fs1, mpc5200-i2c	I2C controller	
usb@ <addr> fsl, mpc5200-ohci, ohci-be USB controller xlb@<addr> fsl, mpc5200-xlb XLB arbitrator</addr></addr>				

fsl, mpc5200-gpt nodes

On the mpc5200 and 5200b, GPTO has a watchdog timer function. If the board design supports the internal wdt, then the device node for GPTO should include the empty property 'fsl, has-wdt'. Note that this does not activate the watchdog. The timer will function as a GPT if the timer api is used, and it will function as watchdog if the watchdog device is used. The watchdog mode has priority over the gpt mode, i.e. if the watchdog is activated, any gpt api call to this timer will fail with -EBUSY.

If you add the property

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 $fsl, wdt-on-boot = \langle n \rangle;$

GPTO will be marked as in-use watchdog, i.e. blocking every gpt access to it. If n>0, the watchdog is started with a timeout of n seconds. If n=0, the configuration of the watchdog is not touched. This is useful in two cases:

- just mark GPTO as watchdog, blocking gpt accesses, and configure it later;
 do not touch a configuration assigned by the boot loader which supervises
- the boot process itself.

The watchdog will respect the CONFIG WATCHDOG NOWAYOUT option.

An mpc5200-gpt can be used as a single line GPIO controller. To do so, add the following properties to the gpt node:

gpio-controller;

 $\#gpio-cells = \langle 2 \rangle;$

When referencing the GPIO line from another node, the first cell must always be zero and the second cell represents the gpio flags and described in the gpio device tree binding.

An mpc5200-gpt can be used as a single line edge sensitive interrupt controller. To do so, add the following properties to the gpt node:

interrupt-controller;

#interrupt-cells = <1>;

When referencing the IRQ line from another node, the cell represents the sense mode; 1 for edge rising, 2 for edge falling.

fsl, mpc5200-psc nodes

The PSCs should include a cell-index which is the index of the PSC in hardware. cell-index is used to determine which shared SoC registers to use when setting up PSC clocking. cell-index number starts at 0. ie: PSC1 has 'cell-index = 0'

PSC4 has 'cell-index = $\langle 3 \rangle$ '

PSC in i2s mode: The mpc5200 and mpc5200b PSCs are not compatible when in i2s mode. An 'mpc5200b-psc-i2s' node cannot include 'mpc5200-psc-i2s' in the compatible field.

fsl, mpc5200-gpio and fsl, mpc5200-gpio-wkup nodes

Each GPIO controller node should have the empty property gpio-controller and #gpio-cells set to 2. First cell is the GPIO number which is interpreted according to the bit numbers in the GPIO control registers. The second cell is for flags which is currently unused.

fsl, mpc5200-fec nodes

The FEC node can specify one of the following properties to configure the MII link:

- fsl, 7-wire-mode An empty property that specifies the link uses 7-wire mode instead of MII
- Specifies that the MII should be configured for a fixed - current-speed This property should contain two cells. first cell specifies the speed in Mbps and the second should be '0' for half duplex and '1' for full duplex
- Contains a phandle to an Ethernet PHY. - phy-handle

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Interrupt controller (fsl, mpc5200-pic) node

The mpc5200 pic binding splits hardware IRQ numbers into two levels. The split reflects the layout of the PIC hardware itself, which groups interrupts into one of three groups; CRIT, MAIN or PERP. Also, the Bestcomm dma engine has it's own set of interrupt sources which are cascaded off of peripheral interrupt 0, which the driver interprets as a fourth group, SDMA.

The interrupts property for device nodes using the mpc5200 pic consists of three cells; $\langle L1\ L2\ level \rangle$

```
L1 := [CRIT=0, MAIN=1, PERP=2, SDMA=3]
L2 := interrupt number; directly mapped from the value in the "ICTL PerStat, MainStat, CritStat Encoded Register"
level := [LEVEL_HIGH=0, EDGE_RISING=1, EDGE_FALLING=2, LEVEL_LOW=3]
```

For external IRQs, use the following interrupt property values (how to specify external interrupts is a frequently asked question): External interrupts:

```
external irq0: interrupts = <0 0 n>;
    external irq1: interrupts = <1 1 n>;
    external irq2: interrupts = <1 2 n>;
    external irq3: interrupts = <1 3 n>;
'n' is sense (0: level high, 1: edge rising, 2: edge falling 3: level low)
```

fsl, mpc5200-mscan nodes

See file can. txt in this directory.