# 0. Overview

The SH7760/SH7763 have an integrated LCD Display controller (LCDC) which supports (in theory) resolutions ranging from 1x1 to 1024x1024, with color depths ranging from 1 to 16 bits, on STN, DSTN and TFT Panels.

#### Caveats

- \* Framebuffer memory must be a large chunk allocated at the top of Area3 (HW requirement). Because of this requirement you should NOT make the driver a module since at runtime it may become impossible to get a large enough contiguous chunk of memory.
- \* The driver does not support changing resolution while loaded (displays aren't hotpluggable anyway)
- \* Heavy flickering may be observed
  - a) if you're using 15/16bit color modes at  $\geq 640$ x480 px resolutions,
  - b) during PCMCIA (or any other slow bus) activity.
- \* Rotation works only 90degress clockwise, and only if horizontal resolution is <= 320 pixels.

files: drivers/video/sh7760fb.c

include/asm-sh/sh7760fb.h Documentation/fb/sh7760fb.txt

# 1. Platform setup

### SH7760:

Video data is fetched via the DMABRG DMA engine, so you have to configure the SH DMAC for DMABRG mode (write 0x94808080 to the DMARSRA register somewhere at boot).

PFC registers PCCR and PCDR must be set to peripheral mode. (write zeros to both).

The driver does NOT do the above for you since board setup is, well, job of the board setup code.

## 2. Panel definitions

The LCDC must explicitly be told about the type of LCD panel attached. Data must be wrapped in a "struct sh7760fb\_platdata" and passed to the driver as platform\_data.

Suggest you take a closer look at the SH7760 Manual, Section 30. (http://documentation.renesas.com/eng/products/mpumcu/e602291 sh7760.pdf)

The following code illustrates what needs to be done to get the framebuffer working on a 640x480 TFT:

```
#include ux/fb.h>
#include <asm/sh7760fb.h>
 * NEC NL6440bc26-01 640x480 TFT
  dotclock 25175 kHz
                                                  480
 * Xres
                        640
                                 Yres
 * Htotal
                800
                                         525
                        Vtotal
 * HsynStart
                        VsynStart
                                         490
                656
 * HsynLenn
                30
                        VsynLenn
 * The linux framebuffer layer does not use the syncstart/synclen
 * values but right/left/upper/lower margin values. The comments
 st for the x margin explain how to calculate those from given
 * panel sync timings.
static struct fb_videomode n16448bc26 = {
       . name
                        = "NL6448BC26",
                        = 60,
       .refresh
                        = 640,
       .xres
       .yres
                        = 480,
                        = 39683,
       .pixclock
                                         /* in picoseconds! */
       .hsync_len
                        = 30,
                        = 2,
       .vsvnc len
                                /* HTOT - (HSYNSLEN + HSYNSTART) */
       .left margin
                        = 114.
       .right margin
                        = 16,
                                /* HSYNSTART - XRES */
                                /* VTOT - (VSYNLEN + VSYNSTART) */
       .upper margin
                        = 33,
                        = 10, /* VSYNSTART - YRES */
= FB_SYNC_HOR_HIGH_ACT | FB_SYNC_VERT_HIGH_ACT,
                        = 10,
       .lower_margin
       .sync
       . vmode
                        = FB VMODE NONINTERLACED,
                        = 0,
       .flag
};
static struct sh7760fb platdata sh7760fb nl6448 = {
       .def mode
                        = &n16448bc26,
                        = LDMTR_TFT_COLOR_16,
= LDDFR_8BPP,
       .ldmtr
                                                  /* 16bit TFT panel */
       .lddfr
                                                  /* we want 8bit output */
       .ldpmmr
                        = 0x0070,
       .ldpspr
                        = 0x0500,
       .ldaclnr
                        = LDICKR CLKSRC (LCDC CLKSRC EXTERNAL)
       .ldickr
                          LDICKR CLKDIV(1),
       .rotate
                        = 0,
                        = 1,
       . novsync
       .blank
                        = NULL,
}:
/* SH7760:
 * 0xFE300800: 256 * 4byte xRGB palette ram
 * 0xFE300C00: 42 bytes ctrl registers
static struct resource sh7760_lcdc res[] = {
       [0] = \{
                . start = 0xFE300800,
                        = 0xFE300CFF,
                . end
                .flags = IORESOURCE MEM,
                                       第 2 页
```

```
sh7760fb.txt
         },
[1] = {
                    . start = 65,
                    . end
                             = 65,
                    .flags = IORESOURCE_IRQ,
         },
static struct platform_device sh7760_lcdc_dev = {
         . dev
                    .platform_data = &sh7760fb_n16448,
         },
         .name = "sh7760-lcdc",
.id = -1,
.resource = sh7760_lcdc_res,
.num_resources = ARRAY_SIZE(sh7760_lcdc_res),
```

};

};