Freescale SoC SEC Security Engines

Required properties:

- compatible : Should contain entries for this and backward compatible
  SEC versions, high to low, e.g., "fsl,sec2.1", "fsl,sec2.0"
- reg : Offset and length of the register set for the device
- interrupts : the SEC's interrupt number
- fsl,num-channels : An integer representing the number of channels
  available.
- fsl,channel-fifo-len : An integer representing the number of
  descriptor pointers each channel fetch fifo can hold.
- fsl,exec-units-mask : The bitmask representing what execution units
  (EUs) are available. It's a single 32-bit cell. EU information
  should be encoded following the SEC's Descriptor Header Dword
  EU_SEL0 field documentation, i.e. as follows:

        bit 0 = reserved - should be 0
        bit 1 = set if SEC has the ARC4 EU (AFEU)
        bit 2 = set if SEC has the DES/3DES EU (DEU)
        bit 3 = set if SEC has the message digest EU (MDEU/MDEU-A)
        bit 4 = set if SEC has the random number generator EU (RNG)
        bit 5 = set if SEC has the public key EU (PKEU)
        bit 6 = set if SEC has the AES EU (AESU)
        bit 7 = set if SEC has the Kasumi EU (KEU)
        bit 8 = set if SEC has the CRC EU (CRCU)
        bit 11 = set if SEC has the message digest EU extended alg set (MDEU-B)

remaining bits are reserved for future SEC EUs.

- fsl,descriptor-types-mask : The bitmask representing what descriptors
  are available. It's a single 32-bit cell. Descriptor type information
  should be encoded following the SEC's Descriptor Header Dword DESC_TYPE
  field documentation, i.e. as follows:

        bit 0 = set if SEC supports the aesu_ctr_nonsnoop desc. type
        bit 1 = set if SEC supports the ipsec_esp descriptor type
        bit 2 = set if SEC supports the common_nonsnoop desc. type
        bit 3 = set if SEC supports the 802.11i AES ccmp desc. type
        bit 4 = set if SEC supports the hmac_snoop_no_afeu desc. type
        bit 5 = set if SEC supports the srtp descriptor type
        bit 6 = set if SEC supports the non_hmac_snoop_no_afeu desc.type
        bit 7 = set if SEC supports the pkeu_assemble descriptor type
        bit 8 = set if SEC supports the aesu_key_expand_output desc.type
        bit 9 = set if SEC supports the pkeu_ptmul descriptor type
        bit 10 = set if SEC supports the common_nonsnoop_afeu desc. type
        bit 11 = set if SEC supports the pkeu_ptadd_dbl descriptor type

  ..and so on and so forth.

Optional properties:

- interrupt-parent : the phandle for the interrupt controller that
  services interrupts for this device.

Example:

```
/* MPC8548E */
crypto@30000 {
        compatible = "fsl,sec2.1", "fsl,sec2.0";
        reg = <0x30000 0x10000>;
        interrupts = <29 2>;
        interrupt-parent = <&mpic>;
        fsl,num-channels = <4>;
        fsl,channel-fifo-len = <24>;
        fsl,exec-units-mask = <0xfe>;
        fsl,descriptor-types-mask = <0x12b0ebf>;
};
```