FFT processor top level diagram:

The N-point FFT processor is interfaced with two sets of RAM memory banks:

a. Memory bank A (RAM0, RAM1, RAM2, RAM3)
b. Memory bank B (RAM4, RAM5, RAM6, RAM7)

Each memory bank is configured at the design time based on the maximum number of FFT point computation supported. The input data values are distributed among different RAM banks in each of the sets. The resulting data from FFT computation are stored back into the memory banks. There are 4 memory banks in each set (A & B) because there are two butterfly units in the FFT processor which require 4 data values in each clock cycle for butterfly operation. In each stage of FFT computation the input values to butterfly units are read from one set (for example set A) and the result of butterfly operation is written to the other set (set B). And in the next stage the input values to butterfly units are read from set B and the output values are written to set A. Likewise input values read from and output values are written into different sets in consecutive stages. This procedure is carried out until all the stages in FFT computation are done.

There are two ROM units (ROM0, ROM1) for storing twiddle factor values. Since there are two butterfly units they require two twiddle factors in each clock cycle for butterfly operation. The twiddle factor values are read from these ROM units and supplied to butterfly units for computation in each clock cycle.

FFT processor internal diagram:

The FFT processor internal components include the following units:

a. **Address generation unit:** This unit generates 4 read addresses corresponding to input values supplied to butterfly units and 4 write addresses corresponding to output values from butterfly units to be stored in the memory. It knows the number of stages involved based on the number of FFT points (N) specified and accordingly generates addresses for all the stages required to carry out FFT computation.

b. **Control unit:** This unit generated control signals required to carry out the FFT computation. The read-write control signal for memory read-write operation, the multiplexer select signals required by the interconnect unit are generated by it. Again this unit is intelligent enough to know the number stages based on the number of FFT points (N) specified by the user.

c. **Interconnect:** The interconnect unit is the mediator between the memory units and the butterfly units. It routes the address and data values to the memory units and to the butterfly units based on the control signals received from the control unit.

d. **Butterfly unit:** The butterfly units perform the actual butterfly operation required in each stage of FFT computation. It accepts input values from read from the memory and after computation sends the result to interconnect unit which routes it to suitable memory bank for storage.