Thesis maturity test

Thesis topic:
Design and implementation of scalable FFT processor for wireless applications

The FFT operation is a very complex and computationally intensive operation. It is mainly required in baseband signal processing in a communication system. It requires to be implemented in dedicated and optimized hardware to meet the timing, cost, area and power constraints. So, this is where the challenge arises for the digital design and communication engineers to figure out the best possible solution for the application in hand. The applications for FFT are mainly the wireless applications which adopt wireless standards such as WLAN (802.11), GSM, 3G and recently the LTE. The extensive research in the field of baseband signal processing has resulted in the new standards which provide increasingly high speed access over wireless networks. And in this regard FFT computation is still an active and challenging area of research in the baseband signal processing for the digital design engineers. And this is the motivation behind taking this topic as the thesis work.

The scope of the thesis work is to design and implement a 16-bit, fixed point, radix-2 N-point FFT processor. It is designed to meet the speed, cost, area and power constraints required for wireless applications.

The N-point FFT processor is made up of following components:
a. Control unit
b. Address generation unit
c. Butterfly unit
d. Interconnect
e. RAM memory storage
f. ROM memory storage

The detailed description of each of the following units is given below.

a. Control unit
This unit is the brain behind the entire FFT core. It has intelligence to generate control signals at the required time intervals. The control signals generated by this unit are required by rest of the other units. Based on the number of FFT points it decides the number of stages of computation and the timing of control signals at each stage. It is implemented using the Moore state machine.

b. Address generation unit

This unit is responsible for generating address for FFT samples and twiddle factors. The address generated is routed via interconnect to RAM and ROM memory banks to read sample values and twiddle factors respectively. And the generated addresses are also required to store the results back to the RAM memory banks after butterfly computation. There are two butterfly units in the system hence it requires 4 sample values and two twiddle factors. The unit generates 4 addresses to read 4 samples from RAM, 2 addresses to read twiddle factors from ROM and 4 more addresses to store the results back to RAM memory banks. The memory addresses are generated every two clock cycles since the butterfly units take two inputs every two clock cycles.

c. Butterfly unit

It is the central processing unit of the FFT core. It performs the butterfly operation on the input sample values and twiddle factors. There are three inputs and two outputs to the butterfly. In every two clock cycles two new butterfly input samples are read along with a twiddle factor. The results are obtained in every clock cycle hence the throughput is 1. The butterfly unit has 3 pipeline stages in which the first stage performs multiplication, the second and third stages perform addition/subtraction operations. There are two multipliers and 4 adders/subtractors. The multipliers are implemented based on the bit parallel multiplication method.

d. Interconnect

Interconnect is a switch network which routes addresses/data between memory and butterfly units. There are two of them in the core, one is interconnectA which is the interface between RAM memory setA and butterfly units and the other one is interconnectB which is the interface between RAM memory setB and butterfly units. Interconnect routes inputs based on the status of control signals from the control unit.

e. RAM memory storage

The RAM memories are to store the FFT sample values at the input stage, during computation to store partial results and at the end to store the final results after the computation. During the computation the input samples are read from the RAM memory and after the butterfly operation is complete the results are stored back to suitable location. There are two sets of RAM memory storage namely setA and setB. Each of these sets contains 4 memory banks. There are 4 memory banks because of two butterfly units which require 4 input samples for computation. At a given stage of FFT computation input samples to butterfly units are read from one memory set and the resulting butterfly outputs are stored into another memory set. The RAM memory bank size depends on the maximum size of FFT computation required by the application.

f. ROM memory storage

The ROM memories are required to store twiddle factors needed in the butterfly operation. There are two of them namely ROM0 and ROM1 storing twiddle factors corresponding to butterfly unit0 and butterfly unit1 respectively. Again the size of the ROM units depends on the size of the FFT computation required by the application.

The scalable FFT processor or N-point FFT processor is called so because at design time we can choose N = 8, 16, 32, 64, 128, 256... (Should be powers of 2) etc. This kind of FFT computation is also required in the software defined radio applications where in the baseband hardware is configurable according the requirements of the application. And moreover it can be used for wireless applications ranging from WLAN, WiMax, 3G and LTE standards based applications. This is possible due to its scalability which reduces design time, cost and time to market.

The FFT processor developed is an IP core implemented using VHDL which makes it portable across multiple platforms without much fuss. The design implementation is verified by running testbenches and analyzing the behavior using Modelsim simulator from Mentor Graphics Inc. The simulated design is synthesized on Altera Stratix II FPGA using Quartus II tools. The synthesis results provide us with the performance parameters such as speed, cost, area and power consumption. These performance parameters are compared against other existing implementations.

This FFT ASIC processor IP core if can be used to build a SoC along with other signal processing capabilities to form a DSP core which can be used for software defined radio and wireless applications. And furthermore it can be a part of further research work to explore the new and better possibilities for FFT computation required in the field of software defined radio or wireless applications.

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