SASTRA UNIVERSITY

(A University under section 3 of the UGC Act, 1956)

B.Tech. Degree Examinations

November 2017

End Semester

Course Code: **BECCEC 702R01 / MCSCEC 702R01**

Course: **VLSI DESIGN**

Question Paper No. : **B0585** Duration: **3** hours

Max. Marks: **100**

PART – A

Answer all the questions **10 x 2 = 20 Marks**

1. State Moore's law.
2. Write an expression for threshold voltage of a MOS transistor.
3. Compare CMOS transistor with Bi-polar technology.
4. List out the advantages of GaAs over Silicon.
5. Mention the expression for fringing field capacitance observed in MOS transistor.
6. Give the formula for area capacitances of CMOS layers.
7. Write the design rules formed by Mead-Conway.
8. What is the restriction of using NMOS switching logic?
9. Write about the concept of fault-coverage in VLSI testing process.

10. What is IDDQ testing?

PART – B

Answer all the questions **4 x 15 = 60 Marks**

11. With neat diagrams, explain the operations involved in enhancement mode and depletion mode of CMOS transistor.

(OR)

12. (a) How does Body-Effect happen in NMOS devices? Explain it with a diagram. (7)
    (b) Draw and explain Pseudo-NMOS NAND gate and apply appropriate ratio rules. (8)

13. Elaborate all the steps involved in NMOS fabrication process.

(OR)

14. (a) Write the salient features of Gallium Arsenide technology. (5)
    (b) How is sheet-resistance concept applied to MOS transistors and inverters? Give a detailed description of this concept. (10)

15. (a) Explain the concept of switch logic observed in pass transistors and transmission gates. (12)
    (b) List out some architectural issues of CMOS sub-system design and layout. (3)

(OR)

16. (a) Sketch circuit symbols, logic symbols and stick diagrams of NMOS, CMOS and Bi-CMOS inverters. (7)
    (b) Explain all the concepts involved in Pseudo-Static RAM-Register cell with diagrams. (8)

17. (a) Explain fault models and CMOS Bridging faults. (10)
    (b) Write a note on ATPG. (5)

(OR)

18. (a) Write about Observability and Controllability. (5)
    (b) Give the salient features of BIST. (10)

PART – C

Answer the following **1 x 20 = 20 Marks**

19. (a) Write expressions for the following related to MOS transistors: (10)
    (a) Parasitic Capacitance
    (b) Carrier Density in Channel
    (c) Gate Delay
    (d) Maximum Operating Frequency
    (e) Power Dissipation Per Gate.

    (b) Design an n-bit parity generator. Draw the basic block diagram, basic one-bit cell, structured design approach and stick diagram for the same. (10)

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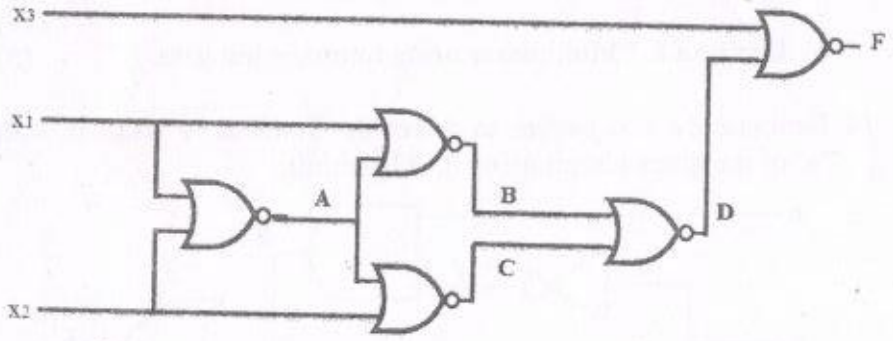
PART – C

Answer the following **1 x 20 = 20 Marks**

17. a) Design the following expression using Dynamic CMOS logic.
$Y = \overline{AB+CD+E}$ (5)

b) Draw the symbolic diagram of BiCMOS inverter. (5)

c) Generate the test pattern to detect the s-a-0 fault in node 'A' of the given circuit using Boolean difference. (10)



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SASTRA DEEMED UNIVERSITY

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End Semester Examinations

Nov 2018

Course Code: **BECCEC 702R02 / MCSCEC 702R02**

Course: **VLSI DESIGN AND TESTING**

Question Paper No. : **B0683** Duration: **3** hours

Max. Marks: **100**

PART – A

Answer all the questions **10 x 2 = 20 Marks**

1. How the original threshold voltage of a MOS device can be adjusted?

2. Realize $Y = \overline{A+BC}$ using dynamic CMOS logic.

3. If W/L ratio of an NMOS transistor is doubled, what will be the change in drain current when
   a) Transistor is operating in linear mode
   b) Transistor operating in saturation mode

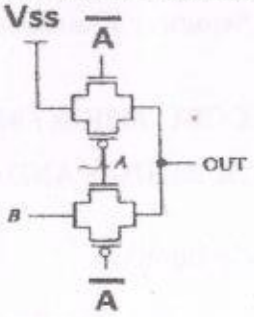
4. A resistor has the following dimensions as drawn:
   Length = 100 microns and Width = 10 microns. The material has a sheet resistance of 80 ohms-per-square. What is its resistance value?

5. Calculate the power dissipated by a circuit if f_{clk} = 40 kHz, V_{DD} = 2 V, C_L (per gate) = 300 fF and the number of logic gates = 10 k.

6. Summarize the effect on subthreshold current due to scaling.

7. Construct the stick diagram of a CMOS inverter.

8. Write the truth table of the following schematic.



9. Differentiate Stuck-at and Stuck-on faults.

10. Why transition count is used in testing?

PART – B

Answer any four questions **4 x 15 = 60 Marks**

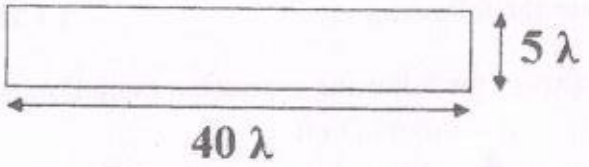
11. a) Implement the following logic expression using Static CMOS logic: (5)

$$X = \overline{(A+B)+\overline{CD}.(A\,.\,B)}$$

b) Find out the threshold voltage of a specific NMOS transistor using the following parameters: (10)
$X_{ox} = 200$ Å , $Qfc = q \times 10^{11}$, $N_A = 10^{15}$ cm^{-3}, $N_{dp} = 10^{19}$ cm^{-3} , $N_{II} = 10^{12}$ and $V_{SB} = 4V$

12. a) For the given area shown in the following figure find out the area capacitance in terms of Cg if the area is:
i) Metal1 ii) Polysilicon iii) Metal 2 iv) Metal 2 to Metal 1
v) Diffusion (active)
Assume 5 µm process. Typical area capacitances are:
Gate to channel = 4×10^{-4}pF/ µm^2, Metal1 = 0.3×10^{-4}pF/µm^2,
Polysilicon = 0.4×10^{-4}pF/ µm^2,

Metal2 = 0.2×10^{-4}pF/ µm^2, Metal2 to Metal1 = 0.4×10^{-4}pF/ µm^2,
Diffusio 0.4×10^{-4}pF/ µm^2



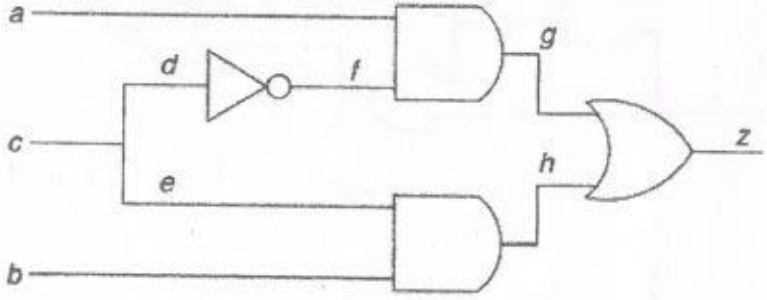
(10)

b) Explain the limitations of scaling on interconnects. (5)

13. a) Explain P-well CMOS fabrication process with neat diagrams. (10)

b) Design a 8:1 Multiplexer using transmission gate. (5)

14. Generate the test pattern to detect the Stuck at '0' fault in node 'a' of the given circuit using D Algorithm.



15. a) Derive expressions for Ids of a MOS transistor operated in three regions. (10)

b) Explain the operation of enhancement mode NMOS transistor with suitable diagram. (5)

16. a) Discuss in detail the design rules for wires and contact cuts. (8)

b) Explain the ad-hoc techniques in design for testability. (7)

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End Semester Examinations

Nov 2018

Course Code: **BECCEC 702R01 / MCSCEC 702R01**

Course: **VLSI DESIGN**

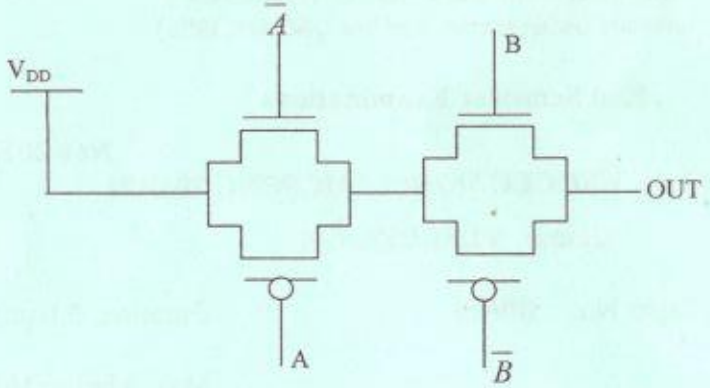
Question Paper No. : **B0680** Duration: **3** hours

Max. Marks: **100**

PART – A

Answer all the questions **10 x 2 = 20 Marks**

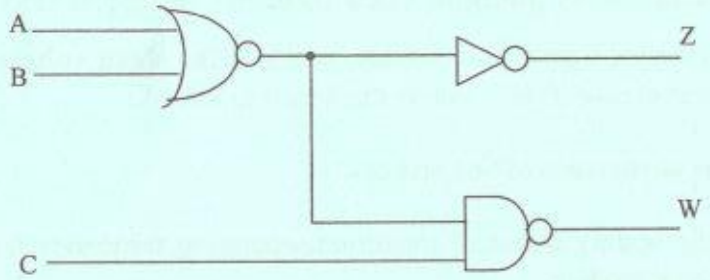
1. How do nMOS and pMOS transistors differ?
2. Give a CMOS implementation of the following function.
   $out = \overline{A}.\overline{B}.C.D$
3. If a depletion PMOS transistor has a threshold voltage of 0.5V when constructed using 200 $\mathring{A}$ oxide, will this threshold voltage increase of decrease if the oxide is thickened to 400°A.
4. List out the advantages of SoI process.
5. Find out the scaling factor of maximum operating frequency(f_0) in all the three models.
6. Provide a truth table that describes the functionality of the circuit in figure 1.



7. Why is polysilicon's parasitic capacitance larger than metal 1s? (Assume the layout of a transistor)

8. A DRAM memory cell should be refreshed after every read of that cell. State True or false.

9. Find the set of all test vectors which detect the stuck-at-1 fault in line C in the given figure.



10. Determine whether leakage current test for chips should be done prior to or after the functional test.

PART – B

Answer all the questions **4 x 15 = 60 Marks**

11. An nMOS, transistor has a device transconductance of $\beta_n = 2.3$ mA/V^2 and a threshold voltage of 0.76V Assume $V_{sBn} = 0V$.
    (a) Find the current if the voltages are set to $V_{asn} = 1$ V, $V_{DSn} = 2.5$ V (5)
    (b) Find the current if the voltages are set to $V_{asn} = 2$ V, $V_{DSn} = 2.5$ V. (5)
    (c) Find the current if the voltages are set to $V_{asn} = 4$ V, $V_{Dsn} = 2.5$ V. (5)

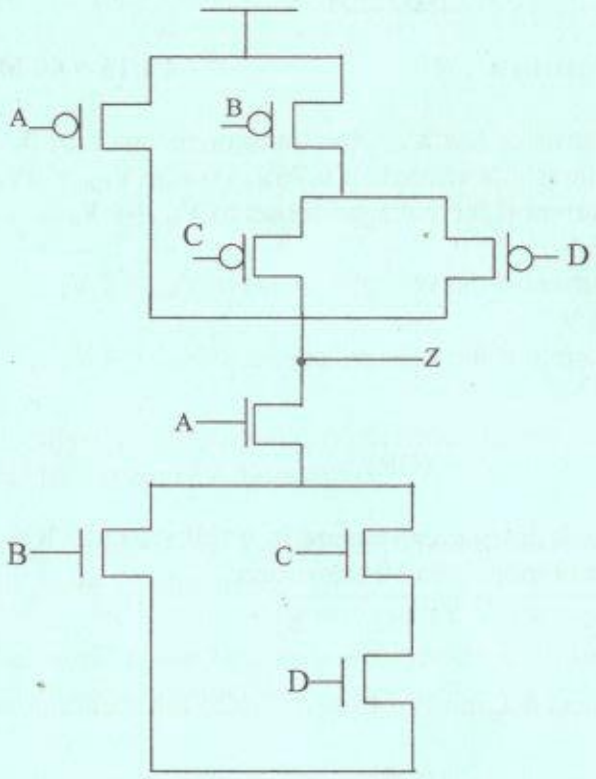
(OR)

12. Implement the following expression in a full static CMOS logic fashion using not more than 10 transistors:
    $Y = \overline{(A.B)+(A.C.E)+(D.E)+(D.C.B)}$

13. Explain with neat diagrams of P-well CMOS fabrication process.

(OR)

14. Size the transistors in the circuit of figure that implements a function $Z = \overline{A(B+CD)}$ so that its worst case current driving capability is equivalent to that of an inverter with $L_p/w_p = 2\lambda/10\lambda = 0.2$ and $L_n/w_n = 2\lambda/4\lambda = 0.5$. Assume that the channel length of all transistors is fixed at 2λ.

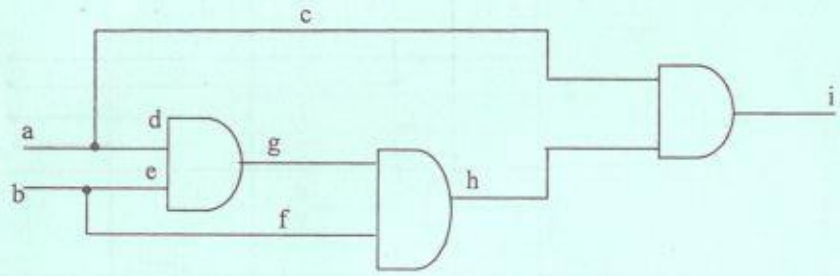


15. Using transmission gates design a circuit whose output is $Out = \left(\overline{A+B+C}\right) + \overline{A}B$ then remove the transistors and switches that are not necessary.

(OR)

16. (a) Draw and explain the operation of 3T DRAM cell. (8)
    (b) With a neat diagram, explain the operation of differential sense amplifier. (7)

17. Using the circuit shown in figure compute the set of all vectors that can detect each of the following faults using Boolean difference: (a) a/1 (b) d/1 (c) g/1. (5 + 5 + 5)



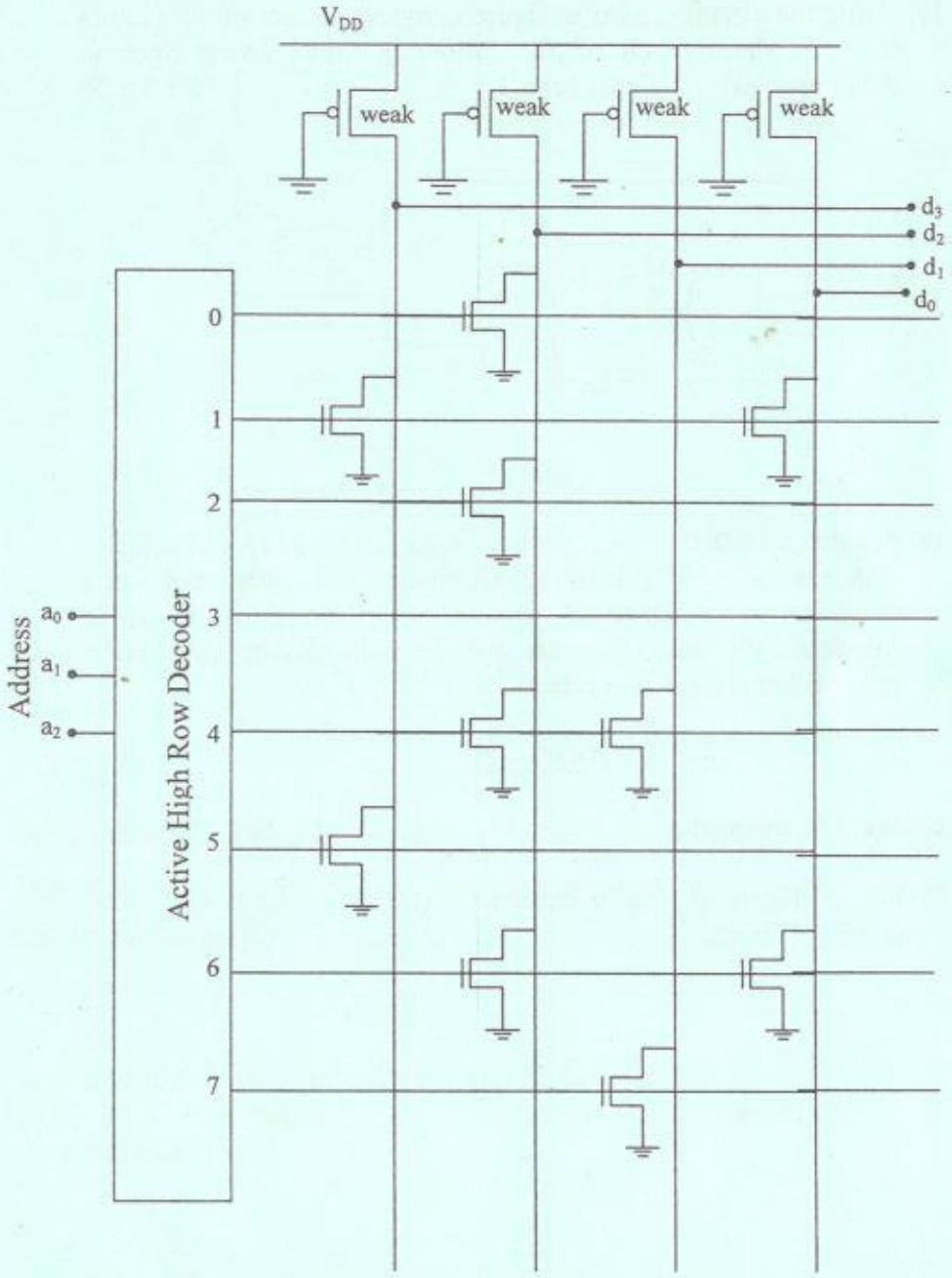
(OR)

18. Assume a fault-free output response R_0 {01101111} and a faulty response R_1= {00110001}. Compute the ones-count and transition count signatures; indicate which compaction scheme can detect the faulty response and show the aliasing probability using either compaction scheme.

PART – C

Answer the following **1 x 20 = 20 Marks**

19. Fill in the truth table at bottom for the following circuit. Also name the circuit.



Address	Data d_3 d_2 d_1 d_0
0	
1	
2	
3	
4	
5	
6	
7	

* * * *

Address	Data d_3 d_2 d_1 d_0
0	
1	
2	
3	
4	
5	
6	
7	

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End Semester Examinations

June 2019

Course Code: **BECCEC 702R01 / MCSCEC 702R01**

Course: **VLSI DESIGN**

Question Paper No. : **B0658** Duration: **3** hours

Max. Marks: **100**

PART – A

Answer all the questions **10 x 2 = 20 Marks**

1. Define Moore's law.

2. Give a CMOS implementation of the following logic function.
$$out = \overline{(A+B).(C+D)}$$

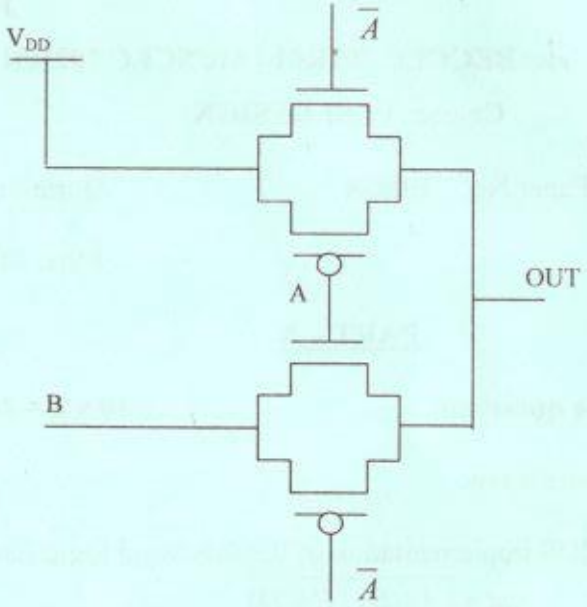
3. If a depletion NMOS transistor has a threshold voltage of -0.5 V when constructed using a 200 $\mathring{A}$ oxide, will this threshold voltage increase or decrease if the oxide is thickened to 400 $\mathring{A}$?

4. Distinguish between the bulk CMOS technology with the SoI technology fabrications.

5. A resistor body has the following dimensions as drawn: length = 95 microns, width = 12 microns. The material has a sheet resistance of 65 Ω/square. When fabricated, the above resistor width measures 0.2 microns smaller than drawn. What is its resistance value?

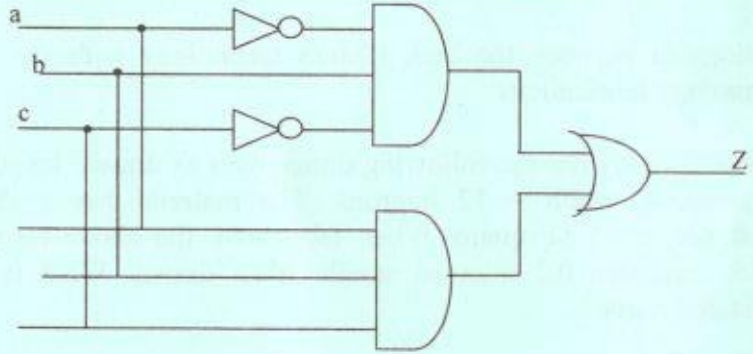
6. Find out the scaling factor of gate capacitance per unit area (C_{ox}) in all the three models.

7. Provide a truth table that described the functionality of the circuit in figure 1.

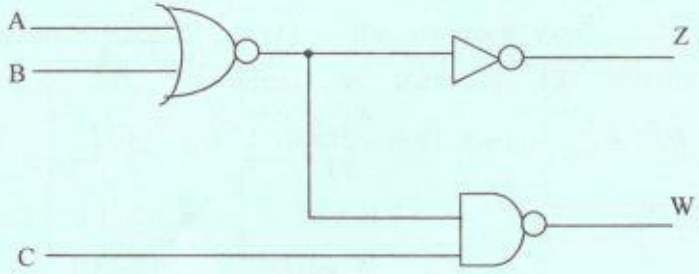


8. The PMOS transistors in a SRAM memory cell generally do not affect read or write speed. State True or False.

9. Consider the combinational logic circuit in figure. How many possible single stuck-at faults does this circuit have.



10. Find the set of all test vectors which detect the stuck-at-0 fault in line B in figure.

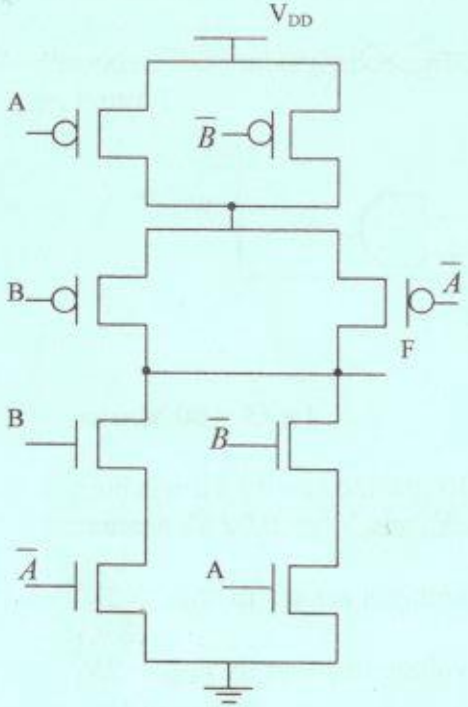


PART – B

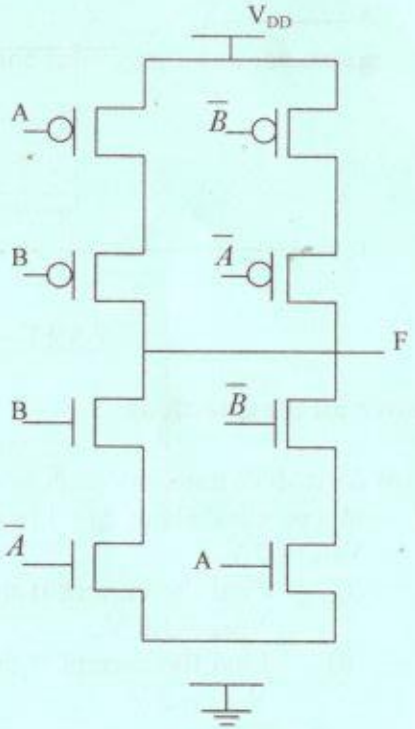
Answer all the questions **4 x 15 = 60 Marks**

11. (a) An nMOS transistor with W = 10 μm and L = 0.35 μm is built in a process where k_n = 110 μA/V^2 and V_{Tn} = 0.70 V. Assume V_{SBn} = 0 V.
    (i) Find the current if the voltages are set to V_{GSn} = 2V, V_{DSn} = 1.0 V. (2 ½)
    (ii) Find the current if the voltages are set to V_{GSn} = 2V, V_{DSn} = 2 V. (2 1/2)

    (b) What is the logic function of circuits A and B in figure? Which one is a dual network and which one is not? Is the nondual network still a valid static logic gate? Explain. List out any 2 advantages of one configuration over the other. (10)



circuit A



circuit B

(OR)

12. Draw the pseudo-nMOS circuits that provide the following logic operations.

(a) $f = \overline{a.b + c}$ (4)

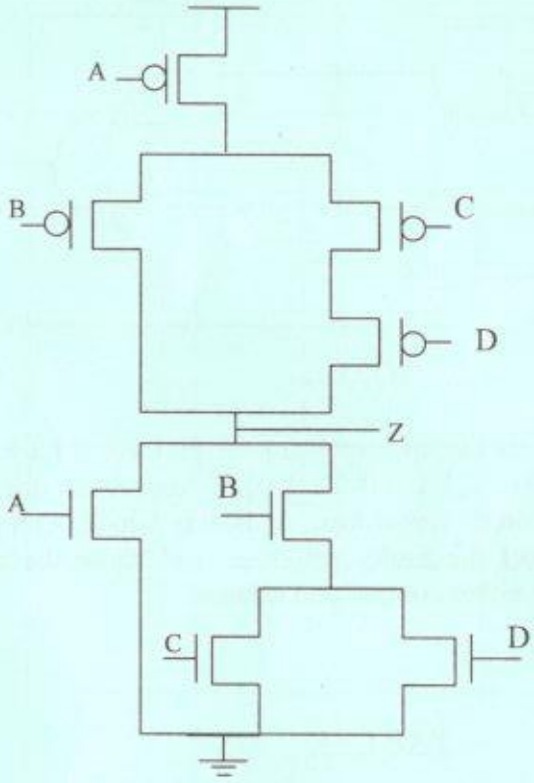
(b) $h = \overline{(a+b+c).x + y.z}$ (5)

(c) $F = \overline{a + \left(c.\left[x + (y.z)\right]\right)}$ (6)

13. Explain with neat diagrams of N-well cMOS fabrication process.

(OR)

14. Size the transistors in the circuit of figure that implements a function $z = \overline{A + B(C + D)}$ so that its worst case current driving capability is equivalent to that of an inverter with $\frac{L_p}{W_p} = \frac{2\lambda}{10\lambda} = 0.2$ and $\frac{L_n}{W_n} = \frac{2\lambda}{4\lambda} = 0.5$. Assume that the channel length of all transistors is fixed at 2 λ.



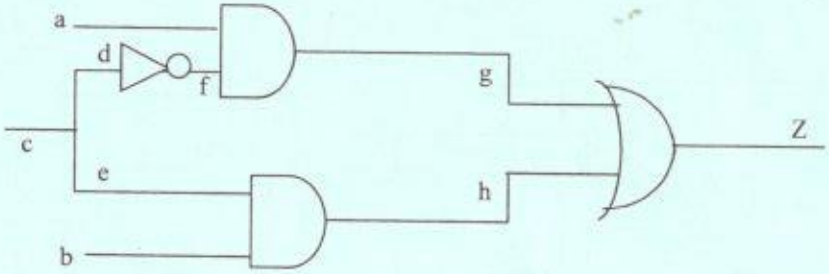
15. Using transmission gates, design a circuit whose output is $Out = \left(\overline{\overline{A + B + \overline{C} + \overline{A}\,\overline{B}}}\right)$. Then remove the transistors and switches that are not necessary.

(OR)

16. Draw and explain the operation of 4T SRAM cell and 6T SRAM cell.

17. Using the circuit shown in figure, compute the set of all vectors that can detect each of the following faults using Boolean difference.

(a) e/o. (7)
(b) e/1. (8)



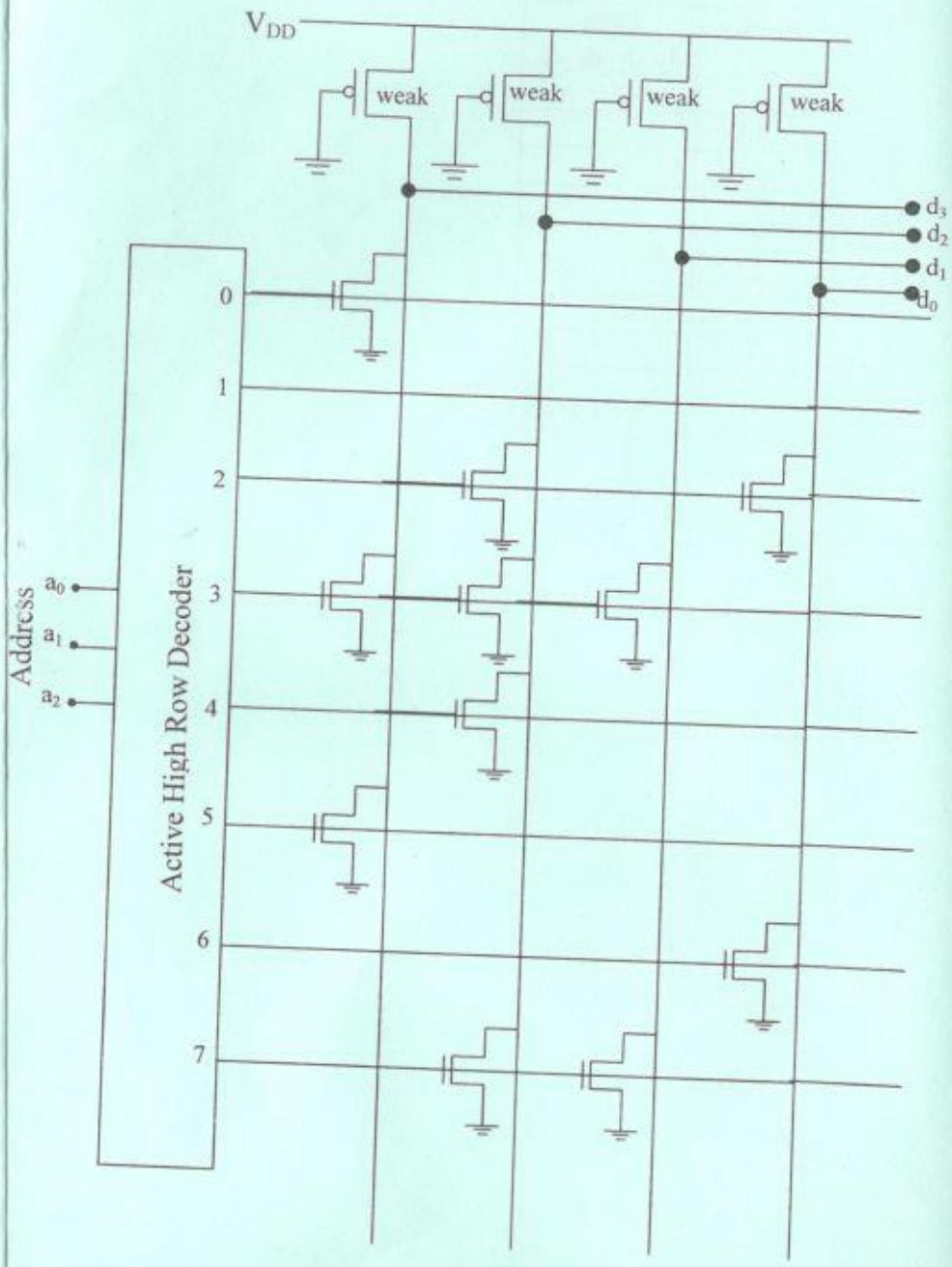
(OR)

18. Assume a fault-free output response $R_0 = \{1\ 1\ 1\ 0\ 0\ 1\ 1\ 0\}$ and a faulty response $R_1 = \{1\ 1\ 0\ 0\ 0\ 1\ 1\ 0\}$. Compute the ones-count and transition-count signatures; indicate which compaction scheme can detect the faulty response, and show the aliasing probability using either compaction scheme.

PART – C

Answer the following **1 x 20 = 20 Marks**

19. Fill in the truth tables at bottom for the following circuit. Also name the circuit.



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End Semester Examinations

June 2019

Course Code: **BECCEC 702R02 / MCSCEC 702R02**

Course: **VLSI DESIGN AND TESTING**

Question Paper No. : **B0661** Duration: **3** hours

Max. Marks**: 100**

PART – A

Answer all the questions **10 x 2 = 20 Marks**

1. Draw the I_D-V_G characteristic for an nMOS enhancement mode and depletion mode transistor.
2. What is drain punch through?
3. Differentiate wet oxidation and dry oxidation.
4. Chart down any four figures of merit of microelectronics technology.
5. What is standard unit of capacitance? What is the significance of it?
6. What is parity generator? Draw the block diagram of parity generator.
7. "Fast circuits consume more area than slow circuits". State whether the statement is true or false and justify your answer.

8. When a fault is termed undetectable?

9. What is the method behind output response analysis using transition count?

10. What are equivalent faults? State the equivalence set for NAND gate.

PART – B

Answer any four questions **4 x 15 = 60 Marks**

11. (a) Derive an expression for the drain current of an enhancement mode nMOS in the non-saturated and saturated region of operation. (11)
    (b) Realize the following Boolean expression using C^2MOS logic $Z = \overline{((A+B)C+D)}$ (4)

12. With neat diagram, explain the steps in the fabrication of CMOS using nwell technology.

13. (a) Derive the scaling factors using constant voltage and constant field model for the following device parameters. (9)
    (i) Power dissipation per gate
    (ii) Maximum operating frequency
    (iii) Channel resistance
    (b) State any six salient features of GaAs technology. (6)

14. With a neat diagram, explain in detail the lambda based design rule for a CMOS technology. Also explain the general observations on the design rules.

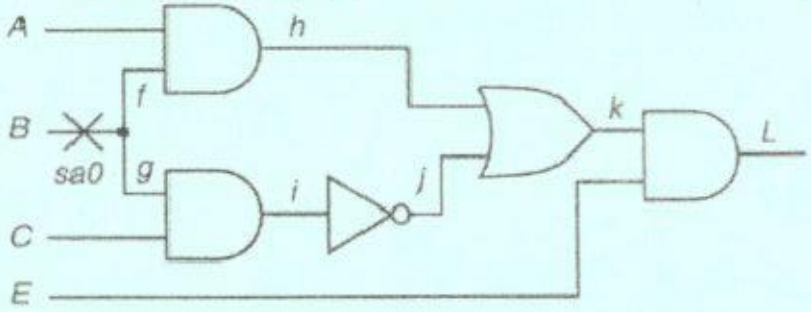
15. Explain in detail the step by step procedure in finding a test for detecting a fault using D-Algorithm. Use the NAND and NOR gate for illustrating the procedure.

16. With neat diagram, explain the working of BILBO BIST architecture.

PART - C

Answer the following **1 x 20 = 20 Marks**

17. Consider the logic circuit shown below.
    (a) Obtain the boolean expression for the node 'k' in the circuit shown below and realize the boolean expression for node 'k' using CMOS logic. (10)
    (b) Obtain a test for the fault node B **s-a-0** using path sensitization technique. (10)



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