SASTRA DEEMED UNIVERSITY

(A University under section 3 of the UGC Act, 1956)

End Semester Examinations

Nov 2018

Course Code: **BECCEC 702R01 / MCSCEC 702R01**

Course: **VLSI DESIGN**

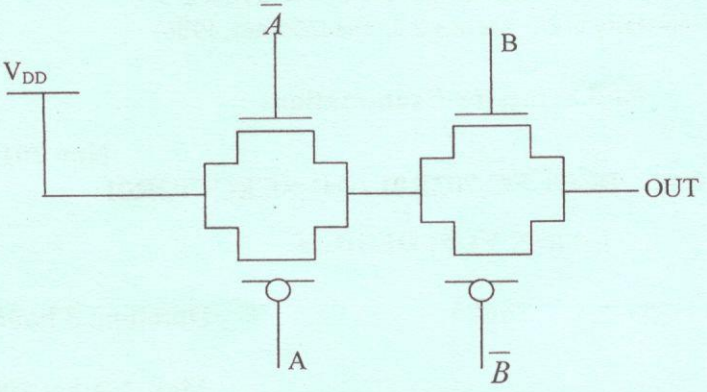
Question Paper No. : **B0680** Duration: **3** hours

Max. Marks: **100**

PART – A

Answer all the questions **10 x 2 = 20 Marks**

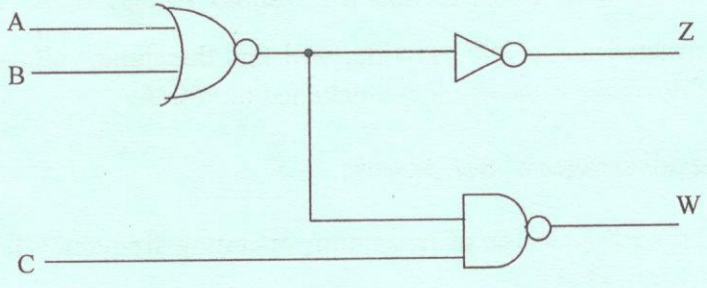
1. How do nMOS and pMOS transistors differ?
2. Give a CMOS implementation of the following function.
   $out = \overline{A}.\overline{B}.C.D$
3. If a depletion PMOS transistor has a threshold voltage of 0.5V when constructed using 200 $\overset{o}{A}$ oxide, will this threshold voltage increase of decrease if the oxide is thickened to 400°A.
4. List out the advantages of SoI process.
5. Find out the scaling factor of maximum operating frequency(f_0) in all the three models.
6. Provide a truth table that describes the functionality of the circuit in figure 1.



7. Why is polysilicon's parasitic capacitance larger than metal 1s? (Assume the layout of a transistor)

8. A DRAM memory cell should be refreshed after every read of that cell. State True or false.

9. Find the set of all test vectors which detect the stuck-at-1 fault in line C in the given figure.



10. Determine whether leakage current test for chips should be done prior to or after the functional test.

PART – B

Answer all the questions **4 x 15 = 60 Marks**

11. An nMOS, transistor has a device transconductance of $\beta_n = 2.3$ mA/V^2 and a threshold voltage of 0.76V Assume $V_{sBn} = 0V$.
    (a) Find the current if the voltages are set to $V_{asn} = 1$ V, $V_{DSn} = 2.5$ V (5)
    (b) Find the current if the voltages are set to $V_{asn} = 2$ V, $V_{DSn} = 2.5$ V. (5)
    (c) Find the current if the voltages are set to $V_{asn} = 4$ V, $V_{Dsn} = 2.5$ V. (5)

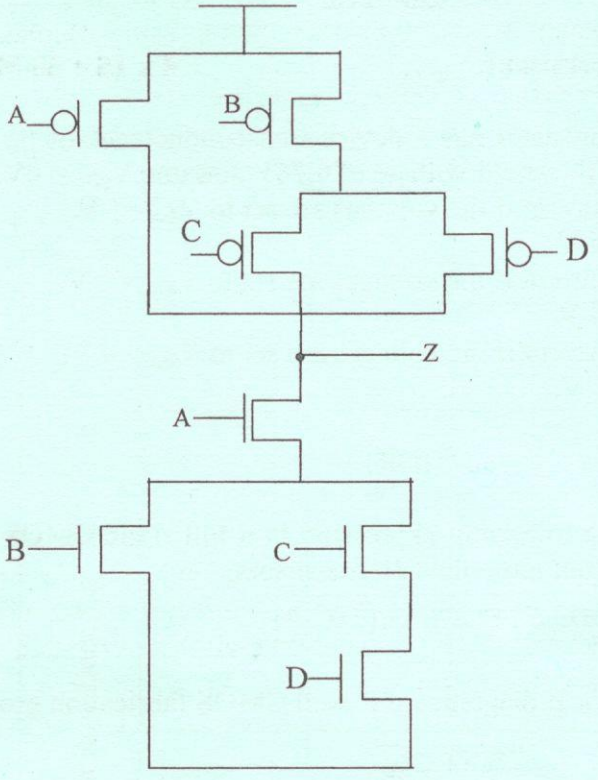
(OR)

12. Implement the following expression in a full static CMOS logic fashion using not more than 10 transistors:
    $Y = \overline{(A.B)+(A.C.E)+(D.E)+(D.C.B)}$

13. Explain with neat diagrams of P-well CMOS fabrication process.

(OR)

14. Size the transistors in the circuit of figure that implements a function $Z = \overline{A(B+CD)}$ so that its worst case current driving capability is equivalent to that of an inverter with $L_p/w_p = 2\lambda/10\lambda = 0.2$ and $L_n/w_n = 2\lambda/4\lambda = 0.5$. Assume that the channel length of all transistors is fixed at 2λ.

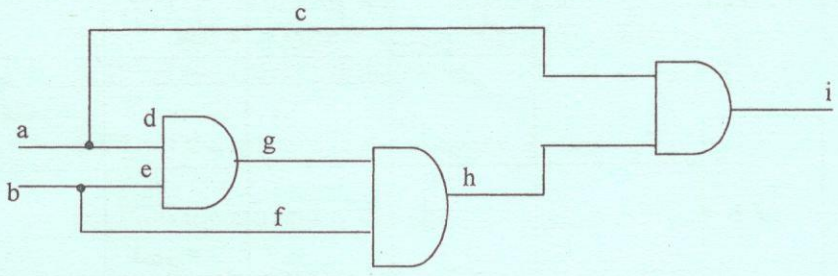


15. Using transmission gates design a circuit whose output is $Out = \left(\overline{A+B+C}\right)+\overline{A}B$ then remove the transistors and switches that are not necessary.

(OR)

16. (a) Draw and explain the operation of 3T DRAM cell. (8)
    (b) With a neat diagram, explain the operation of differential sense amplifier. (7)

17. Using the circuit shown in figure compute the set of all vectors that can detect each of the following faults using Boolean difference: (a) a/1 (b) d/1 (c) g/1. (5 + 5 + 5)



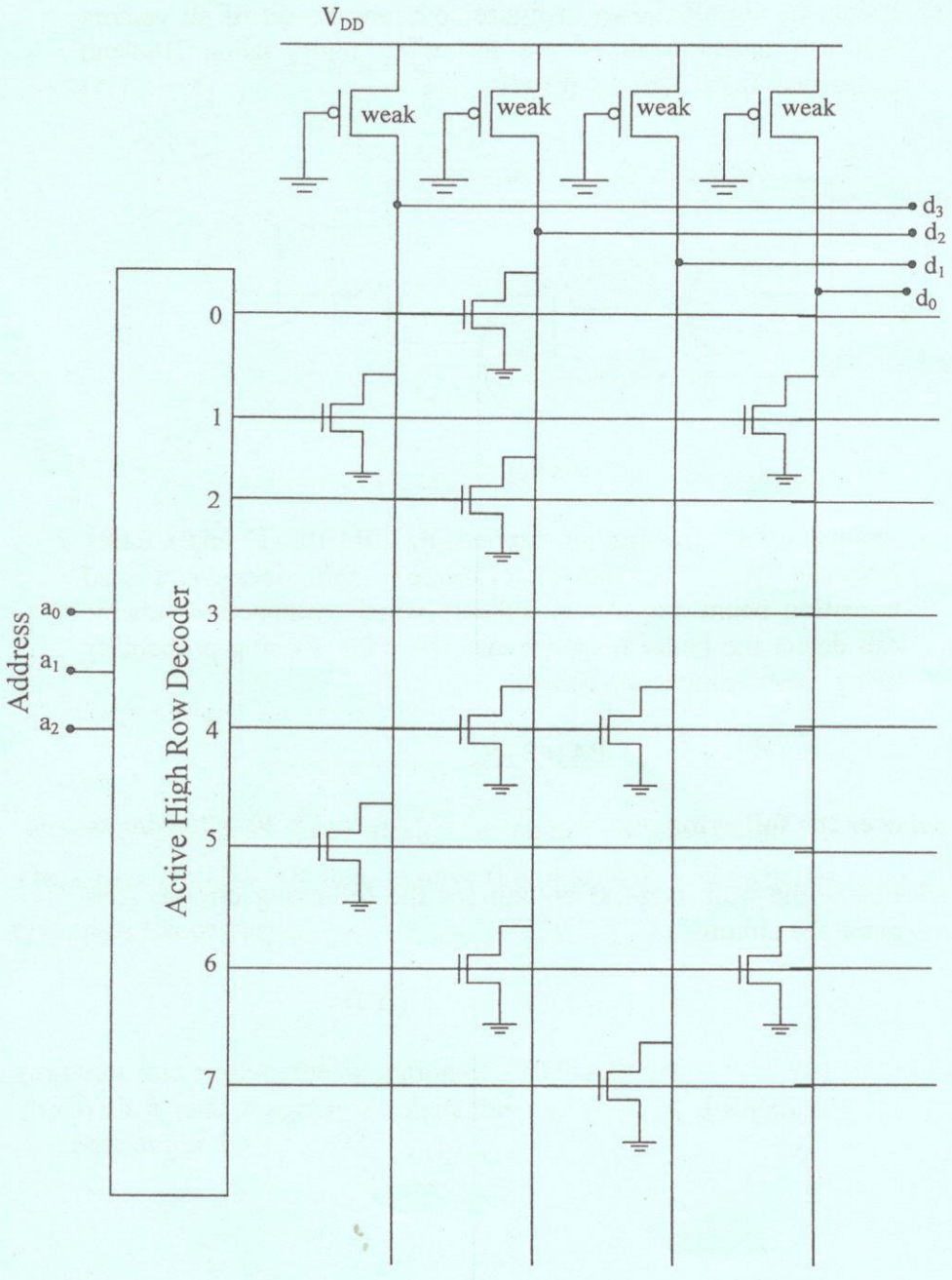
(OR)

18. Assume a fault-free output response R_0 {01101111} and a faulty response R_1= {00110001}. Compute the ones-count and transition count signatures; indicate which compaction scheme can detect the faulty response and show the aliasing probability using either compaction scheme.

PART – C

Answer the following **1 x 20 = 20 Marks**

19. Fill in the truth table at bottom for the following circuit. Also name the circuit.


V_{DD}
weak
weak
weak
weak
d_3
d_2
d_1
d_0
0
1
2
3
4
5
6
7
Active High Row Decoder
Address
a_0
a_1
a_2

Address	Data d_3 d_2 d_1 d_0
0	
1	
2	
3	
4	
5	
6	
7	

* * * *