SASTRA UNIVERSITY

(A University under section 3 of the UGC Act, 1956)

B.Tech. Degree Examinations

November 2013

Seventh Semester

Course Code: **BECCEC 702 / MCSCEC 702**

Course: **VLSI DESIGN**

Question Paper No. : **B0615**

Duration: **3** hours

Max. Marks: **100**

PART – A

Answer all the questions **20 x 2 = 40 Marks**

1. Draw the symbol of n-MOS enhancement mode and depletion mode transistors.

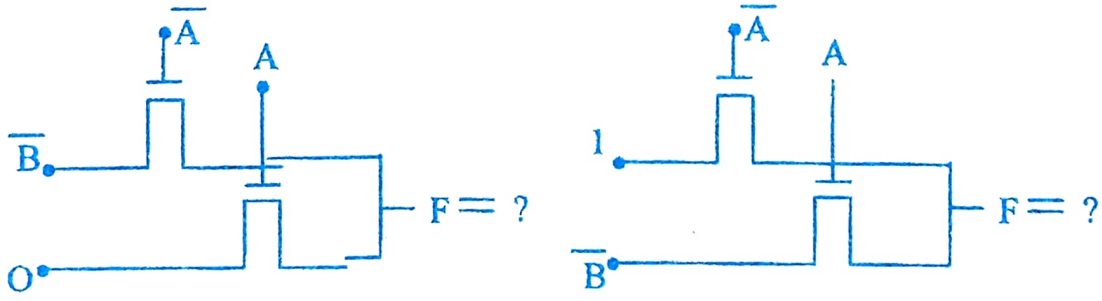
2. Give the mathematical expression for threshold voltage of a MOSFET.

3. What is the effect of body effect on transistor operation?

4. What do you mean by channel length modulation?

5. What are the advantages of transmission gate over n-MOS pass transistor?

6.



7. What are the different design domain for representing digital systems?

8. Define sheet resistance.

9. List some (any four) figures of merit of micro electronic technology.

10. What is the effect of scaling on power dissipation per unit area in combined V & D model?

11. In constant field model switching energy per gate is scaled by what factor?

12. List two salient feature of GaAs technology.

13. What is meant by photo lithography?

14. Draw the stick diagram of 4 : 1 nMOS inverter.

15. State the different levels of testing a chip.

16. What are the categories of design for testability?

17. Draw a block level representation of SRL.

18. Draw two input NOR gate using pseudo nMOS logic.

19. Draw two input NAND gate using C^2MOS logic.

20. Draw stick diagram of 4 : 1 MUX using switch logic.

PART – B

Answer all the questions **4 x 15 = 60 Marks**

21. Explain the operation of nMOS enhancement mode transistor with neat diagrams.

(OR)

22. What is threshold voltage of a MOSFET? Derive expression for it. How it can be adjusted?

23. Write in detail on limits of miniaturization and limit due to subthreshold current.

(OR)

24. What are the advantages of SOI technology? Explain the SOI fabrication process of CMOS with help of neat sketch.

25. What is the need for testing of an IC? With suitable example explain one dimensional path sensitization technique.

(OR)

26. (a) Draw the stick diagram for function (8)
$\overline{F} = X + YZ$ designed using nMOS.
(b) Write in brief on Boundary scan test techniques. (7)

27. Design
(a) $F = \overline{(A.B.C) + D}$ using dynamic CMOS logic.
(b) $F = \overline{((A.B) + C)D}$ using CMOS and C^2 MOS logic.

(OR)

28. What are the general considerations of a subsystem design process, explain briefly

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