SASTRA UNIVERSITY

(A University under section 3 of the UGC Act, 1956)

B.Tech. Degree Examinations

November 2015

Seventh Semester

Course Code: **BECCEC 702R01 / MCSCEC 702R01**

Course: **VLSI DESIGN**

Question Paper No. : **B0616**

Duration: **3 hours**

Max. Marks: **100**

PART – A

Answer all the questions **20 x 2 = 40 Marks**

1. Write the principle of operation of a depletion mode NMOS transistor.

2. Write the threshold voltage equation of a MOS transistor.

3. Define body effect.

4. Design a two input NOR gate using CMOS logic.

5. Find out the effective channel length of a MOS transistor with the following specifications.
   $V_{gs} = 3$ V, $V_{ds} = 5$ V, $V_t = 0.6$ V, $N_A = 3 \times 10^{16}/cm^3$, $L = 3\mu m$.

6. Define C_g.

7. Define self aligning.

8. Differentiate dry and wet oxidation.

9. Write the scaling factors for the following parameters.
   (a) Current density.
   (b) Static power dissipation.

10. Calculate the depletion width of MOS transistor with the following specifications.
    $N_B = 10^{15}/cm^3$, $N_D = 10^{20}/cm^3$ with an applied voltage of 3 V.

11. Why one pass transistor should not drive another pass transistor?

12. Draw the stick diagram of a nMOS inverter.

13. Sketch the transmission gate representation of the expression $Y = \overline{A}B$.

14. Mention λ-based design rules for nMOS and CMOS wires.

15. Differentiate static and dynamic memories.

16. What are the types of bridging faults?

17. What is the use of syndrome checking?

18. What is JTAG? What are the main control signals used in JTAG?

19. What is BIST?

20. Define fault coverage.

PART – B

Answer all the questions **4 x 15 = 60 Marks**

21. (a) For an NMOS transistor with the following specifications, calculate the threshold voltage. Assume zero source to

substrate bias. $X_{OX} = 200$ Å, $\phi_S = 0.6$ V, $Q_{fc} = q \times 10^{11}$, $N_A = 10^{15}/cm^3$, $N_{dp} = 10^{19}/cm^3$ and $N_{II} = 10^{12}$. (10)

(b) Write notes on circuit and system representation. (5)

(OR)

22. (a) Explain the various second order effects in detail. (10)

(b) Design the given Boolean expression using dynamic CMOS logic. (5)

$$X = \overline{\bar{A}B + AB\bar{C} + AD}$$

23. (a) Discuss in detail the CMOS inverter fabrication using SOI process with necessary diagrams. (10)

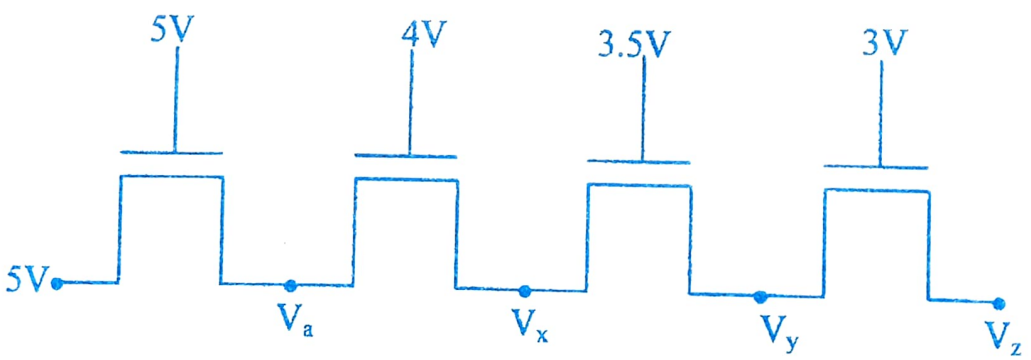
(b) Find out the maximum operating frequency f_0 for the given specifications. w = 1 μm, L = 2.5 μm, μ = 650 cm^2/V-sec, $V_{DD} = 3.3$ V and D = 100 Å. (5)

(OR)

24. (a) Derive expressions for rise time and fall time of CMOS inverter. (8)

(b) Write notes on limits of miniaturization. (7)

25. (a) Calculate Va, Vx, Vy and Vz of the following pass transistor arrangement. Assume $V_{tn} = 0.3\ V_{DD}$ where $V_{DD} = 5$V. (8)



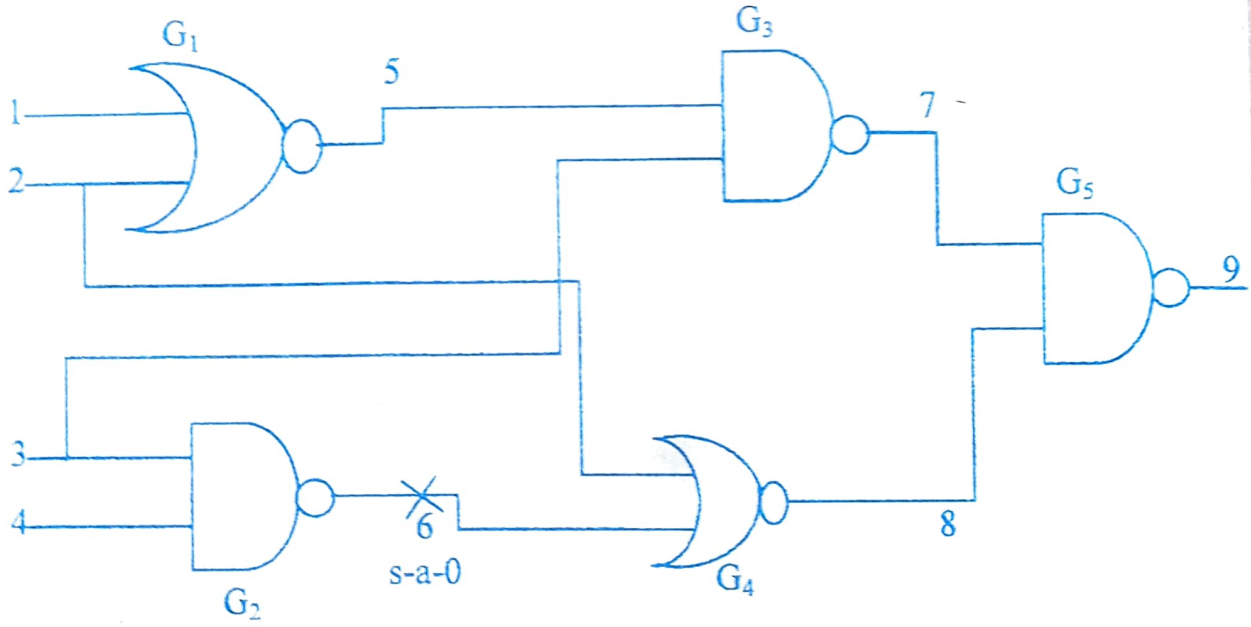
(b) Discuss the lambda based design rules in detail. (7)

(OR)

26. (a) With a neat diagram, explain the working of three transistor dynamic RAM cell. (7)

(b) Discuss in detail the general arrangement of a 4-bit arithmetic processor with necessary diagram. (8)

27. (a) Derive the test pattern to find out a s-a-0 fault at the node number 6 of the given circuit using D algorithm. (10)



(b) Write notes on Ad hoc testing. (5)

(OR)

28. (a) Explain in detail about BILBO with neat diagram. (8)

(b) Discuss in detail about JTAG based boundary scan architecture. (7)

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