SASTRA UNIVERSITY

(A University under section 3 of the UGC Act, 1956)

B.Tech. Degree Examinations

November 2012

Seventh Semester

Course Code: **BECCEC 702 / MCSCEC 702**

Course: **VLSI DESIGN**

Question Paper No. : **B0824**

Duration: 3 hours

Max. Marks: **100**

PART – A

Answer all the questions **20 x 2 = 40 Marks**

1. What is structural representation?
2. What is substrate-bias effect?
3. List out the normal conduction characteristics of an MOS transistor.
4. What is Crowbarred level in CMOS digital circuit?
5. Design a 2-input CMOS NOR gate.
6. Define sheet resistance.
7. List out the salient features of Gallium Arsenide VLSI technology.
8. Define Gate area.
9. How do you express fringing field capacitance?

10. What are the advantages of SOI technology?

11. Draw a P-well CMOS inverter stick diagram.

12. What is functionality test?

13. What is controllability?

14. What is an iterative logic array?

15. What is IDDQ testing?

16. List out the four main affecting levels in critical path.

17. What is Fan-in of a logic gate?

18. What is stage ratio?

19. What is ganged CMOS logic?

20. What are the effects that can result in incorrect functionality of a CMOS logic gate?

PART – B

Answer all the questions **4 x 15 = 60 Marks**

21. Explain accumulation, depletion and inversion modes in an MOS structure.

(OR)

22. Explain the physical structure of MOS transistors and their schematic icons.

23. Explain the limits of interconnect and contact resistance.

(OR)

24. Explain a typical N-well CMOS process in detail.

25. Explain Ad-hoc testing in detail.

(OR)

26. Explain ATPG with suitable example.

27. Explain the clocked CMOS logic in detail.

(OR)

28. Draw a parity generator stick diagram using CMOS logic.

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