SASTRA UNIVERSITY

(A University under section 3 of the UGC Act, 1956)

B.Tech. Degree Examinations

November 2014

Seventh Semester

Course Code: **BECCEC 702R01 / MCSCEC 702R01**

Course: **VLSI DESIGN**

Question Paper No. : **B0630** Duration: **3** hours

Max. Marks: **100**

PART – A

Answer all the questions **20 x 2 = 40 Marks**

1. Which region in MOS transistor is referred as sub threshold region?
2. When crowbarred level exists in CMOS inverter?
3. What are the main attributes of CMOS technology?
4. What is drain punch through condition?
5. Draw a Domino CMOS logic circuit.
6. Define channel resistance.
7. Give an equation for fall-time estimation.
8. What are the different types of scaling model and scaling factors?
9. Mention the effects of scaling on gate area (As) and Capacitance (Cg).

10. What is current density?

11. Draw the OR gate using transmission gate.

12. What is the use of stick diagram?

13. What are the different memory elements?

14. What are the four basic layers used for MOS circuits?

15. Draw the basic block of Parity generator.

16. What is manufacturing test?

17. What is meant by percentage-fault coverage?

18. What is observability?

19. What is meant by design for testability?

20. What is the significance of the IDDQ testing?

PART – B

Answer all the questions **4 x 15 = 60 Marks**

21. (a) Derive Ids for nMOS transistor. (10)
    (b) Discuss channel length modulation. (5)

(OR)

22. Design
    (a) $Z = \overline{A(B+C)+(D\cdot E)}$ using Pseudo nMOS logic and Dynamic CMOS logic. (10)
    (b) $Z = \overline{(B+C)+(A\cdot D)}$ using clocked CMOS logic. (5)

23. (a) Explain CMOS fabrication using P-Well process with a neat diagram. (10)
(b) What are the advantages of SOI technology? (5)

(OR)

24. (a) Explain inverter delay with suitable diagrams. (10)
(b) Discuss the limits of logic level and supply voltage due to noise. (5)

25. (a) Explain four way multiplexer with diagrams. (7)
(b) Explain gray to binary code converter with suitable diagrams. (8)

(OR)

26. (a) Draw a circuit diagram, logic symbol, stick and symbolic diagrams for NMOS, CMOS & BiCMOS inverter. (8)
(b) Brief about an One-Transistor dynamic memory cell with suitable diagrams. (7)

27. (a) Explain Ad-hoc testing with an example of one counter circuits. (5)
(b) Draw and explain the IEEE 1149 boundary scan architecture. (10)

(OR)

28. (a) Explain Level Sensitive Scan Design. (LSSD) (10)
(b) Mention the objectives of BIST and draw the diagram of BIST-signature analysis. (5)

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