SASTRA DEEMED UNIVERSITY

(A University under section 3 of the UGC Act, 1956)

End Semester Examinations

June 2019

Course Code: **BECCEC 702R01 / MCSCEC 702R01**

Course: **VLSI DESIGN**

Question Paper No. : **B0658** Duration: **3** hours

Max. Marks: **100**

PART – A

Answer all the questions **10 x 2 = 20 Marks**

1. Define Moore's law.

2. Give a CMOS implementation of the following logic function.
$$out = \overline{(A+B).(C+D)}$$

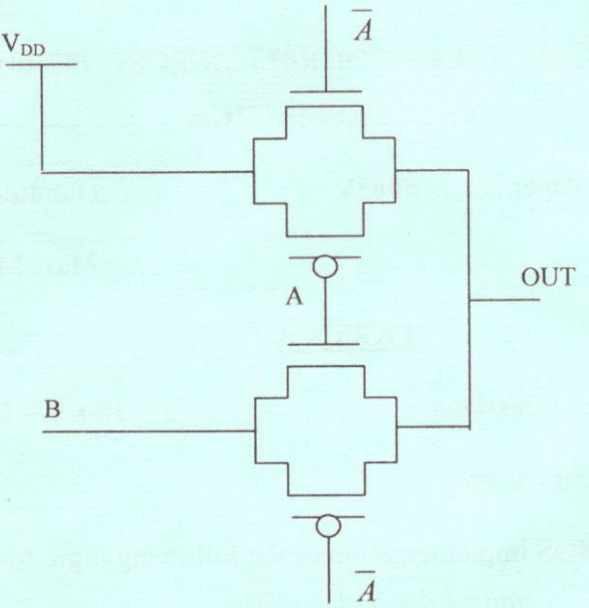
3. If a depletion NMOS transistor has a threshold voltage of -0.5 V when constructed using a 200 $\overset{o}{A}$ oxide, will this threshold voltage increase or decrease if the oxide is thickened to 400 $\overset{o}{A}$?

4. Distinguish between the bulk CMOS technology with the SoI technology fabrications.

5. A resistor body has the following dimensions as drawn: length = 95 microns, width = 12 microns. The material has a sheet resistance of 65 Ω/square. When fabricated, the above resistor width measures 0.2 microns smaller than drawn. What is its resistance value?

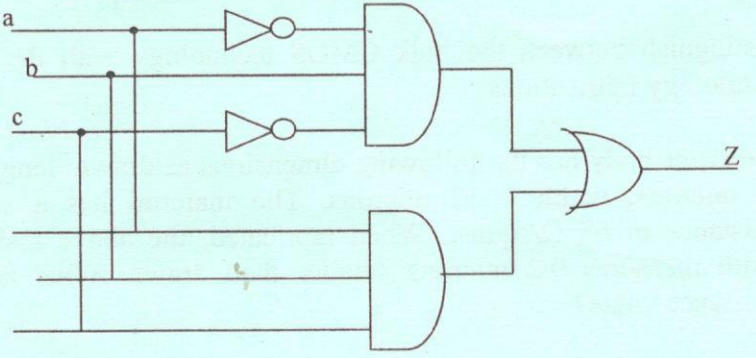
6. Find out the scaling factor of gate capacitance per unit area (C_{ox}) in all the three models.

7. Provide a truth table that described the functionality of the circuit in figure 1.

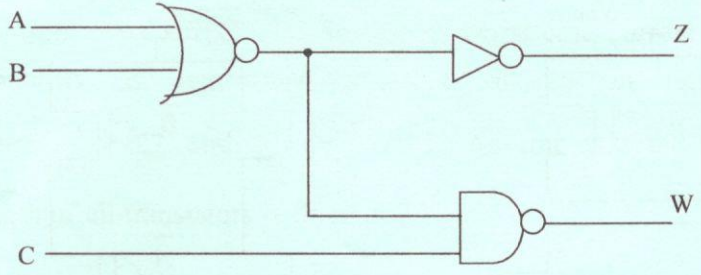


8. The PMOS transistors in a SRAM memory cell generally do not affect read or write speed. State True or False.

9. Consider the combinational logic circuit in figure. How many possible single stuck-at faults does this circuit have.



10. Find the set of all test vectors which detect the stuck-at-0 fault in line B in figure.



PART – B

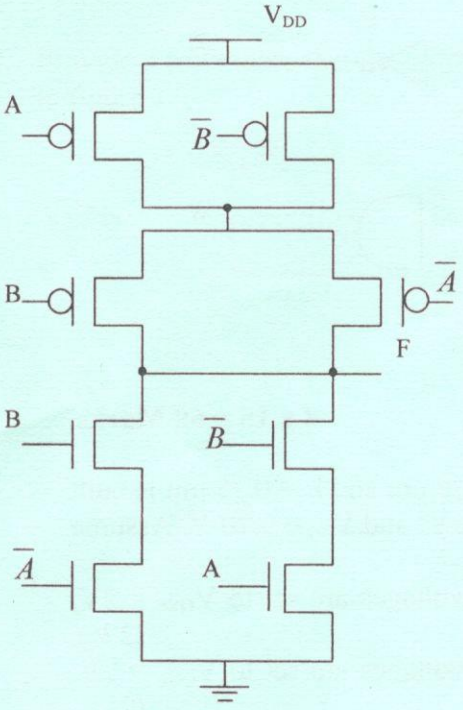
Answer all the questions **4 x 15 = 60 Marks**

11. (a) An nMOS transistor with W = 10 μm and L = 0.35 μm is built in a process where k_n = 110 μA/V^2 and V_{Tn} = 0.70 V. Assume V_{SBn} = 0 V.

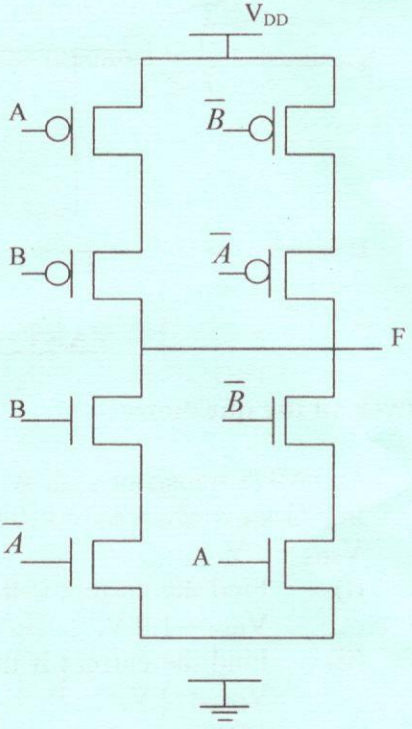
(i) Find the current if the voltages are set to V_{GSn} = 2V, V_{DSn} = 1.0 V. (2 ½)

(ii) Find the current if the voltages are set to V_{GSn} = 2V, V_{DSn} = 2 V. (2 1/2)

(b) What is the logic function of circuits A and B in figure? Which one is a dual network and which one is not? Is the nondual network still a valid static logic gate? Explain. List out any 2 advantages of one configuration over the other. (10)



circuit A



circuit B

(OR)

12. Draw the pseudo-nMOS circuits that provide the following logic operations.

(a) $f = \overline{a.b + c}$ (4)

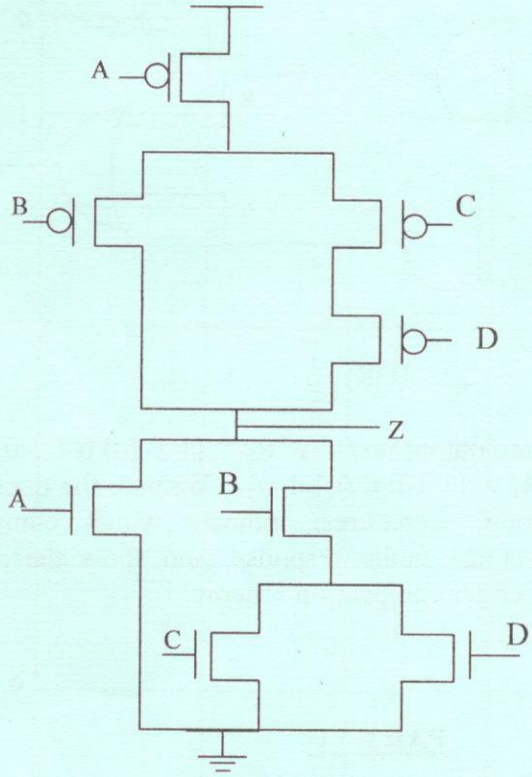
(b) $h = \overline{(a+b+c).x + y.z}$ (5)

(c) $F = \overline{a + \left(c.\left[x + (y.z)\right]\right)}$ (6)

13. Explain with neat diagrams of N-well cMOS fabrication process.

(OR)

14. Size the transistors in the circuit of figure that implements a function $z = \overline{A + B(C + D)}$ so that its worst case current driving capability is equivalent to that of an inverter with $\frac{L_p}{W_p} = \frac{2\lambda}{10\lambda} = 0.2$ and $\frac{L_n}{W_n} = \frac{2\lambda}{4\lambda} = 0.5$. Assume that the channel length of all transistors is fixed at 2 λ.



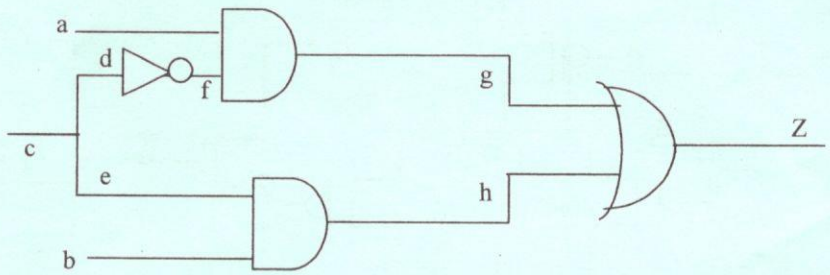
15. Using transmission gates, design a circuit whose output is $Out = \left(\overline{\overline{A + B + \overline{C}} + \overline{A}\,\overline{B}}\right)$. Then remove the transistors and switches that are not necessary.

(OR)

16. Draw and explain the operation of 4T SRAM cell and 6T SRAM cell.

17. Using the circuit shown in figure, compute the set of all vectors that can detect each of the following faults using Boolean difference.

(a) e/o. (7)
(b) e/1. (8)



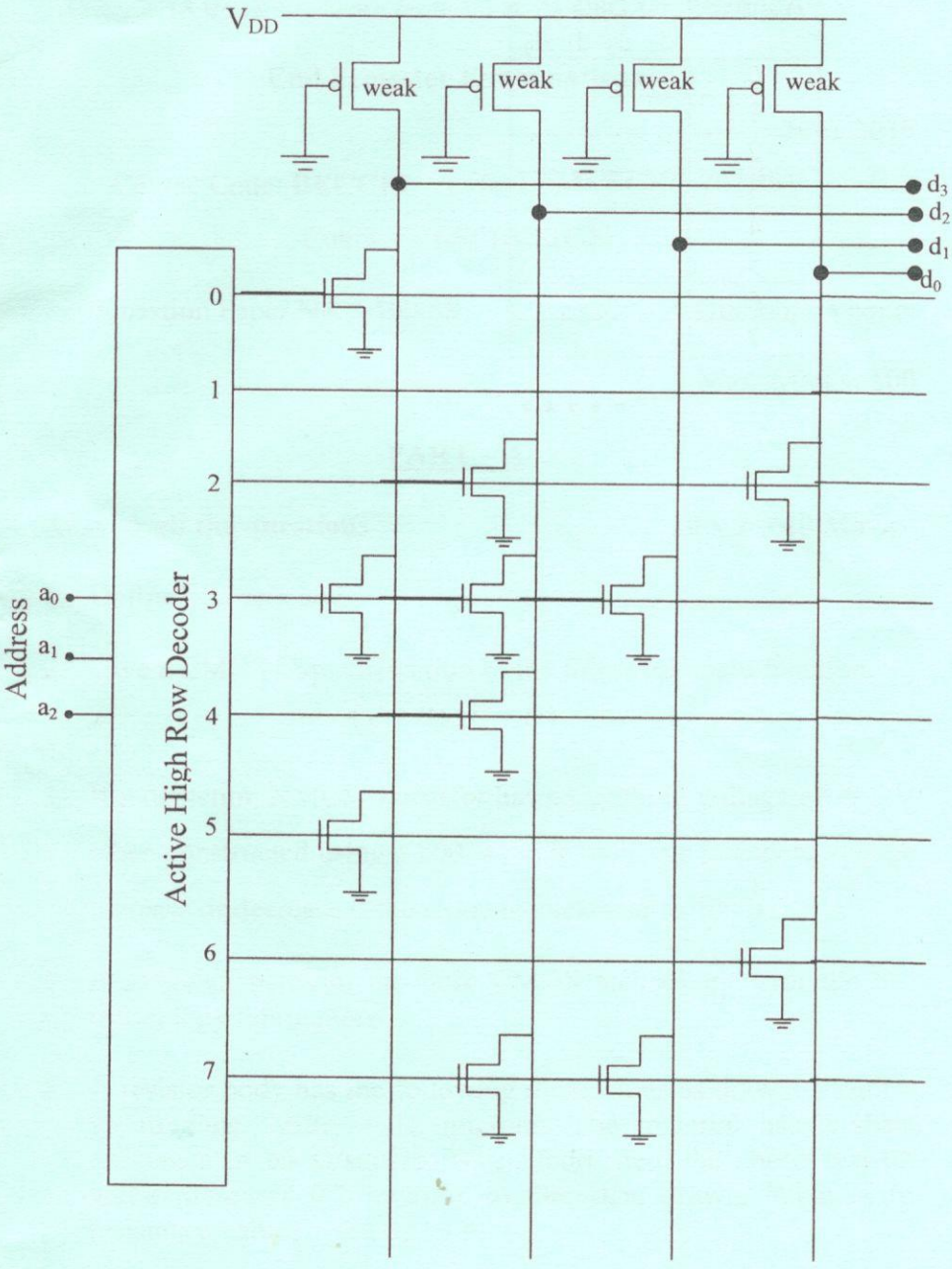
(OR)

18. Assume a fault-free output response $R_0 = \{1\ 1\ 1\ 0\ 0\ 1\ 1\ 0\}$ and a faulty response $R_1 = \{1\ 1\ 0\ 0\ 0\ 1\ 1\ 0\}$. Compute the ones-count and transition-count signatures; indicate which compaction scheme can detect the faulty response, and show the aliasing probability using either compaction scheme.

PART – C

Answer the following **1 x 20 = 20 Marks**

19. Fill in the truth tables at bottom for the following circuit. Also name the circuit.


V_{DD}
weak
weak
weak
weak
d_3
d_2
d_1
d_0
Address
a_0
a_1
a_2
Active High Row Decoder
0
1
2
3
4
5
6
7

Address	Data d_3 d_2 d_1 d_0
0	
1	
2	
3	
4	
5	
6	
7	

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