MULTIPORT VIDEO RAM WITH 256K X 8 DRAM AND 512 X 8 SAM

HIGH PERFORMANCE V52C8256	60	70	80
Max. $\overline{RAS}$ Access Time, (t_{RAC})	60 ns	70 ns	80 ns
Max. $\overline{CAS}$ Access Time, (t_{CAC})	15 ns	20 ns	25 ns
Max. Column Address Access Time, (t_{AA})	30 ns	35 ns	40 ns
Min. Extended-Data-Out Cycle Time, (t_{PC})	30 ns	35 ns	40 ns
Min. Read/Write Cycle Time, (t_{RC})	120 ns	140 ns	150 ns
Max. Serial Access Time, (t_{SCA})	17 ns	17 ns	20 ns
Min. Serial Port Cycle Time, (t_{SCC})	22 ns	22 ns	25 ns

Features

- Organization
  - RAM Port: 262,144 words x 8 bits
  - SAM Port: 512 words x 8 bits
- RAM Port
  - Extended-Data-Out, Read-Modify-Write
  - Persistent Mask Write
  - Block Write/Flash Write
  - 512 Refresh Cycles/8 ms
  - $\overline{CAS}$-before-$\overline{RAS}$ Refresh, Hidden Refresh, $\overline{RAS}$-only Refresh
- SAM Port
  - High Speed Serial Read/Write Capability
  - 512 Tap Locations
  - Programmable Stops
- RAM-SAM Bidirectional Transfer
  - Read/Write Transfer
  - Split Read/Write Transfer
- Low Standby Current – 8 mA
- Package
  - 40 pin 400 mil SOJ

Description

The V52C8256 VRAM is equipped with a 262,144-words by 8-bits dynamic random access memory (RAM) port and a 512-words by 8-bits static serial access memory (SAM) port. The V52C8256 supports three types of operations: random access to and from the RAM port, high speed serial access to and from the SAM port, and bidirectional transfer of data between any selected row in the RAM port and the SAM port. The RAM port and the SAM port can be accessed independently except when data is being transferred between them internally.

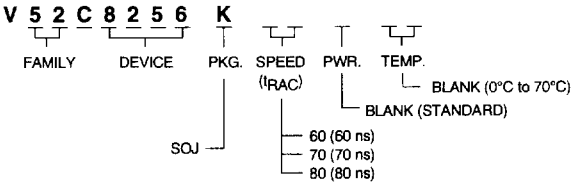
In addition to the conventional multiport video RAM operating modes, the V52C8256 features the persistent mask write, programmable split SAM and split read/write transfer.

The V52C8256 is fabricated in CMOS silicon gate process as well as advanced circuit designs to provide low power dissipation and wide operating margins.

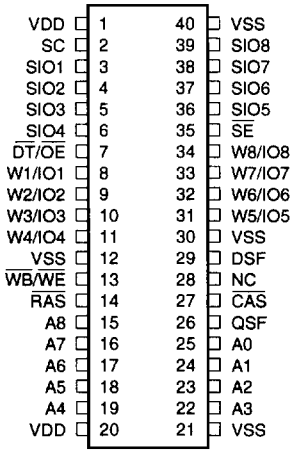
Device Usage Chart

Operating Temperature Range	Package Outline	Access Time (ns)			Power	Temperature Mark
	K	60	70	80	Std	
0°C–70°C	•	•	•	•	•	Blank

Description	Pkg.	Pin Count
SOJ	K	40



40 Lead Pin Configuration



K – SOJ

Pin Names

Name	Description
A0-A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{DT/OE}$	Data Transfer/Output Enable
$\overline{WB/WE}$	Write per Bit/Write Enable
DSF	Special Function Control
W1/IO1-W8/IO8	Write Mask/Data In, Out
SC	Serial Clock
$\overline{SE}$	Serial Enable
SIO1-SIO8	Serial Input/Output
QSF	Special Flag Output
VDD/VSS	Power (5V)/Ground
NC	No Connection

Capacitance*

T_A = 25°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, f = 1MHz

Symbol	Parameter	Min.	Max.	Unit
C_{IN}	Input Capacitance		7	pF
$C_{IN/OUT}$	Input/Output Capacitance		9	pF
C_{OUT}	Output Capacitance (QSF)		9	pF

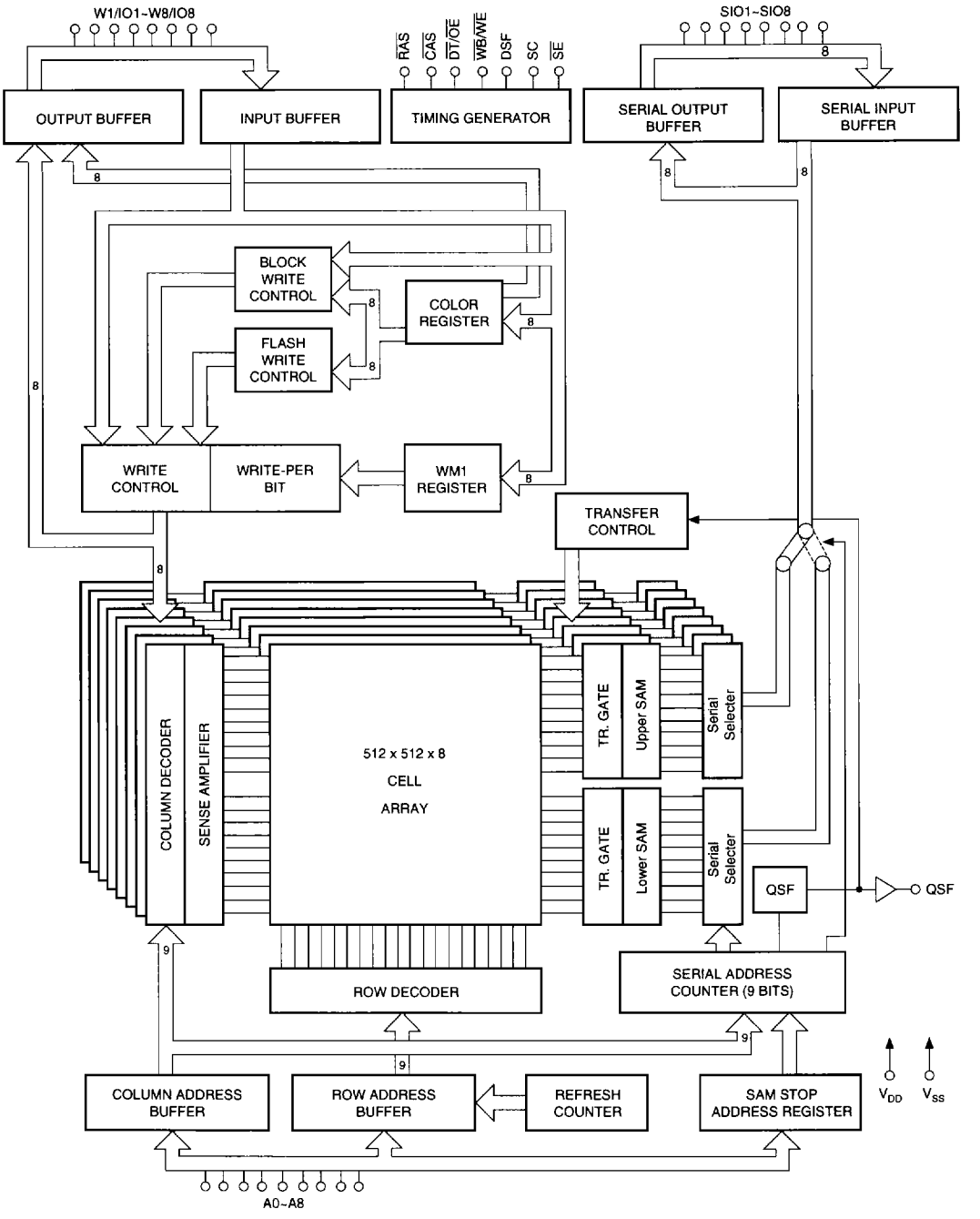
*Note: Capacitance is sampled and not 100% tested.

Absolute Maximum Ratings*

Ambient Temperature
Under Bias ..... −10°C to +80°C
Storage Temperature (plastic) .... −55°C to +125°C
Voltage Relative to V_{SS} ..... −1.0 to +7.0 V
Short Circuit Out Current ..... 50 mA
Power Dissipation ..... 1 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

Functional Diagram



DC and Operating Characteristics

(V_{DD} = 5V ± 10%, T_A = 0–70°C)

Symbol	Parameter (RAM Port)	SAM Port	-60 Min.	-60 Max.	-70 Min.	-70 Max.	-80 Min.	-80 Max.	Unit	Notes
I_{DD1}	Operating Current $\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} Min.	Standby		95		85		75	mA	1, 2
I_{DD1A}		Active		140		130		120	mA	1, 2
I_{DD2}	Standby Current $\overline{RAS}$, $\overline{CAS}$ = V_{IH}	Standby		8		8		8	mA	
I_{DD2A}		Active		60		55		50	mA	1, 2
I_{DD3}	$\overline{RAS}$-Only Refresh Current $\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} Min.	Standby		95		85		75	mA	1, 2
I_{DD3A}		Active		140		130		120	mA	1, 2
I_{DD4}	Page Mode Current $\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling, t_{PC} = t_{PC} Min.	Standby		75		70		65	mA	1, 2
I_{DD4A}		Active		120		115		110	mA	1, 2
I_{DD5}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current $\overline{RAS}$ Cycling, $\overline{CAS}$ before $\overline{RAS}$, t_{RC} = t_{RC} Min.	Standby		95		85		75	mA	1, 2
I_{DD5A}		Active		140		130		120	mA	1, 2
I_{DD6}	Data Transfer Current $\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} Min.	Standby		95		85		75	mA	1, 2
I_{DD6A}		Active		140		130		120	mA	1, 2
I_{DD7}	Flash Write Current $\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} Min.	Standby		95		85		75	mA	1, 2
I_{DD7A}		Active		140		130		120	mA	1, 2
I_{DD8}	Block Write Current $\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} Min.	Standby		95		85		75	mA	1, 2
I_{DD8A}		Active		140		130		120	mA	1, 2
$I_{I(L)}$	Input Leakage Current 0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V		-10	10	-10	10	-10	10	µA	
$I_{O(L)}$	Output Leakage Current 0V ≤ V_{OUT} ≤ 5.5V, Output Disable		-10	10	-10	10	-10	10	µA	
V_{OH}	Output "H" Level Voltage I_{OUT} = -1 mA		2.4		2.4		2.4		V	
V_{OL}	Output "L" Level Voltage I_{OUT} = 2 mA			0.4		0.4		0.4	V	
V_{IH}	Input High Voltage		2.4	V_{DD} + 1	2.4	V_{DD} + 1	2.4	V_{DD} + 1	V	
V_{IL}	Input Low Voltage		-1.0	0.8	-1.0	0.8	-1.0	0.8	V	

AC Electrical Characteristics *Notes: 3, 4, 5*

Symbol	Parameter	-60		-70		-80		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Random Read or Write Cycle Time	120		140		150		ns	
t_{RMW}	Read-Modify-Write Cycle Time	170		185		195		ns	
t_{PC}	Extended-Data-Out Cycle Time	30		35		40		ns	
t_{PRMW}	Extended-Data-Out Read-Modify-Write Cycle Time	85		90		90		ns	
t_{RAC}	Access Time from $\overline{RAS}$		60		70		80	ns	6, 12
t_{AA}	Access Time from Column Address		30		35		40	ns	6, 12
t_{CAC}	Access Time from $\overline{CAS}$		15		20		25	ns	6, 13
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		35		40		45	ns	6, 13
t_{OFF}	Output Buffer Turn-Off Delay	0	15	0	20	0	20	ns	8
t_T	Transition Time (Rise and Fall)	3	35	3	35	3	35	ns	5
t_{RP}	$\overline{RAS}$ Precharge Time	50		60		60		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Extended-Data-Out only)	60	100K	70	100K	80	100K	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	15		20		25		ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60		70		80		ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10K	20	10K	25	10K	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	20	55	ns	12
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	12
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30		35		40		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10		10		ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	10		10		10		ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Extended-Data-Out)	10		10		10		ns	
t_{ASR}	Row Address Setup Time	0		0		0		ns	
t_{RAH}	Row Address Hold Time	10		10		10		ns	
t_{ASC}	Column Address Setup Time	0		0		0		ns	
t_{CAH}	Column Address Hold Time	10		10		12		ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50		55		55		ns	
t_{RCS}	Read Command Setup Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	9
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0		0		0		ns	9
t_{WCH}	Write Command Hold Time	10		12		15		ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	50		55		55		ns	

AC Electrical Characteristics (Cont'd)

Symbol	Parameter	-60		-70		-80		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{WP}	Write Command Pulse Width	10		12		15		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15		20		20		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15		20		20		ns	
t_{DS}	Data Setup Time	0		0		0		ns	10
t_{DH}	Data Hold Time	10		12		15		ns	10
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	50		55		55		ns	
t_{WCS}	Write Command Setup Time	0		0		0		ns	11
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	80		90		100		ns	11
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	50		55		65		ns	11
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	35		40		45		ns	11
t_{DZC}	Data to $\overline{CAS}$ Delay Time	0		0		0		ns	
t_{DZO}	Data to $\overline{OE}$ Delay Time	0		0		0		ns	
t_{OEA}	Access Time from $\overline{OE}$		15		20		20	ns	6
t_{OEZ}	Output Buffer Turn-Off Delay from $\overline{OE}$	0	10	0	10	0	10	ns	8
t_{OED}	$\overline{OE}$ to Data Delay Time	10		10		10		ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	10		10		10		ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10		15		15		ns	
t_{CSR}	$\overline{CAS}$ Setup Time for $\overline{Cas}$-before-$\overline{RAS}$ Cycle	10		10		10		ns	
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Cycle	10		10		10		ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0		0		0		ns	
t_{REF}	Refresh Period		8		8		8	ms	
t_{WSR}	$\overline{WB}$ Setup Time	0		0		0		ns	
t_{RWH}	$\overline{WB}$ Hold Time	10		10		12		ns	
t_{FSR}	DSF Setup Time referenced to $\overline{RAS}$	0		0		0		ns	
t_{RFH}	DSF Hold Time referenced to $\overline{RAS}$ (1)	10		10		12		ns	
t_{FHR}	DSF Hold Time referenced to $\overline{RAS}$ (2)	50		55		55		ns	
t_{FSC}	DSF Setup Time referenced to $\overline{CAS}$	0		0		0		ns	
t_{CFH}	DSF Hold Time referenced to $\overline{CAS}$	10		10		12		ns	
t_{MS}	Write-Per-Bit Mask Data Setup Time	0		0		0		ns	
t_{MH}	Write-Per-Bit Mask Data Hold Time	10		10		12		ns	
t_{THS}	$\overline{DT}$ High Setup Time	0		0		0		ns	
t_{THH}	$\overline{DT}$ High Hold Time	10		10		12		ns	
t_{TLS}	$\overline{DT}$ Low Setup Time	0		0		0		ns	

AC Electrical Characteristics (Cont'd)

Symbol	Parameter	-60		-70		-80		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{TLH}	$\overline{DT}$ Low Hold Time	10	10K	10	10K	12	10K	ns	
t_{RTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{RAS}$ (Real Time Read Transfer)	50	10K	60	10K	65	10K	ns	
t_{ATH}	$\overline{DT}$ Low Hold Time referenced to Column Address (Real Time Read Transfer)	20		25		30		ns	
t_{CTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{CAS}$ (Real Time Read Transfer)	15		20		25		ns	
t_{TRP}	$\overline{DT}$ to $\overline{RAS}$ Precharge Time	50		60		60		ns	
t_{TP}	$\overline{DT}$ Precharge Time	20		20		20		ns	
t_{RSD}	$\overline{RAS}$ to First SC Delay Time	60		70		80		ns	
t_{ASD}	Column Address to First SC Delay Time	40		45		45		ns	
t_{CSD}	$\overline{CAS}$ to First SC Delay Time	20		20		25		ns	
t_{TSL}	Last SC to $\overline{DT}$ Lead Time (Real Time Read Transfer)	5		5		5		ns	
t_{TSD}	$\overline{DT}$ to First SC Delay Time (Read Transfer)	15		15		15		ns	
t_{SRS}	Last SC to $\overline{RAS}$ Setup Time (Serial Input)	20		25		25		ns	
t_{SDD}	$\overline{RAS}$ to Serial Input Delay Time	30		40		40		ns	
t_{SDZ}	Serial Output Buffer Turn-Off Delay from $\overline{RAS}$ (Write Transfer)	10	30	10	40	10	40	ns	8
t_{SCC}	SC Cycle Time	22		22		25		ns	
t_{SC}	SC Pulse Width (SC High Time)	5		5		7		ns	
t_{SCP}	SC Precharge Time (SC Low Time)	5		5		7		ns	
t_{SCA}	Access Time from SC		17		17		20	ns	7
t_{SOH}	Serial Output Hold Time from SC	5		5		5		ns	
t_{SDS}	Serial Input Setup Time	0		0		0		ns	
t_{SDH}	Serial Input Hold Time	10		10		12		ns	
t_{SEA}	Access Time from $\overline{SE}$		17		17		20	ns	7
t_{SE}	$\overline{SE}$ Pulse Width	10		10		10		ns	
t_{SEP}	$\overline{SE}$ Precharge Time	10		10		10		ns	
t_{SEZ}	Serial Output Buffer Turn-Off Delay from $\overline{SE}$	0	20	0	20	0	20	ns	8
t_{SZE}	Serial Input to $\overline{SE}$ Delay Time	0		0		0		ns	
t_{SZS}	Serial Input to First SC Delay Time	0		0		0		ns	
t_{SWS}	Serial Write Enable Setup Time	0		0		0		ns	
t_{SWH}	Serial Write Enable Hold Time	10		10		12		ns	

AC Electrical Characteristics (Cont'd)

Symbol	Parameter	-60		-70		-80		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{SWIS}	Serial Write Disable Setup Time	0		0		0		ns	
t_{SWIH}	Serial Write Disable Hold Time	10		10		12		ns	
t_{STS}	Split Transfer Setup Time	25		25		30		ns	
t_{STH}	Split Transfer Hold Time	25		25		30		ns	
t_{SQD}	SC–QSF Delay Time		25		25		25	ns	
t_{TQD}	$\overline{DT}$–QSF Delay Time		25		25		25	ns	
t_{CQD}	$\overline{CAS}$–QSF Delay Time		30		35		35	ns	
t_{RQD}	$\overline{RAS}$–QSF Delay Time		70		75		75	ns	
t_{RCL}	$\overline{RAS}$–H to $\overline{CAS}$–H Lead Time	0		0		0		ns	
t_{CRL}	$\overline{CAS}$–H to $\overline{RAS}$–H Lead Time	0		0		0		ns	
t_{COH}	Data Output Hold after $\overline{CAS}$ Low	5		5		5		ns	

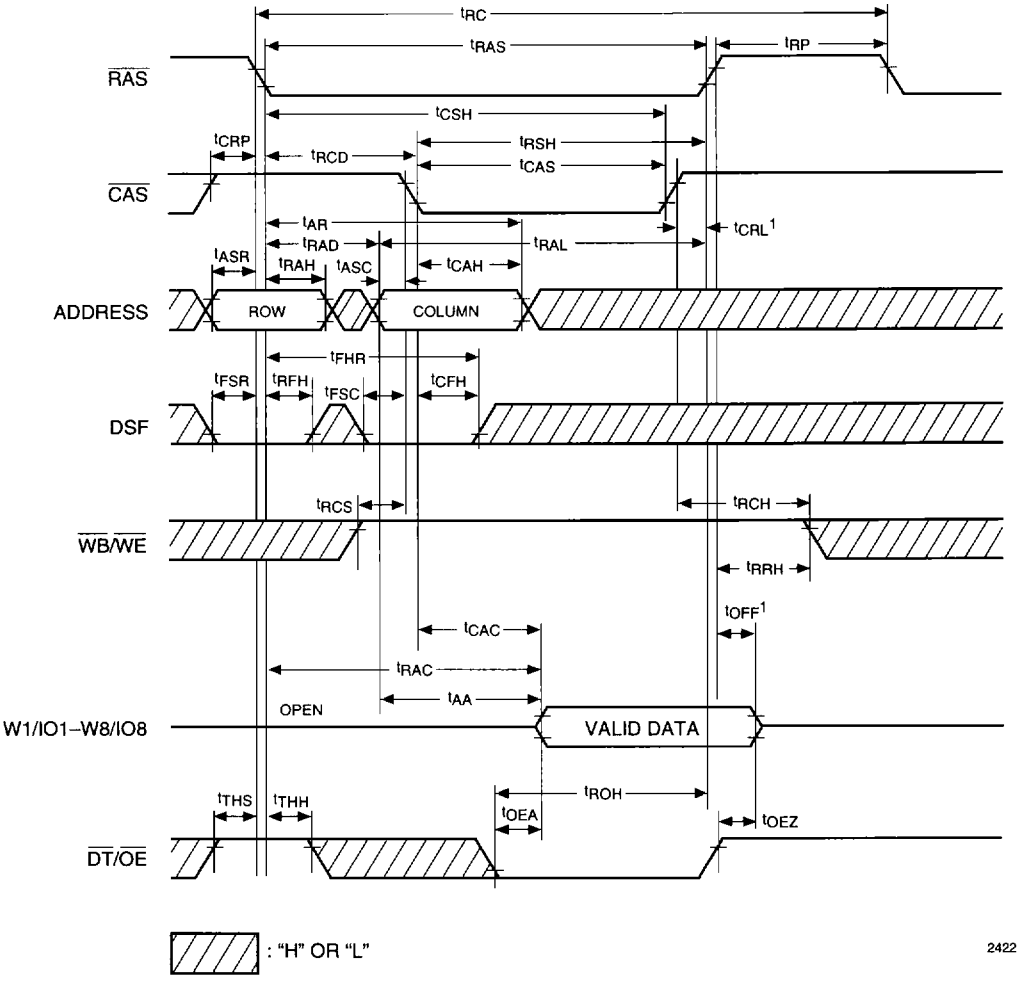
Notes

1. These parameters depend on cycle rate.
2. These parameters depend on output loading. Specified values are obtained with the output open.
3. An initial pause of 200µs is required after power-up, followed by any 8 $\overline{RAS}$ cycles ($\overline{DT}/\overline{OE}$ "high") and any 8 SC cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC measurements assume t_T = 5 ns.
5. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}. Input signals transition from 0 to 3V for AC testing.
6. RAM port outputs are measured with a load equivalent to 1 TTL load and 50 pF. D_{OUT} reference levels: V_{OH}/V_{OL} = 2.0V/0.8V.
7. SAM port outputs are measured with a load equivalent to 1 TTL load and 30 pF. D_{OUT} reference levels: V_{OH}/V_{OL} = 2.0V/0.8V.
8. t_{OFF} (max.), t_{OEZ} (max.), t_{SDZ} (max.) and t_{SEZ} (max.) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to $\overline{CAS}$ leading edge of early write cycles and to $\overline{WB}/\overline{WE}$ leading edge in $\overline{OE}$-controlled write cycles and read-modify-write cycles.
11. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.) and $t_{AWD} \geq t_{AWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
12. Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
13. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

3

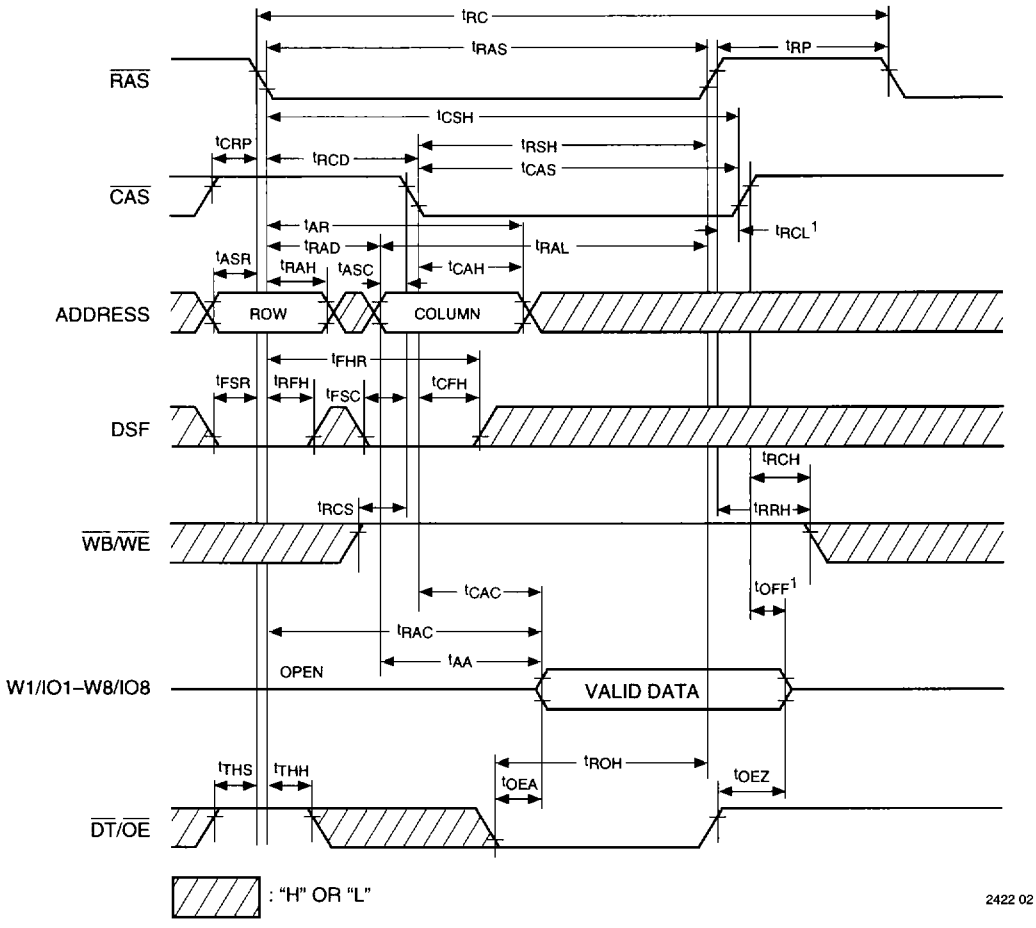
TIMING WAVEFORMS

Read Cycle (Outputs Controlled by $\overline{RAS}$)[1]



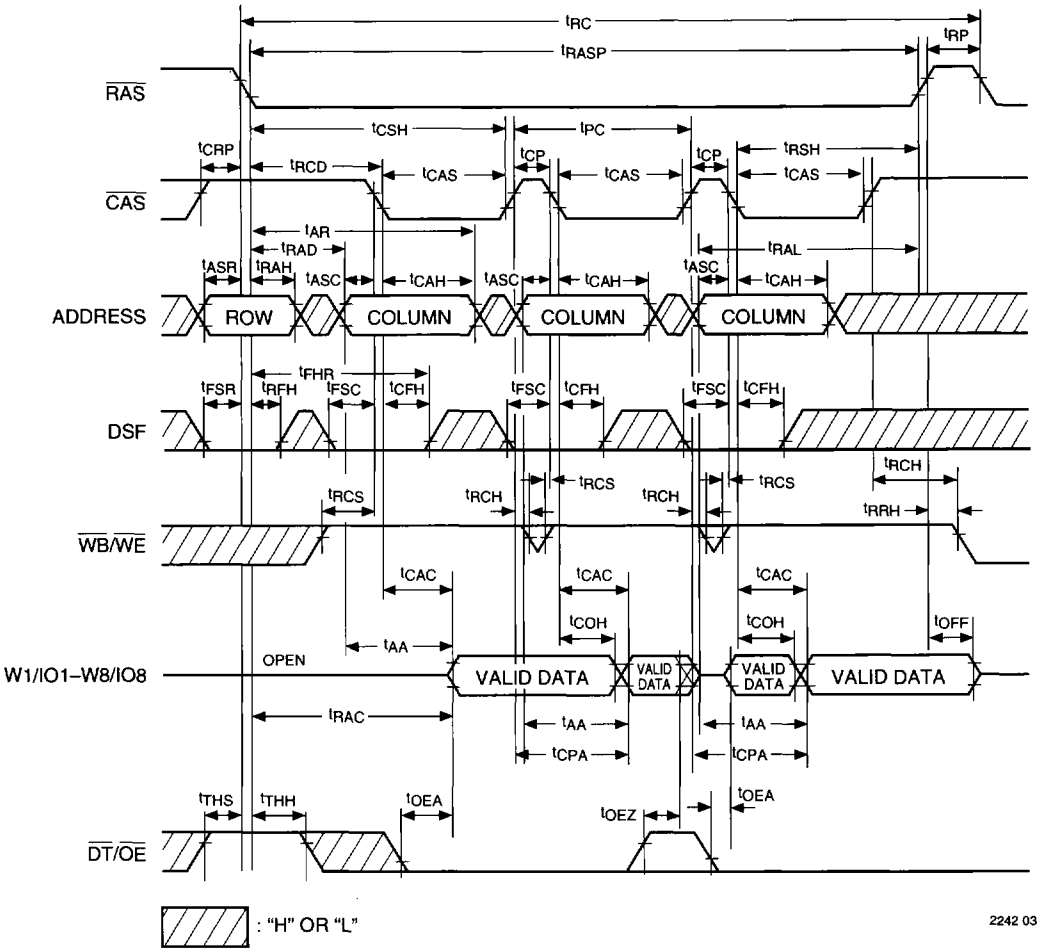
Note: 1. t_{CRL} is a reference parameter. If $\overline{CAS}$ = High before $\overline{RAS}$, t_{OFF} is referenced from the rising edge of $\overline{RAS}$.

Read Cycle (Outputs Controlled by $\overline{CAS}$)[1]



Note: 1. t_{RCL} is a reference parameter. If $\overline{RAS}$ = High before $\overline{CAS}$, t_{OFF} is referenced from the rising edge of $\overline{CAS}$.

Extended-data-out Read Cycle



Note: 1. Write cycles or Read-Modify-Write cycles may be mixed with read cycles while in Extended-Data-Out.

Write Cycle Function Table[1]

Function	Logic States				
	$\overline{RAS}$ Falling Edge			$\overline{CAS}$ Falling Edge	
	A DSF	B $\overline{WB/WE}$	C Wi/IOi	D DSF	E[2] Wi/IOi
Normal DRAM Write	0	1	X	0	DRAM Data
Mask Write to DRAM	0	0	Write Mask[3]	0	DRAM Data (Masked)
Block Write to DRAM (No Bit-Plane Mask)	0	1	X	1	Column Mask
Mask Block Write to DRAM	0	0	Write Mask[3]	1	Column Mask
Mask Flash Write to DRAM	1	0	Write Mask[3]	X	X
Load Mask Data Register	1	1	X	0	Write Mask Data
Load Color Register	1	1	X	1	Color Data

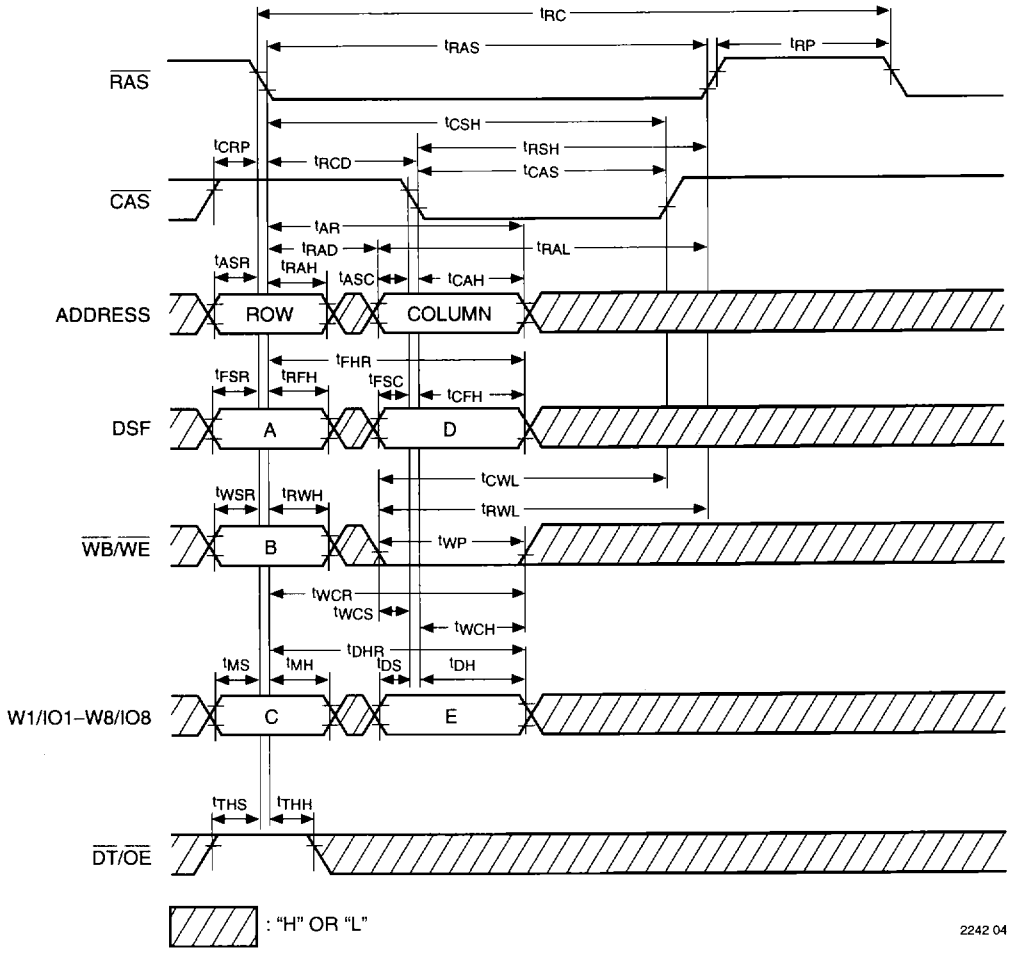
Note: 1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for the Write cycle timing diagrams on the following pages.

2. $\overline{CAS}$ and $\overline{WB/WE}$ falling edge. Whichever occurs later.

3. Mask Data is loaded at $\overline{RAS}$ falling if nonpersistent mode is active. If persistent mode is active, mask data is supplied by the Mask Data Register and the Wi/IOi are "don't care" at the $\overline{RAS}$ falling edge.

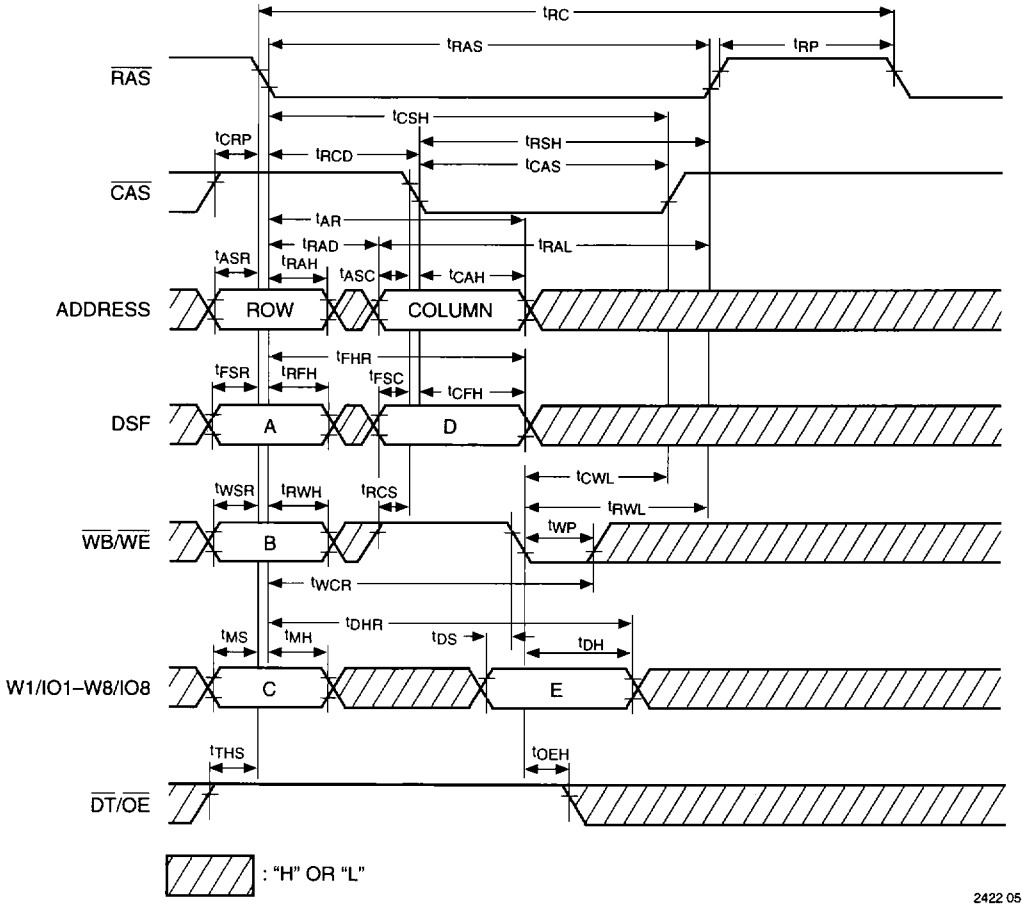
3

Early Write Cycle



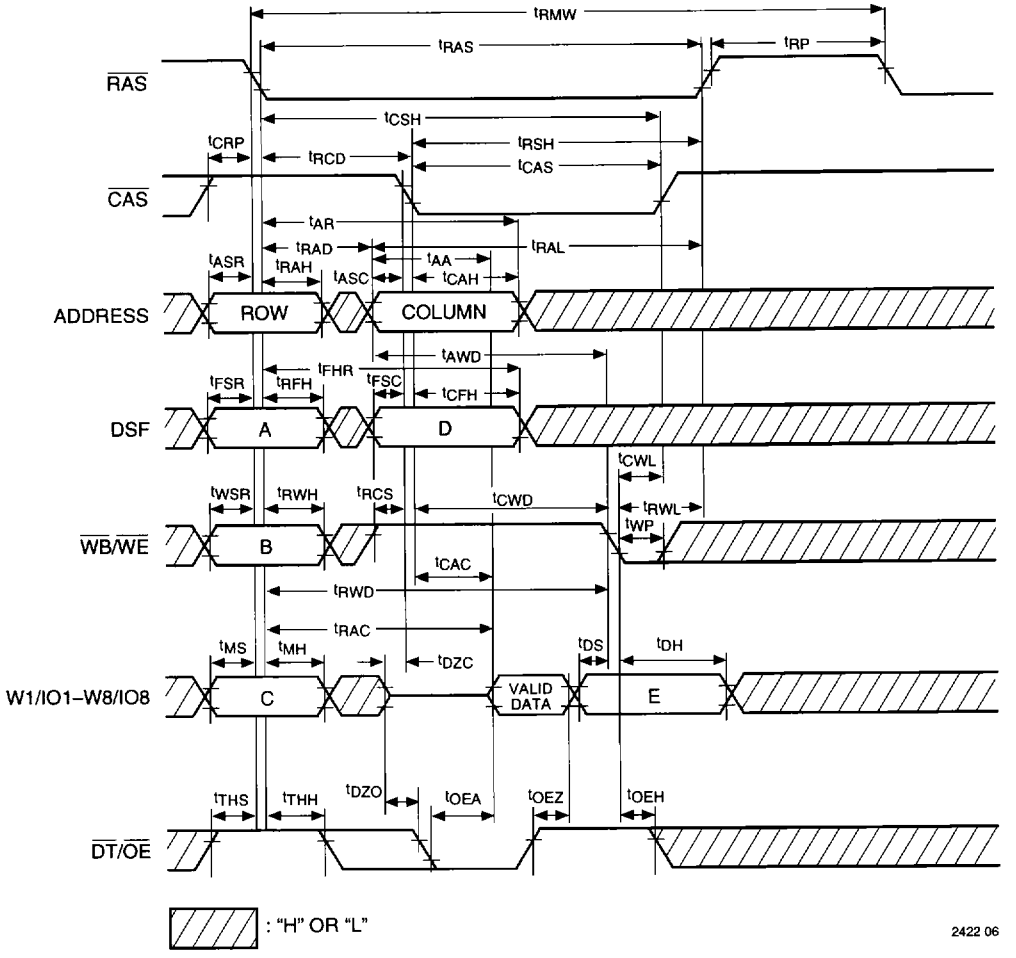
Note: The logic states of "A", "B", "C", "D" and "E" determine the type of write operation performed. See the Write Cycle Function Table for a detailed description.

Late Write Cycle



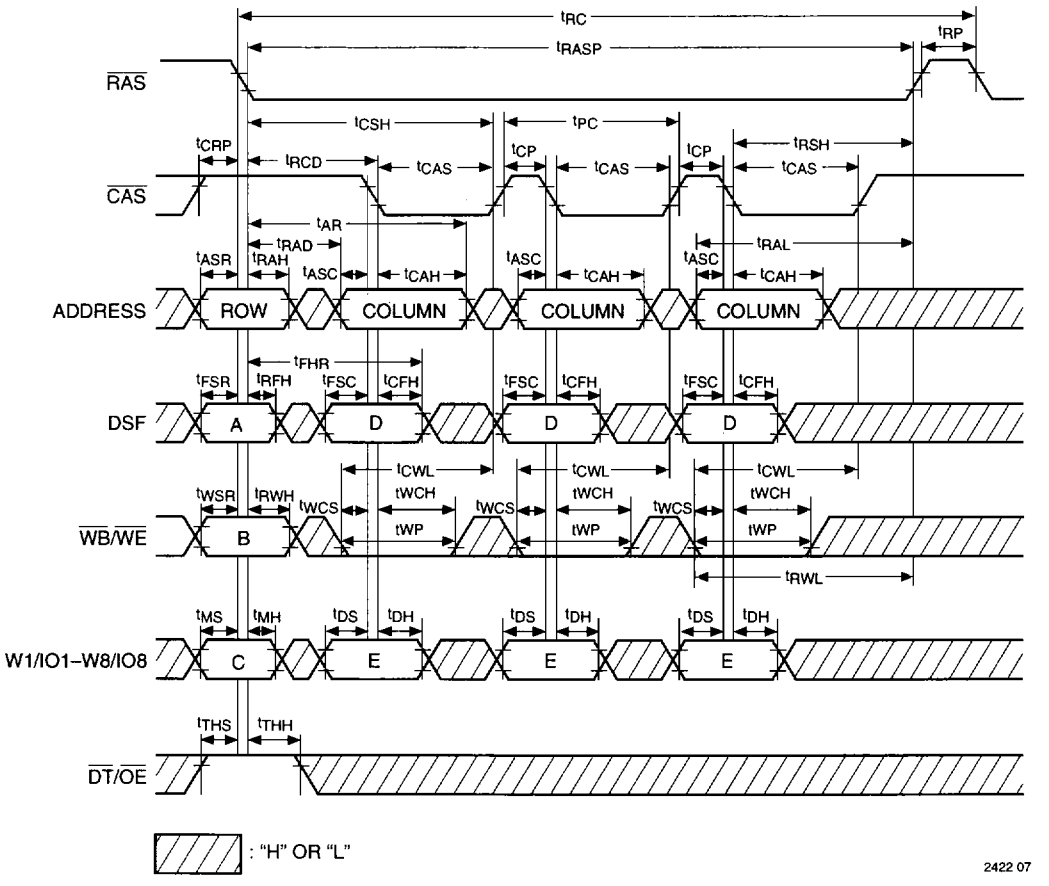
Note: The logic states of "A", "B", "C", "D" and "E" determine the type of write operation performed. See the Write Cycle Function Table for a detailed description.

Read-Modify-Write Cycle



Note: The logic states of "A", "B", "C", "D" and "E" determine the type of write operation performed. See the Write Cycle Function Table for a detailed description.

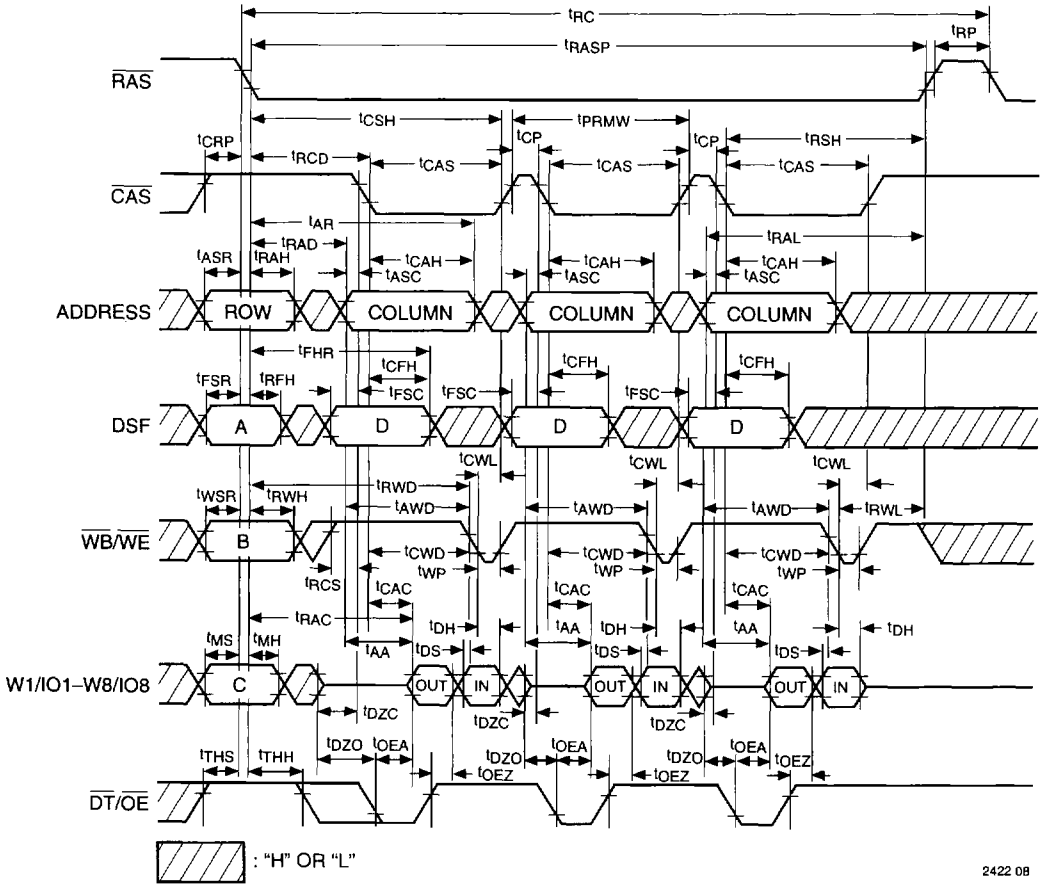
Extended-Data-Out Early Write Cycle



Note: 1. Read cycles or Read-Modify-Write cycles can be mixed with write cycles while in Extended-Data-Out.

2. The logic states of "A", "B", "C", "D" and "E" determine the type of write operation performed. See the Write Cycle Function Table for a detailed description.

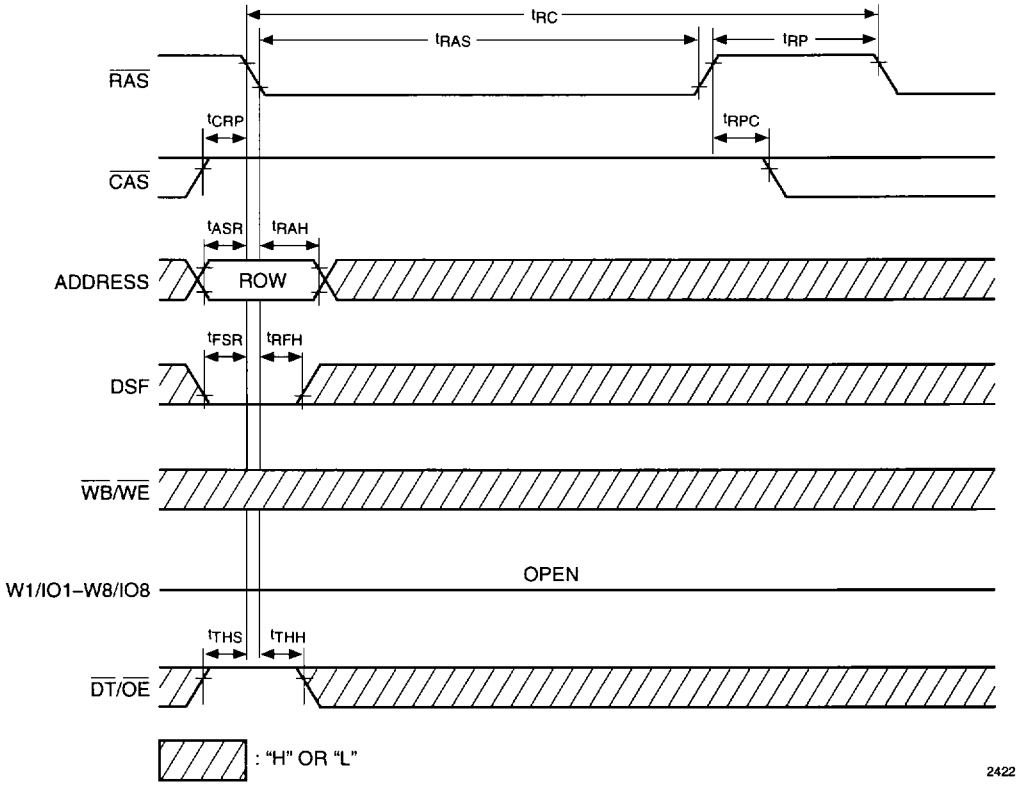
Extended-Data-Out Read-Modify-Write Cycle



Note: 1. Read or Write cycles can be mixed with Read-Modify-Write cycles while in Extended-Data-Out.

2. The logic states of "A", "B", "C", "D" and "E" determine the type of write operation performed. See the Write Cycle Function Table for a detailed description.

$\overline{RAS}$ Only Refresh Cycle



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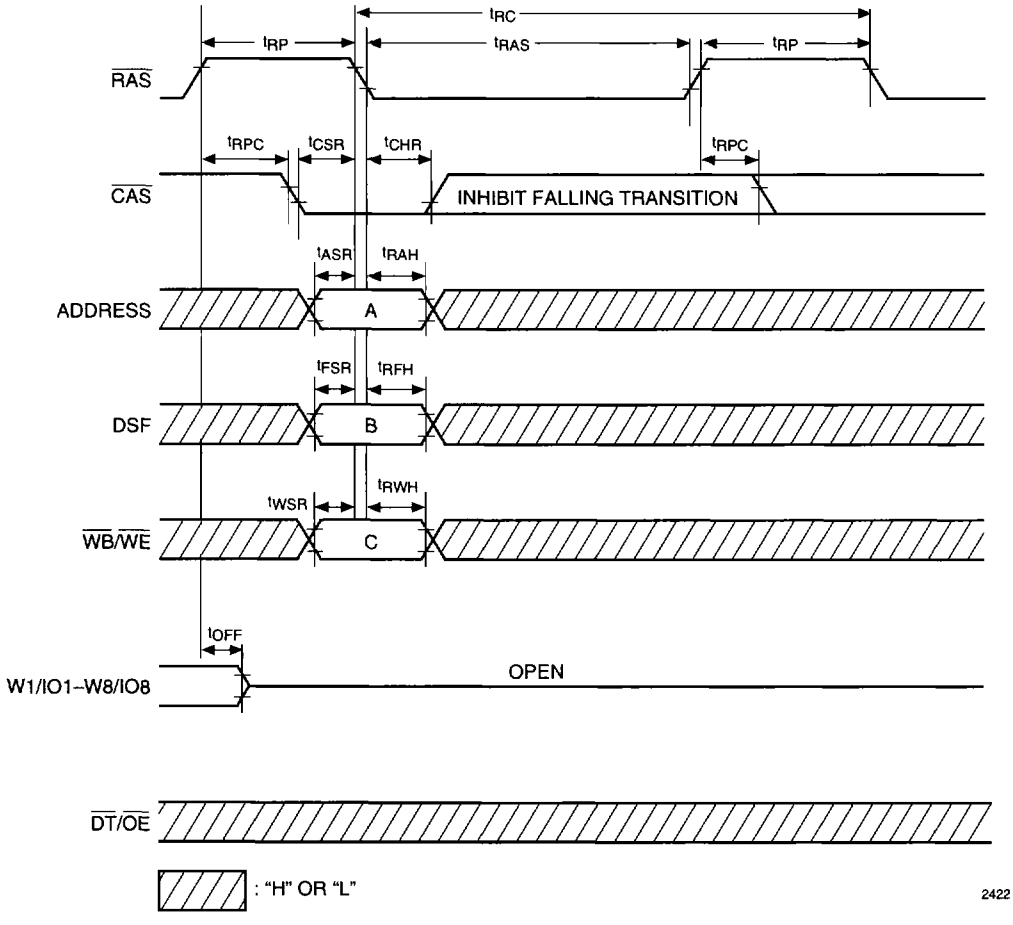
CAS before RAS Refresh Cycle

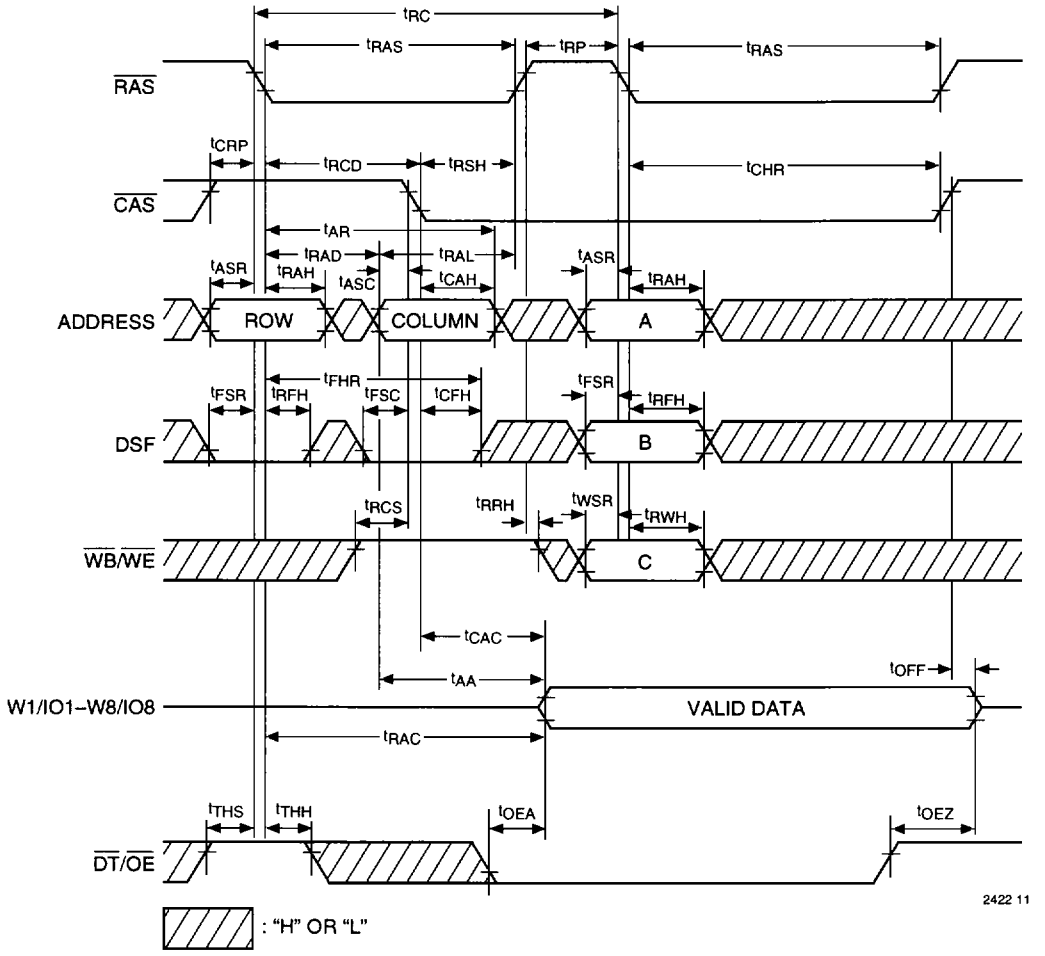


CBR Cycle Function Table

Code	RAS Falling Edge A	B	C	Function
CBRR	X	0	X	CBR refresh (reset all options)
CBRS	STOP address	1	0	CBR refresh (set STOP address)
CBRN	X	1	1	CBR refresh (no reset options)

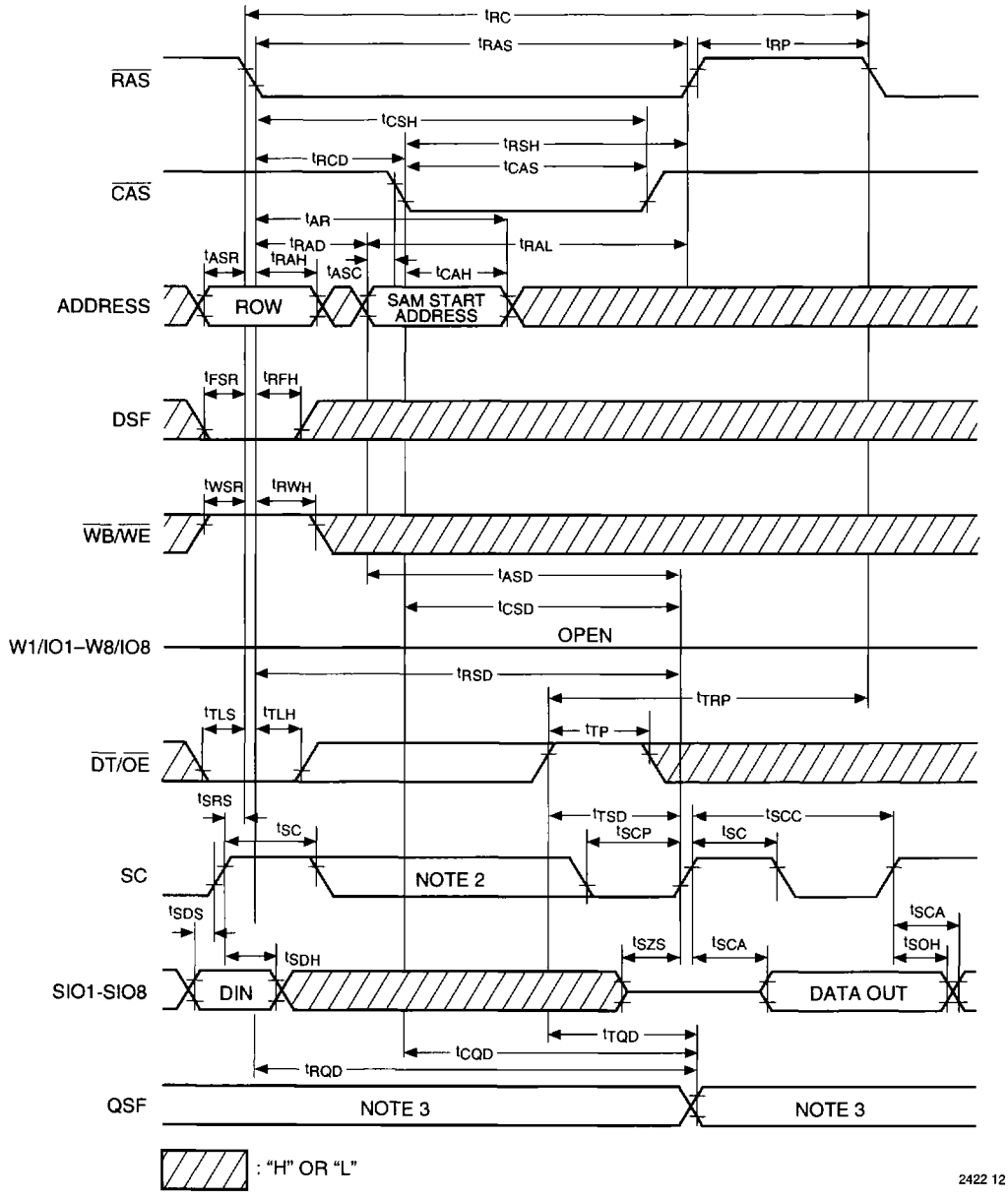
Note: The type of CBR operations are determined by the logic states of "A", "B" and "C".

Hidden Refresh Cycle



Note: The type of CBR operations are determined by the logic states of "A", "B" and "C". See CBR Cycle Function Table for a detailed description.

Read Transfer 1 (When part was previously in the Serial Input Mode)

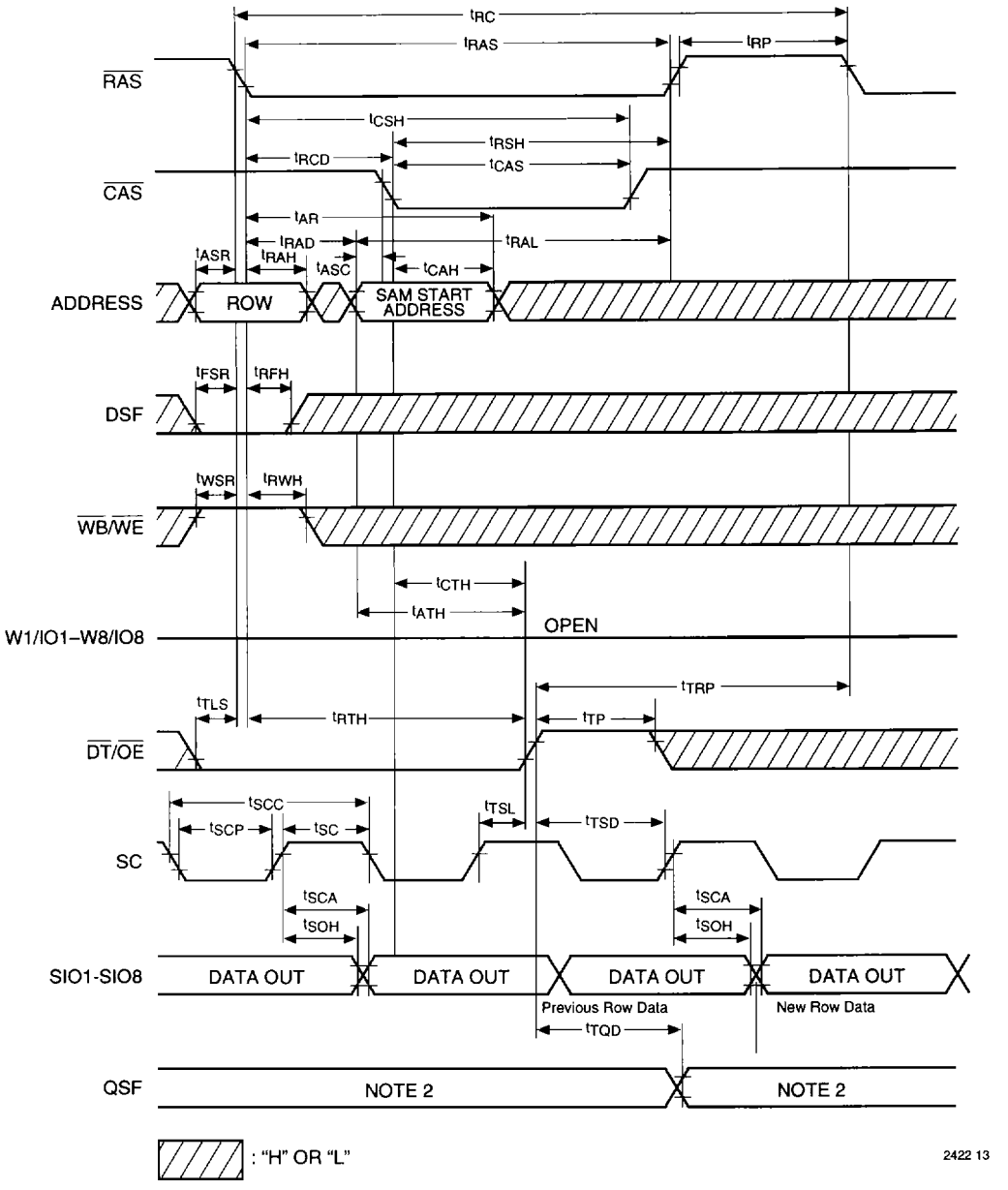


2422 12

Notes:

1. $\overline{SE}$ = "L".
2. There must be no rising transitions.
3. QSF = "L"—Lower SAM (0-255) is active
   QSF = "H"—Upper SAM (256-511) is active.

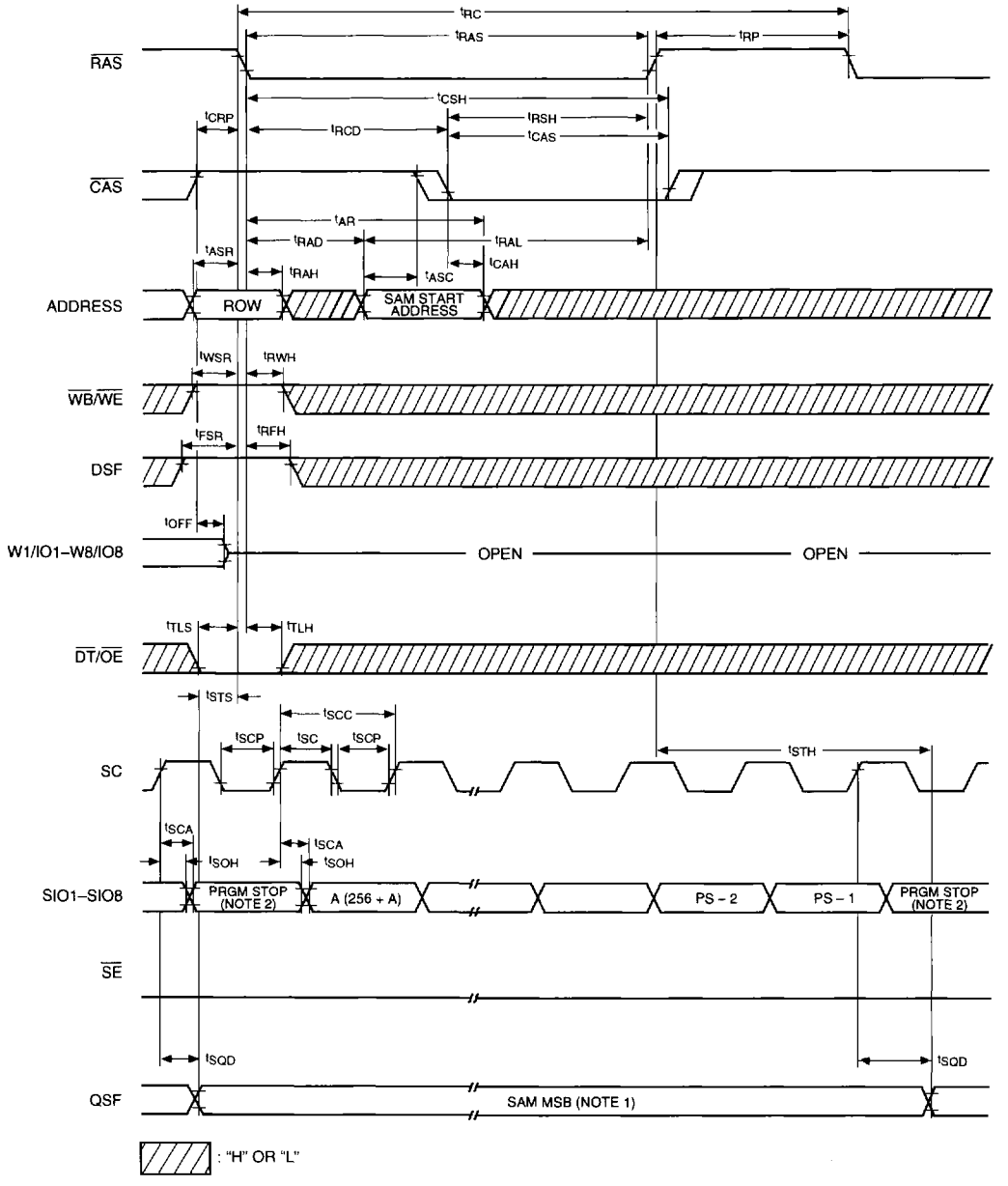
Read Transfer 2 (Real Time Read Transfer)



Notes:

1. $\overline{SE}$ = "L".
2. QSF = "L"—Lower SAM (0-255) is active
   QSF = "H"—Upper SAM (256-511) is active.

Split Read Transfer



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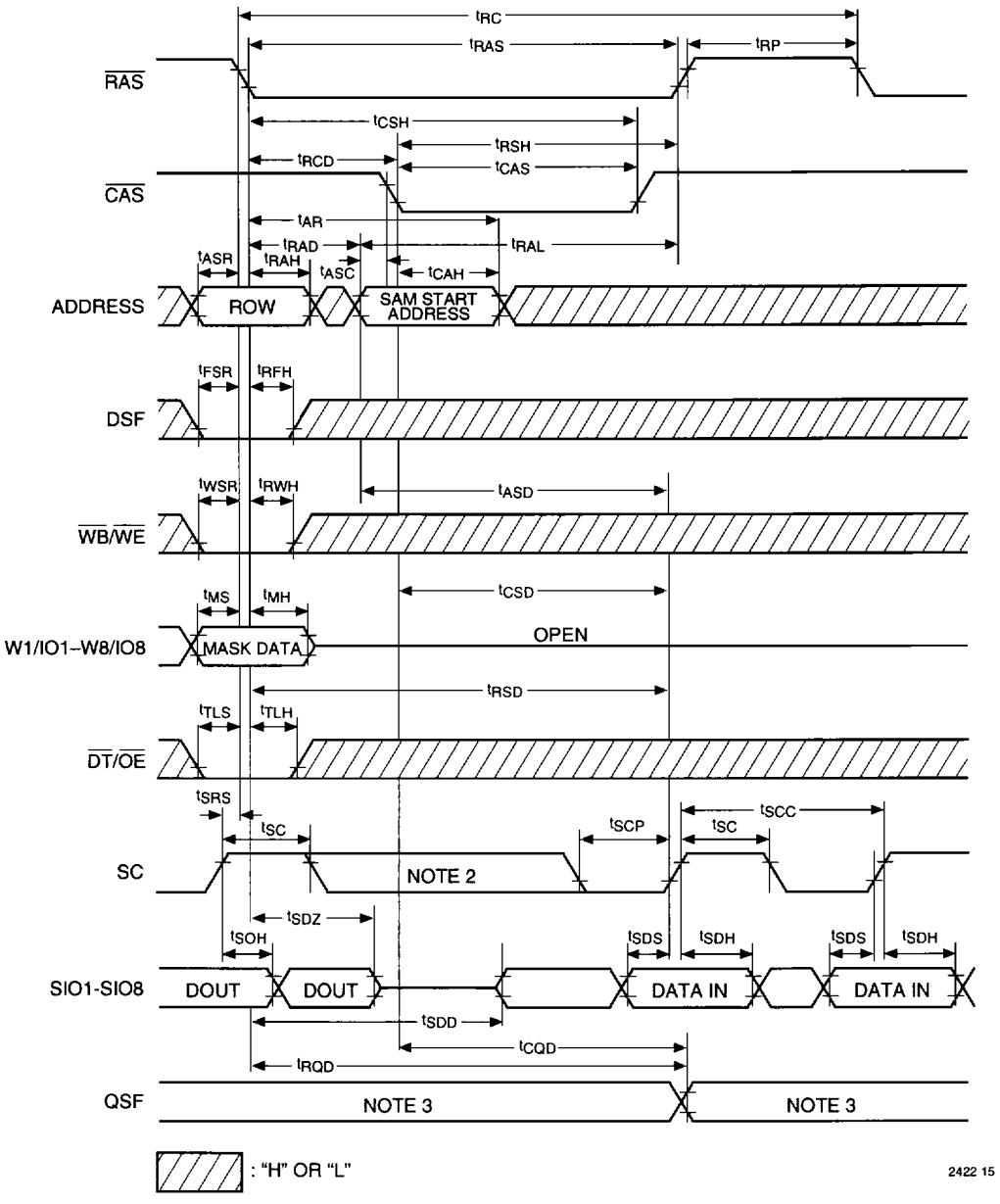
Notes:

1. QSF = "L"—Lower SAM (0-255) is active.
   QSF = "H"—Upper SAM (256-511) is active.
2. Programmable stop address or SAM half boundary (255 or 511). See the Programmable Split SAM functional description for detail.

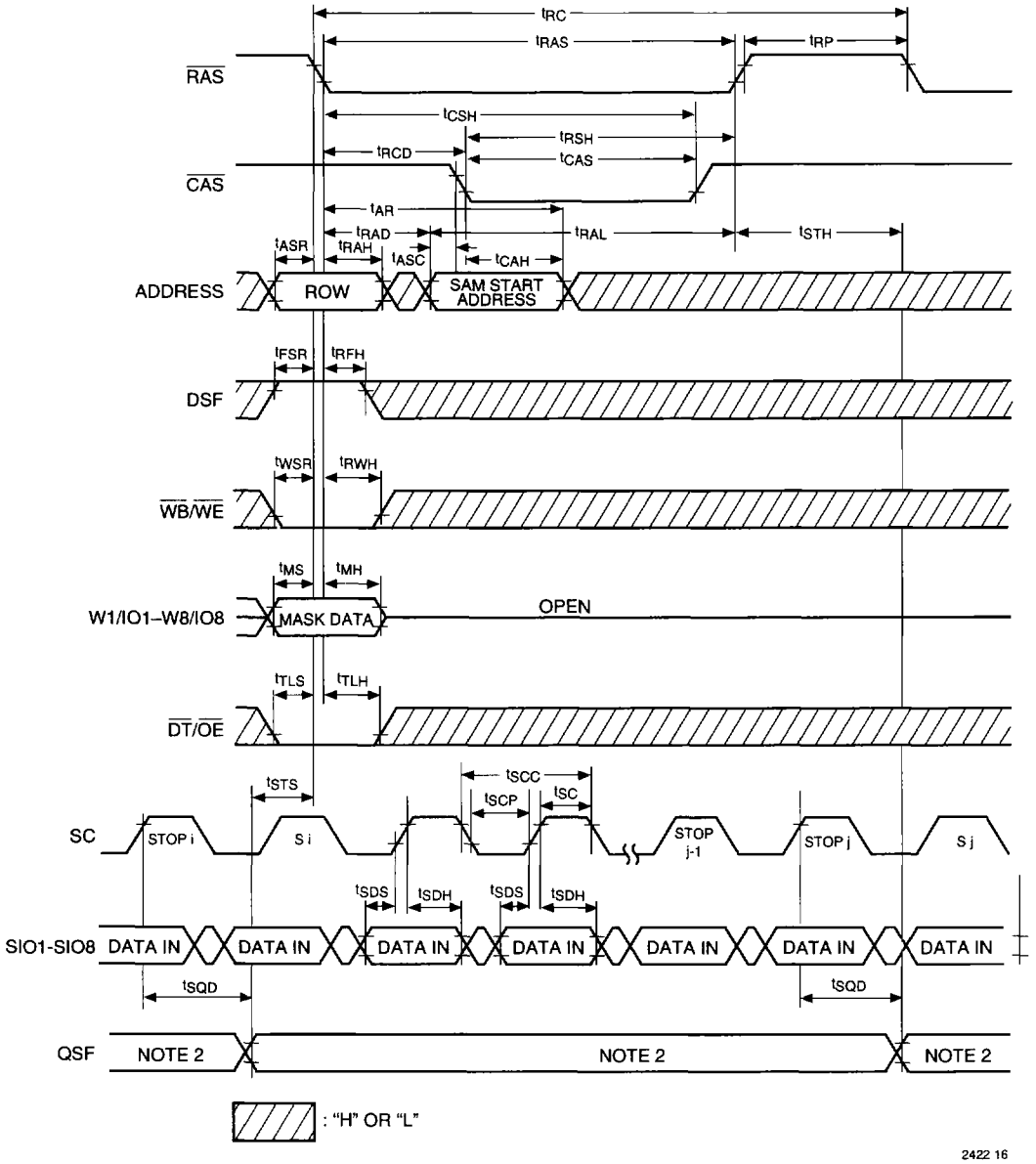
Masked Write Transfer (when part was previously in the serial output mode)



Notes:

1. $\overline{SE}$ = "L".
2. There must be no rising transitions.
3. QSF = "L"—Lower SAM (0-255) is active
   QSF = "H"—Upper SAM (256-511) is active.

Masked Split Write Transfer



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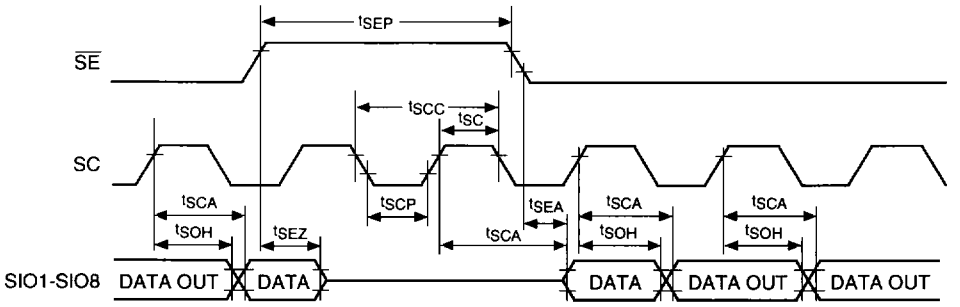
NOTES:

1. $\overline{SE}$ = "L".
2. QSF = "L"—Lower SAM (0-255) is active
   QSF = "H"—Upper SAM (256-511) is active.
3. Si is the SAM start address in before SWT.
4. STOP i and STOP j are programmable stop addresses.

Serial Read Cycle



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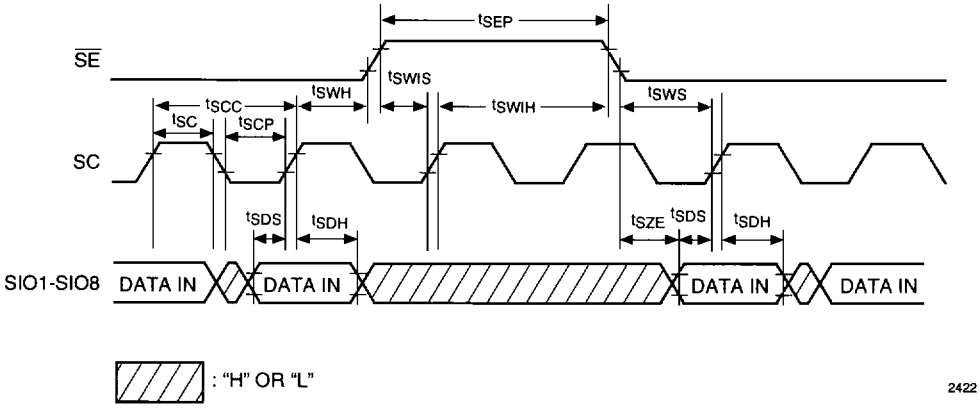
Serial Write Cycle



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Pin Functions

Address Inputs; A0–A8

The 18 address bits required to decode 8 bits of the 2,097,152 cell locations within the dynamic RAM memory array of the V52C8256 are multiplexed onto 9 address input pins (A_0–A_8). Nine row address bits are latched on the falling edge of the row address strobe ($\overline{RAS}$) and the following nine column address bits are latched on the falling edge of the column address strobe ($\overline{CAS}$).

Row Address Strobe: $\overline{RAS}$

A random access cycle or a data transfer cycle begins at the falling edge of $\overline{RAS}$. $\overline{RAS}$ is the control input that latches the row address bits and the states of $\overline{CAS}$, $\overline{DT/OE}$, $\overline{WB/WE}$ and DSF to invoke the various random access and data transfer operating modes shown in Table 1. $\overline{RAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper

device operation and data integrity. The RAM port is placed in standby mode when the $\overline{RAS}$ control is held HIGH.

Column Address Strobe: $\overline{CAS}$

$\overline{CAS}$ is the control input that latches the column address bits and the state of the special function input DSF. DSF is used in conjunction with the $\overline{RAS}$ control to select either read/write operation or the special Block Write feature on the RAM port when DSF is held LOW at the falling edge of $\overline{RAS}$. Refer to the functional truth table shown in Table 1. $\overline{CAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity.

Data Transfer/Output Enable: $\overline{DT/OE}$

The $\overline{DT/OE}$ input is a multifunction pin. When $\overline{DT/OE}$ is HIGH at the falling edge of $\overline{RAS}$, RAM port operations are performed and $\overline{DT/OE}$ is used as an output enable control. When the $\overline{DT/OE}$ is LOW at the falling edge of $\overline{RAS}$, a data transfer operation is started between the RAM port and the SAM port.

Write Per Bit/Write Enable: $\overline{WB/WE}$

The $\overline{WB/WE}$ input is also a multifunction pin. When $\overline{WB/WE}$ is "high" at the falling edge of $\overline{RAS}$, during RAM port operations, it is used to write data into the memory array in the same manner as a standard DRAM. When $\overline{WB/WE}$ is "low" at the falling edge of $\overline{RAS}$, during RAM port operations, the write-per-bit function is enabled. The $\overline{WB/WE}$ input also determines the direction of data transfer between the RAM array and the serial register (SAM).

When $\overline{WB/WE}$ is "high" at the falling edge of $\overline{RAS}$, the data is transferred from RAM to SAM (read transfer). When $\overline{WB/WE}$ is "low" at the falling edge of $\overline{RAS}$, the data is transferred from SAM to RAM (masked write transfer).

Write Mask Data/Data Input and Output: W_1/IO_1–W_8/IO_8

When the nonpersistent mask write function is enabled, the mask data on the W_i/IO_i pins is latched into the write mask register (WM1) at the falling edge of $\overline{RAS}$. Data is written into the DRAM on data lines where the write-mask data is a logic "1". Writing is inhibited on data lines where the write-mask data is a logic "0". The write-mask data is valid for only one cycle. Data is written into the RAM port during a write or read-modify-write cycle. The input data is latched at the falling edge of either $\overline{CAS}$ or $\overline{WB/WE}$, whichever occurs late. During an early-write cycle, the outputs are in the high-impedance state. Data is read out of the RAM port during a read or read-modify-write cycle. The output data becomes valid on the W_i/IO_i pins after the specified access times from $\overline{RAS}$, $\overline{CAS}$, $\overline{DT/OE}$ and column address are satisfied.

Serial Clock: SC

In the serial read cycle, the 4096 bits in the Data Register are available in sequential order on a Low-to-High transition on SC (starting from the location specified in the data transfer cycle).

In the serial write cycle, a Low-to-High transition on SC latches the data on the SIO1-SIO8 input.

The serial clock should not let it be floated. It should be held at either logic LOW or HIGH to prevent false serial counter increment information.

Serial Enable: $\overline{SE}$

The $\overline{SE}$ input is used to enable serial access operation. In a serial read cycle, $\overline{SE}$ is used as an output control. In a serial write cycle, $\overline{SE}$ is used as a write enable control. When $\overline{SE}$ is "high", serial access is disabled, however, the serial address pointer location is still incremented when SC is clocked even when $\overline{SE}$ is "high".

Special Function Control: DSF

Falling edge of $\overline{RAS}$ and $\overline{CAS}$ latch the DSF input level to initiate one of the operations shown in Table 1.

Special Function Output: QSF

QSF indicates which side of the split register is active. QSF high shows that the upper half (addresses 256 through 511) is active; QSF low indicates the lower half (addresses 0 through 255).

Serial Input/Output: SIO1–SIO8

Serial input and output share common I/O pins. Serial input or output mode is determined by the most recent read or write transfer. When a read transfer cycle is performed, the SAM port is in the output mode. When a write transfer cycle is performed, the SAM port is switched from output mode to input mode. During the subsequent write transfer cycle, the SAM remains in the input mode.

Operation Mode

The RAM port and data transfer operating of the V52C8256 are determined by the state of $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ and DSF at the falling edge of $\overline{RAS}$ and by the state of DSF at the falling edge of $\overline{CAS}$. Table 1 shows the functional truth table for a listing of all available RAM port and transfer operations.

Table 1. Functional Truth Table

Code	Function	$\overline{RAS}\downarrow$				$\overline{CAS}\downarrow$	Address		W/IO		Write Mask	Pers. WM	Register	
		$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	DSF	DSF	$\overline{RAS}\downarrow$	$\overline{CAS}\downarrow$	$\overline{RAS}\downarrow$	$\overline{CAS}/\overline{WE}\downarrow$			WM	Color
CBRR	CBR refresh with register reset	0	•	•	0	—	•	•	•	•	—	Reset	Reset	—
CBRS	CBR refresh with stop register set	0	•	0	1	—	STOP	•	•	•	—	—	—	—
CBRN	CBR refresh (no reset)	0	•	1	1	—	•	•	•	•	—	—	—	—
ROR	RAS-only refresh	1	1	•	0	—	Row	—	•	—	—	—	—	—
MWT	Masked write transfer	1	0	0	0	•	Row	TAP	WM1	•	Yes	No/Yes	Load Use	—
MSWT	Masked split write transfer	1	0	0	1	•	Row	TAP	WM1	•	Yes	No/Yes	Load Use	—
RT	Read transfer	1	0	1	0	•	Row	TAP	•	•	—	—	—	—
SRT	Split read transfer	1	0	1	1	•	Row	TAP	•	•	—	—	—	—
RWM	Read/write (new/old mask)	1	1	0	0	0	Row	Column	WM1	D_{IN},D_{OUT}	Yes	No/Yes	Load Use	—
BWM	Masked block write (new/old)	1	1	0	0	1	Row	Column A2c-A8c	WM1	Column Select	Yes	No/Yes	Load Use	Use
FWM	Masked flash write	1	1	0	1	•	Row	•	WM1	—	Yes	No/Yes	Load Use	Use
RW	Read write (no mask)	1	1	1	0	0	Row	Column	•	D_{IN},D_{OUT}	No	No	—	—
BW	Block write (no mask)	1	1	1	0	1	Row	Column A2c-A8c	•	Column Select	No	No	—	Use
LMR	Load/Read mask reg. (old mask set)	1	1	1	1	0	Row	•	•	Mask Data	—	Set	Load	—
LCR	Load/Read color register	1	1	1	1	1	Row	•	•	Color Data	—	—	—	Load

NOTES:

1. With CBRS, SAM operations use stop register.
2. MWT, RWM, BWM, FWM and MSWT use old mask which is loaded by previous LMR cycle and can be reset by CBRR.
3. • = "0" or "1", — = not used, Pers. = persistent

If the DSF is HIGH at the falling edge of $\overline{RAS}$, special functions such as split transfer, flash write, load mask register, load color register, CBRS and CBRN can be invoked.

If the DSF is LOW at the falling edge of $\overline{RAS}$ and HIGH at the falling edge of $\overline{CAS}$, the block write feature can be enabled.

RAM Port Operation

$\overline{RAS}$-Only Refresh

The data in the DRAM requires periodic refreshing to prevent data loss. Refreshing is accomplished by performing a memory cycle at each of the 512 rows in the DRAM array within the specified 8ms refresh period. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with the "$\overline{RAS}$-Only" cycle.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh

The V52C8256 also offers an internal-refresh function. When $\overline{CAS}$ is held "low" for a specified period (t_{CSR}) before $\overline{RAS}$ goes "low", an internal refresh address counter and on-chip refresh control clock generators are enabled and an internal refresh operation takes place. When the refresh operation is completed, the internal refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ cycle. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain "low" while cycling $\overline{RAS}$.

Hidden Refresh

A hidden refresh is a $\overline{CAS}$-before-$\overline{RAS}$ refresh performed by holding $\overline{CAS}$ "low" from a previous read cycle. This allows for the output data from the previous memory cycle to remain valid while performing a refresh. The internal refresh address counter provides the address and the refresh is accomplished by cycling $\overline{RAS}$ after the specified $\overline{RAS}$-precharge period (refer to Figure 1).

Flash Write Cycle, Write Only (FWM new mask)

A single $\overline{RAS}$ cycle clears or sets the eight 512-bit data sets on the selected one of 512 rows. The Color Register data previously stored in provides the Flash Write data. Bit mask data is latched on a falling edge of $\overline{RAS}$ during this cycle. This operation is most effective for fast "clear screen" operations in graphic systems.

Flash Write Cycle, Write only (FWM old mask)

Same as the FWM except the Mask Register provides the bit mask data. The Mask Register data previously stored by the LMR cycle provides the Flash Write mask data.

Load Color Register Cycle, Read & Write (LCR)

Load Color Register cycle is identical to the Load Mask Register cycle except DSF is HIGH when $\overline{CAS}$ goes LOW. An on-chip 8-bit Color Register is provided for use during the Flash or Block Write operation. This cycle is similar to the Load Mask Register read or write cycle. The contents of the 8-bit Color Register are retained until changed by new data. The Color Register data is read or write through the common Wn/IOn pins.

Load Mask Register Cycle (LMR).

In this cycle, data on W_n/IO_n is written to an 8-bit write mask register, where it is retained and used by subsequent masked write and masked block write cycles.

Block Write

Block write is also a special RAM port write operation which, in a single $\overline{RAS}$ cycle, allows for the data in the color register to be written into 4 consecutive column address locations starting from a selected column address in a selected row. The block write operation can be selectively controlled on an I/O basis and a column mask capability is also available.

A block write cycle is performed by holding $\overline{CAS}$ and $\overline{DT/OE}$ "high" and DSF "low" at the falling edge of $\overline{RAS}$ and by holding DSF "high" at the falling edge of $\overline{CAS}$. The state of the $\overline{WB/WE}$ input at the falling edge of $\overline{RAS}$ determines whether or not the I/O data mask is enabled ($\overline{WB/WE}$ must be "low" to enable the I/O data mask or "high" to disable it). At the falling edge of $\overline{RAS}$, a valid row address and I/O mask data are also specified. At the falling edge of

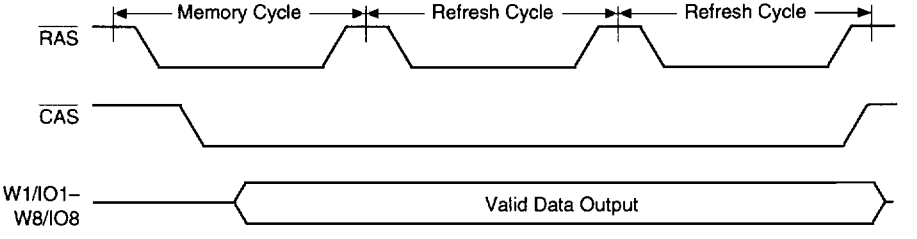

Figure 1. Hidden Refresh Cycle

$\overline{CAS}$, the starting column address location and column mask data must be provided. During a block write cycle, the 2 least significant column address locations (A0C and A1C) are internally controlled and only the seven most significant column addresses (A2C–A8C) are latched at the falling edge of $\overline{CAS}$. (Refer to Figure 2.)

An example of the block write function is shown in Figure 3 with a data mask on W1/IO1, W4/IO4, W6/IO6, W7/IO7 and column 2. Block write is most effective for window clear and fill operations in frame buffer applications, as shown on Figure 4.

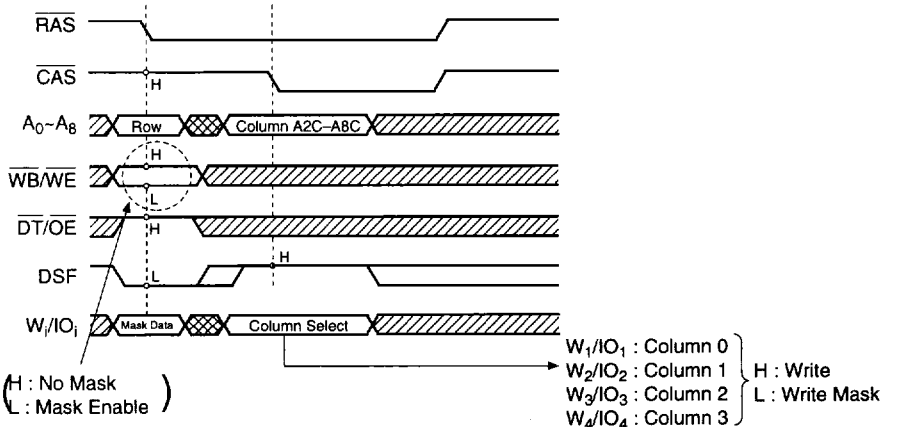

Figure 2. Block Write Timing

	Mask Data	Column Select	Color Register Data
W_1/IO_1	0	1	0
W_2/IO_2	1	1	0
W_3/IO_3	1	0	1
W_4/IO_4	0	1	1
W_5/IO_5	1	—	1
W_6/IO_6	0	—	1
W_7/IO_7	0	—	0
W_8/IO_8	1	—	0

	Column 0	Column 1	Column 2	Column 3	
W_1/IO_1					← Mask
W_2/IO_2	0	0		0	
W_3/IO_3	1	1		1	
W_4/IO_4					← Mask
W_5/IO_5	1	1		1	
W_6/IO_6					← Mask
W_7/IO_7					← Mask
W_8/IO_8	0	0		0	
			↑ Mask		

Figure 3. Example for Block Write

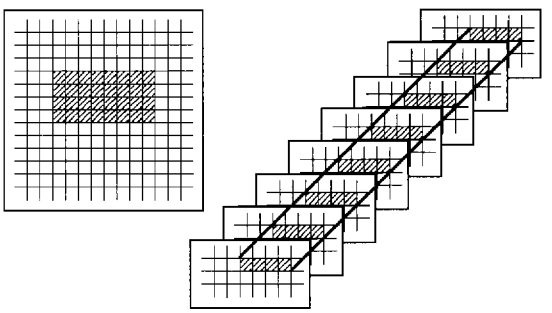

Figure 4. Example of Block Write Application

Block Write Cycle With New Mask, Write only (BWM)

Data on the W1/IO1–W8/IO8 allows for masking during a Block Write cycle. This operation is the same as a standard Masked Write cycle with new mask,but four consecutive columns are written.

Block Write Cycle With Old Mask, Write only (BWM)

Block Write cycle requires the mask data previously stored in the Mask Register. LMR cycle is required to store the mask data. Four consecutive columns are written by a single Block Write cycle.

Hyper-page Mode–Extended Data Output, Read & Write

Hyper-page mode timing is similar to the Fast Page mode. Same as in the Fast Page mode, maintaining $\overline{RAS}$ LOW while a HIGH-to-LOW transition on $\overline{CAS}$ input latches successive column addresses. Hyper-page mode allows conventional read, write and read-modify-write. The Write-Per-Bit control remains effective throughout the mode.

The Hyper-page mode offers an extended data output which eliminates the toff Tri-state and the output data to remain active even $\overline{CAS}$ goes HIGH. Hyper-page mode eliminates the Tri-state data float skew and achieves faster page cycle time.

SAM Port Operation

Serial Port Read

The serial read port is used to serial read the previously loaded contents of the serial data register starting from a specified column address set by the previous read or split read transfer.

Read Data Transfer (RT) Read

In a full-row Read Data transfer cycle, one of the 512 rows is selected by the row address and the transfer starting address is specified by column address, followed by Serial Read cycle, transfers the memory data to the both split Serial Data Registers. A LOW-to-HIGH transition on a $\overline{DT}/\overline{OE}$ input transfers 4096 bits of the memory data to the eight Serial Data Registers. Although the Read Data transfer cycle inhibits the boundary jump in the Read Data transfer, the data in the stop register remains unchanged. During the cycle the QSF output reflects by the column address.

Split Read Data Transfer (SRT), Read

During a split read data transfer cycle, a half row of memory data is transferred to the inactive split half serial registers. The row addresses select the half row to be transferred and the column addresses (A7-A0) set the tap or pointer for the start of the serial read operation. A split read transfer does not change the direction of the serial port I/O.

Serial Port Write

Serial data can be written to Serial Data Register specified by the column address for the starting address specified by the previous write or split write transfer. Subsequently the data can be transferred to memory array location specified by the row address.V52C8256 allows both a split write and full register write transfer.

Masked Write Data Transfer (MWT), Write

The Masked Write Data Transfer with Write-Per-Bit transfers the data from both split Serial Registers to the memory array specified by the row address. Column address specifies the start location of the following Serial Write operation. If Serial Read operation was performed previously, the MWT operation requires the serial I/O direction change. In addition, SC clock should not be applied during all MWT cycles and the system timing must meet the t_{SRS} and t_{RSD}.

Unless the masking or Write-Per-Bit function is applied, the content of the memory array will be effected by the Write Data Transfer. A Write-Per-Bit mask inhibits data from being transferred to the memory array.

The MWT cycle disables the boundary jump function of the Serial Port in the mean time content of the Stop Register is unchanged. QSF output will reflect by the column address during the MWT cycle.

Masked Split Write Data Transfer (MSWT), Write

This mode allows the data transfer from the selected split-half Serial Reister to the half row in the memory array specified by the row address. Serial Port data is always transferred from inactive half of the split register to the half row in the memory array specified by the row address.

The same Write-Per-Bit function works as described in the MWT cycle.

QSF Special Function Output, Read

This output indicates which half of the serial data register is active. The QSF output is synchronized with the SC rising edge. A high indicates an upper half address (256-511) and low indicates a lower half address (0-255).

Stopping Column Control

Unlike 1M-bit VRAM products, the V52C8256 is equipped with an 8-bit Stop Register, indicates a boundary location in each Split half register. The Stop Register value is stored during a special $\overline{CAS}$-Before-$\overline{RAS}$ cycle (CBRS).

A0–A7 data represented as stop value. Stop Register set cycle specifies sixteen different stop boundaries for each half register. Stop Register allows mid-register to mid-register jump (see Table 3).

Table 3. Stop Register Set

Stop Register Value A7–A0	Boundary Location (Jumps to tap after accessing this boundary)
1111 XXXX	255, 511 (default)
0111 XXXX	127, 255, 383, 511
X011 XXXX	63, 127, 191, 255, 319, 383, 447, 511
XX01 XXXX	31, 63, 95, 127, 159, 191, 223, 255, 287, 319, 351, 383, 415, 447, 479, 511
XXX0 XXXX	15, 31, 47, 63, 79, 95, 111, 127, 143, 159, 175, 191, 207, 223, 239, 255, 271, 287, 303, 319, 335, 351, 367, 383, 399, 415, 431, 447, 463, 479, 495, 511

X: Don't care

	①	②	③	③	④	⑤	⑤	⑥	⑦
Power Up	8 RAS Cycles	CBRS or CBR	Read Data Transfer	Split Read Data Xfer	Split Read Data Xfer	Masked Write Data Transfer	Split Write Data Transfers	Split Write Data Transfers	Read Data Transfer	Split Read Data Xfer

NOTES:

1. A CBRS or CBR is required to set up the serial register boundaries. A CBR alone or a CBRS with A7–A0 set to (11111111) sets the serial register to 255 and 511 splits.
2. A full line data transfer is required before a sequence of split read or write transfers.
3. Rising edges of SC clocks are not allowed in this restricted window for serial address 255 and 511. The restricting parameters are t_{STS} and t_{STH}.
4. No SC clocks are allowed during the period specified by t_{SRS}.
5. Rising edges of SC clocks are not allowed in this restricted window for serial addresses 255 and 511. The restricting parameters are t_{STS} and t_{STH}.
6. No SC clocks are allowed during the period specified by t_{SRS}.
7. The numbers at SIO_n indicate the serial read or write address.

Figure 5. Example of Split Read and Split Write Data Transfers (Sheet 1 of 3)

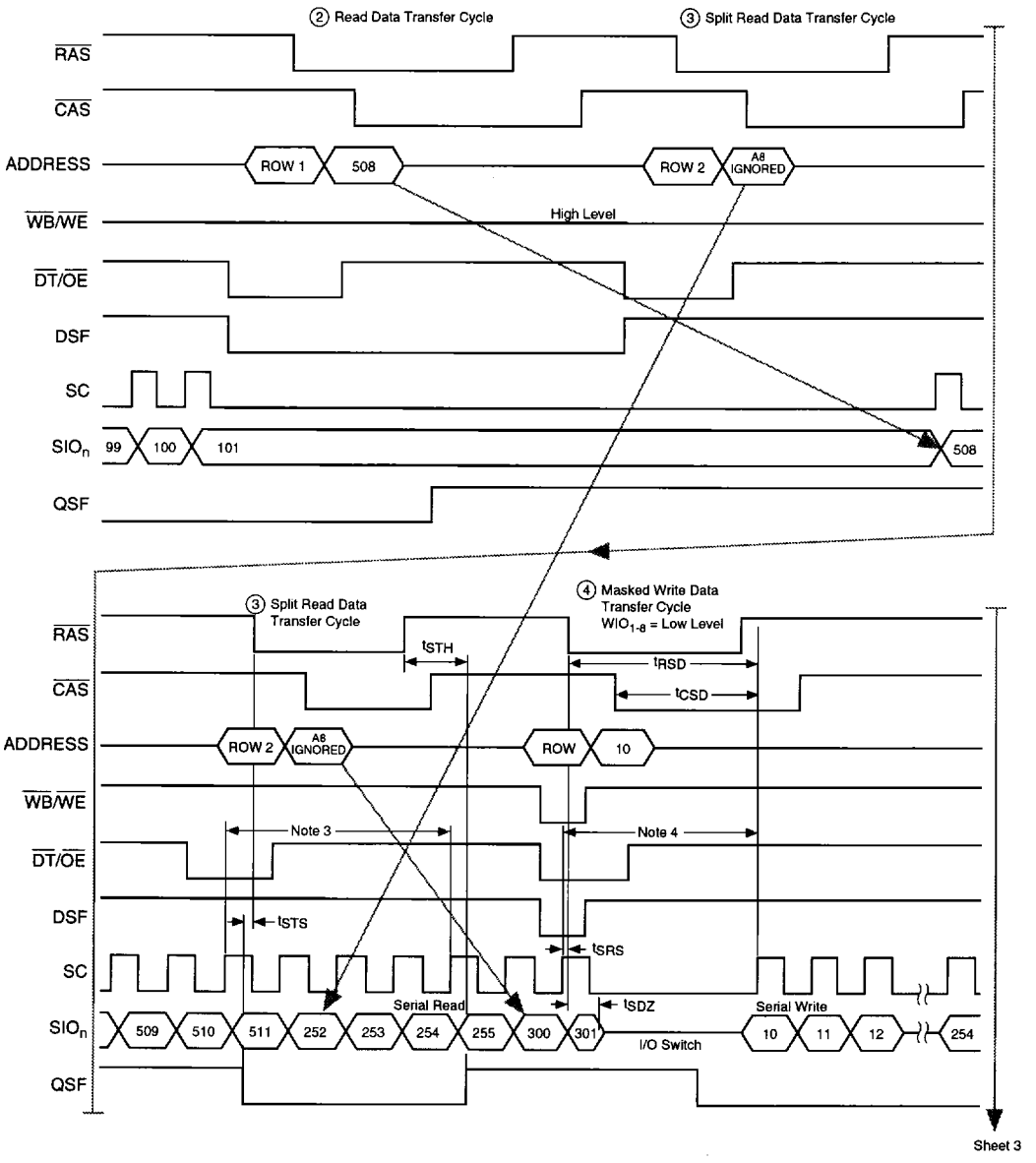

Figure 6. Example of Split Read and Split Write Data Transfers (Sheet 2 of 3)

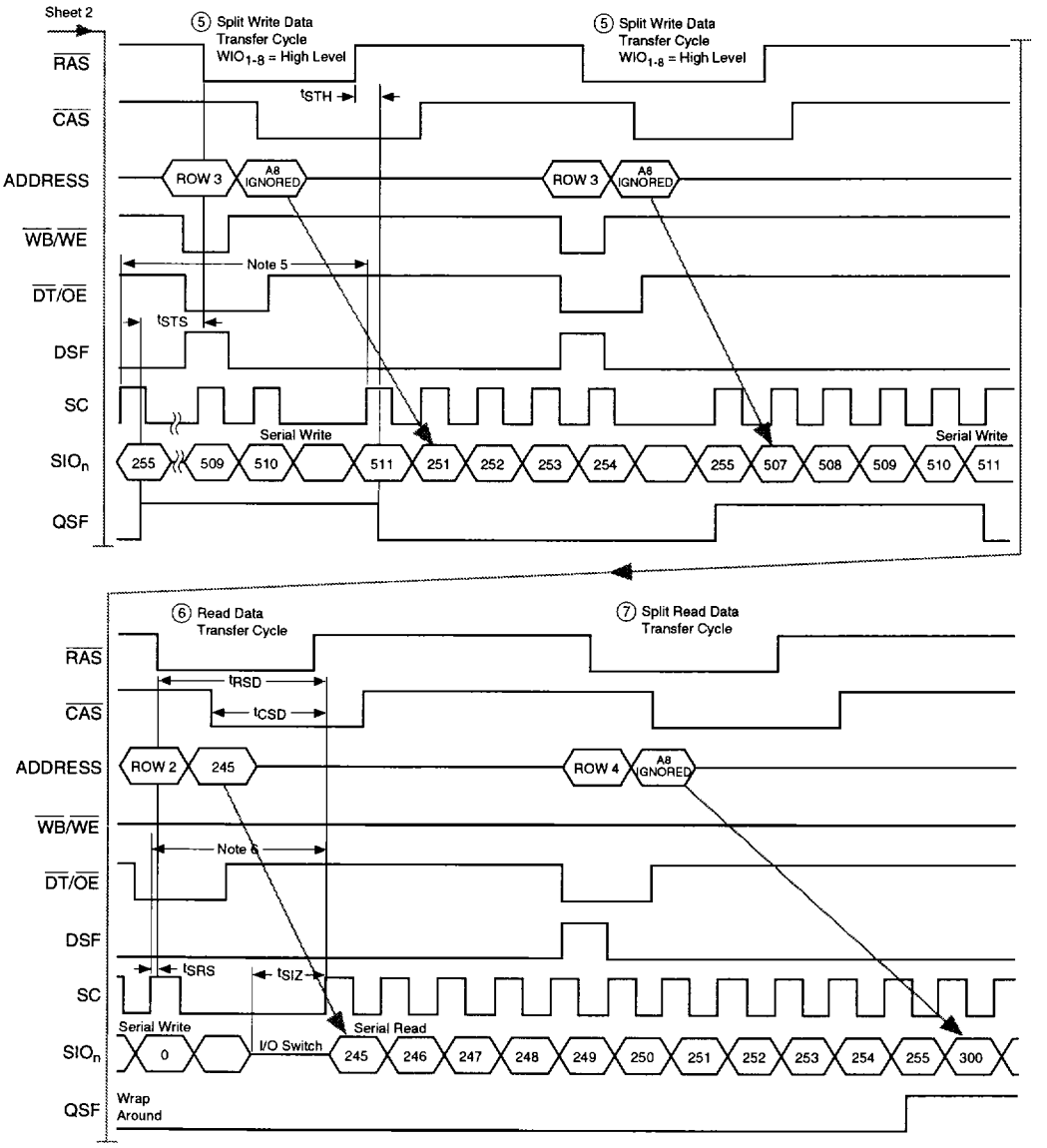

Figure 7. Example of Split Read and Split Write Data Transfers (Sheet 3 of 3)

Power-Up

Power must be applied to the $\overline{RAS}$ and $\overline{DT/OE}$ input signals to pull them "high" before or at the same time as the V_{DD} supply is turned on. After power-up, a pause of 200 µseconds minimum is required with $\overline{RAS}$ and $\overline{DT/OE}$ held "high". After the pause, a minimum of 8 $\overline{RAS}$ and 8 SC dummy cycles must be performed to stabilize the internal circuitry, before valid read, write or transfer operations can begin. During the initialization period, the $\overline{DT/OE}$ signal must be held "high". If the internal refresh counter is used, a minimum 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of 8 $\overline{RAS}$ cycles.

Initial State After Power-Up

When power is achieved with $\overline{RAS}$, $\overline{CAS}$, $\overline{DT/OE}$ and $\overline{WB/WE}$ held "high", the internal state of the V52C8256 is automatically set as follows.

However, the initial state can not be guaranteed for various power-up conditions and input signal levels. Therefore, it is recommended that the initial state be set after the initialization of the device is performed (200 µs pause followed by a minimum of 8 $\overline{RAS}$ cycles and 8 SC cycles) and before valid operations begin.

	State after power-up
SAM port	Input Mode
QSF	0
Color Register	unknown