
Zybo-Z7-20: Prepare Board Files

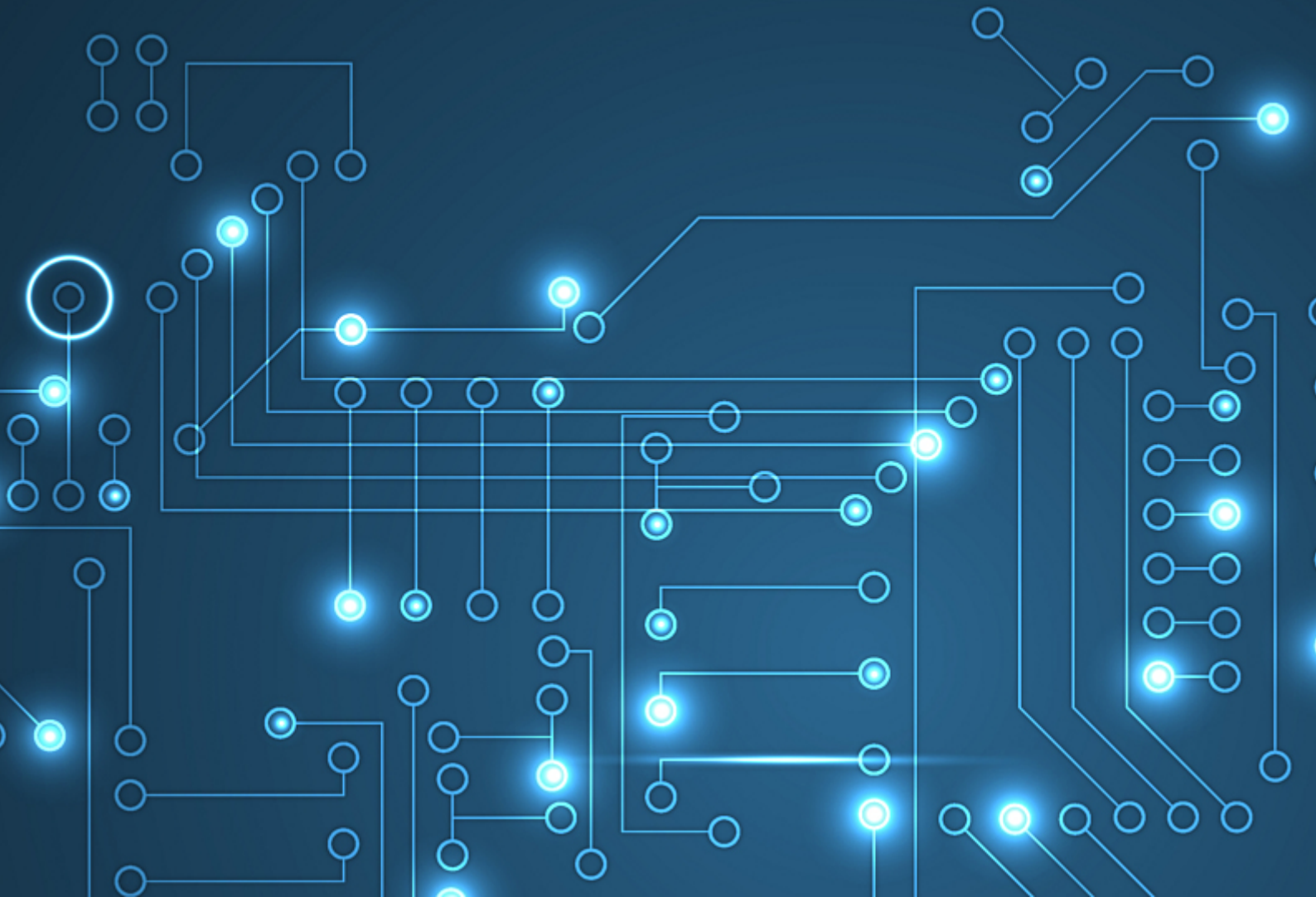
A companion guide to the text book:

A Practical Introduction to the Xilinx Zynq-7000 Adaptive SoC

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Version: 1.0

Date: 29/8/21



Revision History

Version	Date	Comment
1.0	29/8/21	First Version

Table 18.1. Revision History

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1 Introduction

This step-by-step guide provides an optional approach to preparing the Vivado board files for the Zybo-Z7-20 platform. (The steps are also applicable to the Zybo-Z7-10). The main aim is to update the *preset.xml* file with the following changes:

1. The DDR DQS-to-CLK Delay settings are set to zero. This is to suppress a critical warning that occurs due to the values initially being set to negative values. See [Zybo-Z7-20 Hardware Errata](#) on the Digilent Website for more information.
2. The internal pull-ups for MIO50 and MIO51 (BTN4 and BTN5 respectively on the board) are changed from enabled to disabled.

These settings are proven to work with the projects in the related text book, but it is up to the reader if they want to implement them.

2 Procedure

The process starts with the retrieval of the Zybo-Z7-20 board files from the Digilent GitHub repository (<https://github.com/Digilent/vivado-boards>).

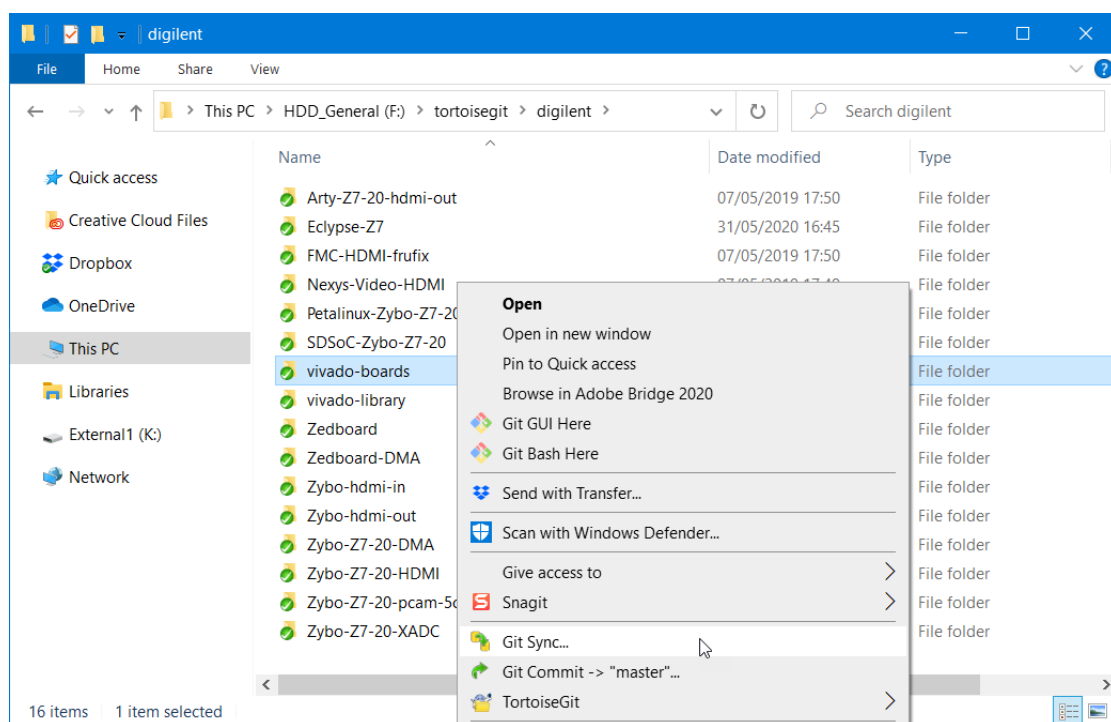


Figure 1. Retrieve the Digilent board files

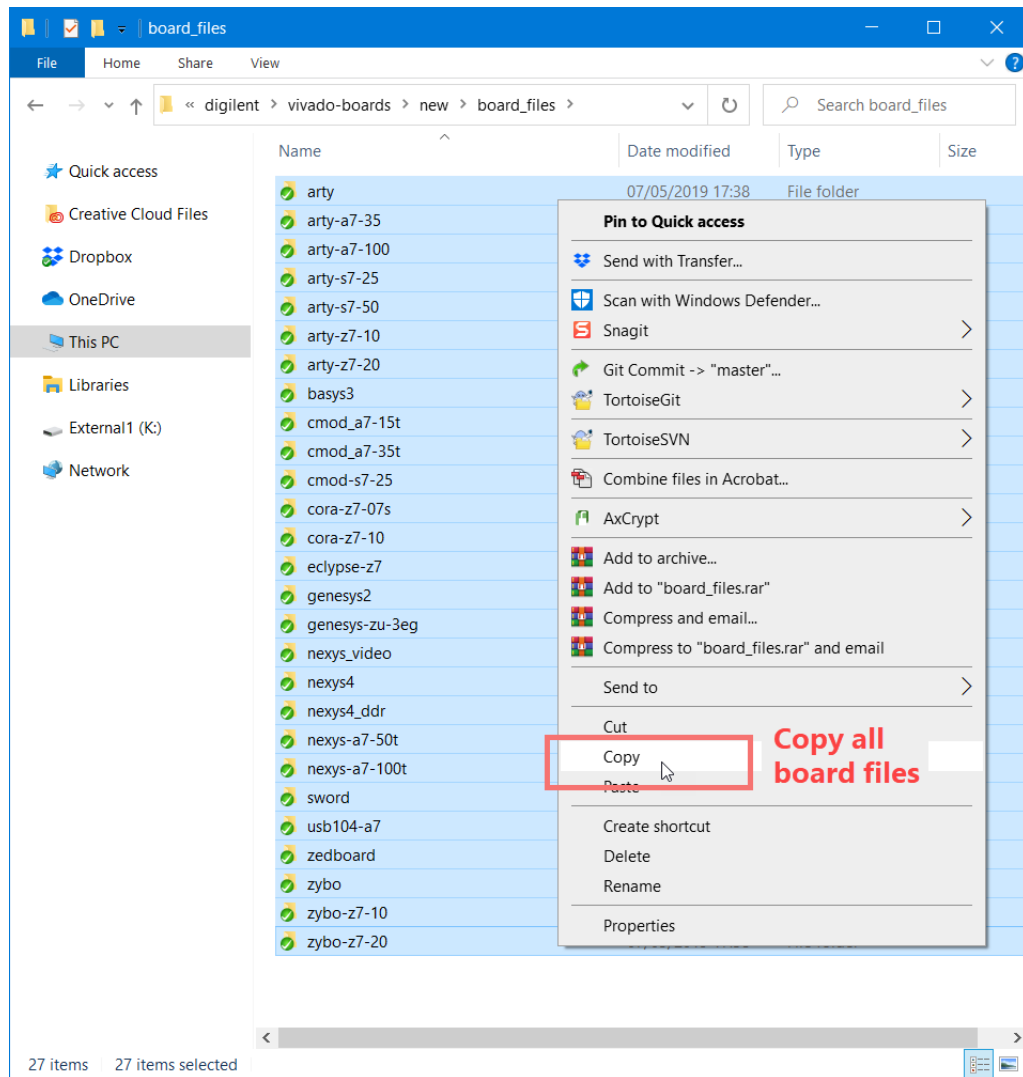


Figure 2. Copy the files

When the files are available, go to: *[Git] -> Digilent -> vivado-boards -> new -> board_files*. Then, copy all board files.

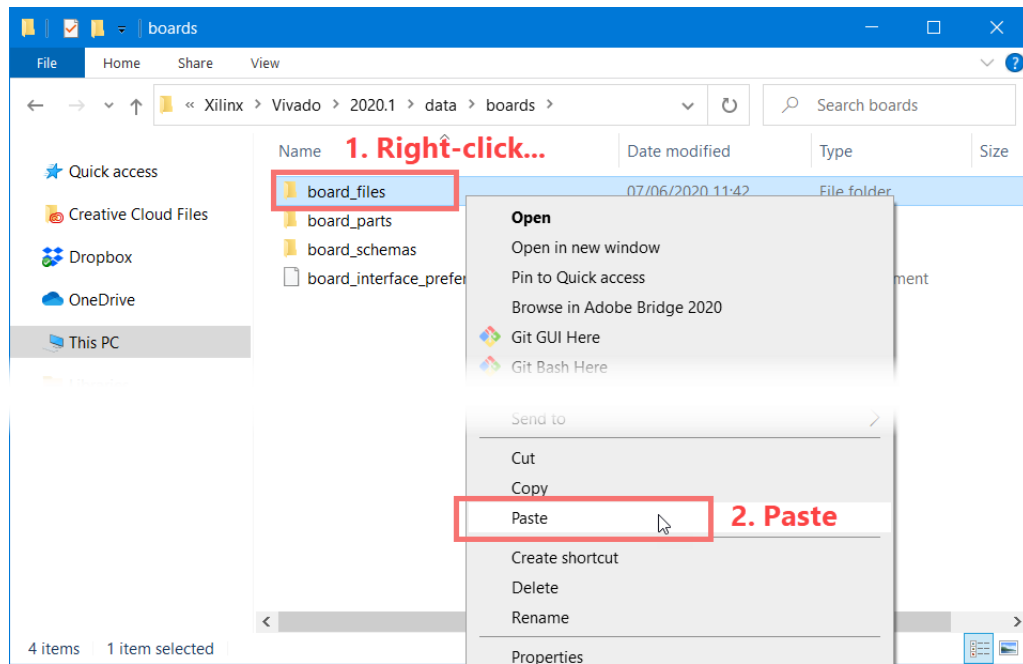


Figure 3. Paste the copied files into the correct location in the Vivado installation

In the Vivado installation directory (usually *C:\Xilinx\Vivado*), paste the copied files to the *board_files* directory: For example, for Vivado 2020.1, the location is:

- C:\Xilinx\Vivado\2020.1\data\boards\board_files

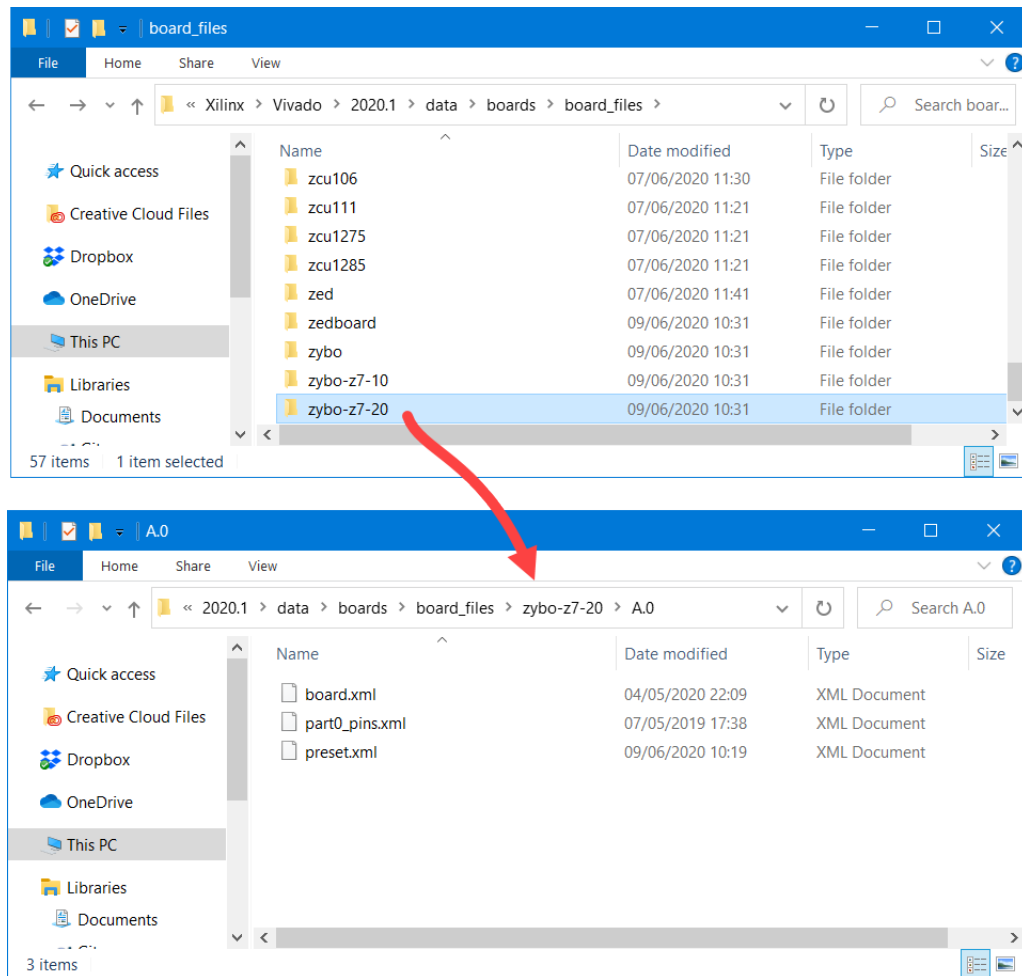


Figure 4. Navigate to the Zybo-Z7-20 (or Zybo-Z7-10) board files directory

In the *board_files* directory, navigate to *zybo-z7-20* -> *A0* (assuming that *A0* is the most up-to-date version). Three files should be present:

- boards.xml
- part0_pins.xml
- preset.xml

(If using the Zybo-Z7-10, navigate to that directory instead. Files with the same names should be present.)

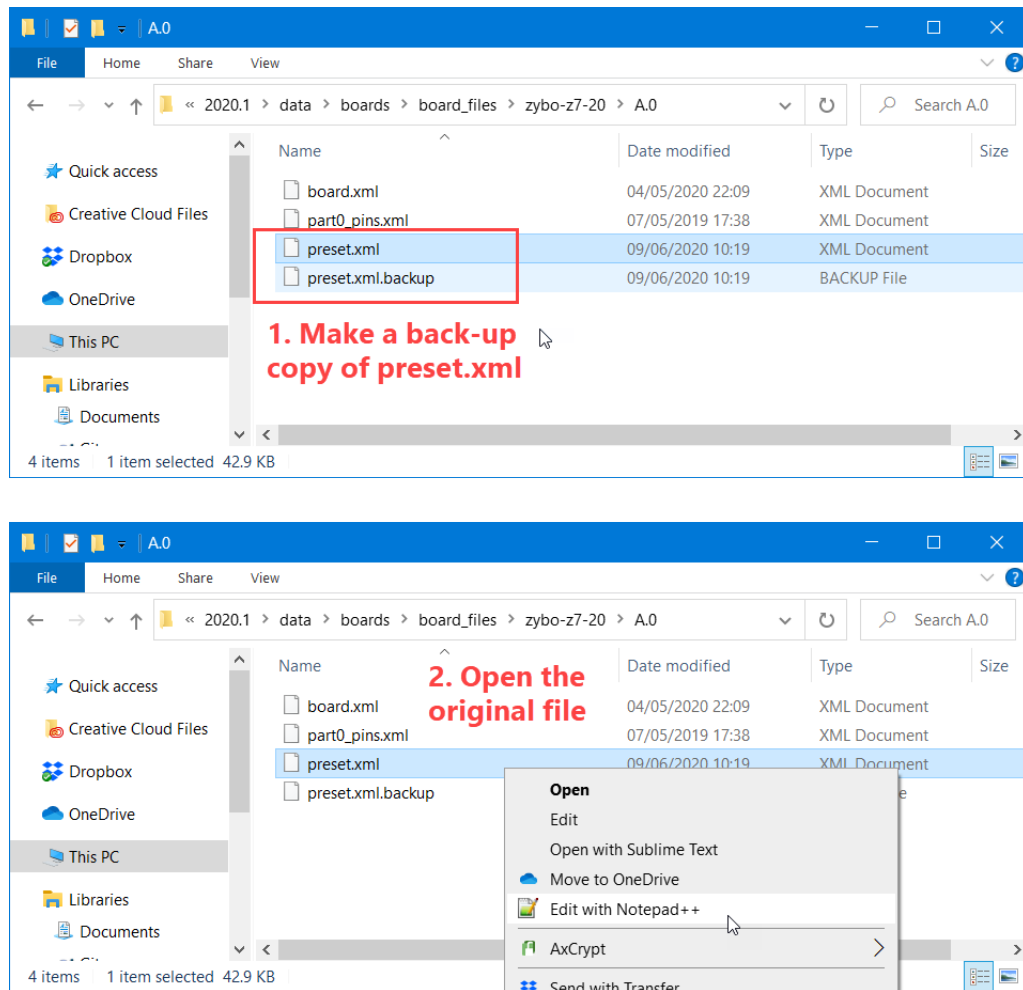
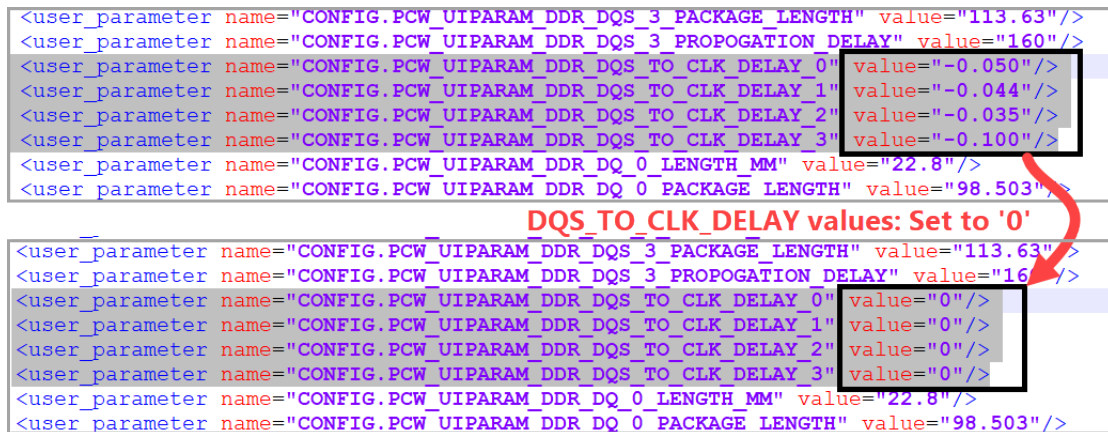


Figure 5. Make a back-up copy of preset.xml, and open the original.

The only file that must be modified is **preset.xml**. First make a back-up copy (**preset.xml.backup**) and then open the original in a suitable text file editor. (Notepad++ is used here.)



```

<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQS_3_PACKAGE_LENGTH" value="113.63"/>
<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQS_3_PROPOGATION_DELAY" value="160"/>
<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_0" value="-0.050"/>
<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_1" value="-0.044"/>
<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_2" value="-0.035"/>
<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_3" value="-0.100"/>
<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQ_0_LENGTH_MM" value="22.8"/>
<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQ_0_PACKAGE_LENGTH" value="98.503"/>

```

DQS_TO_CLK_DELAY values: Set to '0'

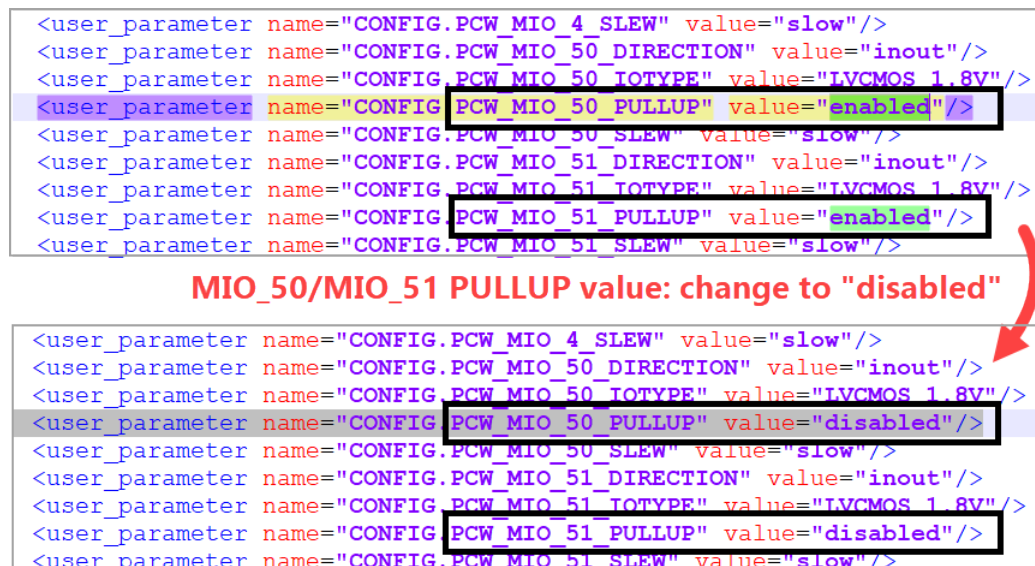
```

<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQS_3_PACKAGE_LENGTH" value="113.63"/>
<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQS_3_PROPOGATION_DELAY" value="160"/>
<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_0" value="0"/>
<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_1" value="0"/>
<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_2" value="0"/>
<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_3" value="0"/>
<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQ_0_LENGTH_MM" value="22.8"/>
<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQ_0_PACKAGE_LENGTH" value="98.503"/>

```

Figure 6. Change the DDR_DQS_TO_CLK_DELAY values to zero.

Search for the **DDR_DQS_TO_CLK_DELAY** values, and change all to zero.



```

<user_parameter name="CONFIG.PCW_MIO_4_SLEW" value="slow"/>
<user_parameter name="CONFIG.PCW_MIO_50_DIRECTION" value="inout"/>
<user_parameter name="CONFIG.PCW_MIO_50_IOTYPE" value="LVCMOS_1.8V"/>
<user_parameter name="CONFIG.PCW_MIO_50_PULLUP" value="enabled"/>
<user_parameter name="CONFIG.PCW_MIO_50_SLEW" value="slow"/>
<user_parameter name="CONFIG.PCW_MIO_51_DIRECTION" value="inout"/>
<user_parameter name="CONFIG.PCW_MIO_51_IOTYPE" value="LVCMOS_1.8V"/>
<user_parameter name="CONFIG.PCW_MIO_51_PULLUP" value="enabled"/>
<user_parameter name="CONFIG.PCW_MIO_51_SLEW" value="slow"/>

```

MIO_50/MIO_51 PULLUP value: change to "disabled"

```

<user_parameter name="CONFIG.PCW_MIO_4_SLEW" value="slow"/>
<user_parameter name="CONFIG.PCW_MIO_50_DIRECTION" value="inout"/>
<user_parameter name="CONFIG.PCW_MIO_50_IOTYPE" value="LVCMOS_1.8V"/>
<user_parameter name="CONFIG.PCW_MIO_50_PULLUP" value="disabled"/>
<user_parameter name="CONFIG.PCW_MIO_50_SLEW" value="slow"/>
<user_parameter name="CONFIG.PCW_MIO_51_DIRECTION" value="inout"/>
<user_parameter name="CONFIG.PCW_MIO_51_IOTYPE" value="LVCMOS_1.8V"/>
<user_parameter name="CONFIG.PCW_MIO_51_PULLUP" value="disabled"/>
<user_parameter name="CONFIG.PCW_MIO_51_SLEW" value="slow"/>

```

Figure 7. Change the MIO50 and MIO51 values to disabled.

Find the **PCW_MIO_50_PULLUP** and **PCW_MIO_51_PULLUP** values, and change to disabled. Save and close the file.

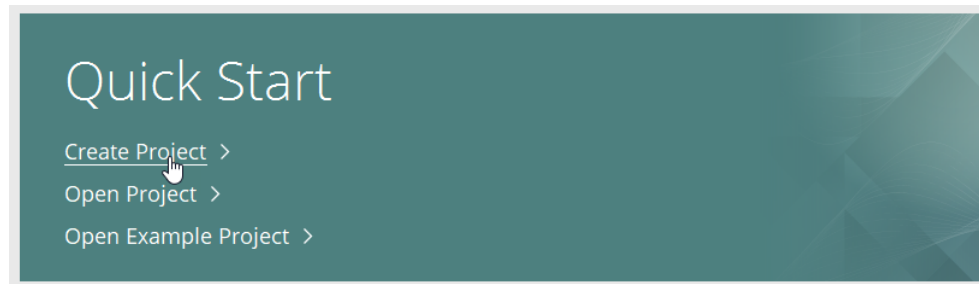


Figure 8. Launch Vivado and create a project

Next, we verify that the changes are updated in Vivado. Launch the IDE for the version where the changes have been made, and select Create Project

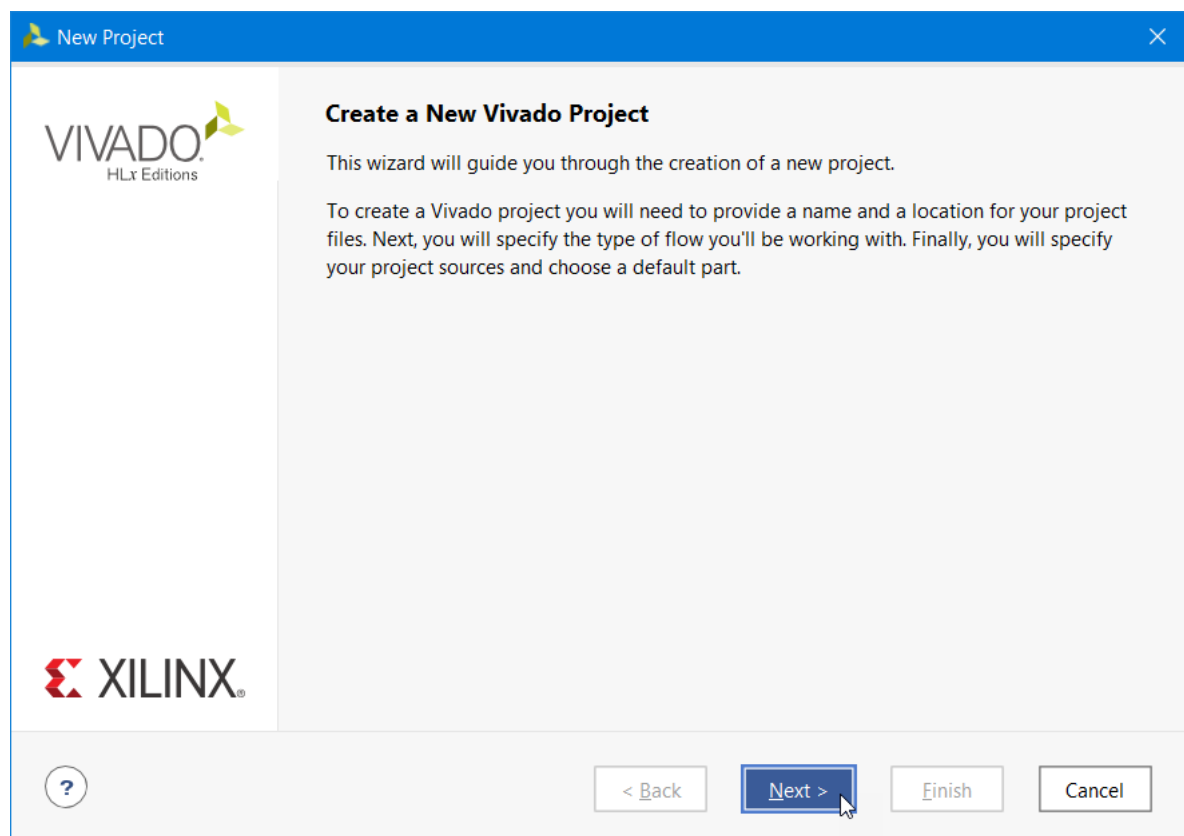
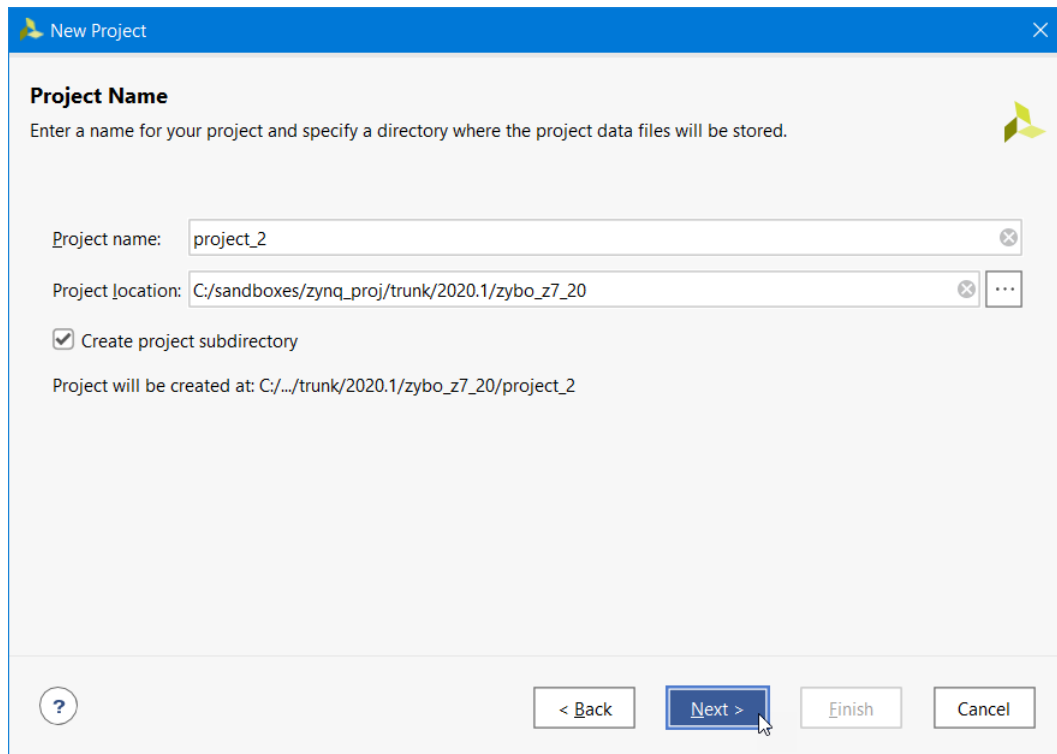


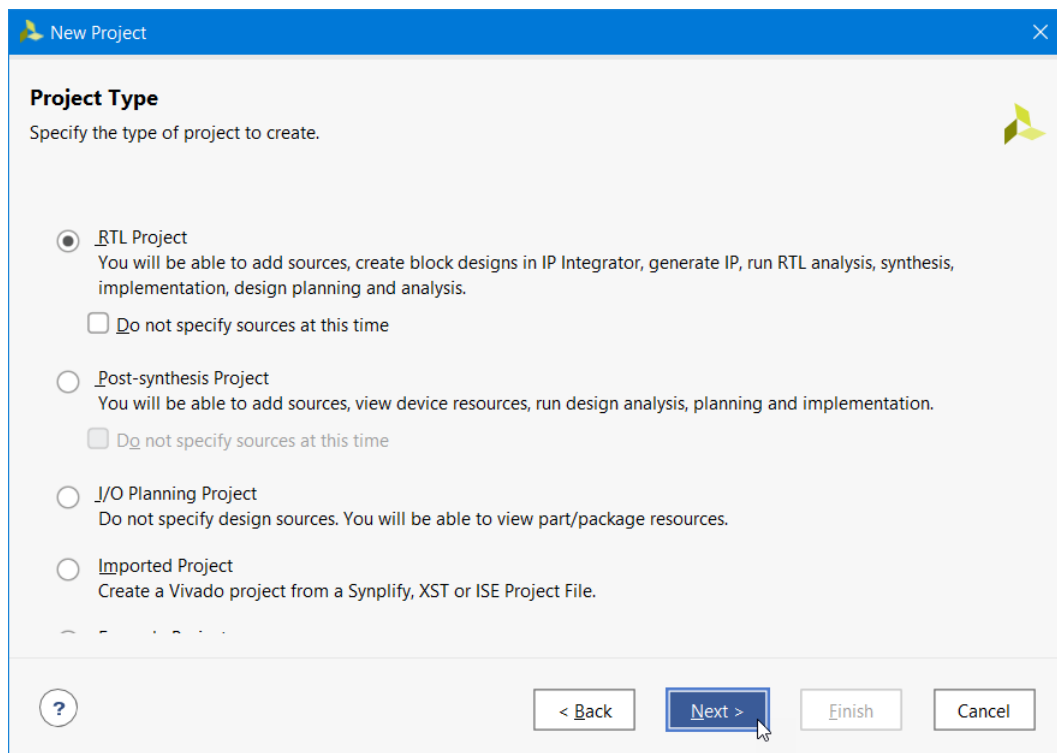
Figure 9. Click Next to continue.



The 'New Project' dialog box is shown with the 'Project Name' tab selected. The title bar reads 'New Project'. Below the title bar, the text 'Project Name' is followed by the instruction 'Enter a name for your project and specify a directory where the project data files will be stored.' There are two input fields: 'Project name:' with the text 'project_2' and 'Project location:' with the text 'C:/sandboxes/zynq_proj/trunk/2020.1/zybo_z7_20'. A checkbox labeled 'Create project subdirectory' is checked. Below this, it says 'Project will be created at: C:/.../trunk/2020.1/zybo_z7_20/project_2'. At the bottom, there are four buttons: a help button (question mark in a circle), '< Back', 'Next >' (highlighted with a mouse cursor), 'Finish', and 'Cancel'.

Figure 10. Select the project name and location

Select the desired project location and choose any suitable project name.



The 'New Project' dialog box is shown with the 'Project Type' tab selected. The title bar reads 'New Project'. Below the title bar, the text 'Project Type' is followed by the instruction 'Specify the type of project to create.' There are four radio button options: 'RTL Project' (selected), 'Post-synthesis Project', 'I/O Planning Project', and 'Imported Project'. Each option has a description. Below the 'RTL Project' option, there is a checkbox 'Do not specify sources at this time'. At the bottom, there are four buttons: a help button (question mark in a circle), '< Back', 'Next >' (highlighted with a mouse cursor), 'Finish', and 'Cancel'.

Figure 11. Select RTL Project

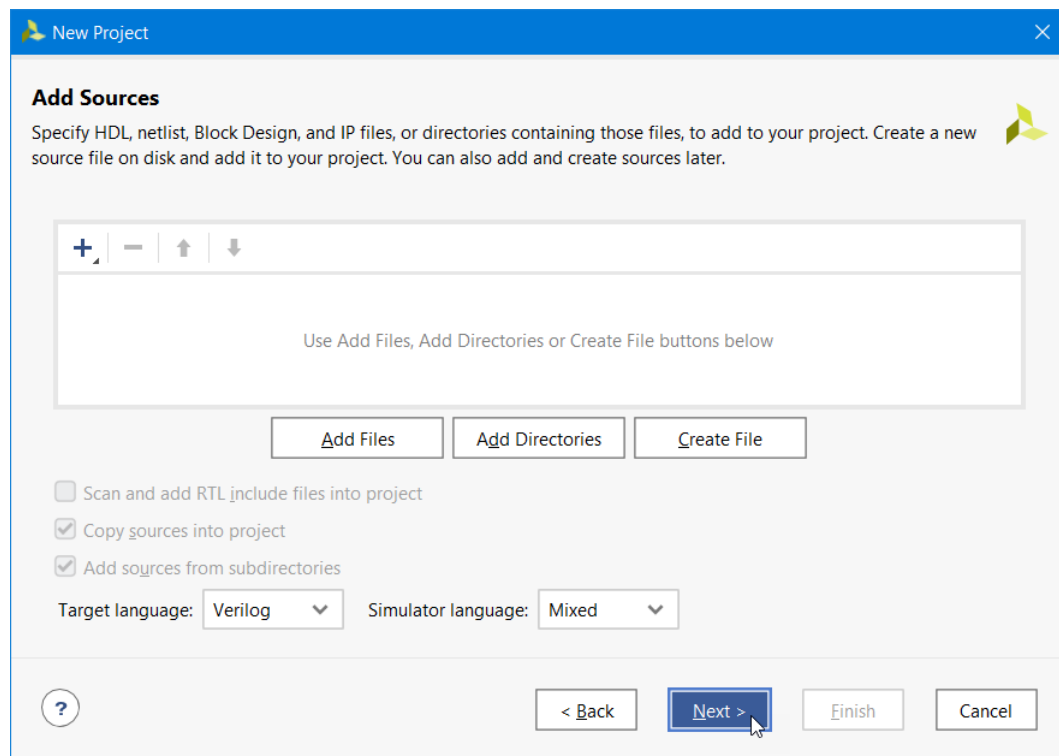


Figure 12. Click Next (as there are no files to be added).

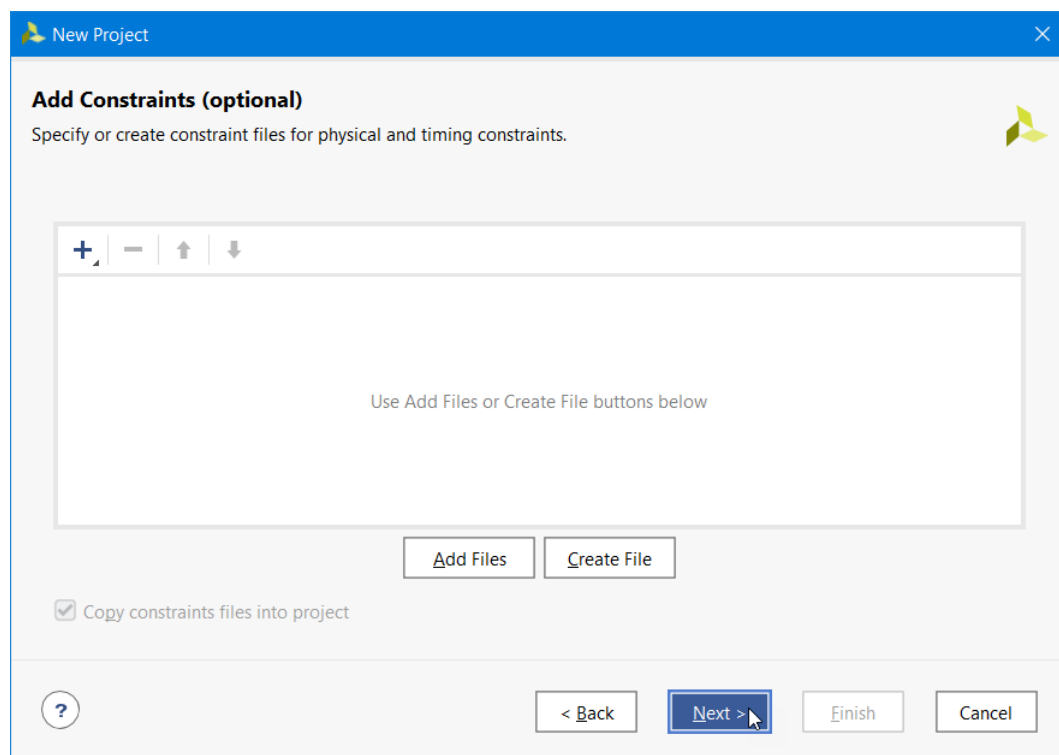


Figure 13. Click Next (No constraints are needed.)

New Project

Default Part
Choose a default Xilinx part or board for your project.

1. Select Boards

Parts | **Boards**


Reset All Filters

Vendor: **digilentinc.com** Name: All Remaining Board Rev: Latest

Install/Update Boards

Search: Q*

2. Set Vendor: digilentinc.com

Display Name	Preview	Vendor	File Ve...	Part	I/O Pin Count	Board Rev
Zedboard		digilentinc.com	1.0	xc7z020clg484-1	484	D.3
Zybo Z7-10		digilentinc.com	1.0	xc7z010clg400-1	400	B.2
Zybo Z7-20		digilentinc.com	1.0	xc7z020clg400-1	400	B.2
Zybo		digilentinc.com	2.0	xc7z010clg400-1	400	B.4

3. Select Zybo Z7-20

< Back Next > Finish Cancel

Next Page

Figure 14. Select the Zybo-Z7-20 (or Zybo-Z7-10) on the Default Parts page.

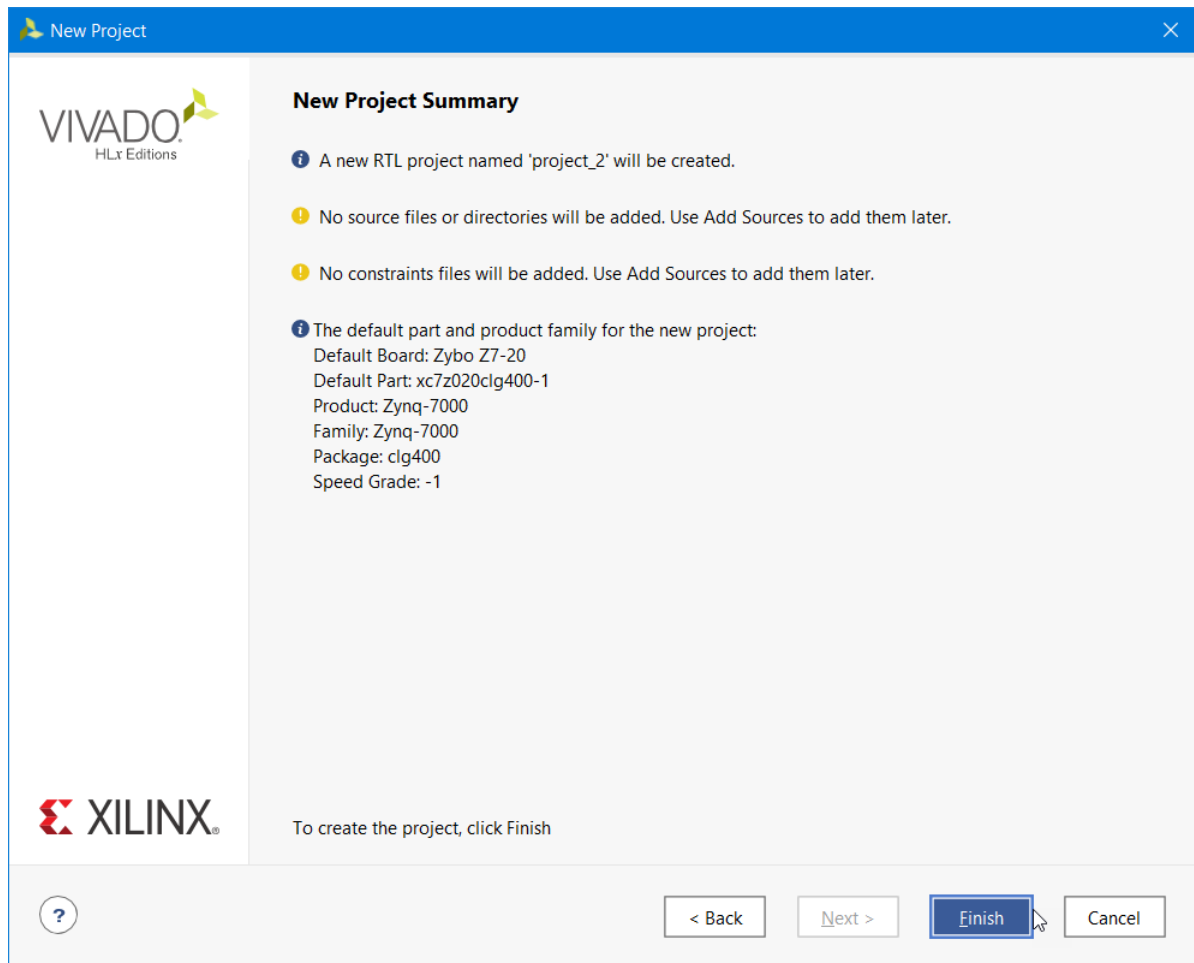


Figure 15. Click Finish to create the project.

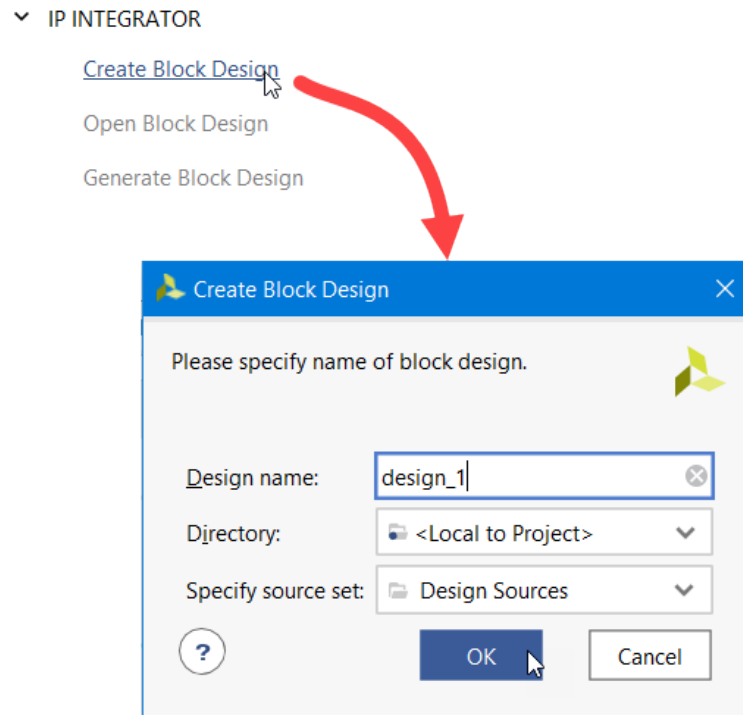


Figure 16. In Vivado, select Create Block Design in the IP Integrator menu

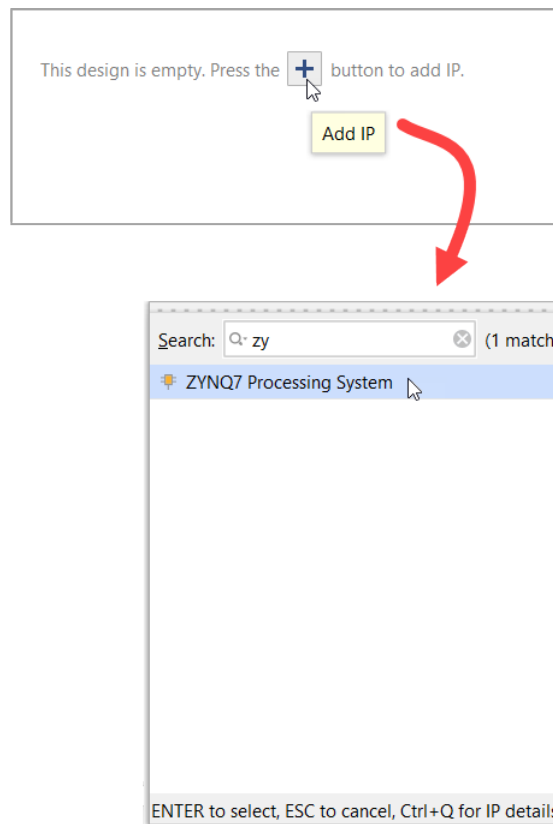


Figure 17. Add the ZYNQ7 Processing System to the canvas

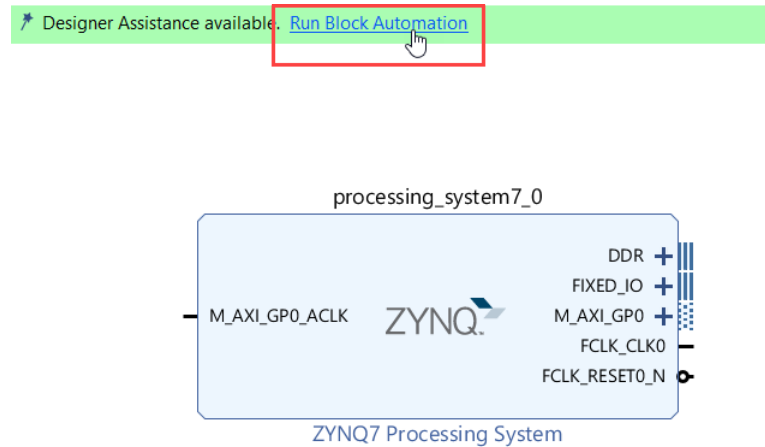


Figure 18. Select Run Block Automation

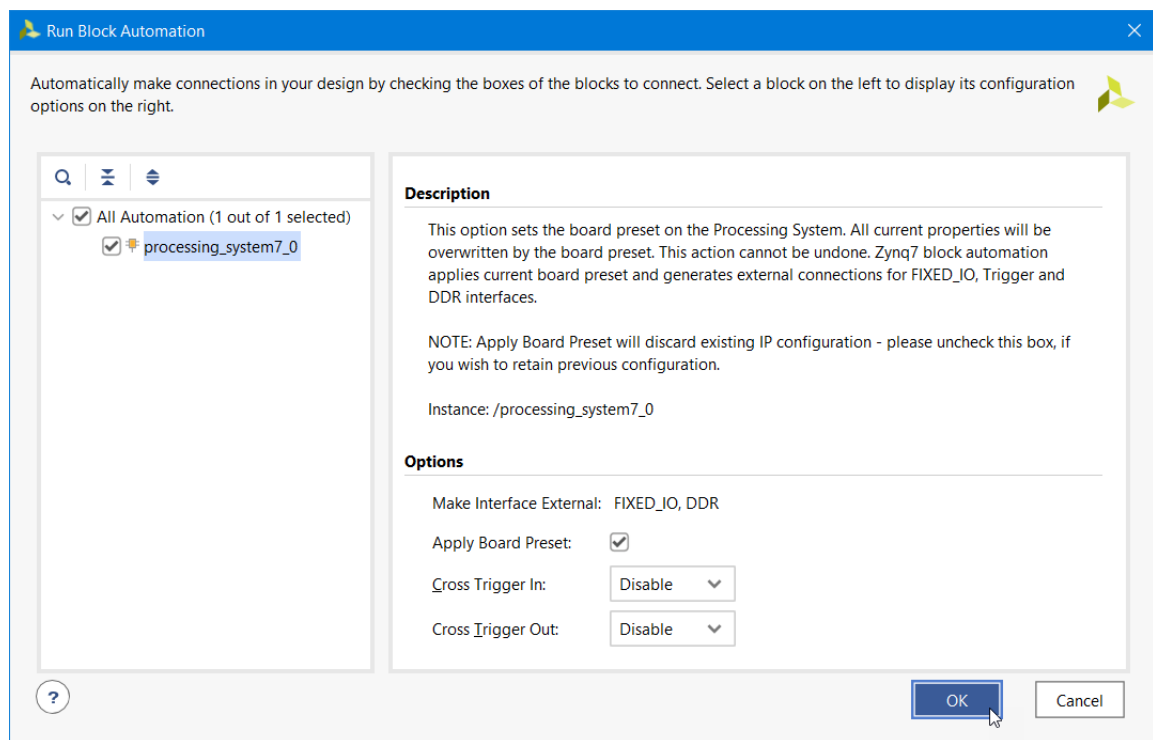


Figure 19. Ensure that the settings are as shown, and select Run Block Automation

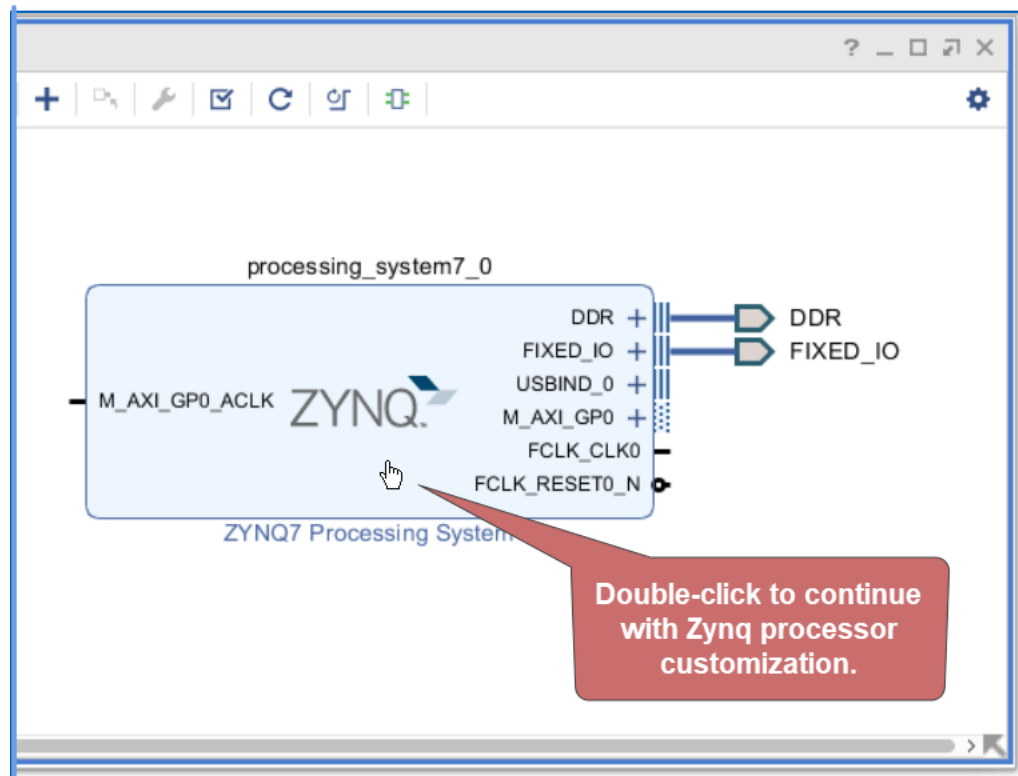


Figure 20. Double-click on the Zynq-7000 module to open the configuration menu

Page Navigator

- Zynq Block Design
- PS-PL Configuration
- Peripheral I/O Pins
- MIO Configuration**
- Clock Configuration
- DDR Configuration
- SMC Timing Calculation
- Interrupts

MIO Configuration

Bank 0 I/O Voltage: LVCMOS 3.3V Bank 1 I/O Voltage: LVCMOS 1.8V

Search:

Peripheral	IO	Signal	IO Type	Speed	Pullup	Direct...	Polarity
CAN 1							
GPIO							
GPIO MIO	MIO						
GPIO	MIO 0	gpio[0]	LVCMOS 3.3V	slo	enabled		inout
GPIO	MIO 7	gpio[7]	LVCMOS 3.3V	slo	disabled		out
GPIO	MIO 9	gpio[9]	LVCMOS 3.3V	slo	enabled		inout
GPIO	MIO 10	gpio[10]	LVCMOS 3.3V	slo	enabled		inout
GPIO	MIO 11	gpio[11]	LVCMOS 3.3V	slo	enabled		inout
GPIO	MIO 12	gpio[12]	LVCMOS 3.3V	slo	enabled		inout
GPIO	MIO 13	gpio[13]	LVCMOS 3.3V	slo	enabled		inout
GPIO	MIO 14	gpio[14]	LVCMOS 3.3V	slo	enabled		inout
GPIO	MIO 15	gpio[15]	LVCMOS 3.3V	slo	enabled		inout
GPIO	MIO 50	gpio[50]	LVCMOS 1.8V	slo	disabled		inout
GPIO	MIO 51	gpio[51]	LVCMOS 1.8V	slo	disabled		inout
EMIO GPIO (Wi...)							

Check that pullups are disabled for MIO50/51

Figure 21. Under 'MIO Configuration', expand the GPIO settings and check that the MIO50/MIO51 pull-ups are disabled.

Page Navigator

- Zynq Block Design
- PS-PL Configuration
- Peripheral I/O Pins
- MIO Configuration
- Clock Configuration
- DDR Configuration**
- SMC Timing Calculation
- Interrupts

DDR Configuration

☒ Enable DDR

Search:

Name	Select	Description
> DDR Controller Configuration		
> Memory Part Configuration		
> Training/Board Details	User Input	
> DRAM Training		
> DQS to Clock Delay (ns)		
DQS0	0	DQS to Clock delay [0] (ns). The DQS path delay subtracted
DQS1	0	DQS to Clock delay [1] (ns). The DQS path delay subtracted
DQS2	0	DQS to Clock delay [2] (ns). The DQS path delay subtracted
DQS3	0	DQS to Clock delay [3] (ns). The DQS path delay subtracted
> Board Delay (ns)		
> Enable Advanced options	<input type="checkbox"/>	Enable Advanced DDR QoS settings

Check that DQS to Clock Delays are set to '0'

Figure 22. Under 'DDR Configuration -> Training/Board Details', check that the DQS to Clock Delay settings are zero. Click OK when finished.

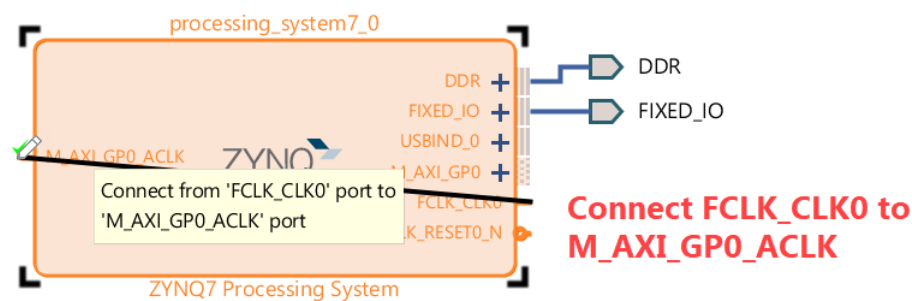


Figure 23. Back at the top-level, connect FCLK_CLK0 to M_AXI_GP0_ACLK.

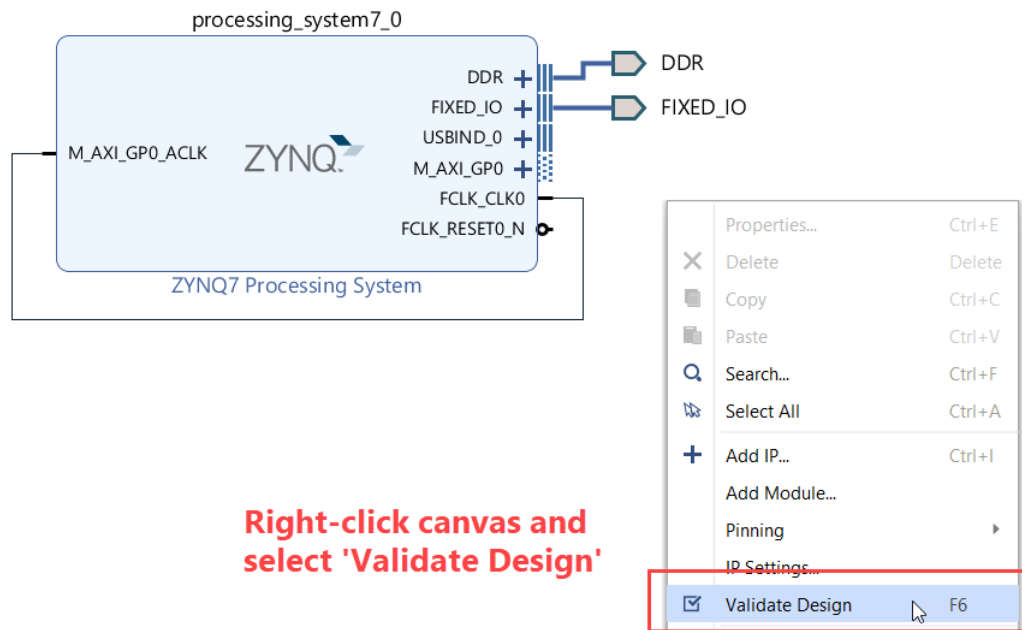


Figure 24. Right-click on the canvas and select 'Validate Design'

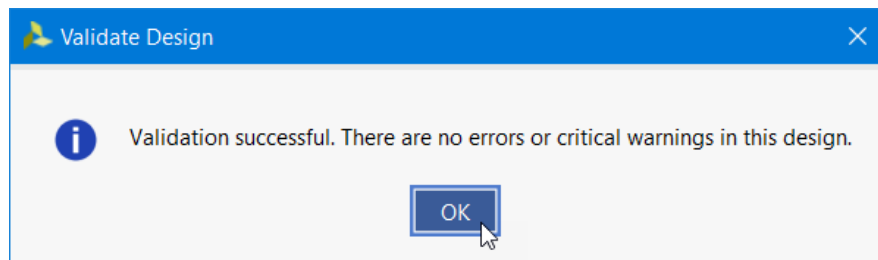


Figure 25. The Validation Success dialog should appear.