Zybo-Z7-20: Prepare Board Files

A companion guide to the text book:

A Practical Introduction to the Xilinx Zynq-7000 Adaptive SoC

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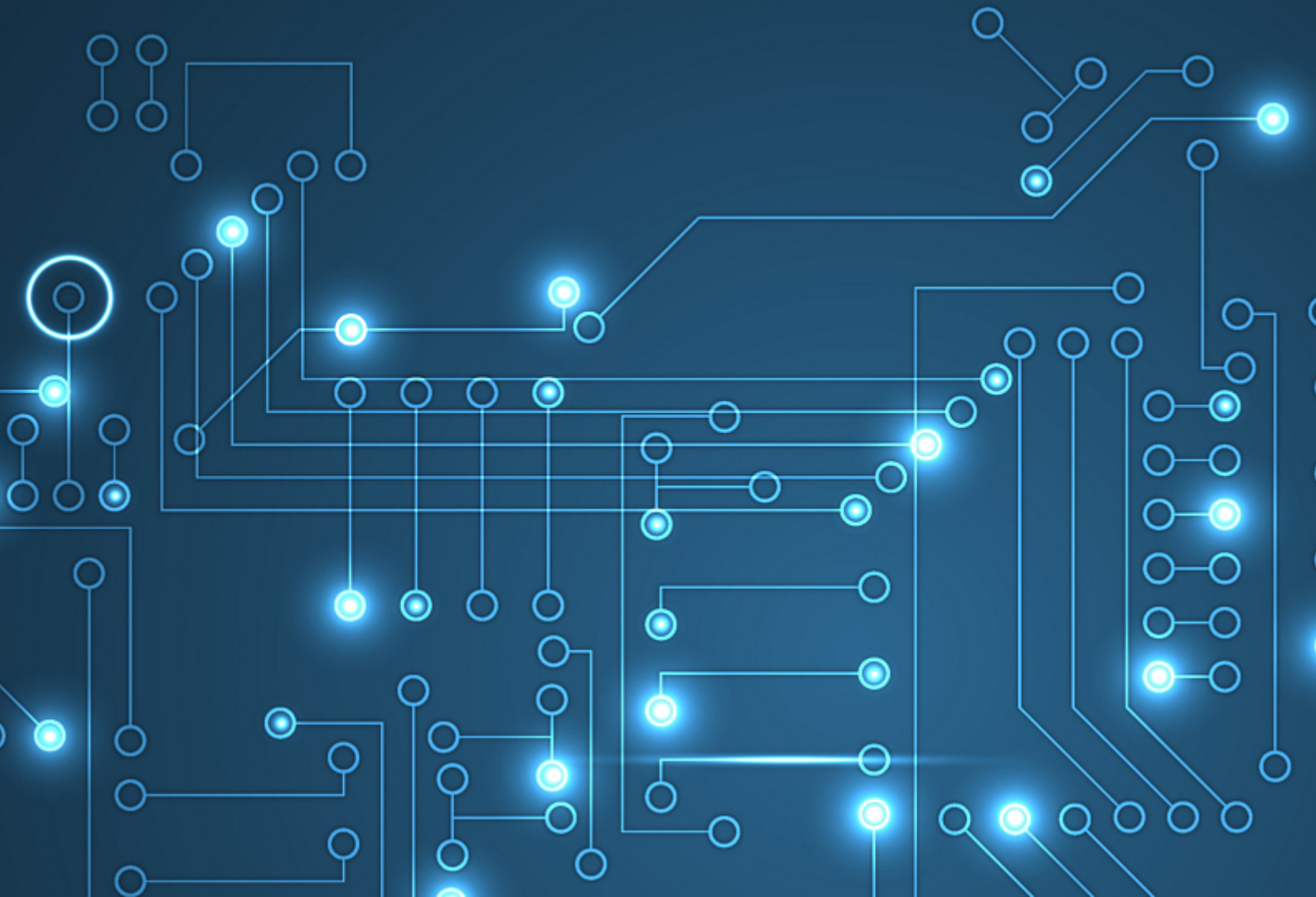
Version: 1.0

Date: 29/8/21



Revision History

Version	Date	Comment
1.0	29/8/21	First Version

Table 18.1. Revision History

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1 Introduction

This step-by-step guide provides an optional approach to preparing the Vivado board files for the Zybo-Z7-20 platform. (The steps are also applicable to the Zybo-Z7-10). The main aim is to update the *preset.xml* file with the following changes:

1. The DDR DQS-to-CLK Delay settings are set to zero. This is to suppress a critical warning that occurs due to the values initially being set to negative values. See Zybo-Z7-20 Hardware Errata on the Digilent Website for more information.
2. The internal pull-ups for MIO50 and MIO51 (BTN4 and BTN5 respectively on the board) are changed from enabled to disabled.

These settings are proven to work with the projects in the related text book, but it is up to the reader if they want to implement them.

2 Procedure

The process starts with the retrieval of the Zybo-Z7-20 board files from the Digilent GitHub repository (https://github.com/Digilent/vivado-boards).

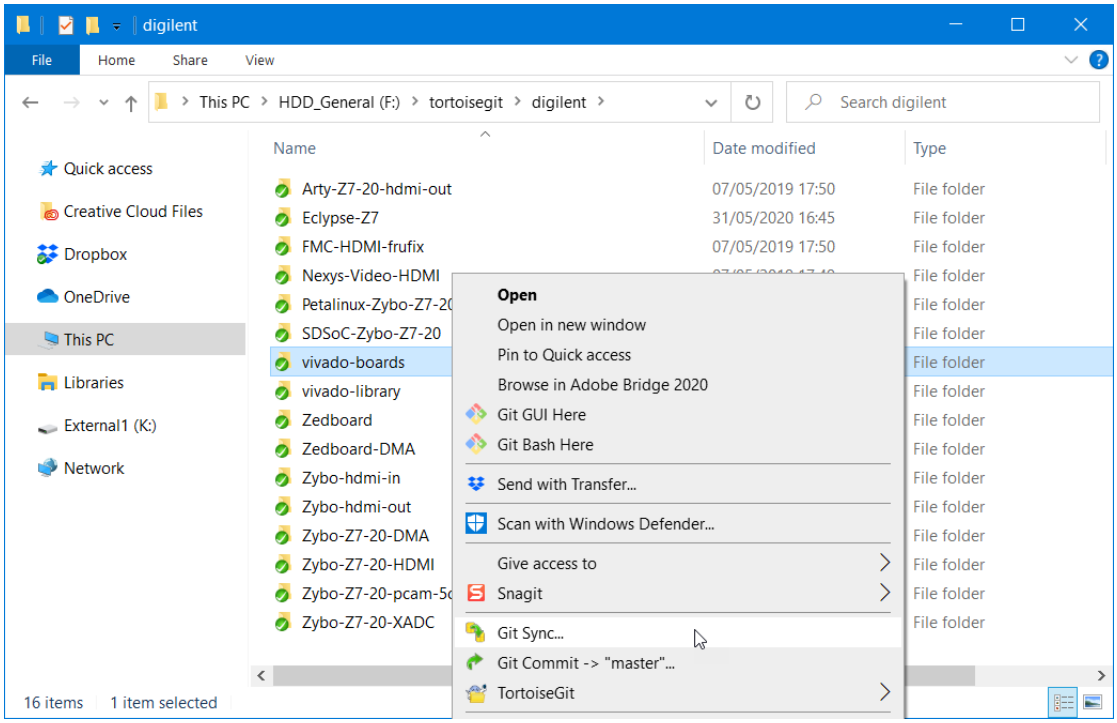

Figure 1. Retrieve the Digilent board files

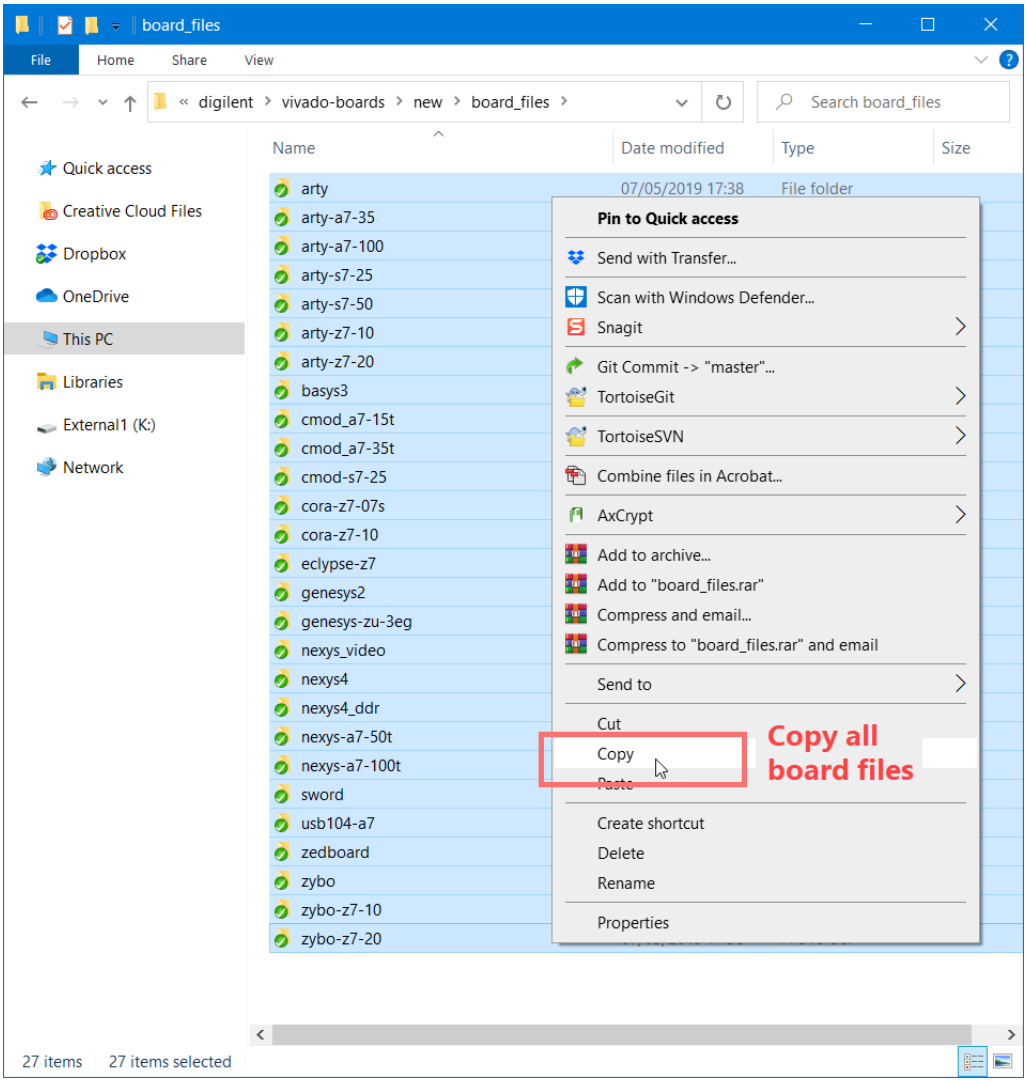

Figure 2. Copy the files

When the files are available, go to: *[Git] -> Digilent -> vivado-boards -> new -> board_files*. Then, copy all board files.

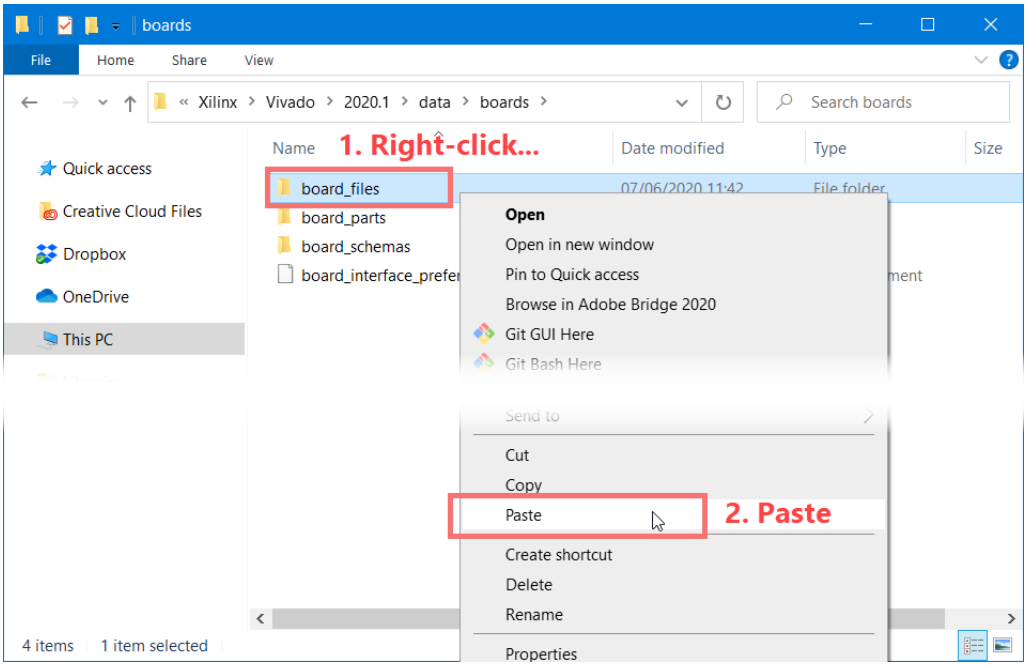

Figure 3. Paste the copied files into the correct location in the Vivado installation

In the Vivado installation directory (usually *C:\Xilinx\Vivado*), paste the copied files to the *board_files* directory: For example, for Vivado 2020.1, the location is:

- C:\Xilinx\Vivado**2020.1**\data\boards\board_files

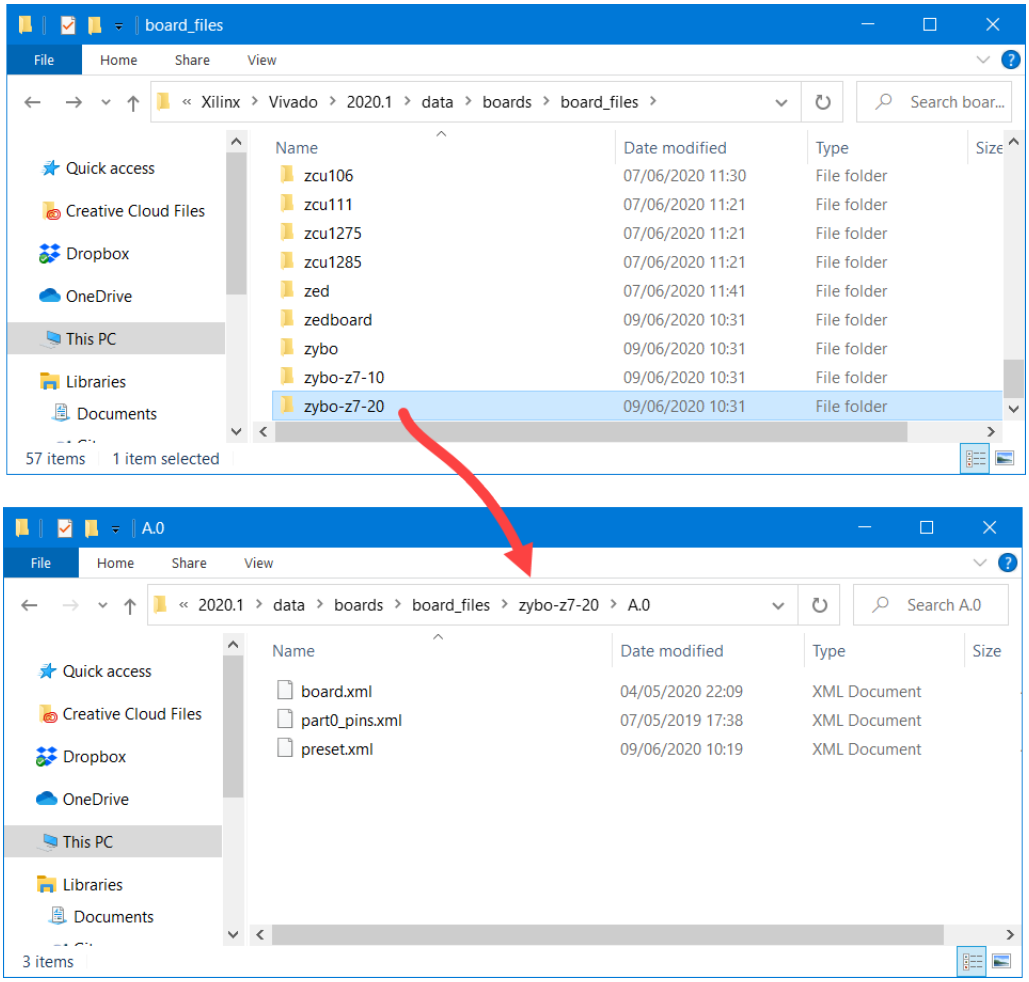

Figure 4. Navigate to the Zybo-Z7-20 (or Zybo-Z7-10) board files directory

In the *board_files* directory, navigate to *zybo-z7-20 -> A0* (assuming that A0 is the most up-to-date version). Three files should be present:

- boards.xml
- part0_pins.xml
- preset.xml

(If using the Zybo-Z7-10, navigate to that directory instead. Files with the same names should be present.)

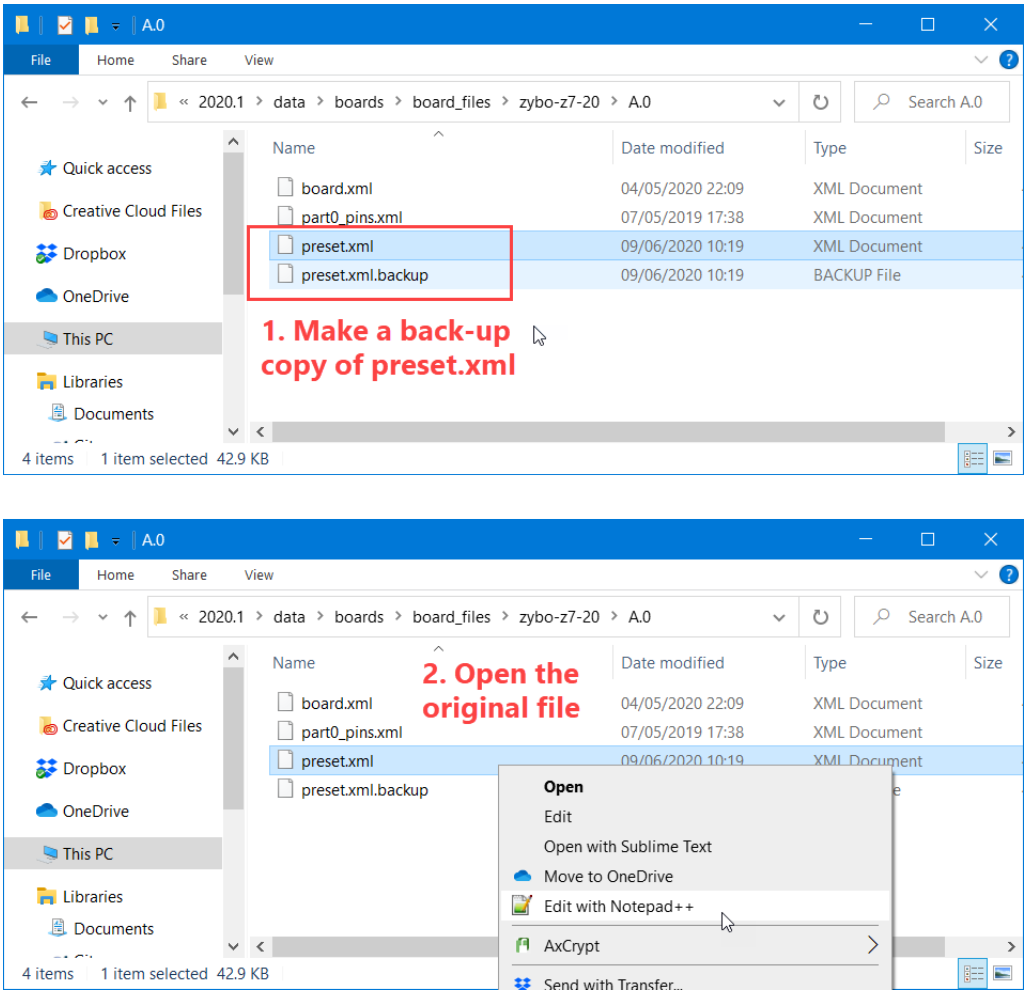

Figure 5. Make a back-up copy of preset.xml, and open the original.

The only file that must be modified is **preset.xml**. First make a back-up copy (**preset.xml.backup**) and then open the original in a suitable text file editor. (Notepad++ is used here.)

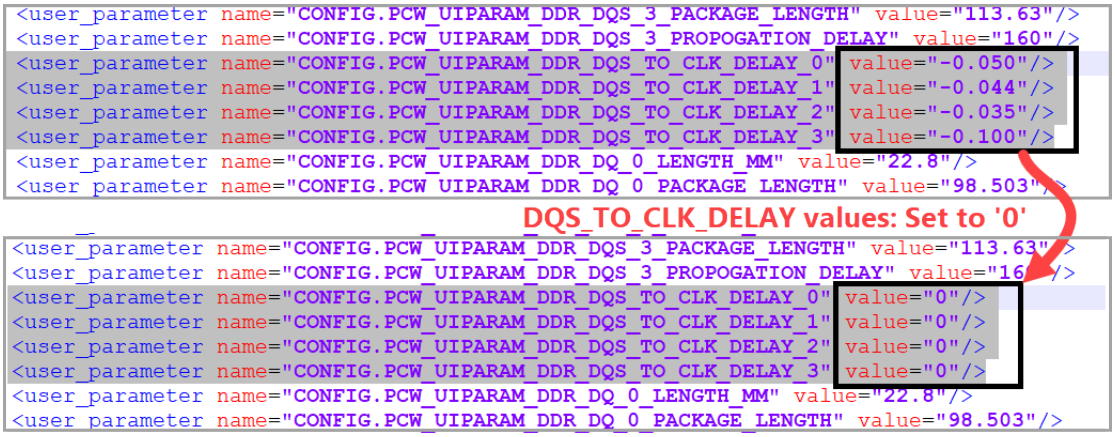

Figure 6. Change the DDR_DQS_TO_CLK_DELAY values to zero.

Search for the **DDR_DQS_TO_CLK_DELAY** values, and change all to zero.

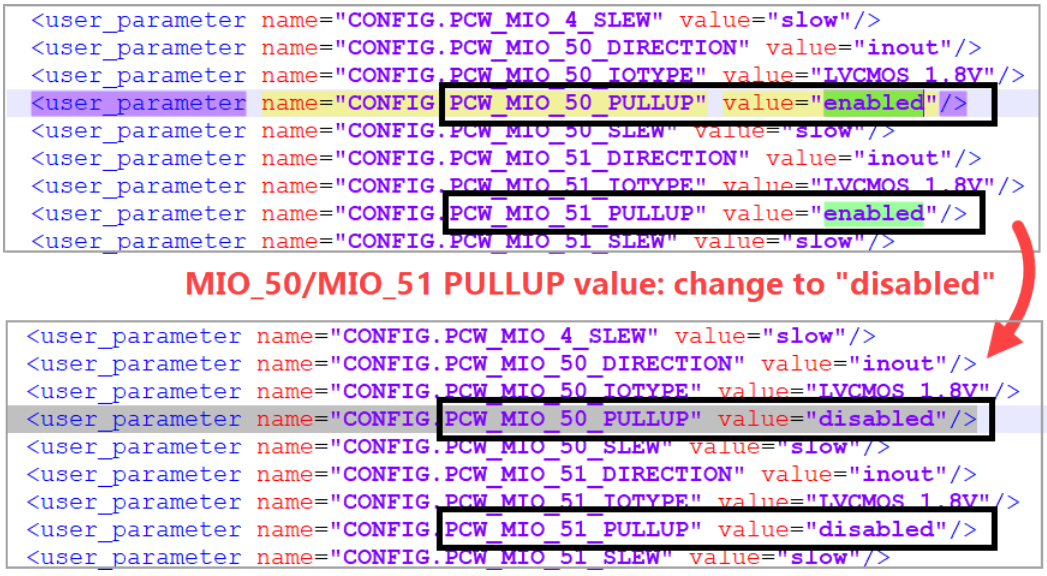

Figure 7. Change the MIO50 and MIO51 values to disabled.

Find the **PCW_MIO_50_PULLUP** and **PCW_MIO_51_PULLUP** values, and change to disabled. Save and close the file.

Figure 8. Launch Vivado and create a project

Next, we verify that the changes are updated in Vivado. Launch the IDE for the version where the changes have been made, and select Create Project

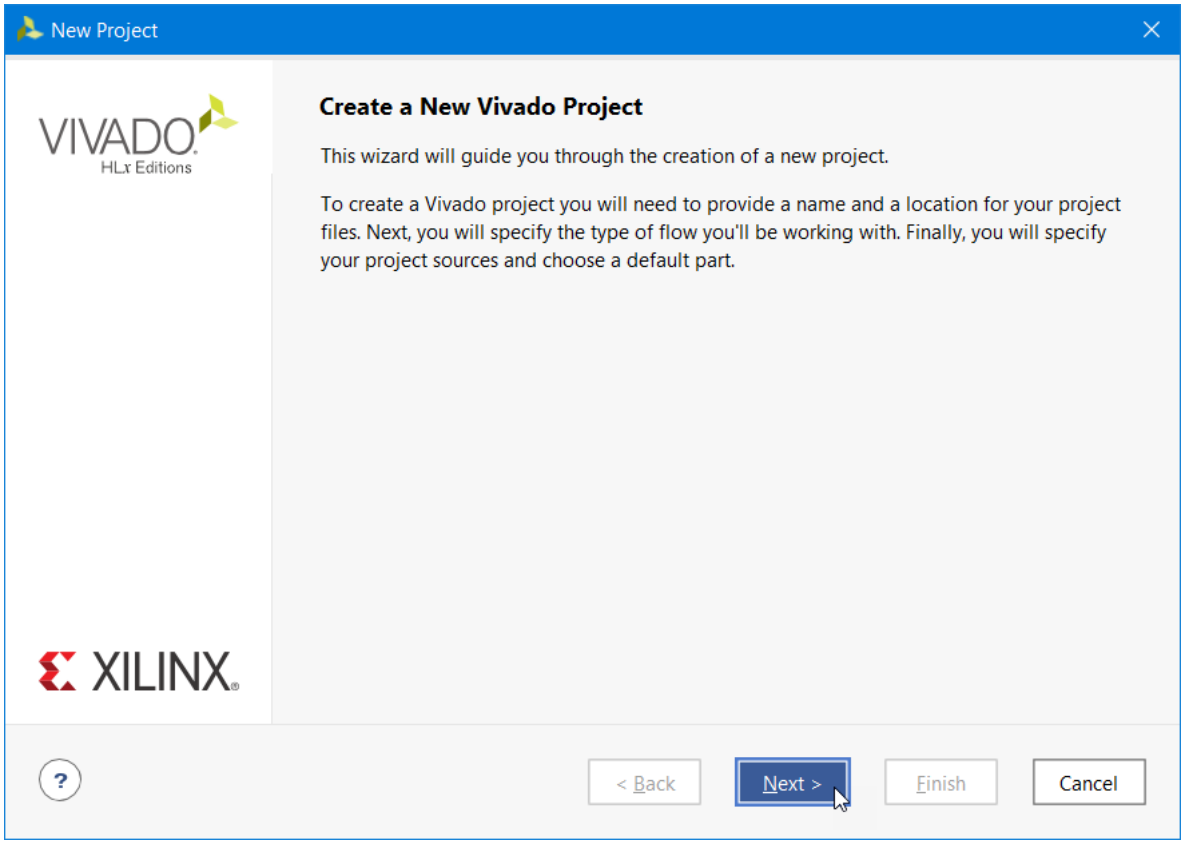

Figure 9. Click Next to continue.

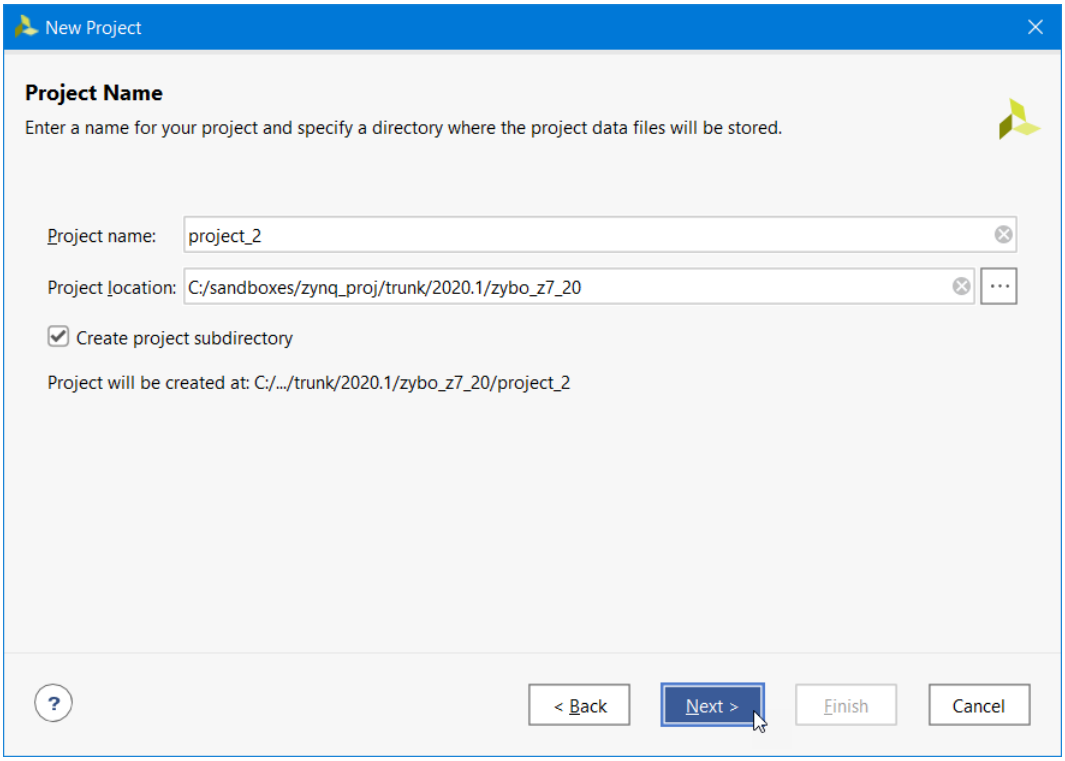

Figure 10. Select the project name and location

Select the desired project location and choose any suitable project name.

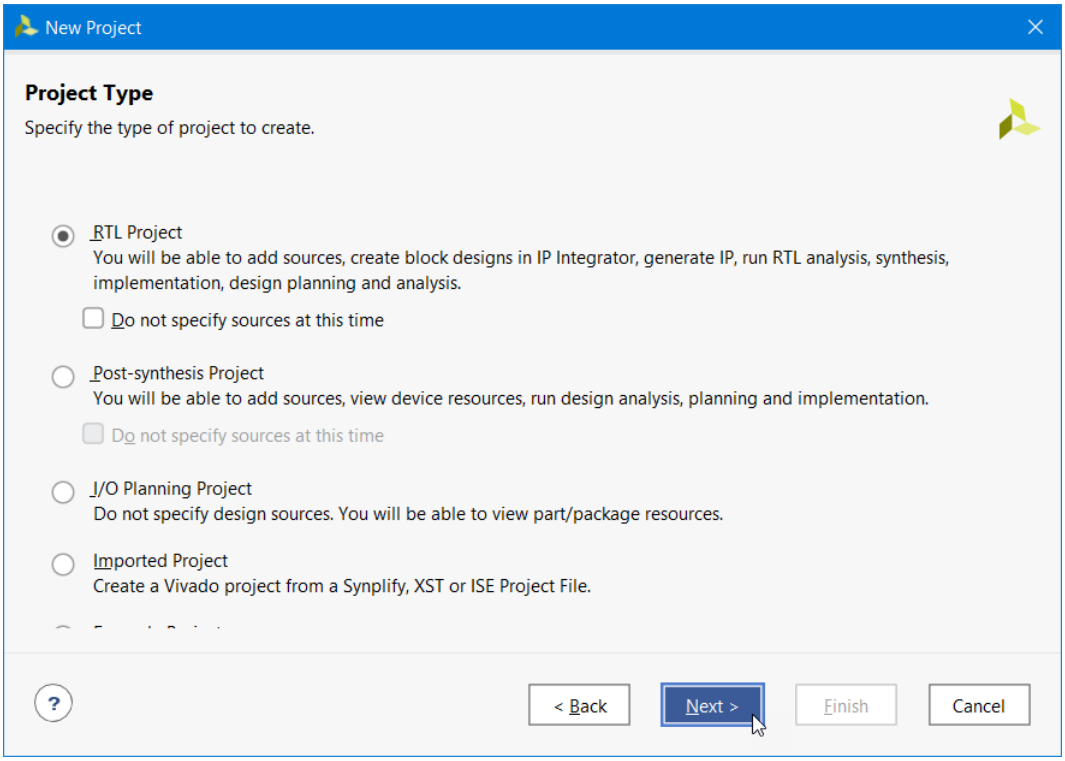

Figure 11. Select RTL Project

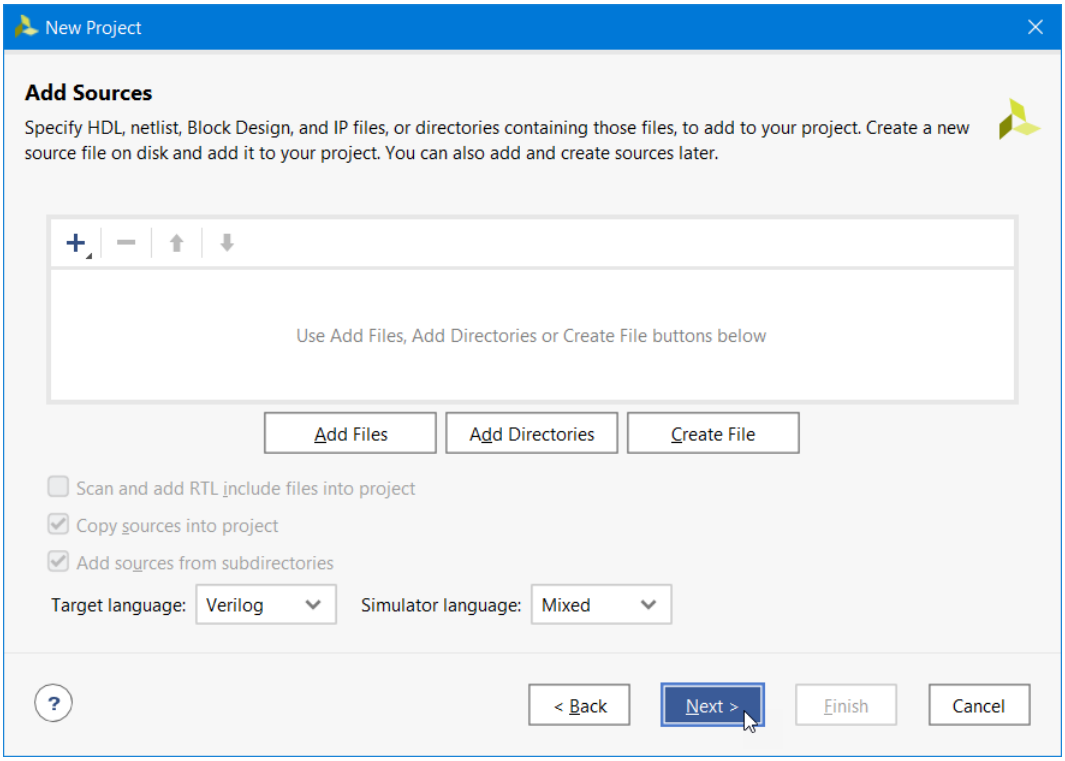

Figure 12. Click Next (as there are no files to be added).

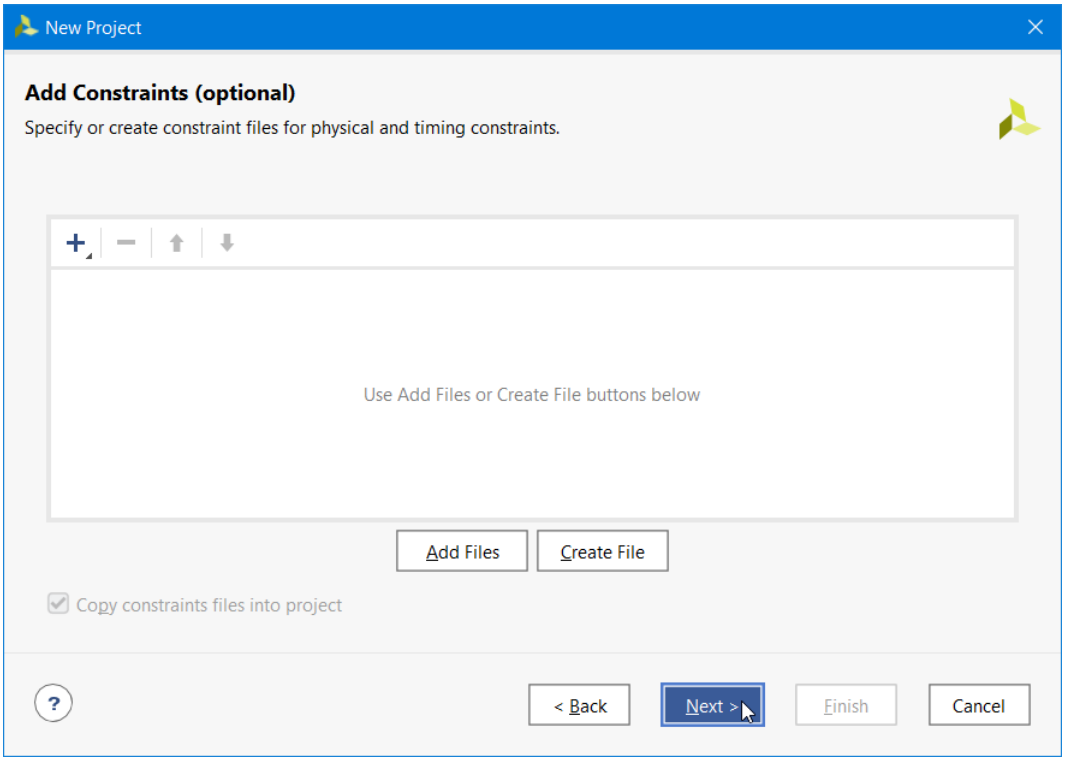

Figure 13. Click Next (No constraints are needed.)

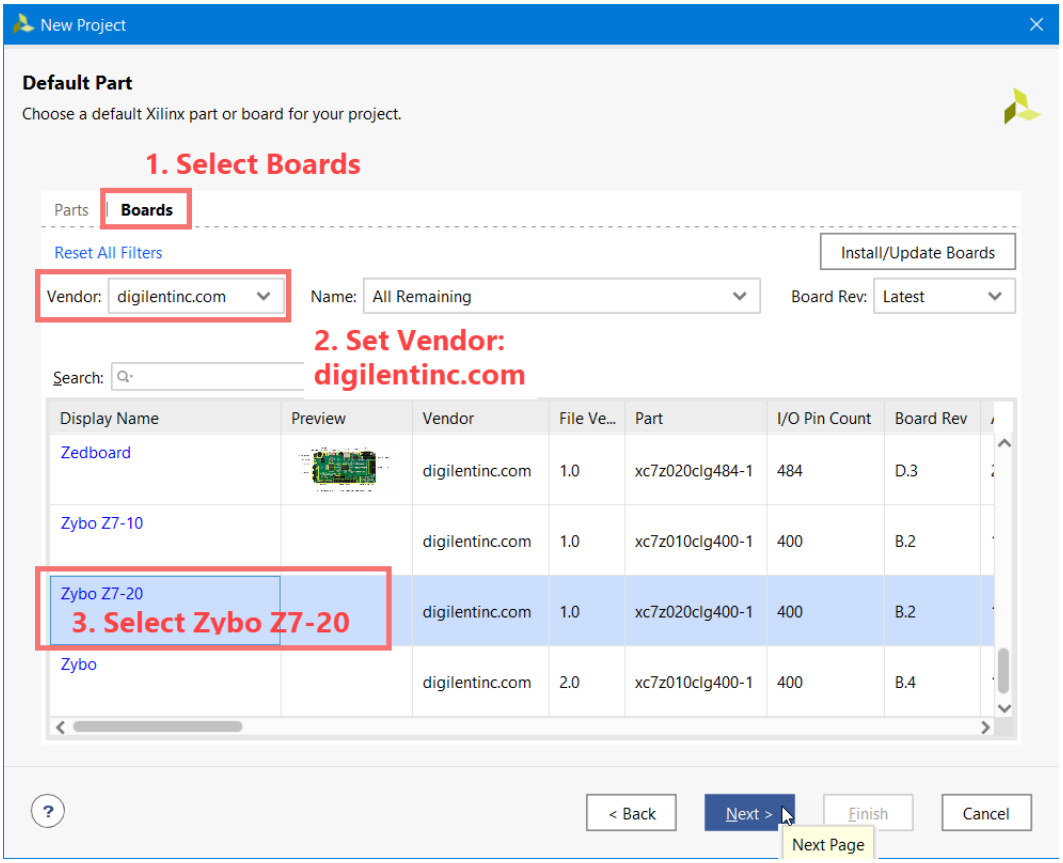

Figure 14. Select the Zybo-Z7-20 (or Zybo-Z7-10) on the Default Parts page.

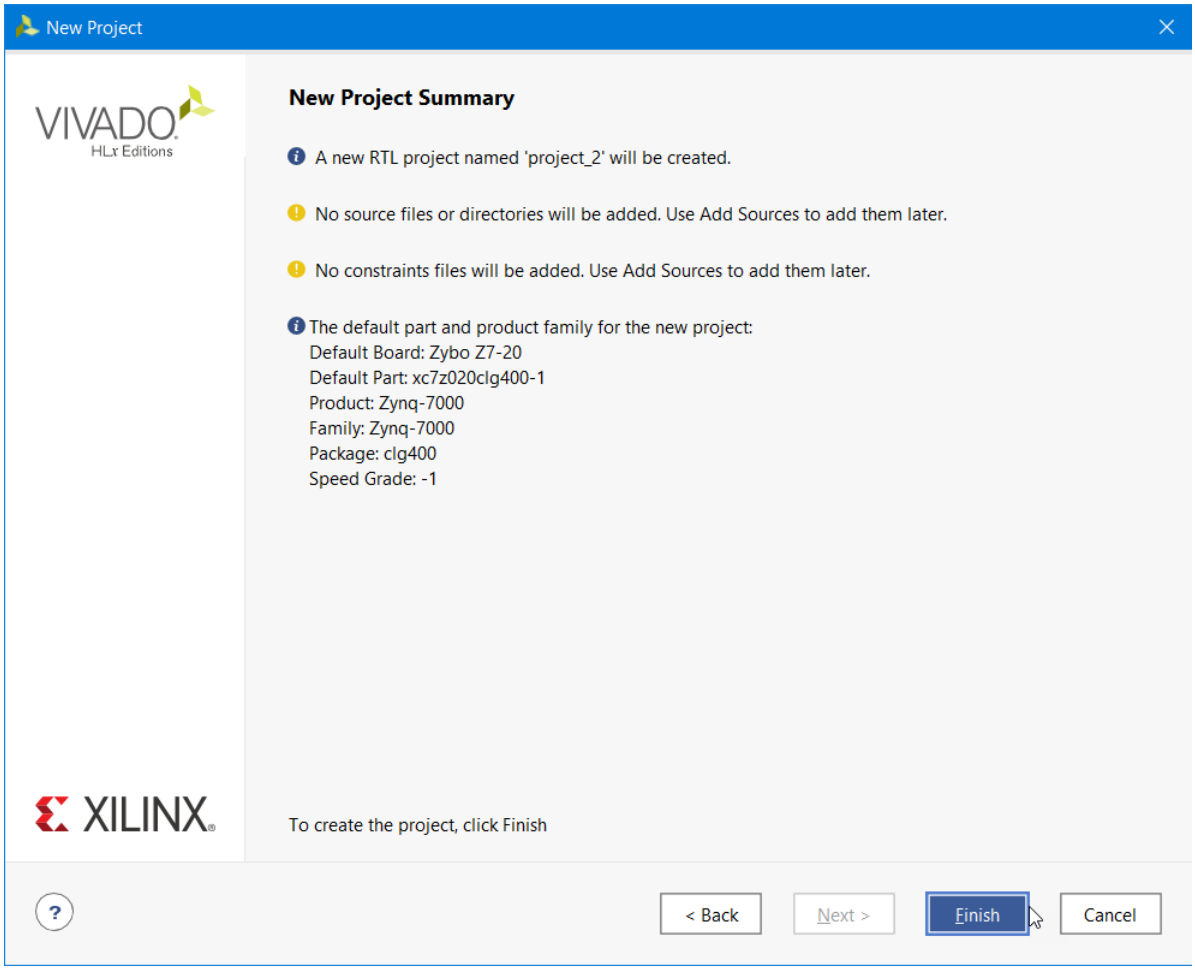

Figure 15. Click Finish to create the project.

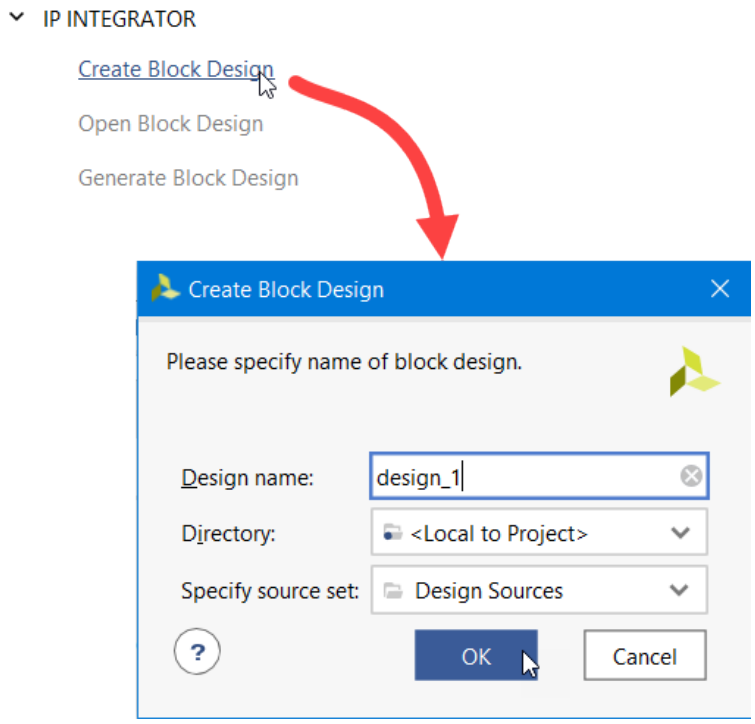

Figure 16. In Vivado, select Create Block Design in the IP Integrator menu

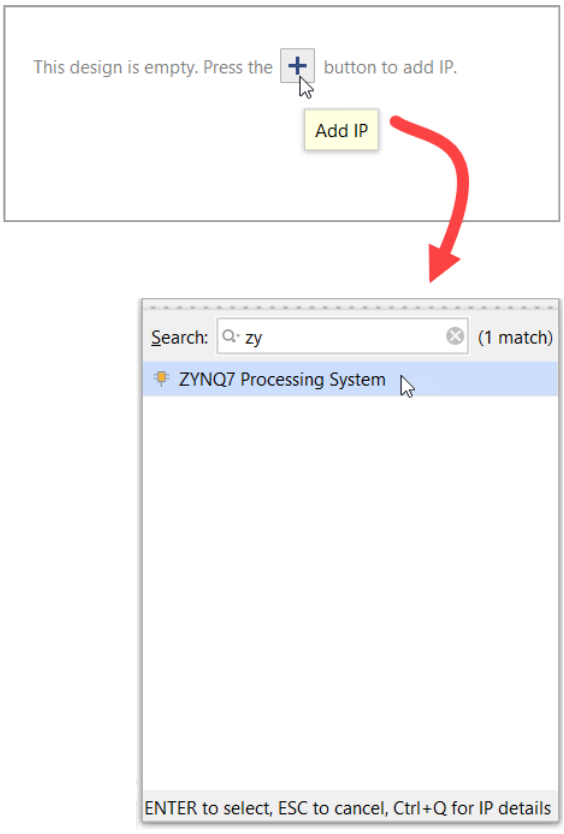

Figure 17. Add the ZYNQ7 Processing System to the canvas

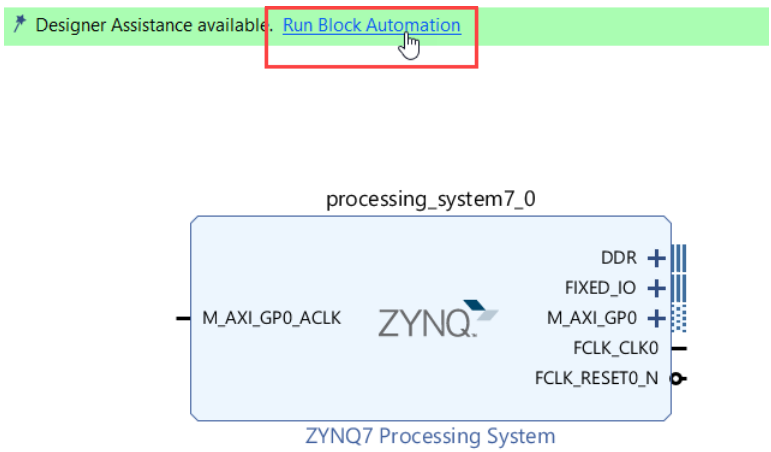

Figure 18. Select Run Block Automation

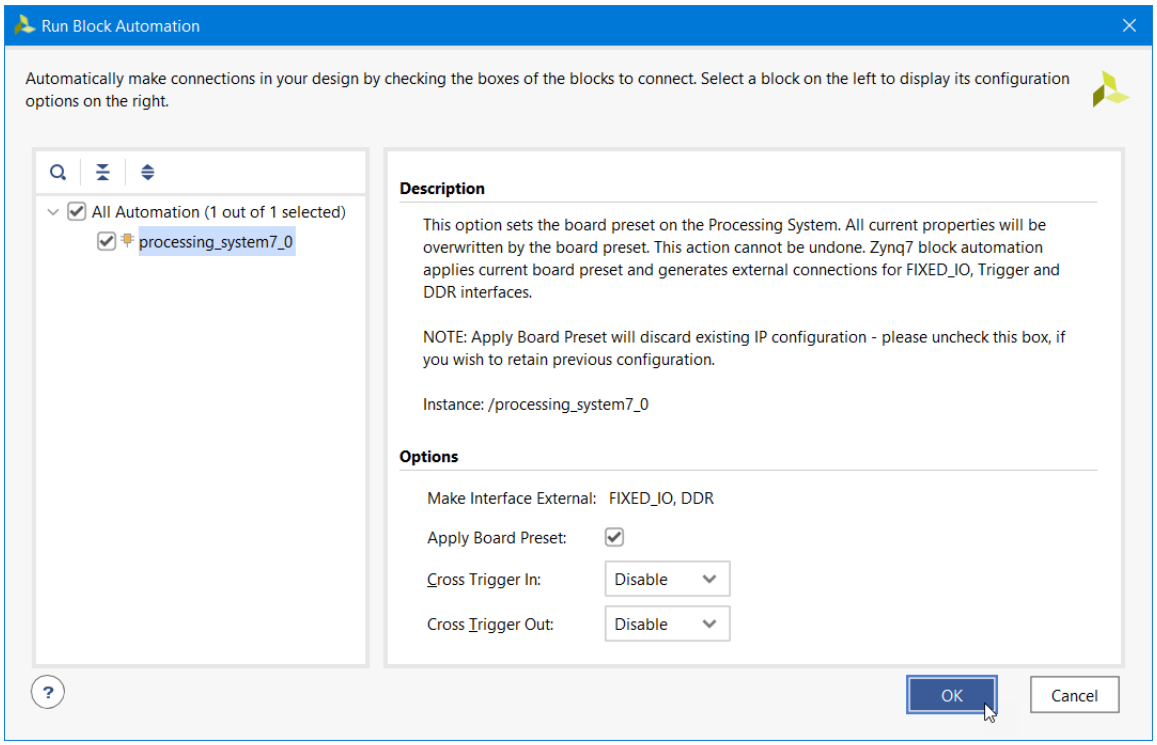

Figure 19. Ensure that the settings are as shown, and select Run Block Automation

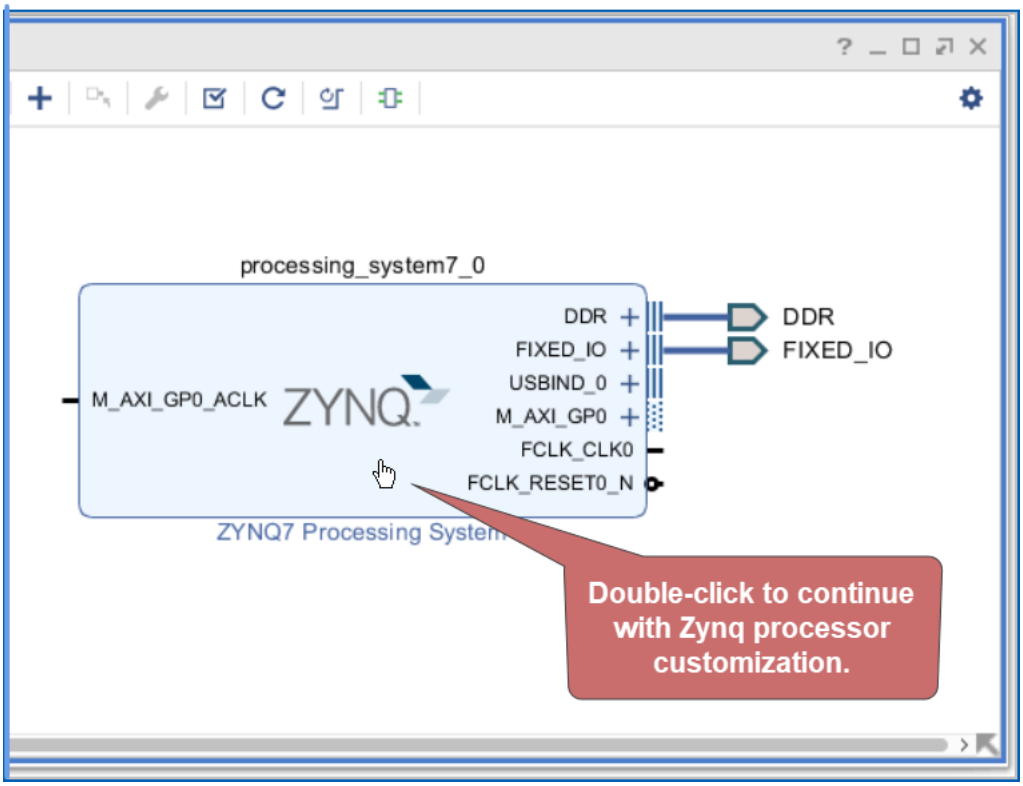

Figure 20. Double-click on the Zynq-7000 module to open the configuration menu

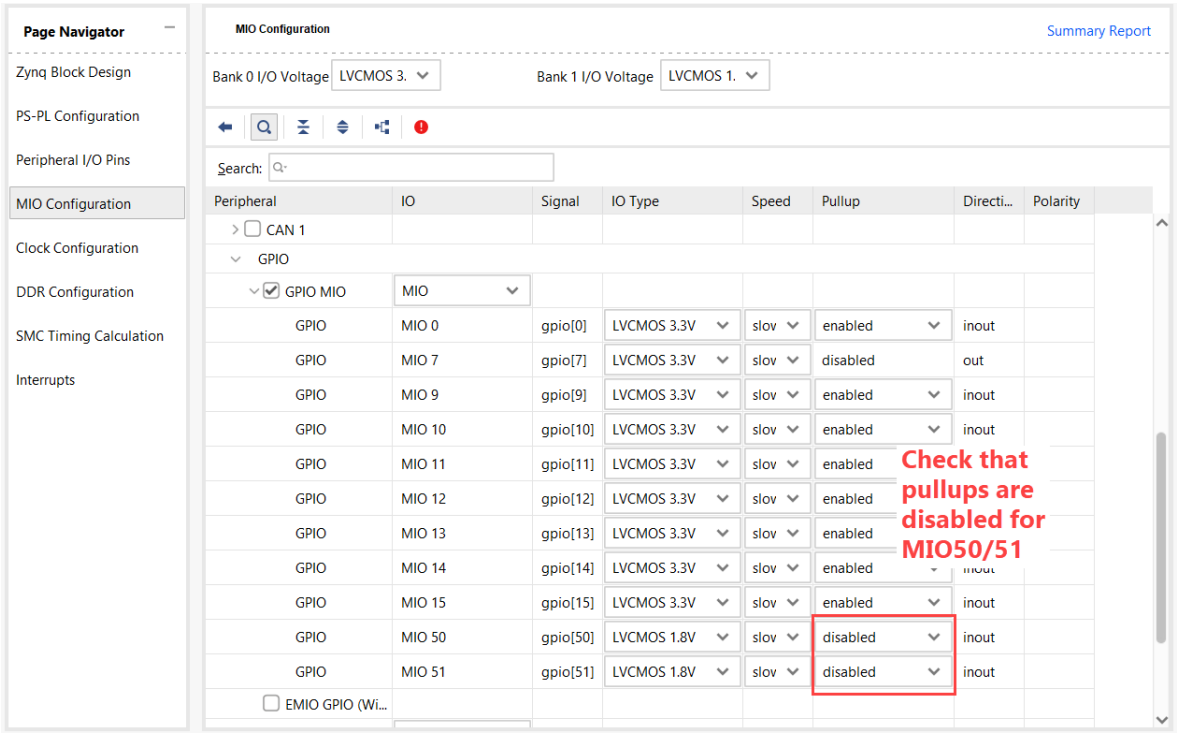

Figure 21. Under 'MIO Configuration', expand the GPIO settings and check that the MIO50/MIO51 pull-ups are disabled.

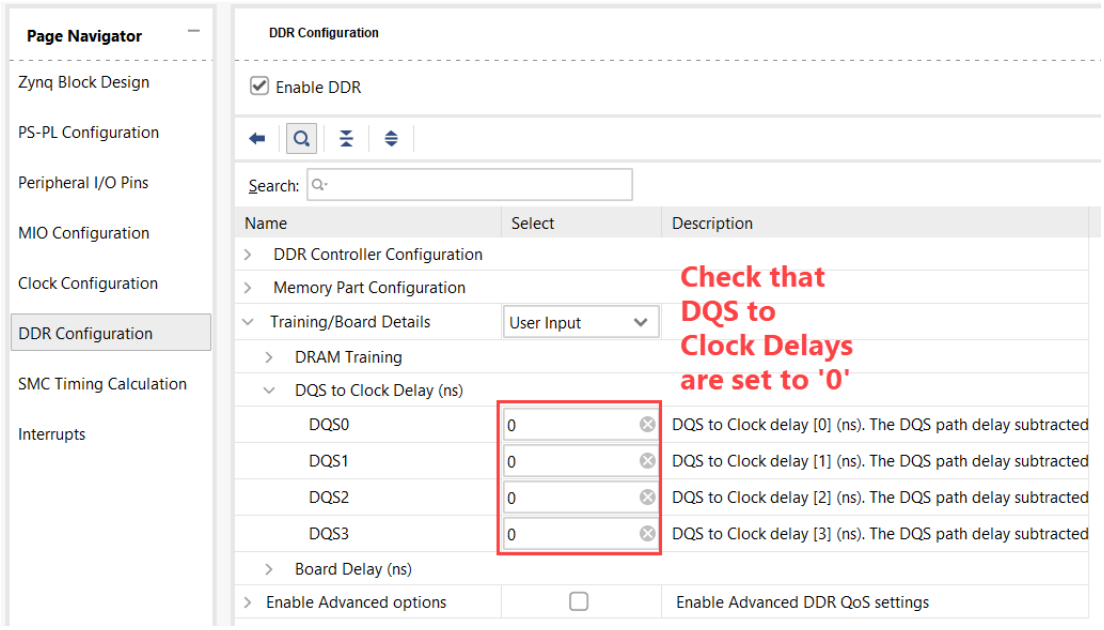

Figure 22. Under 'DDR Configuration -> Training/Board Details', check that the DQS to Clock Delay settings are zero. Click OK when finished.

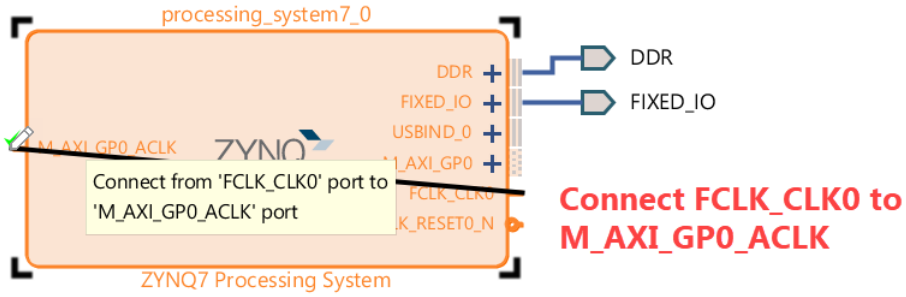

Figure 23. Back at the top-level, connect FCLK_CLK0 to M_AXI_GP0_ALCK.

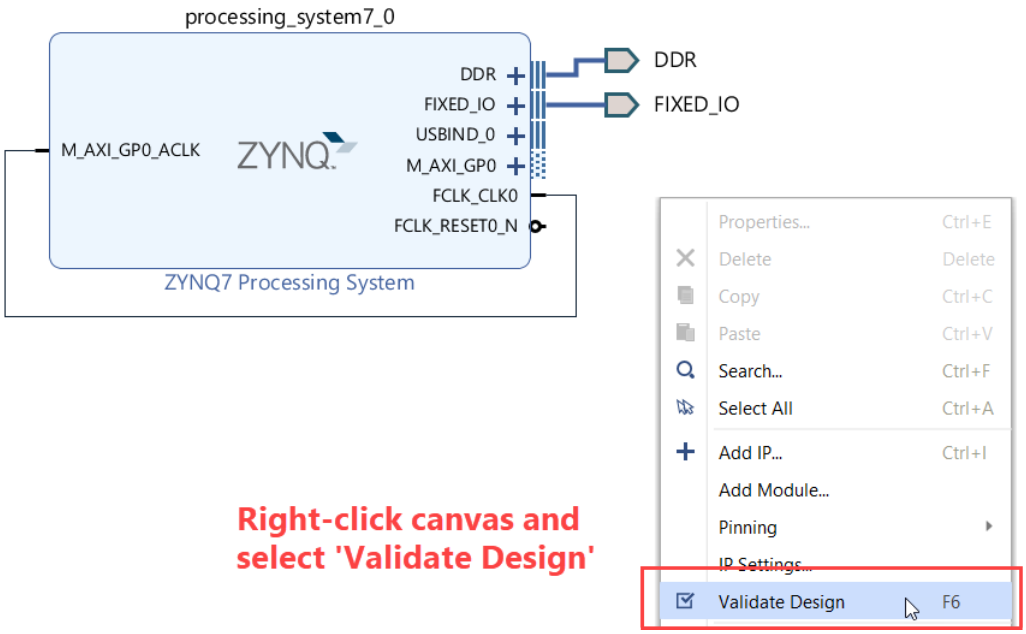

Figure 24. Right-click on the canvas and select 'Validate Design'

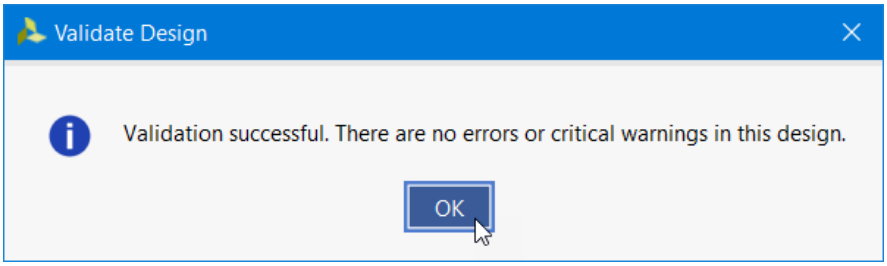

Figure 25. The Validation Success dialog should appear.