

ABC

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1 Heading 1

1.1

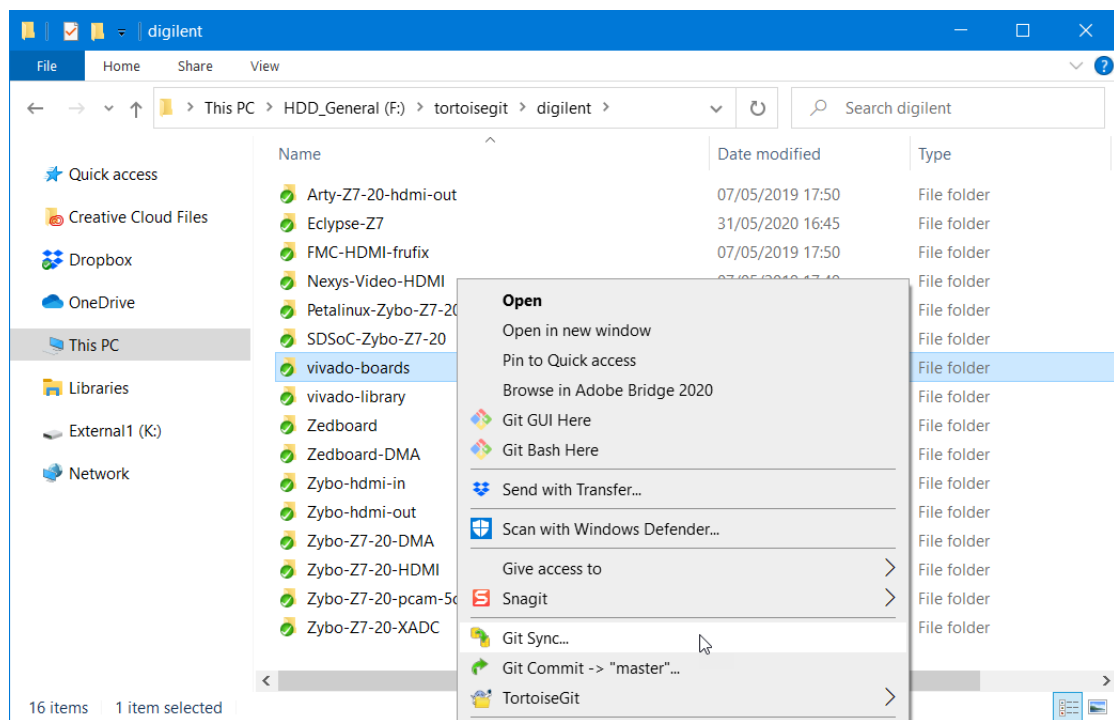


Figure 1. Abc

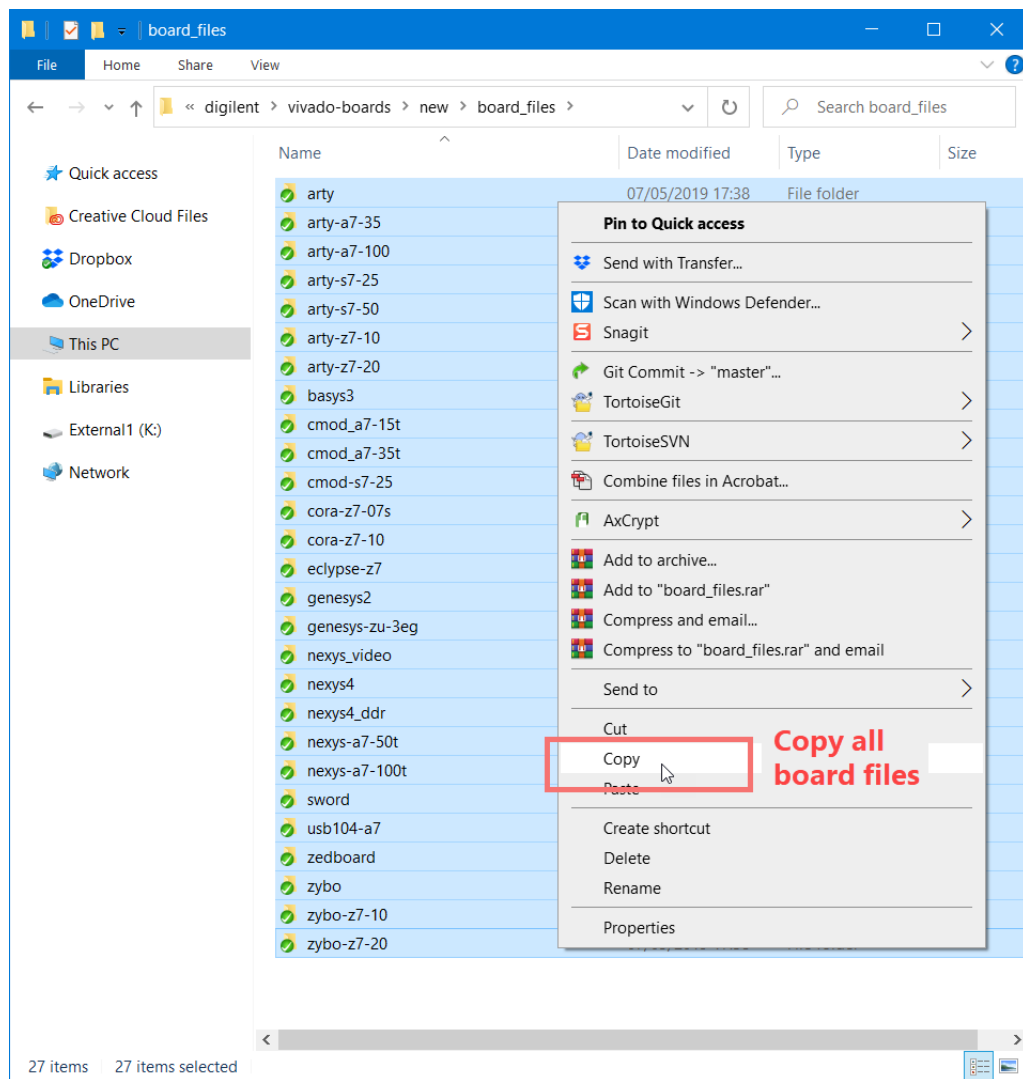


Figure 2. Abc

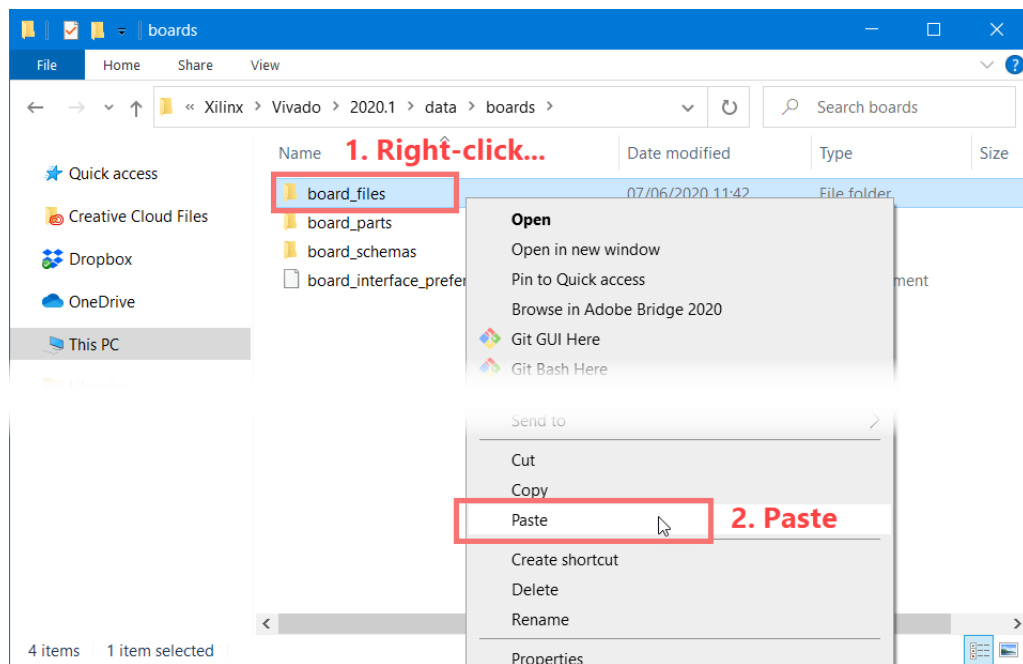


Figure 3. Abc

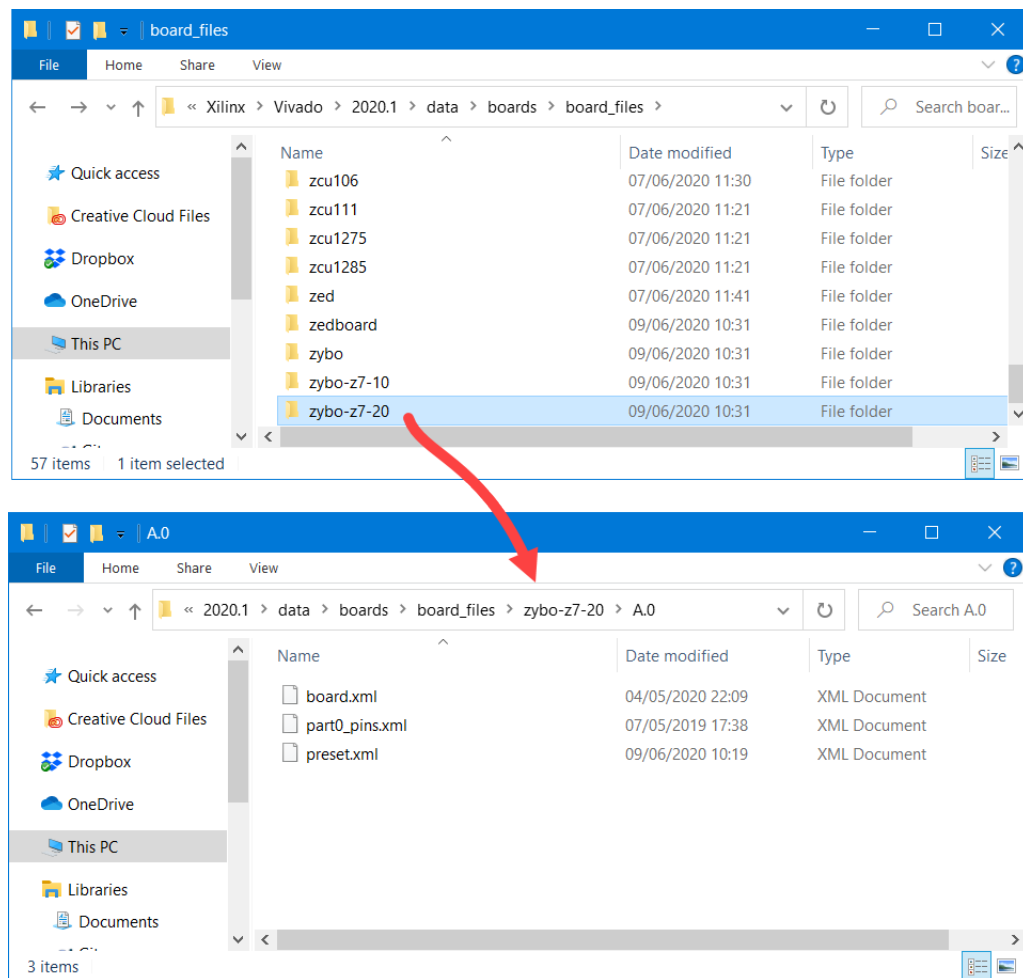


Figure 4. Abc

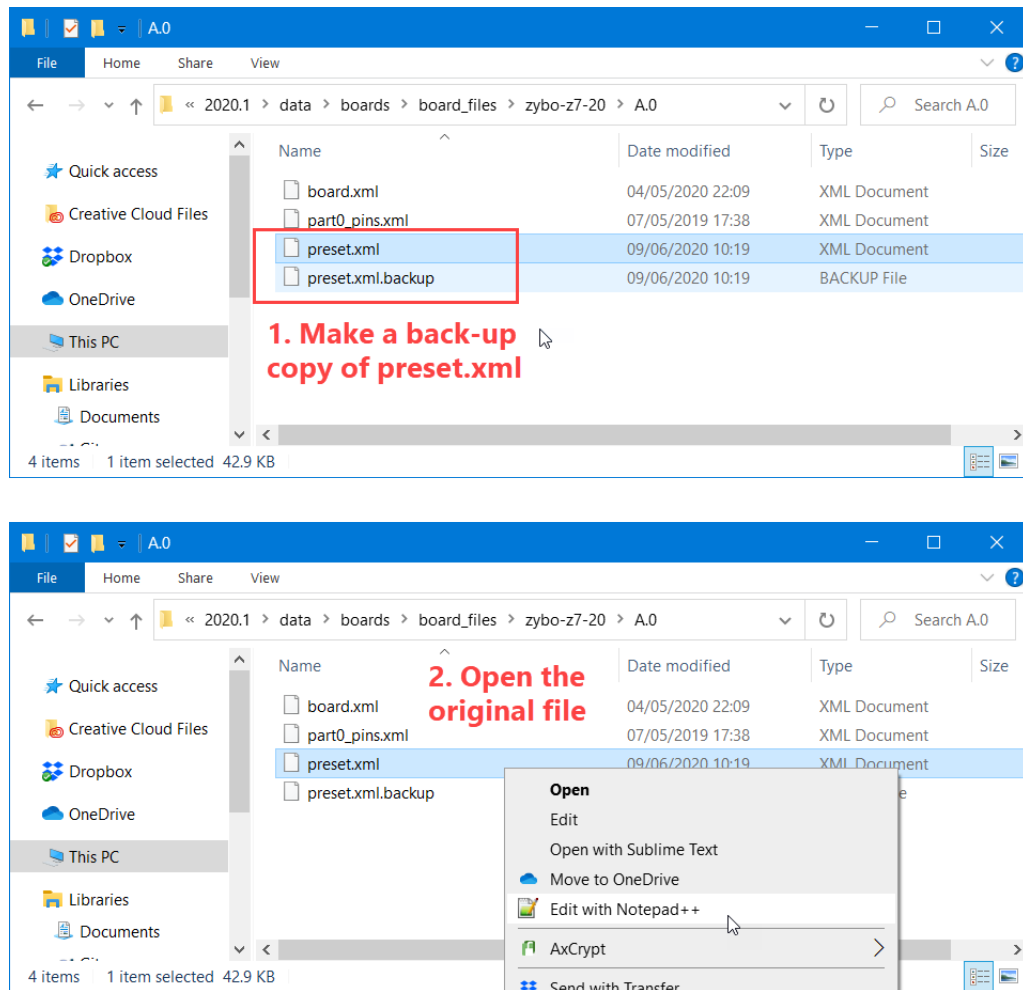


Figure 5. Abc

```

<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQS_3_PACKAGE_LENGTH" value="113.63"/>
<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQS_3_PROPOGATION_DELAY" value="160"/>
<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_0" value="-0.050"/>
<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_1" value="-0.044"/>
<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_2" value="-0.035"/>
<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_3" value="-0.100"/>
<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQ_0_LENGTH_MM" value="22.8"/>
<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQ_0_PACKAGE_LENGTH" value="98.503"/>

```

DQS_TO_CLK_DELAY values: Set to '0'

```

<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQS_3_PACKAGE_LENGTH" value="113.63"/>
<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQS_3_PROPOGATION_DELAY" value="160"/>
<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_0" value="0"/>
<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_1" value="0"/>
<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_2" value="0"/>
<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_3" value="0"/>
<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQ_0_LENGTH_MM" value="22.8"/>
<user_parameter name="CONFIG.PCW_UIPARAM_DDR_DQ_0_PACKAGE_LENGTH" value="98.503"/>

```

Figure 6. Abc

DDR_DQS_TO_CLK_DELAY

```

<user_parameter name="CONFIG.PCW_MIO_4_SLEW" value="slow"/>
<user_parameter name="CONFIG.PCW_MIO_50_DIRECTION" value="inout"/>
<user_parameter name="CONFIG.PCW_MIO_50_IOTYPE" value="LVCMOS 1.8V"/>
<user_parameter name="CONFIG.PCW_MIO_50_PULLUP" value="enabled"/>
<user_parameter name="CONFIG.PCW_MIO_50_SLEW" value="slow"/>
<user_parameter name="CONFIG.PCW_MIO_51_DIRECTION" value="inout"/>
<user_parameter name="CONFIG.PCW_MIO_51_IOTYPE" value="LVCMOS 1.8V"/>
<user_parameter name="CONFIG.PCW_MIO_51_PULLUP" value="enabled"/>
<user_parameter name="CONFIG.PCW_MIO_51_SLEW" value="slow"/>

```

MIO_50/MIO_51 PULLUP value: change to "disabled"

```

<user_parameter name="CONFIG.PCW_MIO_4_SLEW" value="slow"/>
<user_parameter name="CONFIG.PCW_MIO_50_DIRECTION" value="inout"/>
<user_parameter name="CONFIG.PCW_MIO_50_IOTYPE" value="LVCMOS 1.8V"/>
<user_parameter name="CONFIG.PCW_MIO_50_PULLUP" value="disabled"/>
<user_parameter name="CONFIG.PCW_MIO_50_SLEW" value="slow"/>
<user_parameter name="CONFIG.PCW_MIO_51_DIRECTION" value="inout"/>
<user_parameter name="CONFIG.PCW_MIO_51_IOTYPE" value="LVCMOS 1.8V"/>
<user_parameter name="CONFIG.PCW_MIO_51_PULLUP" value="disabled"/>
<user_parameter name="CONFIG.PCW_MIO_51_SLEW" value="slow"/>

```

Figure 7. Abc

PCW_MIO_50_PULLUP



Figure 8. Abc

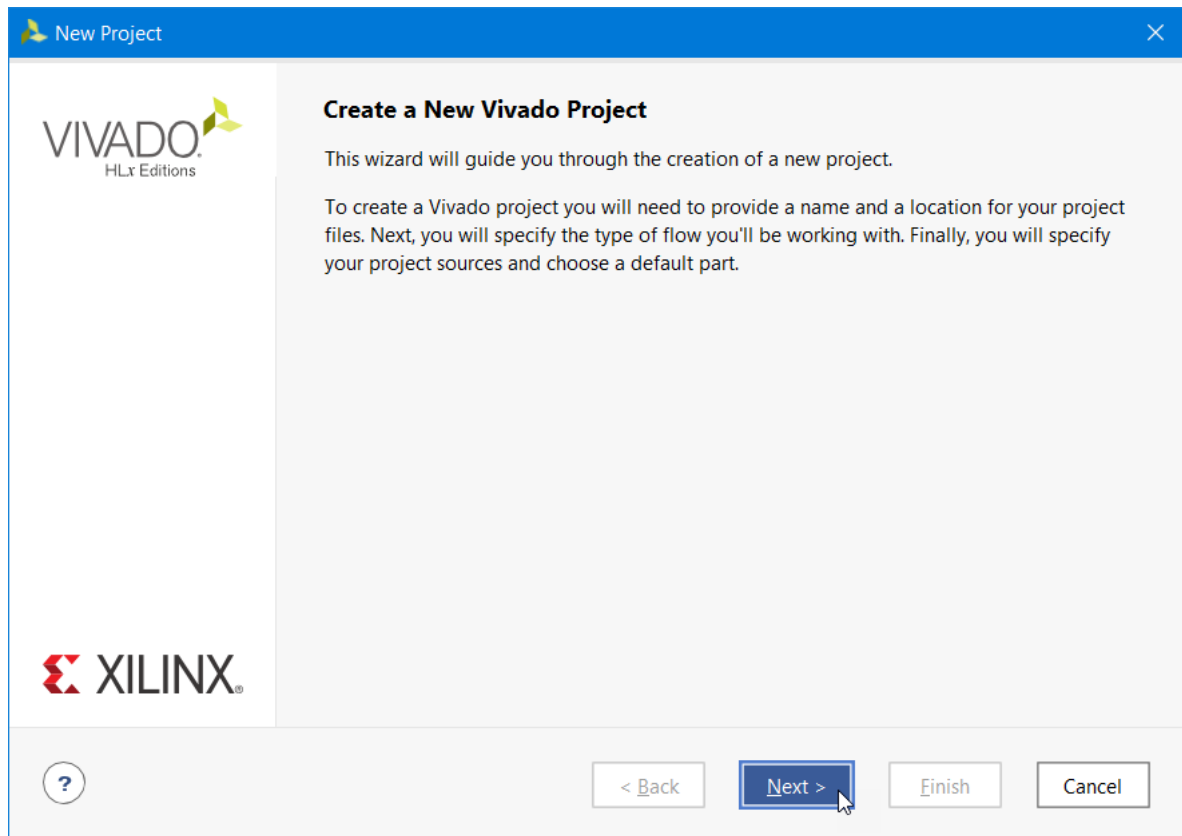
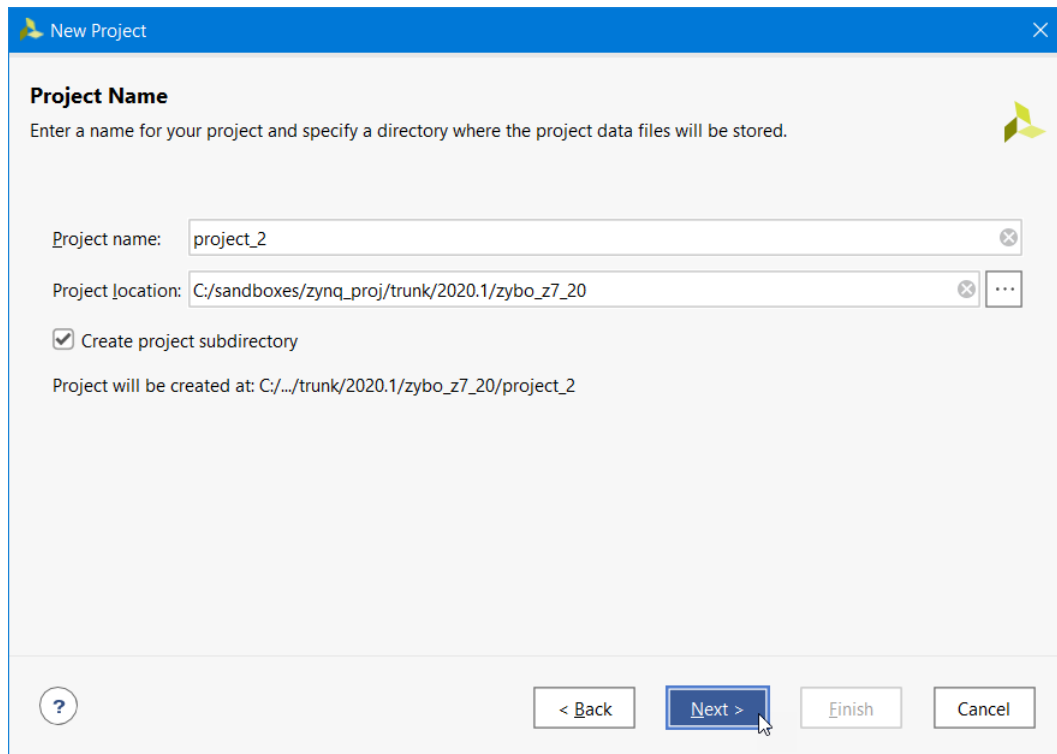


Figure 9. Abc



The image shows a 'New Project' dialog box with a blue title bar. The main area is light gray. At the top, it says 'Project Name' and 'Enter a name for your project and specify a directory where the project data files will be stored.' Below this, there are two text input fields. The first is labeled 'Project name:' and contains the text 'project_2'. The second is labeled 'Project location:' and contains the text 'C:/sandboxes/zynq_proj/trunk/2020.1/zybo_z7_20'. To the right of the second field is a button with three dots. Below the input fields, there is a checkbox labeled 'Create project subdirectory' which is checked. Below the checkbox, it says 'Project will be created at: C:/.../trunk/2020.1/zybo_z7_20/project_2'. At the bottom of the dialog, there are four buttons: a help button with a question mark, a '< Back' button, a 'Next >' button (which is highlighted with a mouse cursor), an 'Finish' button, and a 'Cancel' button.

New Project

Project Name
Enter a name for your project and specify a directory where the project data files will be stored.

Project name:

Project location:

☒ Create project subdirectory

Project will be created at: C:/.../trunk/2020.1/zybo_z7_20/project_2

? < Back Next > Finish Cancel

Figure 10. Abc

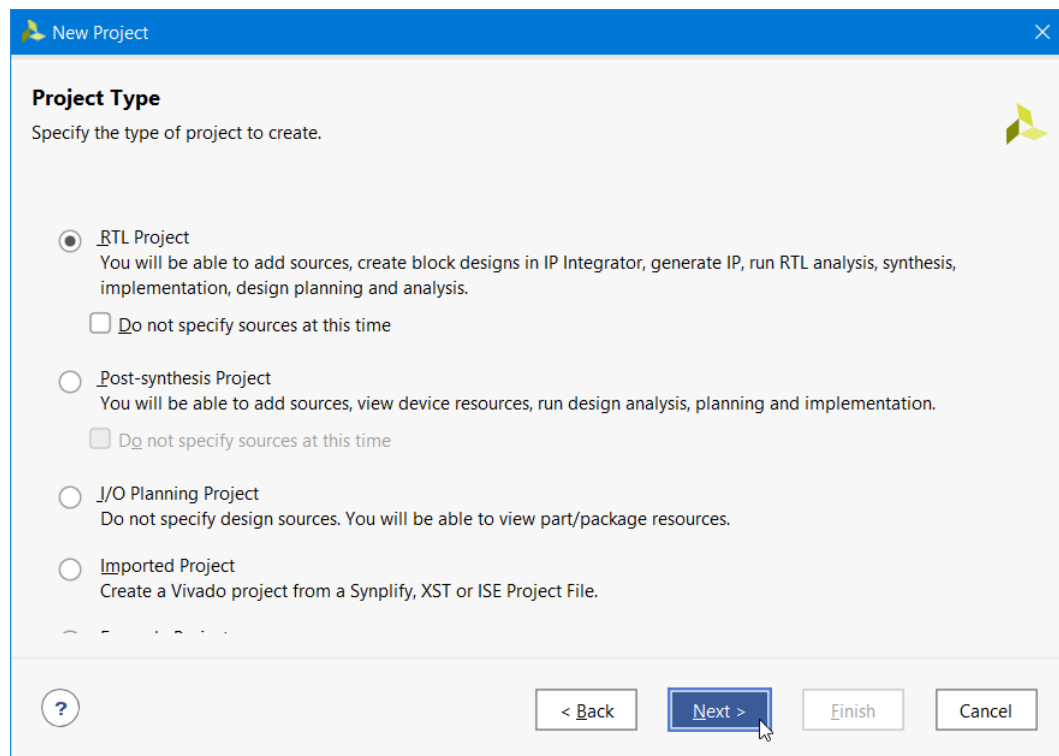


Figure 11. Abc

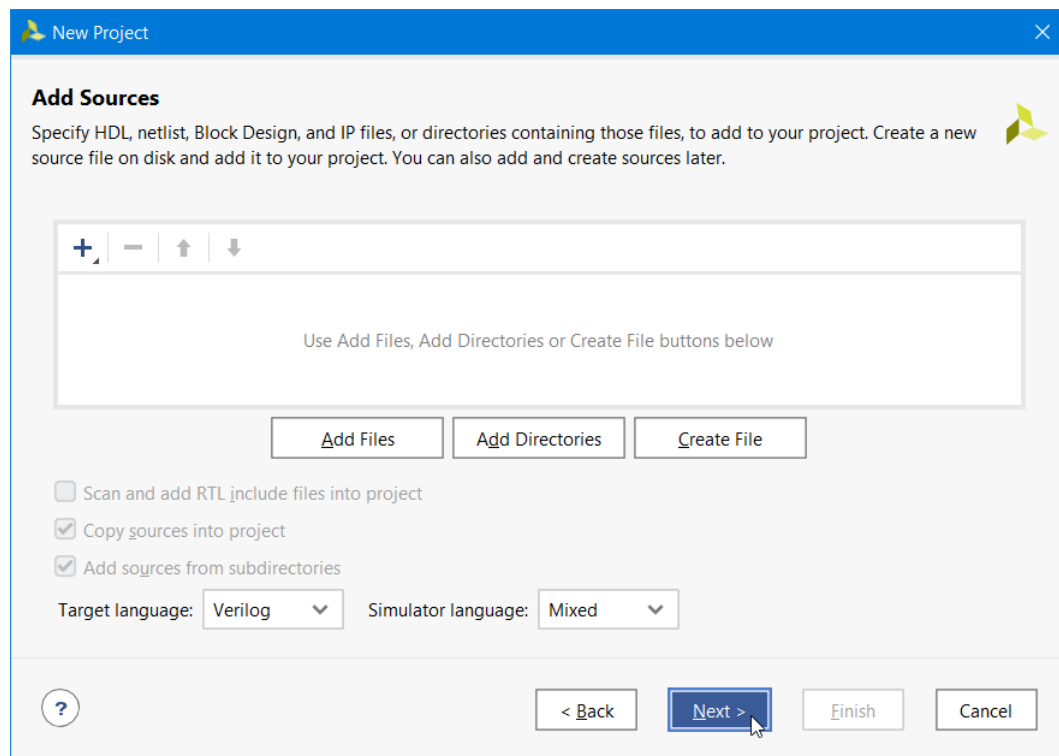


Figure 12. Abc

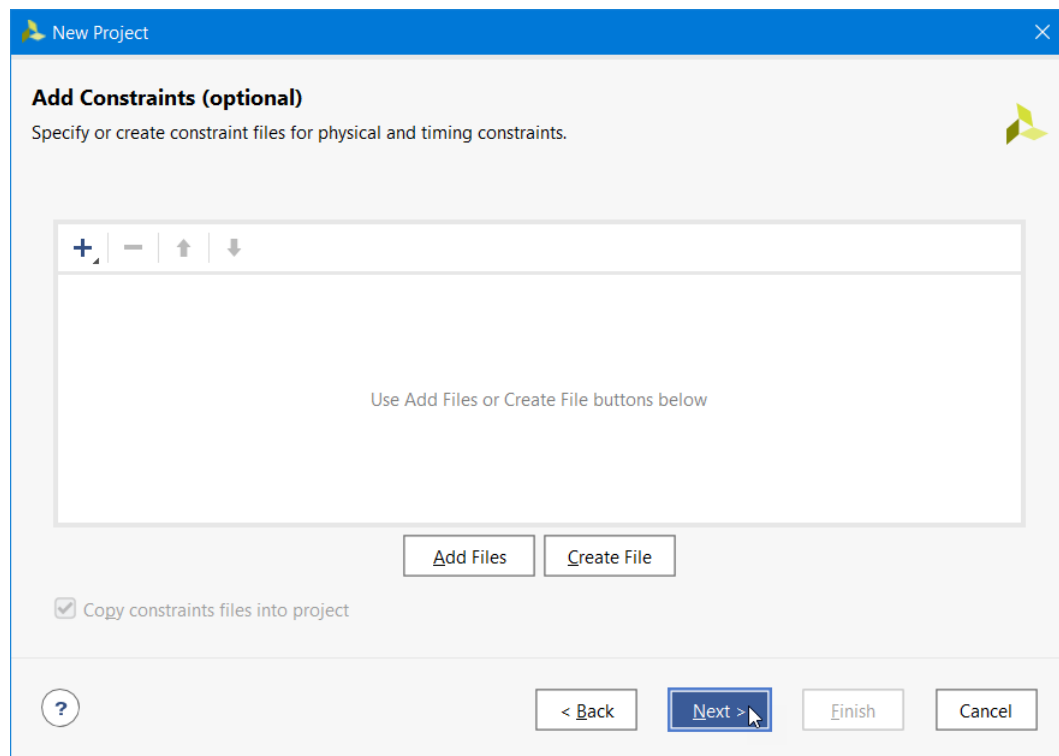


Figure 13. Abc

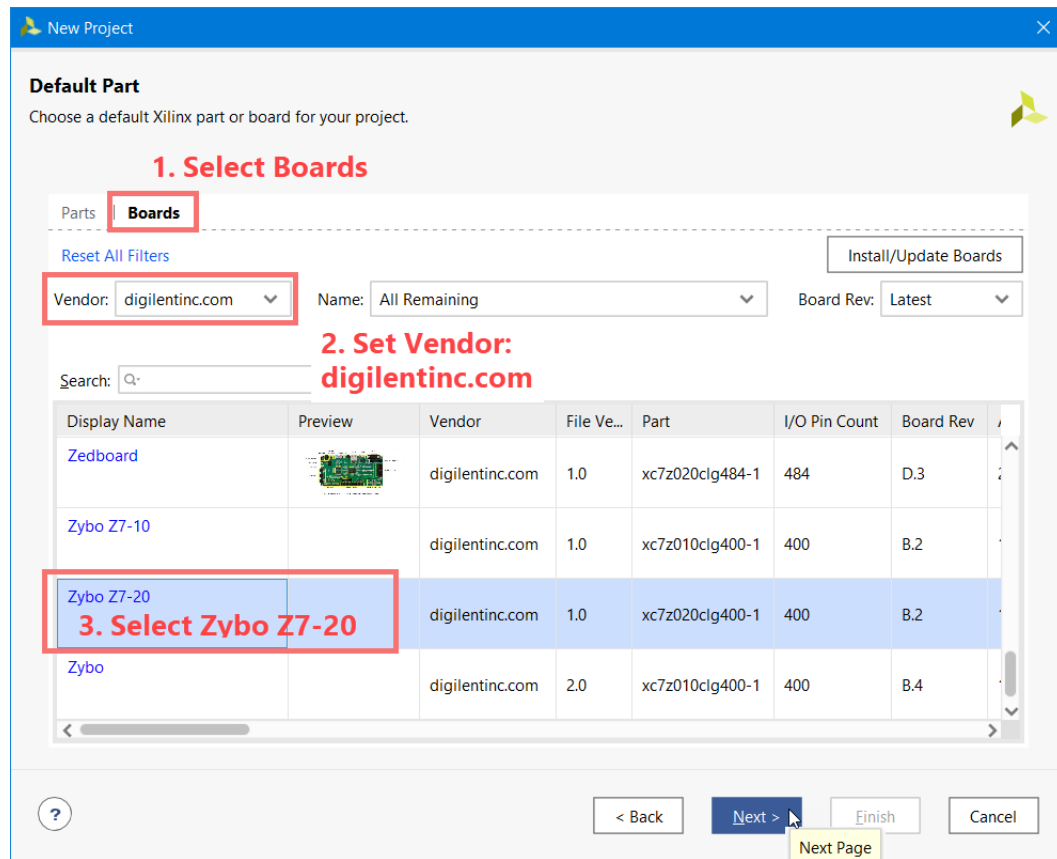


Figure 14. Abc

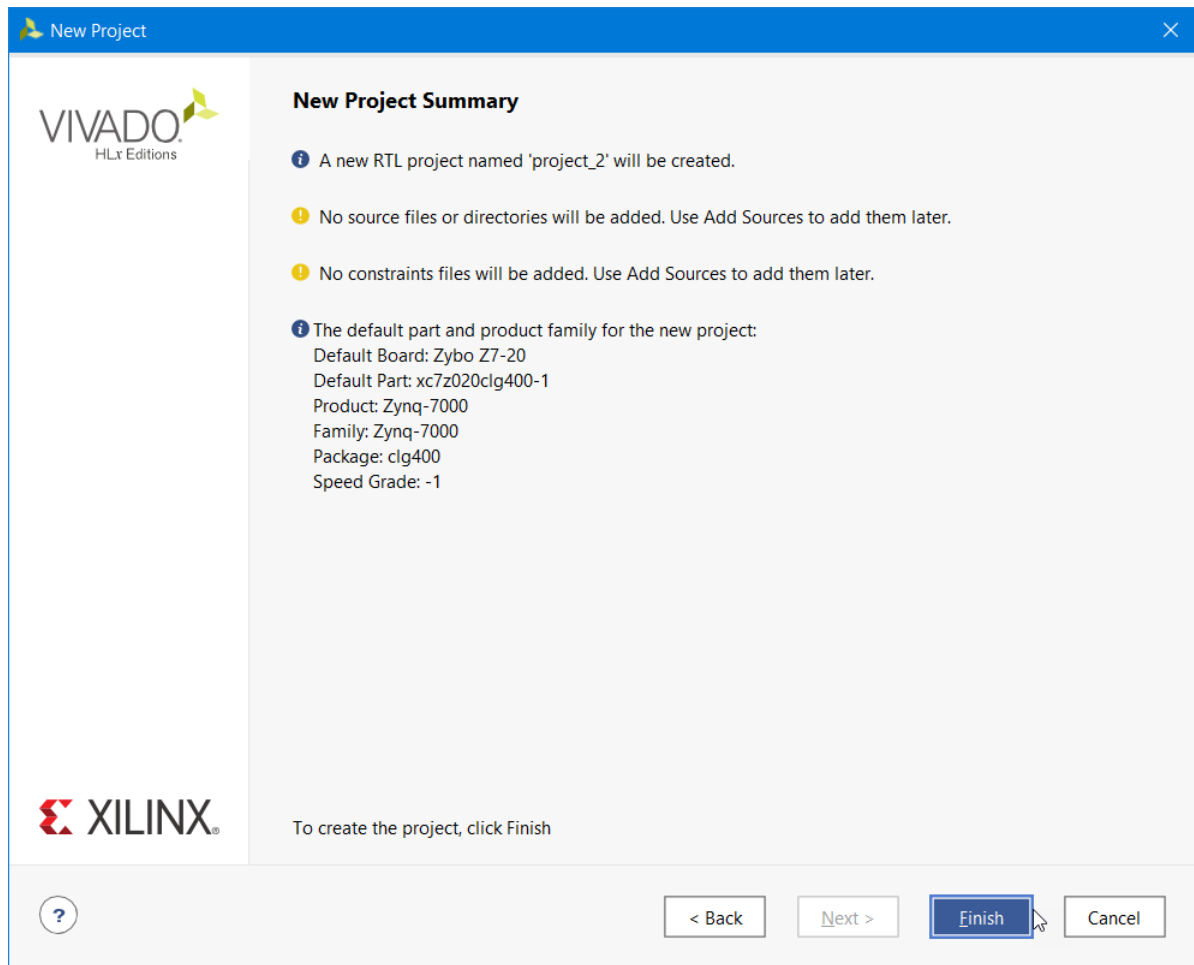



Figure 15. Abc

▼ IP INTEGRATOR

[Create Block Design](#)

Open Block Design

Generate Block Design



Create Block Design

Please specify name of block design.

Design name:

design_1

Directory:

<Local to Project>

Specify source set:

Design Sources

?

OK

Cancel

Figure 16. Abc

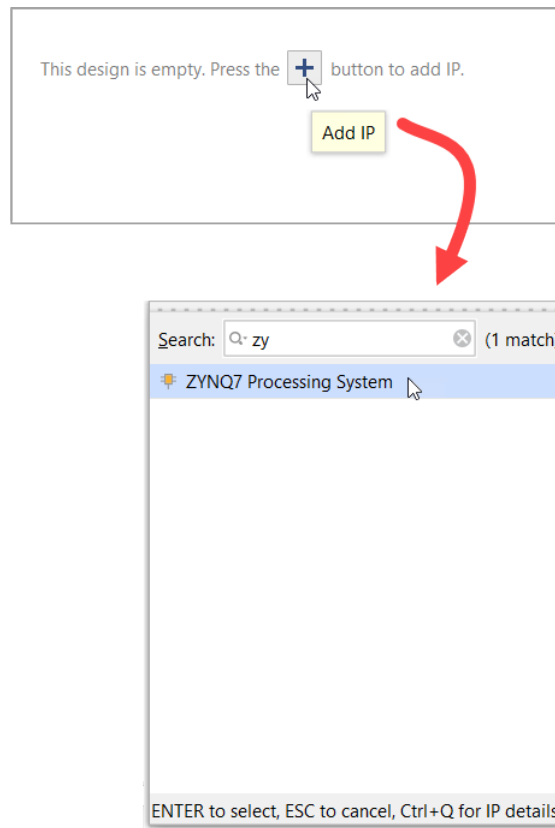


Figure 17. Abc

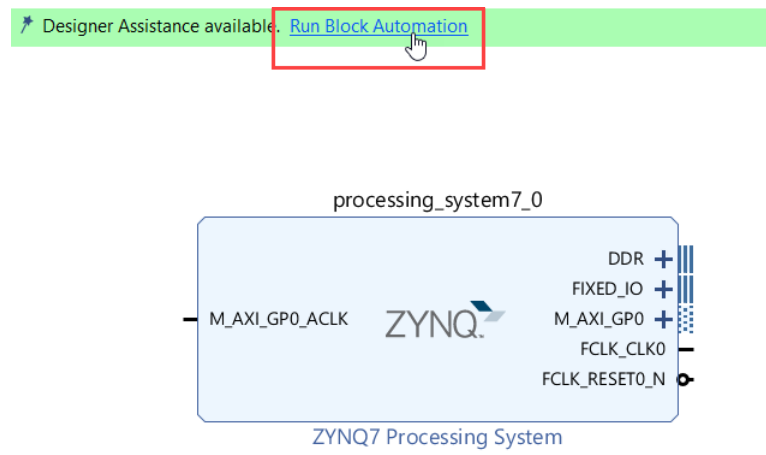


Figure 18. Abc

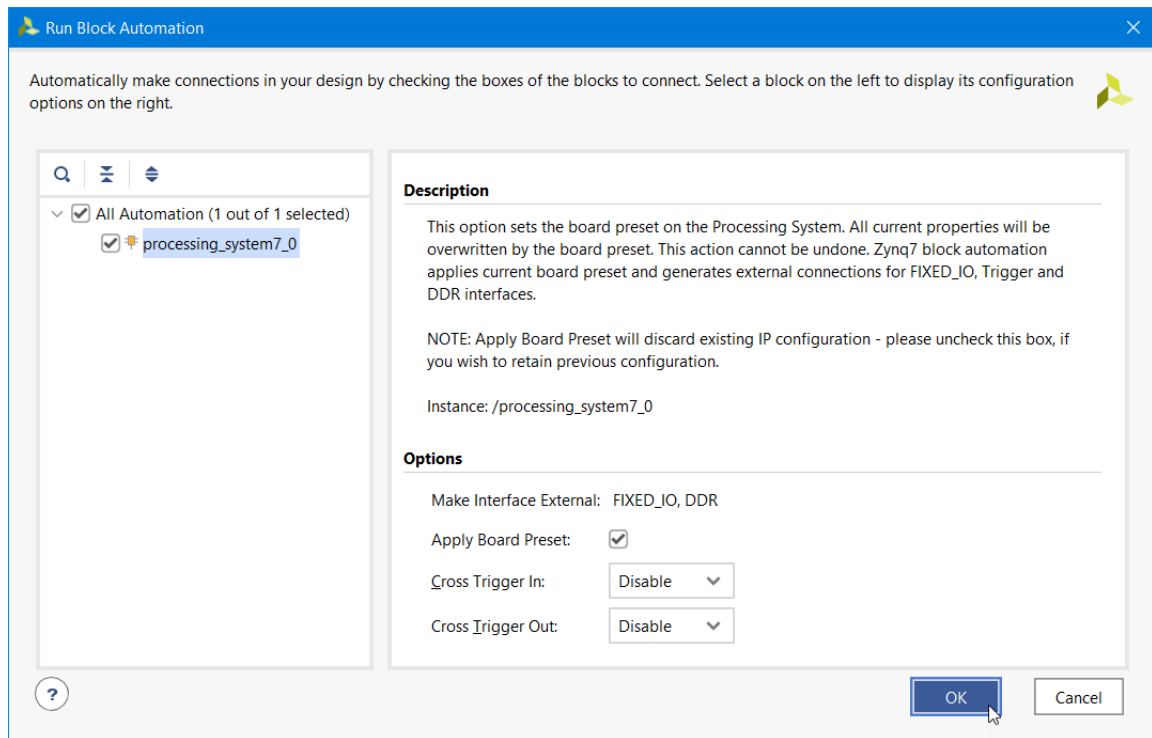


Figure 19. Abc

Page Navigator

- Zynq Block Design
- PS-PL Configuration
- Peripheral I/O Pins
- MIO Configuration**
- Clock Configuration
- DDR Configuration
- SMC Timing Calculation
- Interrupts

MIO Configuration [Summary Report](#)

Bank 0 I/O Voltage: LVCMOS 3.3V Bank 1 I/O Voltage: LVCMOS 1.8V

Search:

Peripheral	IO	Signal	IO Type	Speed	Pullup	Directi...	Polarity
> <input type="checkbox"/> CAN 1							
> <input type="checkbox"/> GPIO							
> <input checked="" type="checkbox"/> GPIO MIO	MIO <input type="text"/>						
GPIO	MIO 0	gpio[0]	LVCMOS 3.3V	slov	enabled	inout	
GPIO	MIO 7	gpio[7]	LVCMOS 3.3V	slov	disabled	out	
GPIO	MIO 9	gpio[9]	LVCMOS 3.3V	slov	enabled	inout	
GPIO	MIO 10	gpio[10]	LVCMOS 3.3V	slov	enabled	inout	
GPIO	MIO 11	gpio[11]	LVCMOS 3.3V	slov	enabled	inout	
GPIO	MIO 12	gpio[12]	LVCMOS 3.3V	slov	enabled	inout	
GPIO	MIO 13	gpio[13]	LVCMOS 3.3V	slov	enabled	inout	
GPIO	MIO 14	gpio[14]	LVCMOS 3.3V	slov	enabled	inout	
GPIO	MIO 15	gpio[15]	LVCMOS 3.3V	slov	enabled	inout	
GPIO	MIO 50	gpio[50]	LVCMOS 1.8V	slov	disabled	inout	
GPIO	MIO 51	gpio[51]	LVCMOS 1.8V	slov	disabled	inout	
<input type="checkbox"/> EMIO GPIO (Wi...							

Check that pullups are disabled for MIO50/51

Figure 20. Abc

Page Navigator

Zynq Block Design

PS-PL Configuration

Peripheral I/O Pins

MIO Configuration

Clock Configuration

DDR Configuration

SMC Timing Calculation

Interrupts

DDR Configuration

☒ Enable DDR

←

Q

≡

⌵

Search:

Name	Select	Description
> DDR Controller Configuration		
> Memory Part Configuration		
▼ Training/Board Details	User Input	
> DRAM Training		
▼ DQS to Clock Delay (ns)		
DQS0	<input type="text" value="0"/>	DQS to Clock delay [0] (ns). The DQS path delay subtracted
DQS1	<input type="text" value="0"/>	DQS to Clock delay [1] (ns). The DQS path delay subtracted
DQS2	<input type="text" value="0"/>	DQS to Clock delay [2] (ns). The DQS path delay subtracted
DQS3	<input type="text" value="0"/>	DQS to Clock delay [3] (ns). The DQS path delay subtracted
> Board Delay (ns)		
> Enable Advanced options	<input type="checkbox"/>	Enable Advanced DDR QoS settings

Check that
DQS to
Clock Delays
are set to '0'

Figure 21. Abc

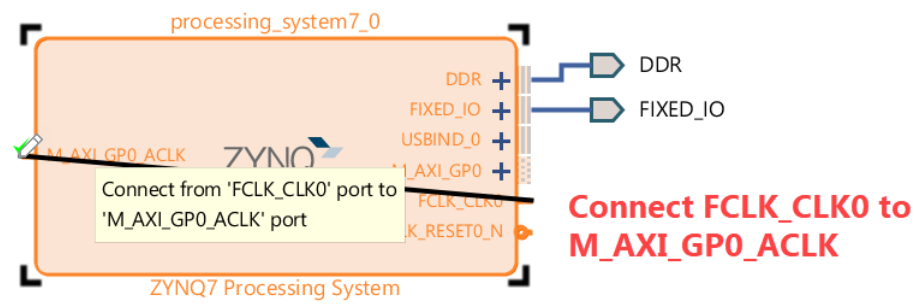


Figure 22. Abc

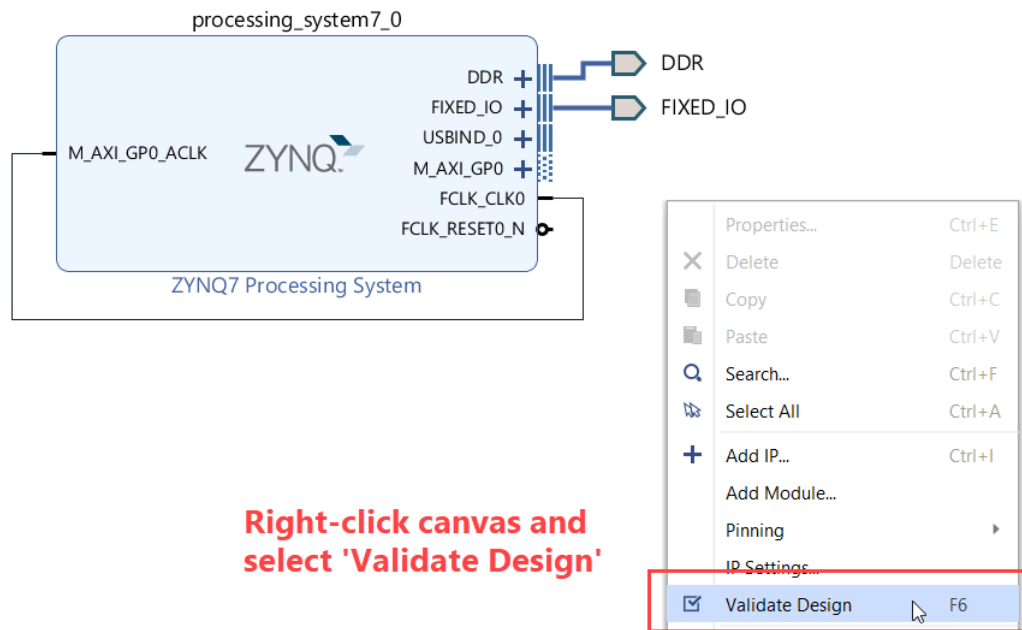


Figure 23. Abc

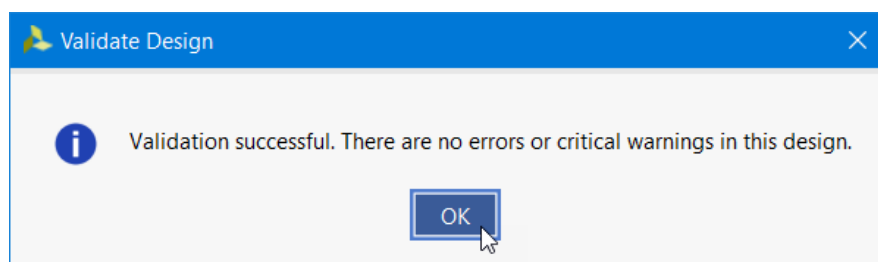


Figure 24. Abc

