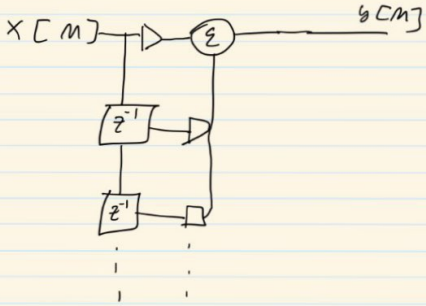
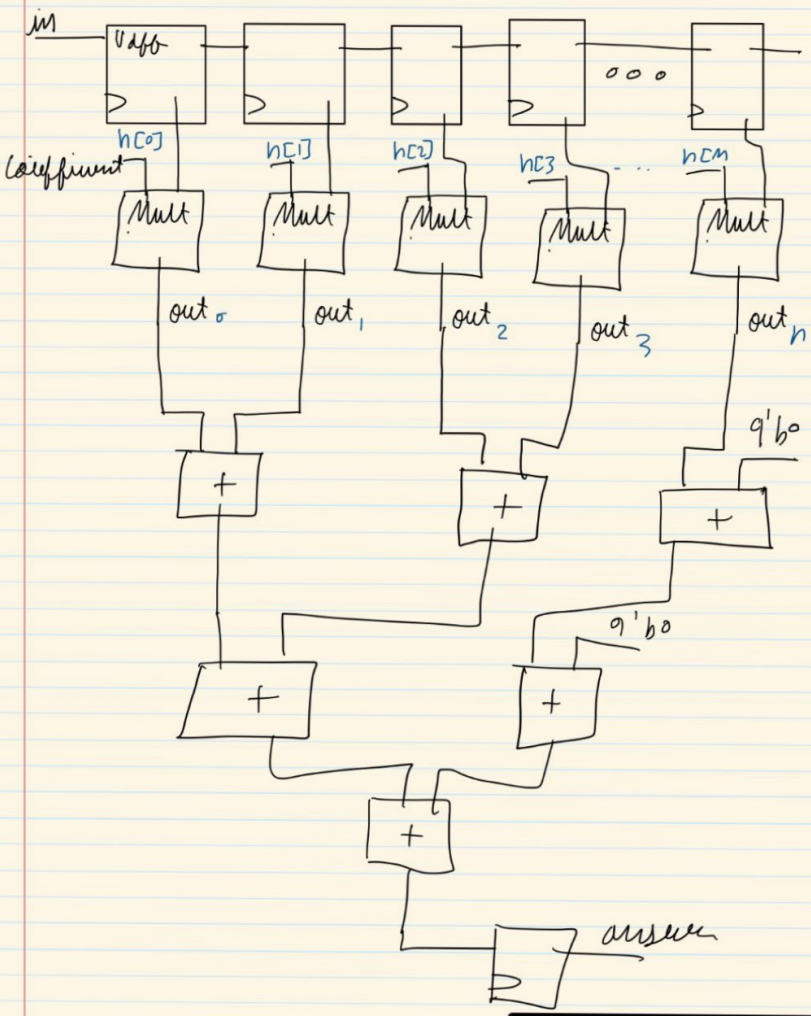
N-TAP FIR filter

Tuesday, November 26, 2019 4:12 AM



I have 3 different approches to this design problem

#1 Pyramid adder + fully parallel multiplier



Analysis

This implementation allows you to have a much higher FMAX, at the cost of more PLB usage.

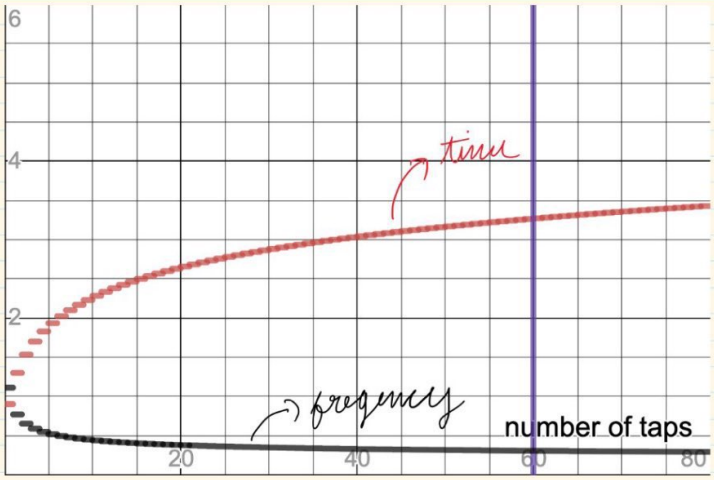
Delay analysis

$t =$ Multiplier delay + adder delay

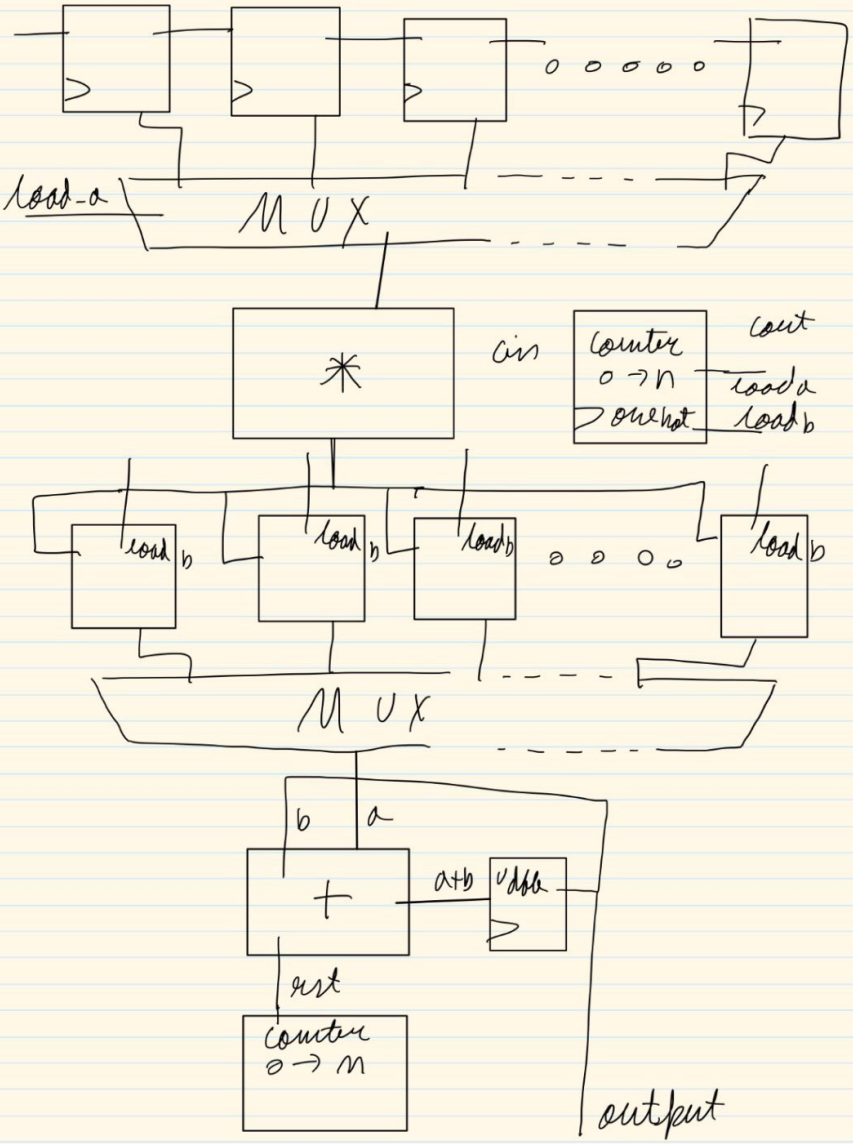
$t = t_{mult} + t_{add} * \frac{\log_e(N)}{\log_e(2)} \Rightarrow$ frequency $= 1/t$

Where N is the number of taps

To give you a rough idea



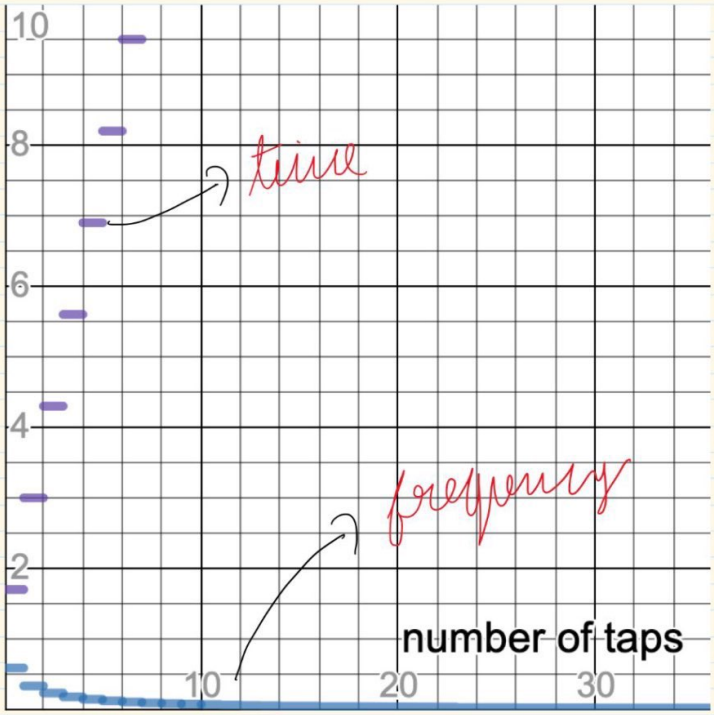
#2 Serial multiplier + serial adder



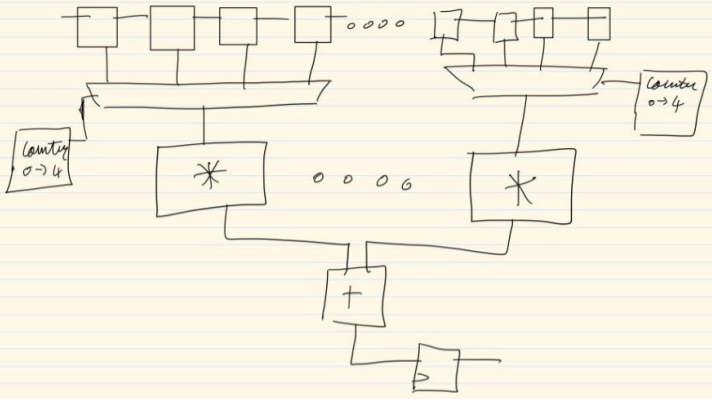
Analysis

Here you will get much slower FMAX, and the sampling maximum frequency will be greatly decreased,
however you will get a much better Area/power parameter with this design

$$t = Mux\ delay + N * Mult\ delay + Udff\ delay + Mux\ delay + N * adder\ delay + udff\ delay$$
$$= 2 * t_{mux} + N*(t_{mult} + t_{adder}) + 2 * t_{Udff}$$



#3 HYBRID windowing approach



best of both the worlds

now

we will need to optimize time and area by using KKT Lagrange.

$$\delta(t) = t = N/L\,(Mux + Mult) + \frac{\log_e(N/L)}{\log_e(2)}\,\text{adder delay}$$

$$= \frac{N}{L}\left(t_{mux} + t_{mult}\right) + \frac{\log_e(N/L)}{\log_e 2}\,t_{odd}$$

area = say some funtion of N

$= \delta(N)$

so it depends where or not you should implement it