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Course Code : MCS-012

Course Title : Computer Organisation and Assembly Language Programming

Q1:

(a) Please refer to Figure 4 of Unit 1 of Block 1 on page 11 of Instruction execution example. Assuming a similar machine is to be used for execution of the following three consecutive instructions:

LDA A ; Load the content of Memory location A into the Accumulator Register.

ADD B ; Add the content of memory location B from Accumulator Register.

STR C ; Stores the content of Accumulator register to memory location C.

However, this machine is different from the example of Figure 4 in the following ways:

- Each memory word of this new machine is of 32 bits in length.
- Each instruction is of length 32 bits with 16 bits for operation code (opcode) and 16 bits for specifying one direct operand.
- The Main Memory of the machine would be of size 64 KB.
- The three consecutive instructions are placed starting from memory location (200E)h ; operand A is at location (500A)h and contains a value (00010056)h, Operand B is at location (500B)h and contains a value (0122A0EE)h and operand C is at location (500C)h and contains a value (00000000)h.
- The AC, IR and MBR registers are of size 32 bits, whereas PC and MAR registers are of size 16 bits. The initial content of PC register is (200E)h

Draw the diagrams showing the following information:

(i) Initial State of the machine with the addresses and content of memory locations in hexadecimal. Show only those address locations of the memory that store the instruction and data. Also show content of all the stated registers. (2 Marks)

Ans:-

0			200E	PC
1	LOAD A		-	AC
2	ADD B		-	IR
3	STORE C			
-				
-				
500A	0010056	A	1	MAR
500B	0122A0EE	B		
500C	-	C	-	MBR

(ii) Draw three more diagrams, each showing the state of machine after execution of every instruction viz. LDA, ADD and STR. Show the changes in the values of Registers and memory locations, if any, due to execution of instruction. Show all the addresses and values in hexadecimal notations.

Ans:-

STEP :-1

0			200F	PC
1	LOAD A		-	AC
2	ADD B		LOAD A	IR
3	STORE C			
-				
-				
500A	0010056	A	1	MAR
500B	0122A0EE	B		
500C	-	C	LOAD A	MBR



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STEP:-2

0			2010	PC
1	LOAD A			AC
2	ADD B		ADD B	IR
3	STORE C		1	MAR
-			ADD B	MBR
-				
500A	0010056	A		
500B	0122A0EE	B		
500C	-	C		

STEP:-3

0			2011	PC
1	LOAD A			AC
2	ADD B		STORE C	IR
3	STORE C		1	MAR
-			123A144	MBR
-				
500A	0010056	A		
500B	0122A0EE	B		
500C	123A144	C		

(b) Perform the following conversion of numbers: (2 Marks)

i) Decimal (3216547890)₁₀ to binary and hexadecimal

Ans:-

Decimal to binary calculation steps

Divide by the base 2 to get the digits from the remainders:

Division by 2	Quotient	Remainder (Digit)	Bit #
(3216547890)/2	1608273945	0	0
(1608273945)/2	804136972	1	1
(804136972)/2	402068486	0	2
(402068486)/2	201034243	0	3
(201034243)/2	100517121	1	4
(100517121)/2	50258560	1	5
(50258560)/2	25129280	0	6
(25129280)/2	12564640	0	7
(12564640)/2	6282320	0	8
(6282320)/2	3141160	0	9
(3141160)/2	1570580	0	10
(1570580)/2	785290	0	11
(785290)/2	392645	0	12
(392645)/2	196322	1	13
(196322)/2	98161	0	14
(98161)/2	49080	1	15
(49080)/2	24540	0	16
(24540)/2	12270	0	17

Disclaimer/Note

These are just the sample of the answers/solution to some of the questions given in the assignments. Student should read and refer the official study material provided by the university.



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Division by 2	Quotient	Remainder (Digit)	Bit #
(12270)/2	6135	0	18
(6135)/2	3067	1	19
(3067)/2	1533	1	20
(1533)/2	766	1	21
(766)/2	383	0	22
(383)/2	191	1	23
(191)/2	95	1	24
(95)/2	47	1	25
(47)/2	23	1	26
(23)/2	11	1	27
(11)/2	5	1	28
(5)/2	2	1	29
(2)/2	1	0	30
(1)/2	0	1	31

$$= (101111110111000101000000110010)_2$$

Decimal to hex calculation steps

Divide by the base 16 to get the digits from the remainders:

Division by 16	Quotient	Remainder (Digit)	Digit #
(3216547890)/16	201034243	2	0
(201034243)/16	12564640	3	1
(12564640)/16	785290	0	2
(785290)/16	49080	10	3
(49080)/16	3067	8	4
(3067)/16	191	11	5
(191)/16	11	15	6
(11)/16	0	11	7

$$= (\text{BFB8A032})_{16}$$

ii) Hexadecimal (666777888)h into Octal.

Ans:-

STEP 1-HEXADECIMAL TO BINARY

In the first step, we convert the hexadecimal number to binary.

$$011060110601106011170111701117100081000810008$$

To convert a hexadecimal number to binary, we write 4 bit binary equivalent of each hexadecimal digit in the same order.

$$(\text{666777888})_{16} = (\text{011001100110011101110111100010001000})_2$$

STEP 2-BINARY TO OCTAL

In the second step, we convert the binary number to octal.

$$301110014100611030115101611071114100201010010000$$

Starting from the least significant bit, we partition the binary number into groups of 3 bits and proceed to the left.

$$(\text{011001100110011101110111100010001000})_2 = (\text{314635674210})_8$$

COMBINING RESULTS

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Using the equalities we obtained in steps 1 and 2, we reach the following result.

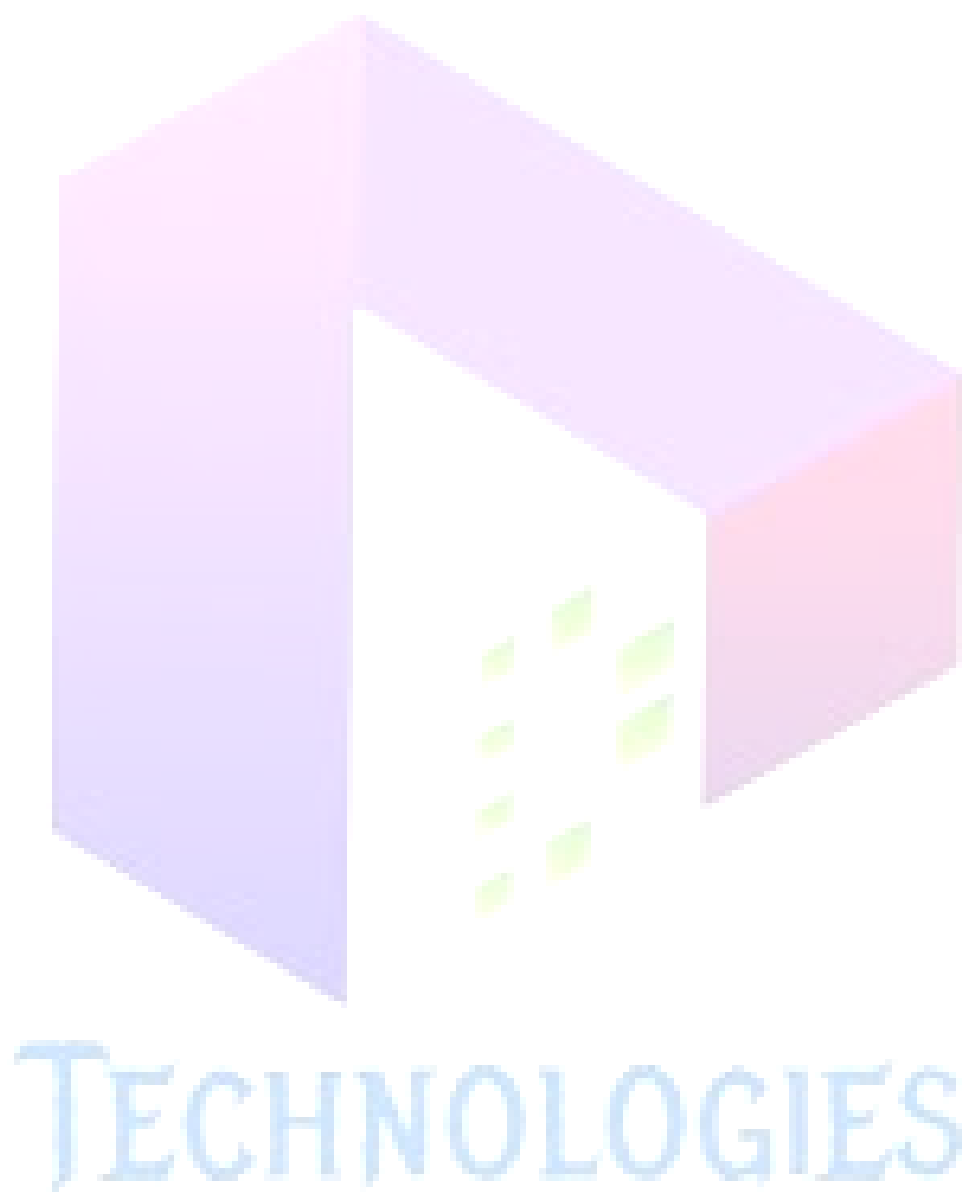
$$(666777888)_{16} = (314635674210)_8$$

iii) String “MCS12 is part of BCA” into UTF 8

Ans:-

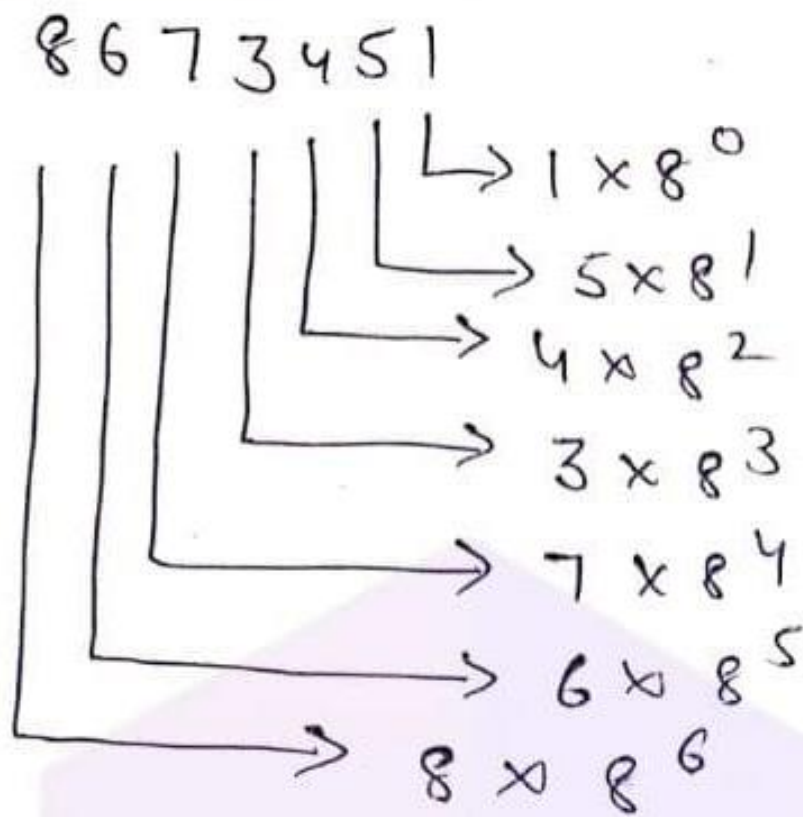
`\x4D\x43\x53\x31\x32\x20\x69\x73\x20\x70\x61\x72\x74\x20\x6F\x66\x20\x42\x43\x41`

iv) Octal (8673451)O into Decimal





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$$(8673451)_8 = (8 \times 8^6) + (6 \times 8^5) + (7 \times 8^4) + (3 \times 8^3) + (4 \times 8^2) + (5 \times 8^1) + (1 \times 8^0)$$

$$= (8 \times 262144) + (6 \times 32768) + (7 \times 4096) + (3 \times 512) + (4 \times 64) + 40 + 8$$

$$= 2097152 + 196608 + 28672 + 1536 + 256 + 40 + 8$$

$$= (2324272)_{10}$$

(c) Simplify the following function using K-map: $F(A, B, C, D) = \Sigma (2, 3, 6, 7, 10, 14)$ Draw the circuit for the function using NAND gates. (2 Marks)



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$$F(A, B, C, D) = \Sigma(2, 3, 6, 7, 10, 14)$$

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	1	3	2
$\bar{A}B$	4	5	7	6
AB	12	13	15	14
$A\bar{B}$	8	9	11	10

$$F(A, B, C, D) = \bar{A}C + C\bar{D}$$

$$= C(\bar{A} + \bar{D})$$

$$= C \cdot (\bar{A} + \bar{D})$$

$$= (\bar{A} + \bar{D}) \cdot C$$

∴ if

$$Y = (\bar{A} + \bar{D}) \cdot C$$

$$\bar{Y} = \overline{(\bar{A} + \bar{D}) \cdot C}$$

Apply the De-Morgan's

$$\bar{Y} = \overline{(\bar{A} + \bar{D}) \cdot C}$$

$$= \overline{(\bar{A} + \bar{D})} + \bar{C}$$

$$\because \overline{A \cdot B} = \bar{A} + \bar{B}$$

$$\overline{\bar{A} + \bar{D}} = \bar{\bar{A}} \cdot \bar{\bar{D}}$$

$$\because \overline{A + B} = \bar{A} \cdot \bar{B}$$

$$= A \cdot D$$

(A · D) Replace this term with $(\overline{\bar{A} + \bar{D}})$



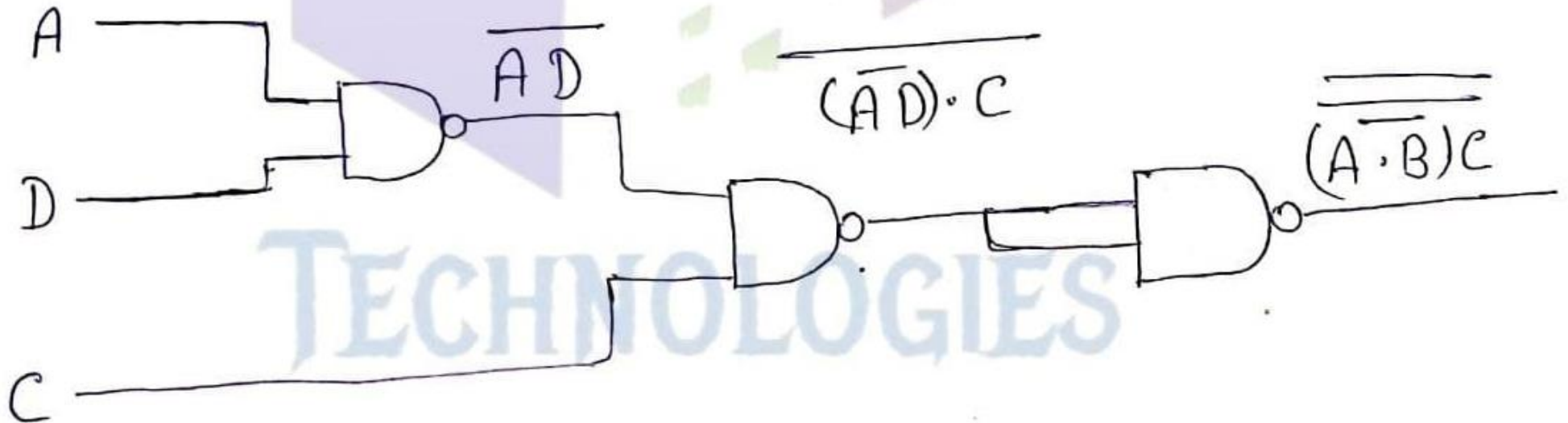
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$$\overline{AD + \bar{C}}$$

$$= (\overline{A \cdot B}) \cdot \bar{\bar{C}}$$

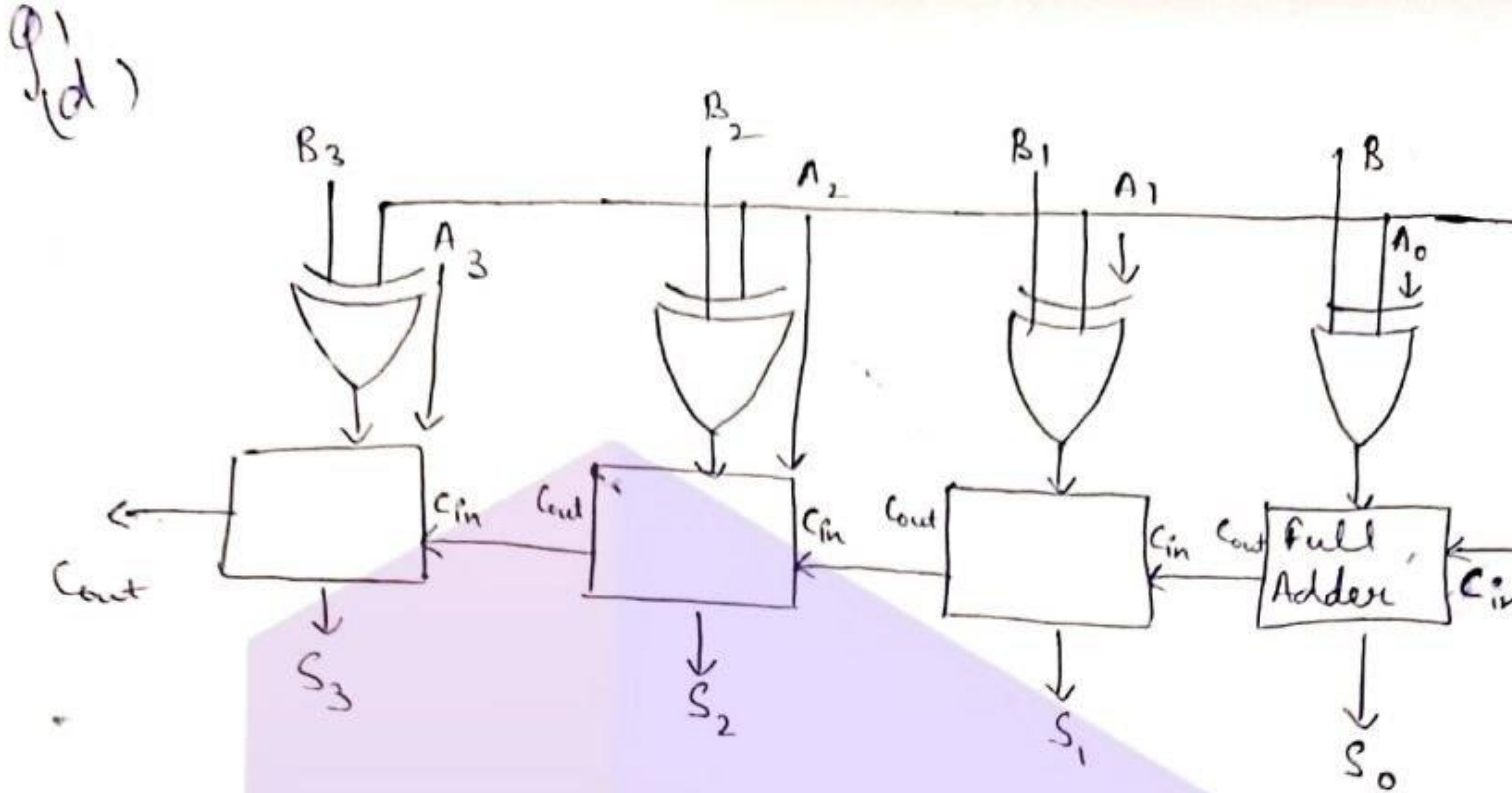
$$= (\overline{A \cdot B}) \cdot C$$

Now



(d) Consider the Adder-Subtractor circuit as shown in Figure 3.15 page 76 of Block 1. Explain how this circuit will perform subtraction (A-B), if the value of A is 0111 and B is 0001. You must list all the bit values including Cin and Cout and overflow, if any. (1 Mark)

Ans.



We know that the subtraction of A by B is obtained by taking 2's complement of B and adding it to A. The 2's complement of least significant pair of bits. Hence in this circuit 1's complement of B is obtained with the inverters (not gate) and 1 can be added to the sum through the input carry.

$$A(0111) \quad (A_3 \ A_2 \ A_1 \ A_0)$$

$$B(0001) \quad (B_3 \ B_2 \ B_1 \ B_0)$$

Calculate $A - B$

First find the 2's complement of B as $(0001 + 1) = 0010$ this is the value of $-B$ Now calculate $= A + (-B)$

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$A(A_3 A_2 A_1 A_0)$	0	1	1	1
$B(B_3 B_2 B_1 B_0)$	0	0	1	0
Sum ($S_3 S_2 S_1 S_0$)	1	0	0	1
	An FA gets input as $A_3 B_3$ & carry in & produce S_3	An FA gets input as $A_2 B_2$ & carry in & produce S_2	An FA gets input as $A_1 B_1$ and carry in & produce S_1	An FA gets input as $A_0 B_0$ & carry in and produce S_0

There is no extra carry at the end which is showing overflow in this circuit

(e) Explain the functioning of a 3×8 Decoder. You should draw its truth table and explain its logic diagram with the help of an example input. (2 Marks)

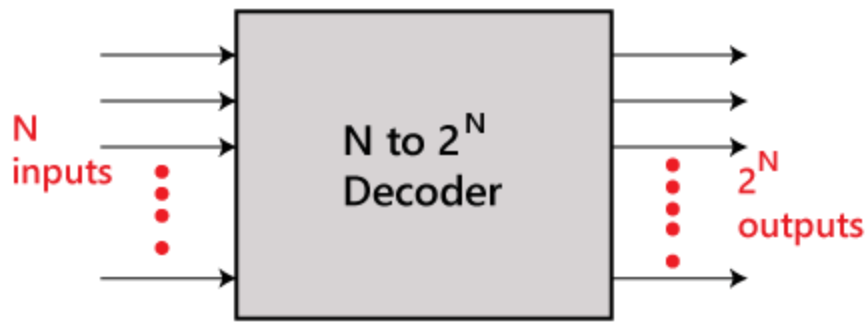
Ans.

Decoder:-

The combinational circuit that change the binary information into 2^N output lines is known as Decoders. The binary information is passed in the form of N input lines. The output lines define the 2^N -bit code for the binary information. In simple words, the Decoder performs the reverse operation of the Encoder. At a time, only one input line is activated for simplicity. The produced 2^N -bit output code is equivalent to the binary information.



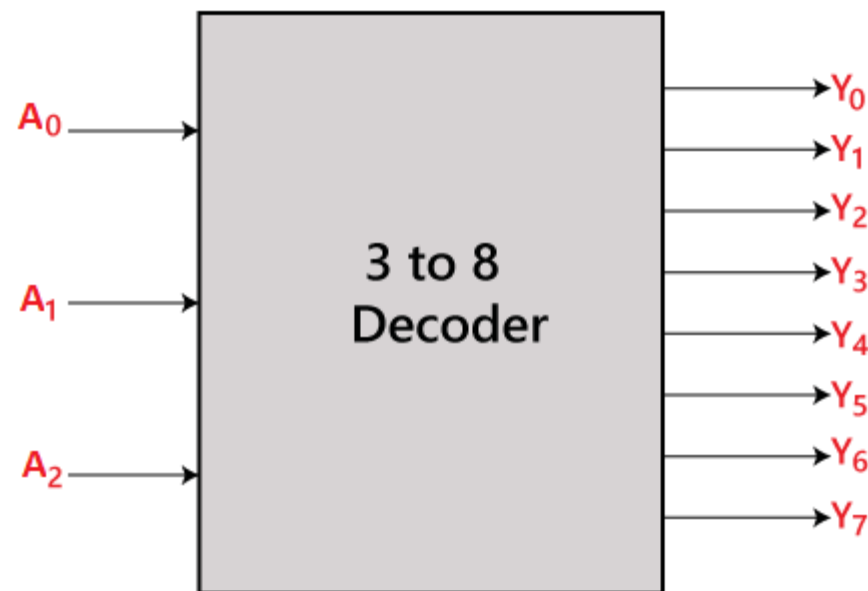
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3 to 8 line decoder:

The 3 to 8 line decoder is also known as Binary to Octal Decoder. In a 3 to 8 line decoder, there is a total of eight outputs, i.e., Y₀, Y₁, Y₂, Y₃, Y₄, Y₅, Y₆, and Y₇ and three outputs, i.e., A₀, A₁, and A₂. This circuit has an enable input 'E'. Just like 2 to 4 line decoder, when enable 'E' is set to 1, one of these four outputs will be 1. The block diagram and the truth table of the 3 to 8 line encoder are given below.

Block Diagram:



Truth Table:

Enable	INPUTS			Outputs							
E	A ₂	A ₁	A ₀	Y ₇	Y ₆	Y ₅	Y ₄	Y ₃	Y ₂	Y ₁	Y ₀
0	x	x	x	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	1	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

The logical expression of the term Y₀, Y₁, Y₂, Y₃, Y₄, Y₅, Y₆, and Y₇ is as follows:

$$Y_0 = A_0' \cdot A_1' \cdot A_2'$$

$$Y_1 = A_0 \cdot A_1' \cdot A_2'$$

$$Y_2 = A_0' \cdot A_1 \cdot A_2'$$



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$$Y_3 = A_0.A_1.A_2'$$

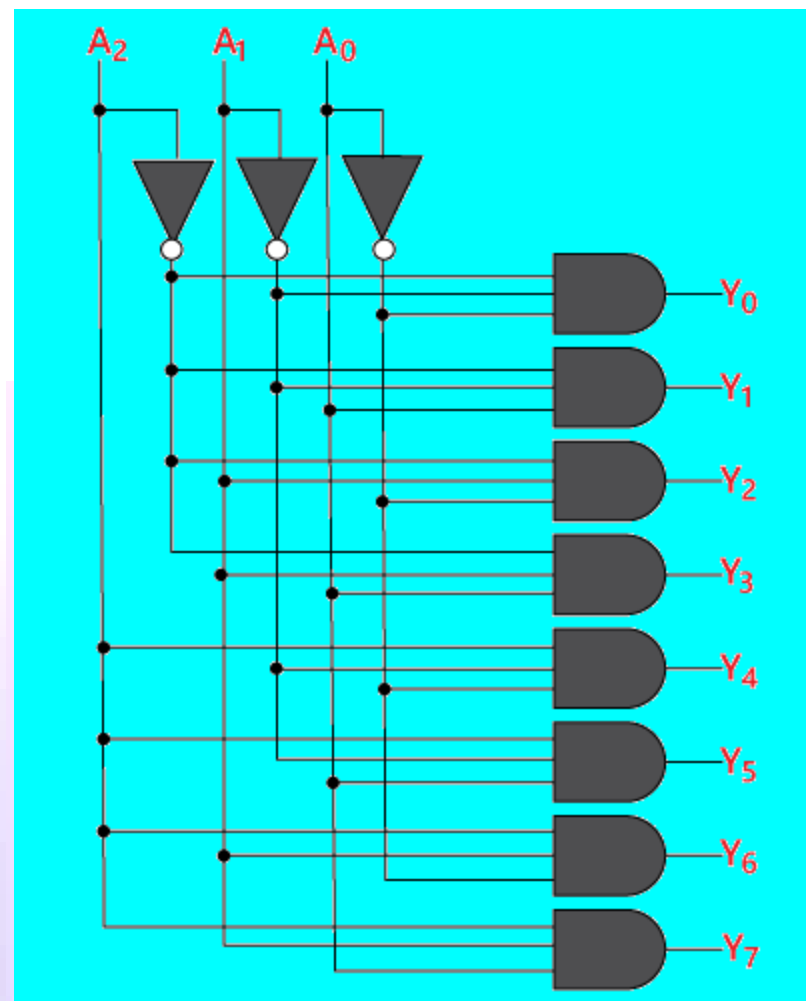
$$Y_4 = A_0'.A_1'.A_2$$

$$Y_5 = A_0.A_1'.A_2$$

$$Y_6 = A_0'.A_1.A_2$$

$$Y_7 = A_0.A_1.A_2$$

Logical circuit of the above expressions is given below:



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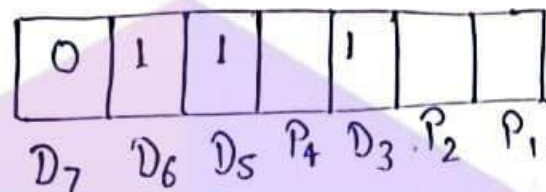
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(f) Assume that a source data value 0111 was received at a destination as 0101. Show how Hamming's Error-Correcting code bits will be appended to source data, so this error of one bit is identified and corrected at the destination. You may assume that transmission error occurs only in the source data and not the source parity bits. (2 Marks)

Ans:-

Q:- (f) Source data value $\Rightarrow 0111$

Apply the Hamming code and find out the parity bit



$$P_1 \Rightarrow D_3 = 1, D_5 = 1, D_7 = 0$$

$$P_1 \text{ [Even]} = 0$$

$$P_2 \Rightarrow D_3 = 1, D_6 = 1, D_7 = 0$$

$$P_2 \Rightarrow \text{[Even]} = 0$$

$$P_4 \Rightarrow D_5 = 1, D_6 = 1, D_7 = 0$$

$$P_4 \Rightarrow \text{[Even]} = 0$$

Put the P_1, P_2, P_4 value in Source Data

0 1 1 0 1 0 0

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Now Received the Data
= 0 1 0 1

⇒ 0 1 0 1, Add Parity Data in
the Data value,

0	1	0	0	1	0	0
D_7	D_6	D_5	P_4	D_3	P_2	P_1

Now find out the Error

$$P_1 \Rightarrow D_3 = 1, D_5 = 0, D_7 = 0$$

$$P_1 \text{ [ODD]} \Rightarrow 1 \quad (\because \text{change the value})$$

$$P_2 \Rightarrow D_3 = 1, D_6 = 1, D_7 = 0$$

$$P_2 \text{ [EVEN]} \Rightarrow 0 \quad (\because \text{No change})$$

$$P_4 \Rightarrow D_5 = 0, D_6 = 1, D_7 = 0$$

$$P_4 \text{ [ODD]} \Rightarrow 1 \quad (\because \text{change the value})$$

$$\text{So, } P_4, P_2, P_1 \Rightarrow 1, 0, 1$$

$$\Rightarrow 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0$$

$$= 4 + 0 + 1$$



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$$\Rightarrow 4+1 \Rightarrow 5$$

it means that 5th No of bit is Error bit, So change it

So Correct Data will be CAN \rightarrow

$$\Rightarrow 0, 1, \overset{\text{Error}}{\boxed{0}}, 0, 1, 0, 0$$

$$= 0, 1, 1, 0, 1, 0, 0$$

Remove the Parity bit

$$= 0111 \text{ (Correct Data)}$$

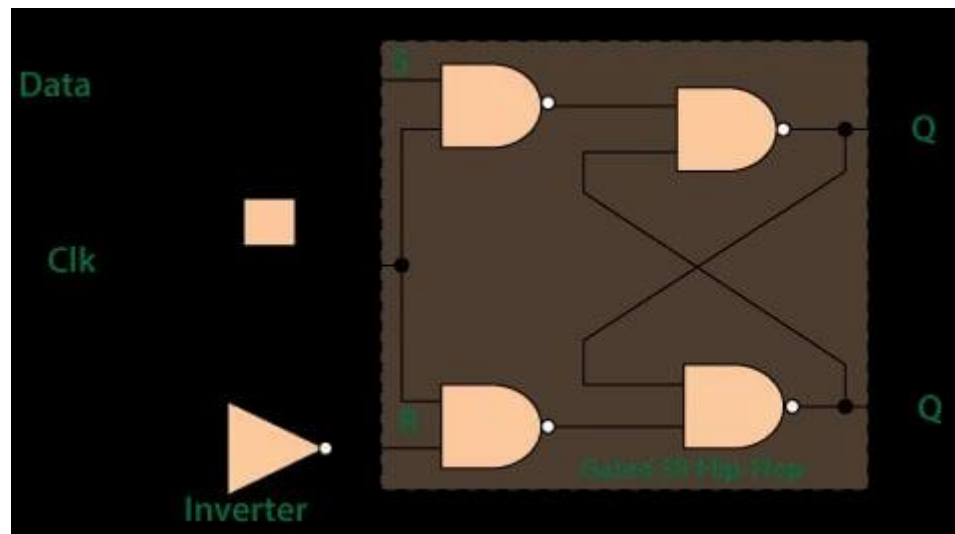
(g) Explain functioning of D flip flop with the help of a logic diagram and characteristic table. Also explain the excitation table of this flip-flop. (2 Marks)

Ans:-

Circuit Diagram for D flipflop:



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We know that the SR flip-flop requires two inputs, i.e., one to "SET" the output and another to "RESET" the output. By using an inverter, we can set and reset the outputs with only one input as now the two input signals complement each other. In SR flip flop, when both the inputs are 0, that state is no longer possible. It is an ambiguity that is removed by the complement in D-flip flop.

In D flip flop, the single input "D" is referred to as the "Data" input. When the data input is set to 1, the flip flop would be set, and when it is set to 0, the flip flop would change and become reset. However, this would be pointless since the output of the flip flop would always change on every pulse applied to this data input.

The "CLOCK" or "ENABLE" input is used to avoid this for isolating the data input from the flip flop's latching circuitry. When the clock input is set to true, the D input condition is only copied to the output Q. This forms the basis of another sequential device referred to as **D Flip Flop**.

When the clock input is set to 1, the "set" and "reset" inputs of the flip-flop are both set to 1. So it will not change the state and store the data present on its output before the clock transition occurred. In simple words, the output is "latched" at either 0 or 1.

Truth Table for the D-type Flip Flop

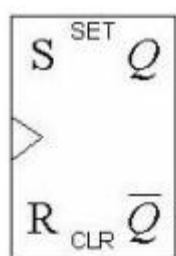
Clock	D	Q	Q'	Description
↓ » 0	X	Q	Q'	Memory no change
↑ » 1	0	0	1	Reset Q » 0
↑ » 1	1	1	0	Set Q » 1

(h) Explain the functioning of an edge triggered flip-flop and a 4 × 1 multiplexer with the help of a diagram of each. (2 Marks)

Ans:-

An edge-triggered flip-flop changes states either at the positive edge (rising edge) or at the negative edge (falling edge) of the clock pulse on the control input. The three basic types are introduced here: **S-R**, **J-K** and **D**.

Click on one the following types of flip-flop. Then its logic symbol will be shown on the left. Notice the small triangle, called the **dynamic input indicator**, is used to identify an edge-triggered flip-flop.



Positive edge-triggered (without bubble at Clock input):
S-R, **J-K**, and **D**.

Negative edge-triggered (with bubble at Clock input):
S-R, **J-K**, and **D**.

The S-R, J-K and D inputs are called synchronous inputs because data on these inputs are transferred to the flip-flop's output only on the triggering edge of the clock pulse. On the other hand, the direct set (SET) and clear (CLR) inputs are



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called **asynchronous inputs**, as they are inputs that affect the state of the flip-flop independent of the clock. For the synchronous operations to work properly, these asynchronous inputs must both be kept LOW.

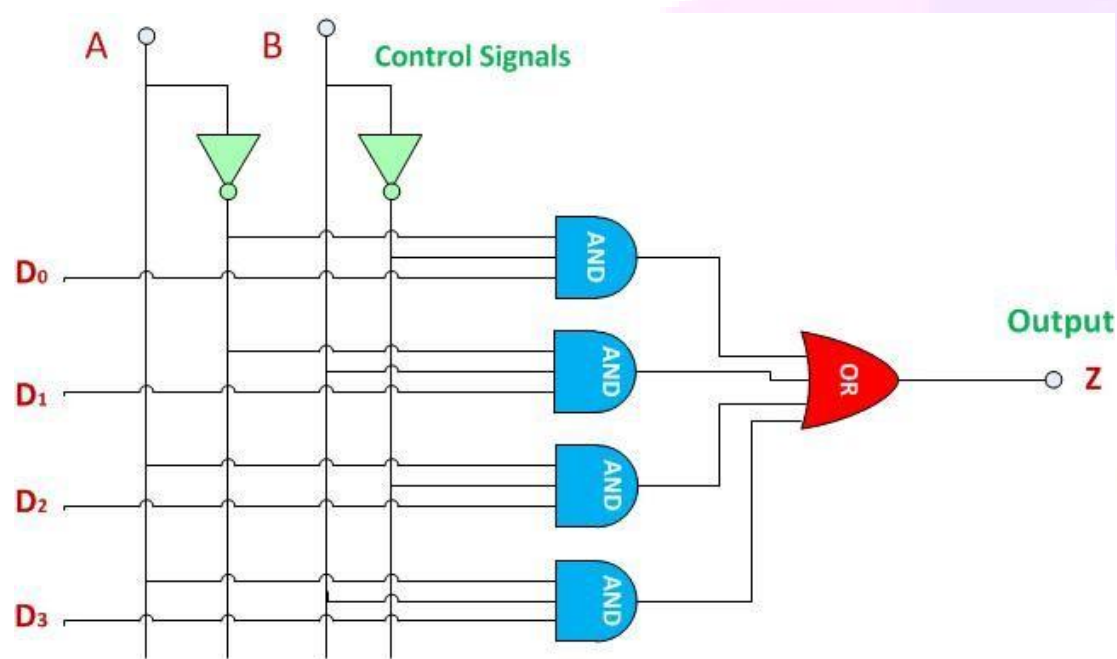
A multiplexer can be designed with various inputs according to our needs. If we have four inputs and we want to select a single one then we can use four-to-one (4:1) MUX. If we have 8 inputs we can design a multiplexer with 8 input lines, but the selection line should be in accordance with the above-mentioned equation.

In this article, we will discuss the designing of 4:1 MUX with the help of its circuit diagram, input line selection diagram and truth table.

Four-to-One Multiplexer

In 4:1 MUX, there will be 4 input lines and 1 output line. And to control which input should be selected out of these 4, we need 2 selection lines.

Thus, it is evident from the diagram below that D0, D1, D2 and D3 are the input lines and A, B are the two selection lines. The combination of binary numbers given as a selection line will determine the output of the MUX.



Four – To – One Multiplexer

Now, there will be 4 cases as described below:-

Case 1: When the selection line A represents 0 and selection line B also represents 0 then the input line which will be selected to pass from multiplexer will be D0. Thus, MUX will be a short circuit for input line D0 and will be open circuited for other input lines.

Case 2: When the selection line A represents 0 while selection line B represents 1, then the input line which will be selected will be D1. In this case, MUX will behave as a short circuit for input line D1 while it will behave as an open circuit for other input lines.

Case 3: When the selection line A is 1 and B is 0 then the input line D2 will be generated at the output. In this scenario, the MUX will allow only D2 to pass through it and other input will be blocked.

Case 4: When both the selection line represents 1, then the last input line will be selected i.e. D3. In this case, the MUX will allow the only D3 to pass through it and other input lines get blocked from passing through MUX.



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Truth table

Data Select Inputs		Input Selected	Input	Output
A	B	D	D	Z
0	0	D0	0 1	0 1
0	1	D1	0 1	0 1
1	0	D2	0 1	0 1
1	1	D3	0 1	0 1

Q2: (i) Represent $(-34.0625)_{10}$ and $(0.000000000125)_{10}$ in IEEE 754 single precision and double precision formats. (2 Marks)

$(-34.0625)_{10}$ in single

-34.0625

Most accurate representation = $-3.40625E1$

0xC2084000 = 11000010 00001000 01000000 00000000

Sign	Exponent	Mantissa
1	10000100	000100001000000000000000

$(0.000000000125)_{10}$ in single

0.000000000125

Most accurate representation = $1.25000001668928995002261217451E-11$

0x2D5BE6FF = 00101101 01011011 11100110 11111111

Sign	Exponent	Mantissa
0	01011010	101101111100110111111111

$(-34.0625)_{10}$ in IEEE 754 double

**Double
-34.0625**

**Most accurate
representation = -
3.40625E1**

Disclaimer/Note

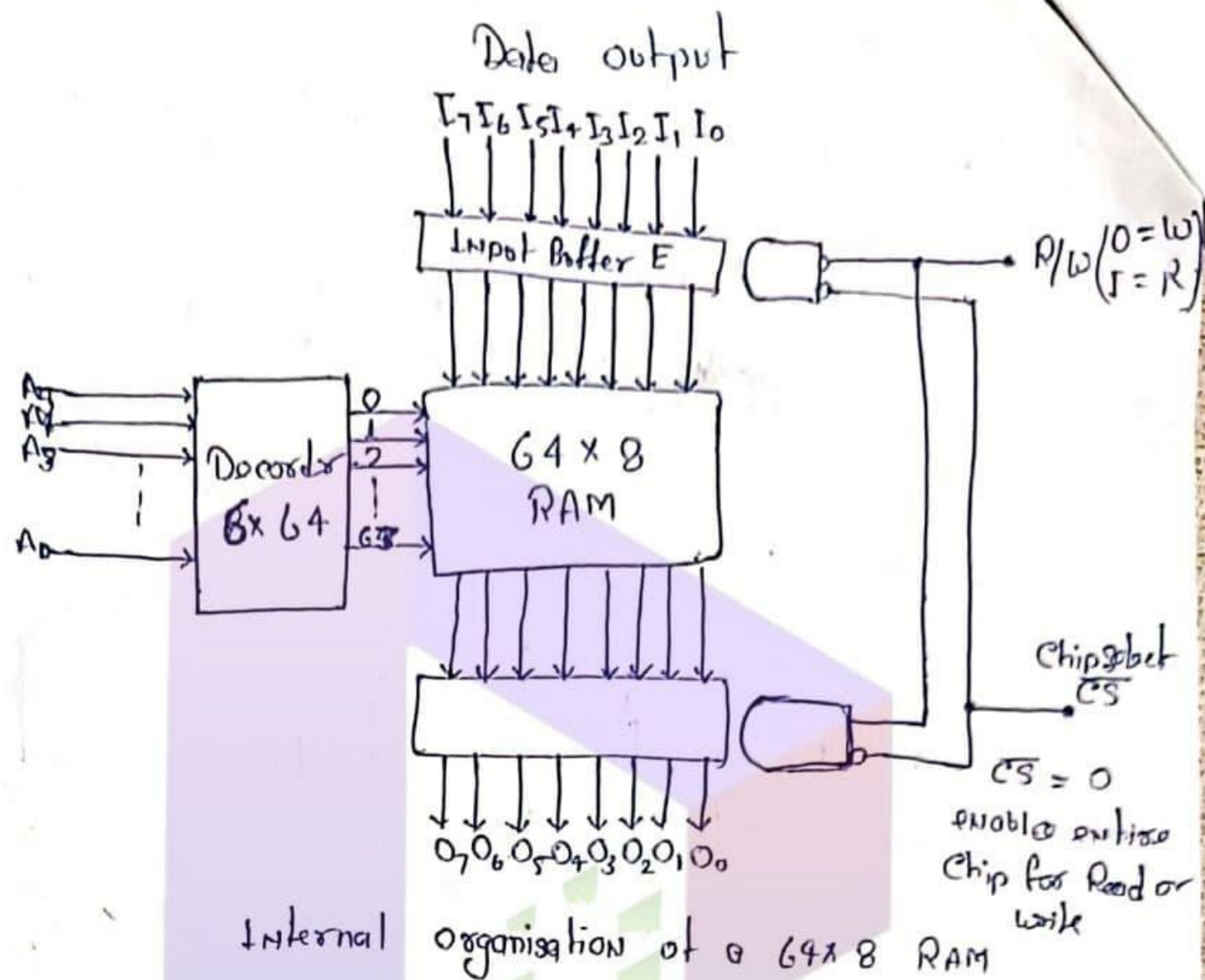
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(i) Ans According to the Diagram of a 64x8 RAM
input and output line = 8

(ii) According to the Diagram of a 64x8 RAM
Decoder is 6x64 whose 6 is input and
output 64, then the Address
 $2^6 = 64$, Address $\Rightarrow 6$ (line)

(b) A computer has 16 MB RAM with each memory word of 32 bits. It has cache memory having 512 blocks having a size of 128 bits (4 memory words). Show how the main memory address (CA30FB)h will be mapped to cache address, if

(i) Direct cache mapping is used

(ii) Associative cache mapping is used

(iii) Two way set associative cache mapping is used.

You should show the size of tag, index, main memory block address and offset in your answer.

Ans:-



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Data:

Main memory size = 16 MB = 216B = 2^{16} B = 216B

Cache memory size = 128B = 27B = 128B = 2^7 B = 128B = 27B

Block size = 512 = 512 = 512 block = 29 = 2^9 = 29

Number of sets = $29/22 = 27 = 2^9/2^2 = 2^7 = 29/22 = 27$

Here 7 would be the required for index

Number of bits for tag = 256

Blocks can be anywhere in the cache.

Size of cache = 7

Location of block 12 in cache = $12 \bmod 8 = 4$

Number of blocks in set = 2

Number of sets = 256

Number of bits for tag = $24 - (7 + 8) = 9$



(c) What is the need of I/O interface in a computer? What are the functions of I/O interface? Explain the structure of I/O interface with the help of a diagram. (3 Marks)

Just as the API provides a conformable way for applications to usage the resources of the computer system, a user interface (UI) brings structure to the interaction between a user and the computer.

Put merely, a user interface is the point of human-computer interaction and communication on a device, webpage, or app. This can consider display screens, keyboards, a mouse, and the appearance of a desktop. User interfaces enable users to efficaciously control the computer or device they are interacting with.

The OS provides a user interface (UI), an environment for the user to act with the machine. The UI is either graphical or text-based.

In the industrial design field of human-computer interaction, a user interface (UI) is the space where interactions between humans and machines occur.

The major functions of an I/O module are as follows:

1. Control and Timing
2. Processor Communication
3. Device communication
4. Data buffering
5. Error Detection

Control and Timing

This function is used for synchronizing the traffic flow between an external device and an internal resource. In order to understand how this function works, consider the following example wherein the transfer of data between an external device and a processor is controlled.

The following steps are involved in this process.

Step 1



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Examining I/O module to verify the status of an attached device.

Step 2

Returning the status of attached device.

Step 3

Requesting transfer of data by a processor to an I/O module using a command. This step can be performed only when the device is operational and can readily transmit.

Step 4

Acquiring a single unit of data from an external device.

Step 5

Transferring the data from an I/O module to the processor.

When a bus is used by the system, then every interaction occurred between a processor and an I/O module contains either one or more than one bus arbitration.

Processor Communication

This function performs the following operations:

Decoding commands

The commands are retrieved by I/O module from the processor and then transmitted onto the control bus as signals.

Example

Following are the commands which an I/O module of the disk drive can receive

- Write sector
- READ sector
- SCAN record ID
- SEEK track number

The commands SEEK track number and SCAN record ID contains a parameter which is transmitted on to the data bus.

Exchanging Data

The data is exchanged using a data bus between a processor and an I/O module.

Reporting status

It gives the knowledge regarding the status of an I/O module since the working of peripherals is quite slow.

Example

In few cases, the I/O module might not be ready to transfer the data to the processor, as it may be busy in executing the previous I/O command. Such a condition can be indicated using common status signals lie READY and BUSY.

Identifying Address

Every I/O device is associated with a unique address. Therefore, an I/O module has to identify the peripherals associated with it using their unique addresses.

Device Communication

This function contains data, commands and status information. An I/O module should be capable enough of performing this function.



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Data Buffering

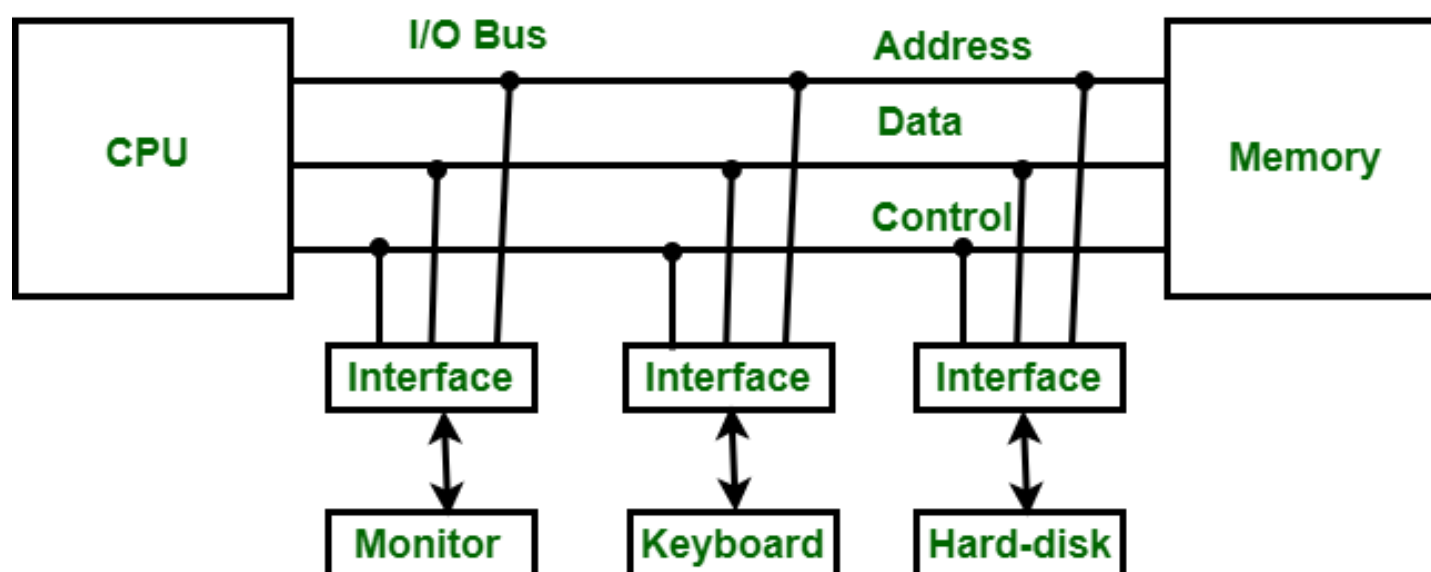
This function is one of the most prominent task of an I/O module. The rate at which the data is transferred in or out of the processor is very high. However, in case of peripheral devices, although the orders of magnitude is less, it still contains a wide range. The data which is retrieved from the processor is transmitted to an I/O module in an instantaneous break. Buffering of this data is done and it is transmitted at its data rate to a peripheral device. Whereas in the other case, buffering of data is done to avoid the tie up of memory in terms of a slow transfer operation. Therefore an I/O module should be capable of operating at the speeds of both memory and device. In case if the operating speed of an I/O device is greater than the speed of memory access, then the buffering operation required is performed by the I/O module.

Error Detection

This function of an I/O module is used for both detecting and reporting errors to a processor. Generally there are two classes of errors. The first class comprises of electrical and mechanical malfunctions, which are identified by the device. The second class includes the unintentional changes made to the bit pattern while it is being transferred from the device to an I/O module. This type of transmission errors can be identified using any form of error-detecting code.

Example

An IRA character code covers almost 7 bits of a byte, leaving 8th bit vacant. This eighth bit must be set in such a way that the total number of 1's in the byte is either an even parity or an odd parity. On receiving this byte the parity is checked by an I/O module for identifying the occurrence of any error.



(d) What is Interrupt driven I/O? Explain with the help of a flowchart. Differentiate between the working of Interrupt driven I/O and Programmed I/O. (2 Marks)

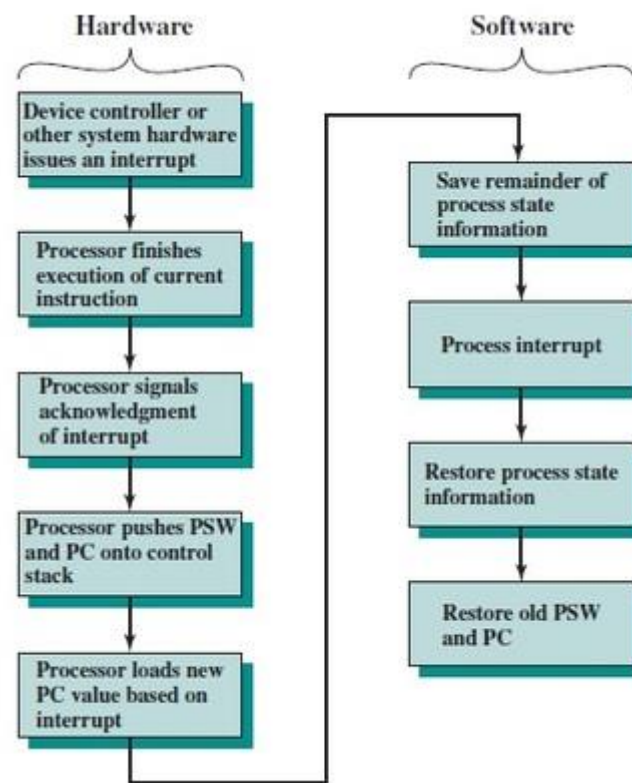
Ans: Interrupt driven I/O is an alternative scheme dealing with I/O. Interrupt I/O is a way of controlling input/output activity whereby a peripheral or terminal that needs to make or receive a data transfer sends a signal. This will cause a program interrupt to be set. At a time appropriate to the priority level of the I/O interrupt. Relative to the total interrupt system, the processors enter an interrupt service routine. The function of the routine will depend upon the system of interrupt levels and priorities that is implemented in the processor. The interrupt technique requires more complex hardware and software, but makes far more efficient use of the computer's time and capacities. Figure 2 shows the simple interrupt processing.

For **input**, the device interrupts the CPU when new data has arrived and is ready to be retrieved by the system processor. The actual actions to perform depend on whether the device uses I/O ports or memory mapping.

For **output**, the device delivers an interrupt either when it is ready to accept new data or to acknowledge a successful data transfer. Memory-mapped and DMA-capable devices usually generate interrupts to tell the system they are done with the buffer. Here the CPU works on its given tasks continuously. When an input is available, such as when someone types a key on the keyboard, then the CPU is interrupted from its work to take care of the input data. The CPU can work continuously on a task without checking the input devices, allowing the devices themselves to interrupt it as



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Basic Operations of Interrupt

1. CPU issues read command.
2. I/O module gets data from peripheral whilst CPU does other work.
3. I/O module interrupts CPU.
4. CPU requests data.
5. I/O module transfers data.

Interrupt Processing

1. A device driver initiates an I/O request on behalf of a process.
2. The device driver signals the I/O controller for the proper device, which initiates the requested I/O.
3. The device signals the I/O controller that is ready to retrieve input, the output is complete or that an error has been generated.
4. The CPU receives the interrupt signal on the interrupt-request line and transfer control over the interrupt handler routine.
5. The interrupt handler determines the cause of the interrupt, performs the necessary processing and executes a "return from" interrupt instruction.
6. The CPU returns to the execution state prior to the interrupt being signaled.

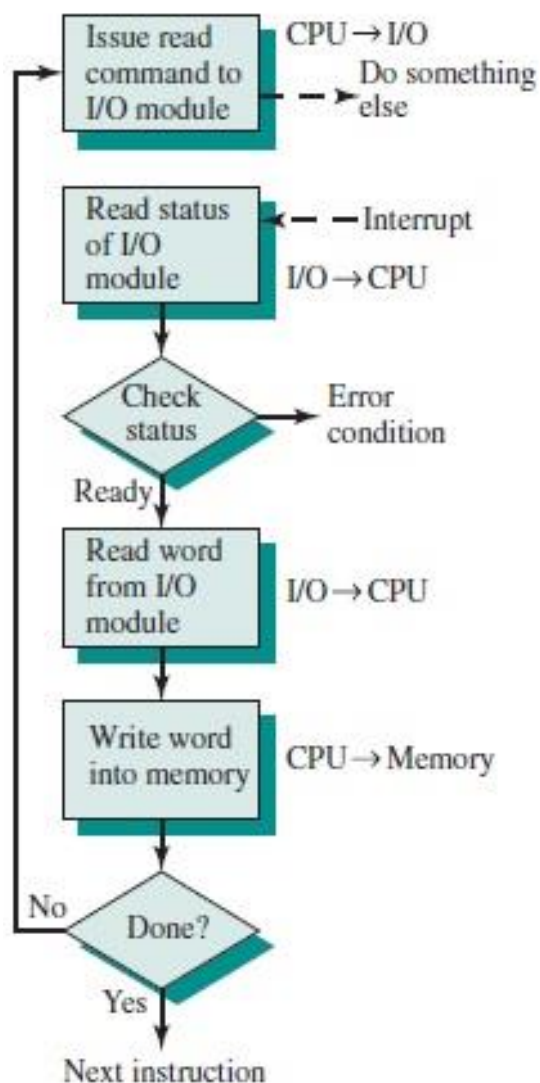
The CPU continues processing until the cycle begins again.

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Differentiate between the working of Interrupt driven I/O and Programmed I/O

Programmed I/O	Interrupt Initiated I/O
Data transfer is initiated by the means of instructions stored in the computer program. Whenever there is a request for I/O transfer the instructions are executed from the program.	The I/O transfer is initiated by the interrupt command issued to the CPU.
The CPU stays in the loop to know if the device is ready for transfer and has to continuously monitor the peripheral device.	There is no need for the CPU to stay in the loop as the interrupt command interrupts the CPU when the device is ready for data transfer.
This leads to the wastage of CPU cycles as CPU remains busy needlessly and thus the efficiency of system gets reduced.	The CPU cycles are not wasted as CPU continues with other work during this time and hence this method is more efficient.
CPU cannot do any work until the transfer is complete as it has to stay in the loop to continuously monitor the peripheral device.	CPU can do any other work until it is interrupted by the command indicating the readiness of device for data transfer
Its module is treated as a slow module.	Its module is faster than programmed I/O module.
It is quite easy to program and understand.	It can be tricky and complicated to understand if one uses low level language.
The performance of the system is severely degraded.	The performance of the system is enhanced to some extent.

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(e) Assume that a disk has 512 tracks, with each track having 128 sectors and each sector is of size 8 M bits. The cluster size in this system can be assumed to be as 8 sectors. A file having the name assignmentofsemester1.txt is of size 512 MB. Assume that disk has 128 free - continuous clusters. How can this file be allotted space on the disk? Also show the content of FAT after the space allocation to this file. You may make suitable assumptions. (4 Marks)

Ans.

$$\text{Cluster_size (M)} = \text{sector_size} \times \text{cluster_size (sector)}$$

$$= 8 \text{ M} \times 8 \text{ Sector}$$

$$= 64 \text{ M}$$

$$\text{File size (M)} / \text{Cluster size (M)} = 512 / 64 \text{ M}$$

$$= 4 \text{ Cluster-for-file}$$

$$\text{Cluster - one - track} = \text{cluster - each track} / \text{Cluster size (M)}$$

$$= 128 / 64 = 2 \text{ cluster on each track}$$

8 Contiguous clusters on consecutive track will be allocated for the file

Directory :

File Name : assignmentofsemester1.txt

First cluster no. of file 2

In fixed-size allocation, the storage space in a disk drive is partitioned into blocks of one single size. The host system to which the disk drive is attached allocates disk space by such fixed-size blocks. As many blocks as necessary are allocated to store a user file or record. All the blocks of the same file should be physically contiguous, or sequential, so as to gain the performance benefit of locality of access. FAT uses an index table stored on the device to identify chains of data storage areas associated with a file, the File Allocation Table. The FAT is statically allocated at the time of formatting and its table is a linked list of entries for each cluster, a contiguous area of disk storage.

(f) Explain the following, giving their uses and advantages/disadvantages. (Word limit for answer of each part is 50 words ONLY) (6 Marks)

(i) External Communication Interfaces of computers

Ans. Universal Serial Bus (USB) is the de facto interface for computer peripherals to communicate with the personal computers. The interface that saw the light of day around the mid-1990s was a joint effort of seven companies – Compaq, DEC, IBM, Intel,



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Microsoft, Nortel, and NEC. These companies were aiming to replace the then parallel ports and the external power chargers with a universal communication standard that could simplify data exchange and could double duty to supply power as well.

Any USB interface connects two devices where one device is connected as Host and the other device connects as peripheral. For example, when a USB flash drive (Pen drive) is inserted into USB port of a personal computer, the flash drive is the peripheral and a personal computer is the host device. By the "Host", here means that the data communication is managed by the host device with the help of relevant driver software. Many peripherals can be connected to a single host device. Even a single USB port can be extended to multiple USB ports using an extension hub.

Advantages of USB:

- **Ease of Use:** USB was for obvious reasons designed to be a simplified interface. The simplicity of the interface lies with following aspects:
 - **Single Interface for multiple devices:** The versatile nature of USB removes the complexity of different connector type and hardware requirements for each peripheral
 - **Auto-configuration:** The operating system of the host device only needs to install the USB device driver for once. Later whenever the peripheral device is plugged in, the driver is automatically loaded to configure the plugged in device. Usually, the device driver specific to any USB peripheral is automatically installed the first time device is connected with the host.
 - **Easy to expand:** Generally personal computers (Motherboards) have 3 or 4 USB ports. In case if more USB ports are required, USB hubs can be used to add external ports.
- **Compact Size:** USB sockets are small in dimensions as compared to RS232 or parallel ports.
- **No external power needed:** The USB interface was developed from the first day to double duty as DC power supply. Any host device through its USB port can supply 5V DC delivering 500mA (USB 1.0 and 2.0) to 900 mA (USB 3.0) to the peripheral.
- **Speed:** USB provides various speed modes which make it more efficient and swift compared to RS232 and parallel ports. It offers speed ranges from 1.5Mbit/s to 5Gbit/s. With the introduction of USB 3.1 in 2013, the speed has been increased to 10Gbit/s. It is also referred as Super Speed+.
- **Reliability:** The USB protocol can catch errors during data transfer and notify the transmitter to retransmit the data. The generic USB driver and specific driver software ensure an error-free data communication.
- **Low cost:** With its versatile nature and high demand, it has become inexpensive to manufacture USB supported devices as the manufacturing can be easily scaled. So the components, connector, and cable are also easily available at low cost.
- **Low power consumption:** The USB devices generally works on +5V and consumes current in Milliampere. During **Suspend mode**, the peripheral consumes 500 microamperes or less for USB 2.0 and 2.5 milliampere **or less for USB 3.0**.

Besides so many advantages there are some limitations which make USB ineffective for some task.

Limitations:

- **Speed:** With the introduction of USB 3.0, it is possible to achieve 5Gbits/sec. But it is still lower than Gigabit Ethernet. The FireWire 800(IEEE-1394b) is also a competitor for USB.
- **Peer to Peer Communication:** As per the USB standard, the communication takes place between the host and the peripheral. Two hosts cannot communicate directly to each other. Same is the case for a peripheral. On the other hand, interfaces like FireWire supports peripheral to peripheral communication. For overcoming this limitation, the USB introduced the concept of OTG (On The Go). The OTG device normally functions as peripheral, but it can also function as host with some limited capability when required.
- **Distance:** According to USB standards, the connecting cable can be as long as 5 meters, beyond which, USB hubs need to be used for expanding the connectivity.
- **Broadcasting:** Universal Serial Bus does not provide the broadcasting feature, only individual messages can be communicated between host and peripheral.

(ii) Keyboard technology



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Ans. The keyboard is the most common and widely used input device.



It is made up of buttons called 'keys'. The keys are arranged into sections:

- Alphabet keys
- Function or F keys (F1, F2, F3)
- Numeric keys (one set above the alphabet keys and a numeric keypad on the right)
- Arrow keys
- Command keys (insert, delete, home, end, page up/down)

Most keyboards are called 'QWERTY' keyboards. This name comes from the first six letters on the top row of the alphabet keys.

Using a keyboard for too long can lead to health problems such as repetitive strain injury (RSI).

To try to overcome this, different styles of keyboard have been developed, for example, the ergonomic keyboard. They are supposed to put your hands into a much more natural position than a traditional keyboard.

Advantages of keyboards	Disadvantages of keyboards
Most computers come with a keyboard supplied	It is easy to make mistakes when typing in data
People are used to using keyboards to enter data, they need very little training	If you can't touch type, it can be time consuming to enter data
A skilled typist can enter data very quickly	Keyboards are not suitable for creating diagrams
Specialist keyboards are available e.g. ergonomic, gaming keyboards	Disabled people often find keyboards difficult to use
	Excessive use can lead to health problems such as repetitive strain injury (R.S.I.)

(iii) DVD-ROM

Ans:-

Uses

As we know that DVD is a types of compact disk able to store large amount of data, especially high resolution audiovisual material so when you have comparing your data storage options, there is no one size fits at all approaches. At that time you may find DVD storage is perfect for your situation, while another user may find it inconvenient. Here this post gives the information about merits or advantages and disadvantages or demerits of DVD to better understand this topic.

Advantages of DVDs:

- Very large storage capacity.
- Increasing availability.
- It is easily available in every store.
- It is portable.
- High data stability.
- The DVD drive can read CDs.
- DVDs are now mass-produced so they are relatively cheap.
- Sound and picture quality is excellent which makes them suitable for sound and video.
- Price is dropping for both DVDs as well as for the DVD drives.

Disadvantages of DVDs:

- DVDs do not work in CD ROM drives.

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- It is not easy to change data.
- There is no single standard on DVD.
- When we have to use DVD, it has built-in copy protection and regional lockout.
- Still a relatively new technology so still expensive compared to CD-ROMs and VCR.
- It require a burning software to record some information to it.
- DVD uses digital compression. poorly compressed audio or video may be like fuzzy, harsh or vague and blocky.
- DVD doesn't fully support HDTV.
- They can be easily damaged by breaking or by some of the scratching.
- Some DVD players and drives can't read record-able DVDs.
- Some DVD players and drives can't read CDs.
- View a few players can play in reverse at normal speed.
- Variations and options such as like DVD audio, DVD-VR and DTS audio tracks are not supported by all players.
- Most of the DVD players and drives can't read DVD-RAM discs.

(iv) DMA

Ans. The term DMA stands for direct memory access. The hardware device used for direct memory access is called the DMA controller. DMA controller is a control unit, part of I/O device's interface circuit, which can transfer blocks of data between I/O devices and main memory with minimal intervention from the processor.

Advantages and Disadvantages of DMA Controller

The advantages and disadvantages of DMA controller include the following.

Advantages

- DMA speedups the memory operations by bypassing the involvement of the CPU.
- The work overload on the CPU decreases.
- For each transfer, only a few numbers of clock cycles are required

Disadvantages

- Cache coherence problem can be seen when DMA is used for data transfer.
- Increases the price of the system.

DMA (Direct Memory Access) controller is being used in graphics cards, network cards, sound cards etc... DMA is also used for intra-chip transfer in multi-core processors. Operating in one of its three modes, DMA can considerably reduce the load of the processor.

(v) Video Memory

VRAM (video RAM) refers to any type of random access memory (RAM) specifically used to store image data for a computer display. VRAM's purpose is to ensure the even and smooth execution of graphics display. It is most important in applications that display complex image textures or render polygon-based three-dimensional (3D) structures. People commonly use VRAM for applications such as video games or 3D graphic design programs. All types of VRAM are special arrangements of dynamic RAM (DRAM). VRAM is a buffer between the computer processor and the display and is often called the frame buffer. When images are to be sent to the display, they are first read by the processor as data from some form of main (non-video) RAM and then written to VRAM.

From VRAM, the data is sent as a digital signal via a digital video interface or high-definition multimedia interface, or HDMI, video port to a modern, flat-screen LED (light-emitting diode) display. If the display is an older cathode ray tube model, or if the modern display is connected by an older VGA (video graphics array) connector to the video card, the video signal is first converted by a RAM digital-to-analog converter into analog signals that are sent to the display.

Advantage :-



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1. Performance

2. Gaming

3. Memory Usage

4. Video Experience

Disadvantage:-

1. Cost

2. Speed

3. Overheating

4. Weight

5. Power Consumption

(vi) LCD Monitor Technology

A Liquid crystal display is a passive device, which means it doesn't produce any light to display characters, images, video and animations. But it simply alters the light traveling through it. The internal construction of LCD describes how the light altered when it passes through it in order to produce any characters, images etc.

LCD screens are an array of small segments called pixels, which can be manipulated for information displaying. Such displays have several layers, where two panels, made of glass material free of sodium and called substrate, play a crucial role. The substrate contains a thin layer of liquid crystals between them. The panels have flutes that direct the crystals, giving them a distinctive orientation. Flutes are parallel on each panel but are perpendicular between the two of them. Longitudinal flutes are obtained as a result of placing on the glass surface thin films of transparent plastic, which are then processed in a particular way. In contact with the flutes, the molecules are oriented identically in all the cells. The liquid crystal panel is illuminated by a light source, depending on where it is located, as the LCD panels operate on reflection or light transmission. The plane of polarization of the light beam is rotated by 90° as one panel passes. When an electric field appears, the molecules are partially aligned along it, and the angle of rotation of the plane of polarization of light becomes different from 90° . By producing screens using LCD monitor technology, the backlight of the monitor is used to output a color image so that light is generated at the back of the LCD monitors. It is necessary to be able to have a picture with good quality, even if it is dark. The color is obtained using three filters, which distinguish three principal components from the radiation of a white light source. By combining the three primary colors for each pixel of the screen, you can reproduce any color.

Disadvantages of LCD :

- Slightly more expensive than CRT
- Can't act as a portal to another dimension
- Suffer from a motion blur effect
- High refresh rate
- Like the backlight ages, it can change colors slightly
- The aspect ratio and resolution are fixed
- Not proficient at producing black or very dark grays colors
- Restricted viewing angles
- Slow response times

Q3:

(a) A uni-processor system, having single core, has 8 general purpose registers. The machine has 256-byte RAM. The

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size of every register and memory word is 16 bits. The computer uses fixed length instructions of size 16 bits each. An instruction of the machine can have only one operand, which can be either a direct memory operand or a register operand. Both these operands use direct addressing. An instruction of a machine consists of bits for operation code, one bit for addressing mode, and bits for memory operand or register operand. The machine has about 128 different operation codes. The addressing mode bits specifies addressing mode as:

Addressing mode bit Register Operand Memory Operand

0 - Direct

1 Direct -

The special purpose registers, which are other than general purpose registers, are - Program Counter (PC), Memory Address Register (MAR), Data Register (DR) and Flag registers (FR). The first register of the general-purpose registers can be used as Accumulator Register. The size of Integer operands on the machine may be assumed to be equal to the size of accumulator register. In order to execute instructions the machine has another special register called Instruction Register (IR) of size 16 bits, as each instruction is of this size. Perform the following tasks for the machine. (Make and state suitable assumptions, if any.)

(i) Design suitable instruction formats for the machine. Specify the size of different fields that are needed in the instruction format. Also indicate how many bits of the instructions are unused for this machine. Explain your design of instruction format. Also indicate the size of each register.

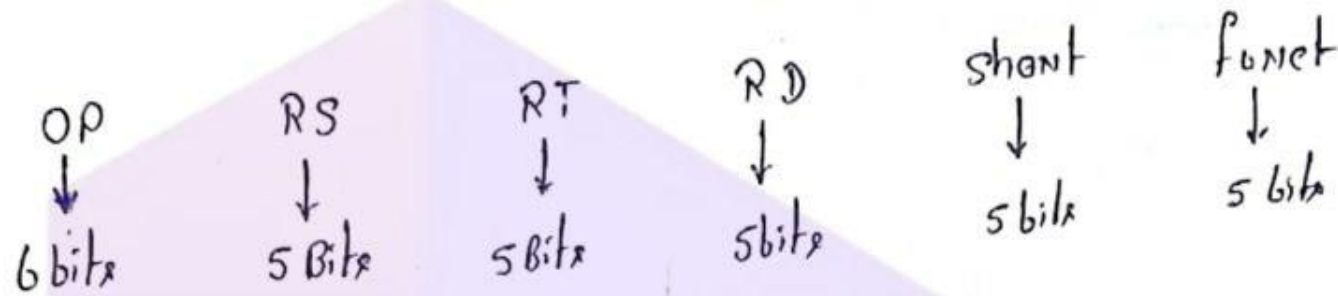
(ii) List at least two valid instructions; put some valid data values in registers and memory locations; and demonstrate examples of different addressing modes for this machine.

(iii) Assuming that the instructions are first fetched to Instruction Register (IR), memory operand is brought to DR register and result of an operation is stored in the Accumulator register; write and explain the sequence of micro-operations that are required to fetch and execute an instruction, which performs addition of register operand to the accumulator register. Make and state suitable assumptions, if any. (5 Marks)

Ans.

Q:-

Register type (R-Type) used for arithmetic instruction is as follows :-



Here,

OP :- operation code or opcode

RS :- The first Register Source operand

RT :- Second Register Source operand

RD :- Destination operand, stores the Result of the operation,

Shift :- used in case of shift operation

Funct :- This field selected the specific variable of the operation in the opcode field, and is sometime referred to as function, code-

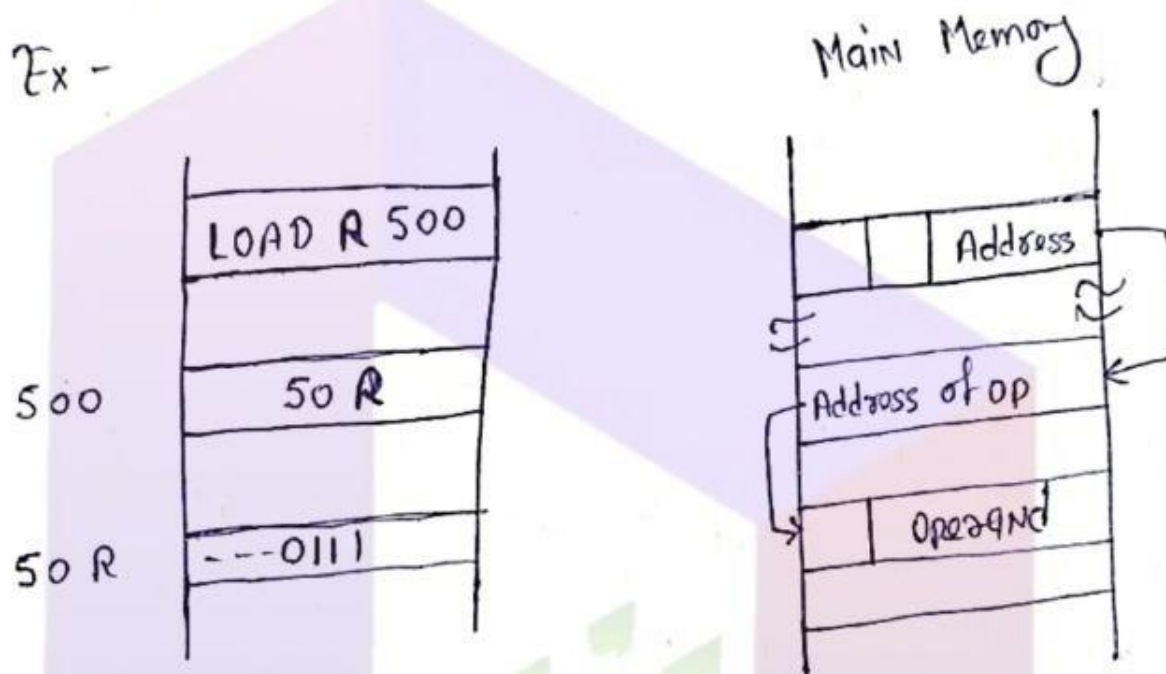
Here total $2^6 = 32$ operation can be coded for this machine as we have 6 bit as opcode size.

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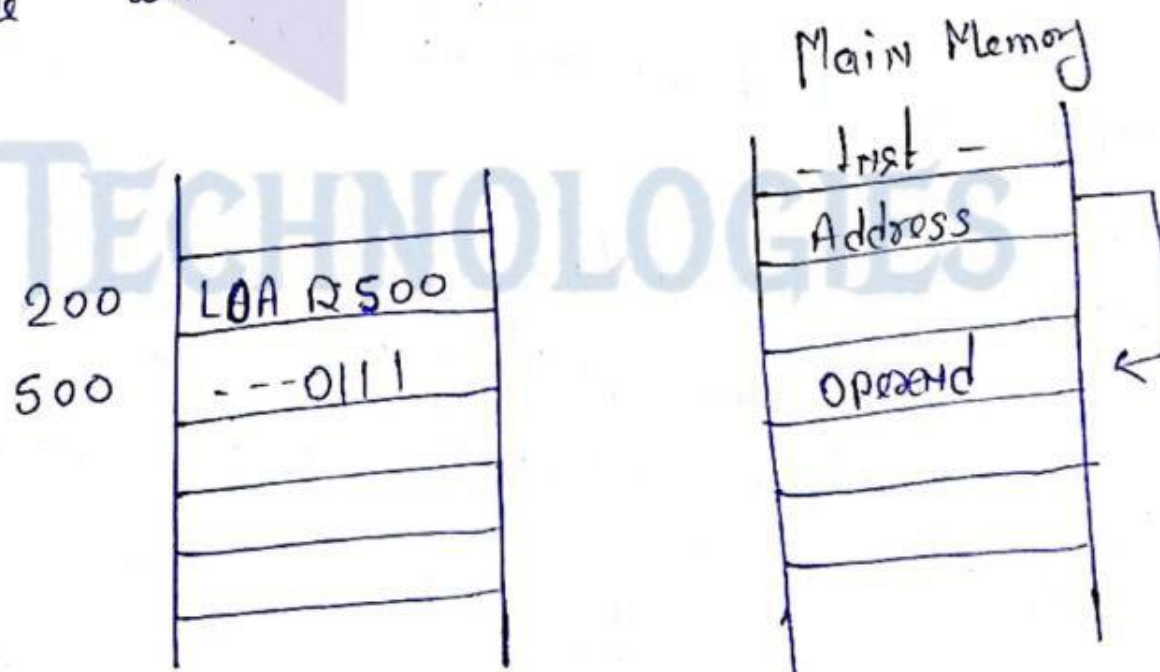
(ii) Indirect addressing mode and direct addressing mode can be used in the given machine.

When Addressing mode bit is '0' indirect addressing mode will be used

Ex -



When address mode bit is '1', direct addressing mode will be used.



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(iii) given that the inst are first fetched to Inst- , Register (IR) , memory operand is brought to DR Register , Indirect operation is brought to AC Register . Final Result of operation is stored in AC Register

Sequence of micro-operation for the given sequence will be as follows:-

$IR \leftarrow DR$

$MAR \leftarrow PC$

// Above inst- will transfer the address of PC to MR

$DR \leftarrow (MAR) , PC \leftarrow PC + 1$

MAR put its value on the address bus for main memory location .

$IR \leftarrow DR$



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So obtained is transferred from data Register to the Instruction Register for the ~~future~~ future processing

ADD AC DR

The DR and AC value are added and stored in Register AC.

(b) Assume that you have a machine, as shown in section 3.2.2 of Block 3 having the micro-operations given in Figure 10 on page 62 of Block 3. Consider that R1 and R2 both are 8 bit registers and contains 11110000 and 00110110 respectively. What will be the values of select inputs, carry-in input and result of operation (including carry out bit) if the following micro-operations are performed? (For each micro-operation you may assume the initial value of R1 and R2 as given above)

- (i) Decrement R1**
 - (ii) Add R1 and R2 with carry**
 - (iii) AND R1 and R2**
 - (iv) Shift right R1**
- Ans.**



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Q 3(b)

$$R_1 = 11110000$$

$$R_2 = 00110110$$

(i)

$$\begin{array}{r} \text{Decrement } R_1 = 11110000 \\ -1 \\ \hline 01110111 \end{array}$$

(ii) Add R_1 & R_2 with carry

$$R_1 = 11110000$$

$$R_2 = 00110110$$

$$\begin{array}{r} 10010010 \\ \downarrow \\ \text{Carry} \end{array}$$

(iii) R_1 AND R_2

$$11110000 \text{ AND } (2) \text{ } 00110110$$

$$\text{Ans} \rightarrow 00110000$$

(iv) Shift Right R_1

$$11110000$$

Number of bit to shift (Assume) = 1

$$\text{Ans} \rightarrow 1111000$$



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(c) Consider that an instruction pipeline has only three stages namely instruction fetch and decode (IFD), Operand Fetch (OF) and Instruction execute and store results (IES). Draw an instruction pipeline diagram showing execution of 5 sequential instructions. What are the problems of this instruction pipelining? (3 Marks)

Ans:-

	Timing ----->						
	1	2	3	4	5	6	7
Instruction 0	IFD	OF	IES				
Instruction 1		IFD	OF	IES			
Instruction 2			IFD	OF	IES		
Instruction 3				IFD	OF	IES	
Instruction 4					IFD	OF	IES

If these Three stages are not of equal duration, there will be some waiting involved at various pipeline stages. Another difficulty is the conditional branch instruction, which can invalidate several instruction fetches. A similar unpredictable event is an interrupt.

(d) Explain the functioning of Wilkes control unit with the help of a diagram. Also differentiate between Hardwired control and micro-programmed control. (2 Marks)

Ans. Prof. M. V. Wilkes of the Cambridge University Mathematical Laboratory coined the term microprogramming in 1951. He provided a systematic alternative procedure for designing the control unit of a digital computer. During instruction executing a machine instruction, a sequence of transformations and transfer of information from one register in the processor to another take place. These were also called the micro operations. Because of the analogy between the execution of individual steps in a machine instruction to the execution of the individual instruction in a program, Wilkes introduced the concept of microprogramming. The Wilkes control unit replaces the sequential and combinational circuits of hardwired control unit by a simple control unit in conjunction with a storage unit that stores the sequence of steps of instruction that is a micro-program.

In Wilkes microinstruction has two major components:

- Control field which indicates the control lines which are to be activated and
- Address field, which provides the address of the next microinstruction to be executed.

The figure 4 below is an example of Wilkes control unit design

The figure 4 below is an example of Wilkes control unit design.

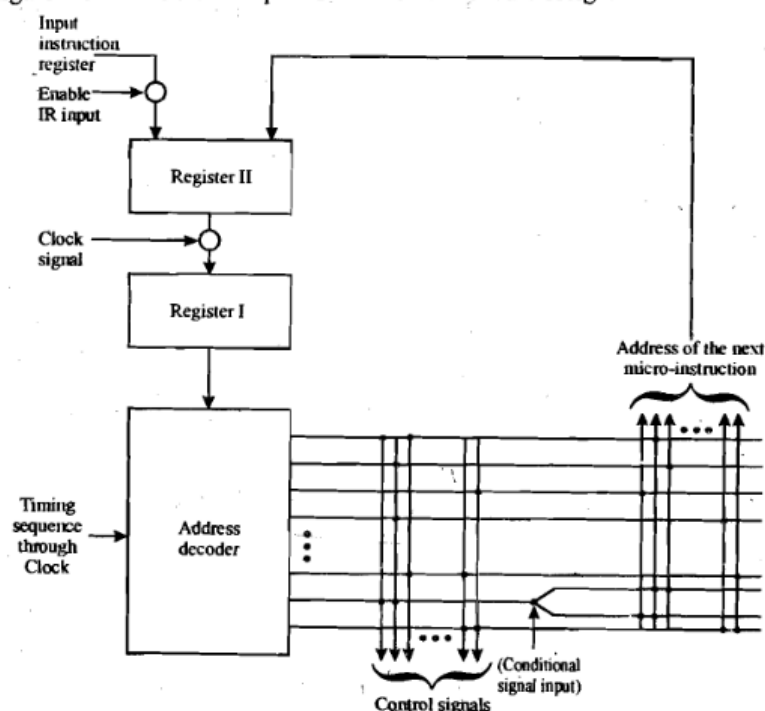


Figure 4: Wilkes Control Unit

The control memory in Wilkes control is organized, as a PLA's like matrix made of diodes. This is partial matrix and consists of two components, the control signals and the address of the next micro-instruction. The register I contains the address of the next micro-instruction that is one step of instruction execution, for example T I in M I or T2 in M2 etc. as in Figure 2. On decoding the control signals are generated that cause execution of micro-operation@) of that step. In addition, the control unit indicates the address of the next micro-operation which gets loaded through register I1 to register I. Register I can also be loaded by register I1 and "enable IR input" control signal. Thrs will pass the address of first micro-instruction of execute cycle. During a machine

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cycle one row of the matrix is activated. The first part of the row generates the control signals that control the operations of the processor. The second part generates the address of the row to be selected in the next machine cycle.

At the beginning of the cycle, the address of the row to be selected is contained in register I. This address is the input to the decoder, which is activated by a clock pulse.

This activates the row of the control matrix. The two-register arrangement is needed, as the decoder is a combinational circuit; with only one register, the output would become the input during a cycle. This may be an unstable condition due to repetitive loop.

Hardwired Control Unit	Microprogrammed Control Unit
Hardwired control unit generates the control signals needed for the processor using logic circuits	Microprogrammed control unit generates the control signals with the help of micro instructions stored in control memory
Hardwired control unit is faster when compared to microprogrammed control unit as the required control signals are generated with the help of hardware	This is slower than the other as micro instructions are used for generating signals here
Difficult to modify as the control signals that need to be generated are hard wired	Easy to modify as the modification need to be done only at the instruction level
More costlier as everything has to be realized in terms of logic gates	Less costlier than hardwired control as only micro instructions are used for generating control signals
It cannot handle complex instructions as the circuit design for it becomes complex	It can handle complex instructions
Only limited number of instructions are used due to the hardware implementation	Control signals for many instructions can be generated
Used in computer that makes use of Reduced Instruction Set Computers(RISC)	Used in computer that makes use of Complex Instruction Set Computers(CISC)

(e) Explain the characteristics of a RISC machine. RISC machines, in general, have large register file. How can this register file be used for parameter passing? Explain with the help of a diagram. What are the advantages of using instruction pipelining in a RISC processor? (3 Marks)

Ans. Reduced Instruction Set Architecture (RISC) -

The main idea behind is to make hardware simpler by using an instruction set composed of a few basic steps for loading, evaluating, and storing operations just like a load command will load data, store command will store the data.

RISC: Reduce the cycles per instruction at the cost of the number of instructions per program.

In general, the register storage is faster than the main memory and the cache. Also the register addressing uses much shorter addresses than the addresses for main memory and the cache. However, the numbers of registers in a machine are less as generally the same chip contains the ALU and control unit. Thus, a strategy is needed that will optimize the register use and, thus, allow the most frequently accessed operands to be kept in registers in order to minimize register-memory operations. Such optimisation can either be entrusted to an optimising compiler, which requires techniques for program analysis; or we can follow some hardware related techniques.

The hardware approach will require the use of more registers so that more variables can be held in registers for longer periods of time, This technique is used in RISC machines. On the face of it the use of a large set of registers should lead to fewer memory accesses, however in general about 32 registers were considered optimum. So how does this large register file further optimize the program execution?

Since most operand references are to local variables of a function in C they are the obvious choice for storing in registers. Some registers can also be used for global variables. However, the problem here is that the program follows function call - return so the local variables are related to most recent local function, in addition this call - return expects saving the context of calling program and return address. This also requires parameter passing on call. On return, from a call the variables of the calling program must be restored and the results must be passed back to the calling program.

RISC register file provides a support for such call- returns with the help of register windows. Register files are broken into multiple small sets of registers and assigned to a different function. A function call automatically changes each of these sets. The use from

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one fixed size window of registers to another, rather than saving registers in memory as done in CISC. Windows for adjacent procedures are overlapped. This feature allows parameter passing without naming the variables at all.

Instruction pipelining is often used to enhance performance. Let us consider this in the context of RISC architecture. In RISC machines most of the operations are register-to-register. Therefore, the instructions can be executed in two phases:

F: Instruction Fetch to get the instruction.

E: Instruction Execute on register operands and store the results in register. In general, the memory access in RISC is performed through LOAD and STORE operations.

For such instructions the following steps may be needed:

F: Instruction Fetch to get the instruction

E: Effective address calculation for the desired memory operand

D: Memory to register or register to memory data transfer through bus.

Let us explain pipelining in RISC with an example program execution sample. Take the following program (R indicates register).

```

LOAD RA      (Load from memory location A)
LOAD RB      (Load from memory location B)
ADD RC, RA, RB  (RC = RA + RB)
SUB RD, RA, RB  (RD = RA - RB)
MUL RE, RC, RD  (RE = RC × RD)
STOR RE      (Store in memory location C)
Return to main.
  
```

Load R _A ← M(A)	F	E	D														
Load R _B ← M(B)				F	E	D											
Add R _C ← R _A + R _B							F	E									
Sub R _D ← R _A - R _B								F	E								
Mul R _E ← R _C × R _D									F	E							
Stor R _E → M(C)											F	E	D				
Return														F	E		
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

Characteristic of RISC –

1. Simpler instruction, hence simple instruction decoding.
2. Instruction comes under size of one word.
3. Instruction takes a single clock cycle to get executed.
4. More number of general-purpose registers.
5. Simple Addressing Modes.
6. Less Data types.
7. Pipeline can be achieved.

Q4:

(a) Write a program using 8086 assembly Language (with proper comments) that accepts a two-digit input from the keyboard, converts it into an equivalent binary number and subtracts this value from every element of an array of length ten bytes. Assume that the array is stored in the memory. Make suitable assumptions, if any. (7 Marks)

Ans:-

DATA SEGMENT



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array DB 21, 22, 23, 24, 25, 26, 27, 28, 29, 20

MSG_ENTER DB 10,13,"Enter TWO number: \$"

DATA ENDS

CODE SEGMENT

ASSUME DS:DATA,CS:CODE

START:

MOV AX,DATA

MOV DS,AX

MOV ES,AX

LEA DX,MSG_ENTER ; "Enter ..."

MOV AH,9 ; Display string

INT 21H

MOV AH,1 ; Waiting for a key press

INT 21H

; AL = ASCII code of key pressed

SUB AL, 30H ; AL NUMBER

XOR DX, DX ; DX = 0

mov DL,AL ; first digit

MOV AH,1 ; Waiting for a key press

INT 21H

; AL = ASCII code of key pressed

SUB AL,30H ; AL NUMBER

XOR BX, BX

mov BL,AL ; second digit

; Calculate tens

XOR AX,AX ; AX = 0 before multiplication AX=0

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MOV CL,10

MOV AL, DL ; tens

MUL CL ; <number of tens>*10

MOV DX,AX ; tens

ADD DX,BX ; RESULT

LEA SI,array ; address of array

MOV CX, 10 ; counter

L1:

MOV AL,[SI] ; AL = array[i]

SUB AL, DL ; array[i] - number

MOV [SI],AL ; save

INC SI ; next address in array

LOOP L1

mov ah, 4ch ; exit

int 21h

CODE ENDS

END START

(b) Write a NEAR subroutine using 8086 assembly Language (with proper comments) that returns the smallest byte value in a byte array of length 5-bytes. The array is declared in the calling program and the base address of the array is passed to the subroutine in the stack. You should write both the calling program and subroutine. (7 Marks)

Ans.

; 8086 assembly Language

; DosBox

org 100h

.model small

.stack 200h

.data

array DB 10,3,2,5,9 ; a byte array of length 5-bytes

.code

start:

mov ax,@data ;set segment DATA

mov ds,ax



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mov es,ax

; the base address of the array is passed

; to the subroutine in the stack

mov dx, offset array

PUSH DX

CALL My_PROC

NOP

mov ah, 4ch

int 21h ; exit

;*****

; PROC My_PROC

; Input: array address in stack

; Output: AL Smallest byte value

;*****

My_PROC PROC NEAR

ADD SP, 2

POP SI ; array address

MOV AL, [SI] ; Smallest = array[0]

MOV CX, 4 ; counter

L1:

INC SI ; address of next byte

MOV AH, [SI] ; AH = array[i]

CMP AH,AL ; compare Smallest and array[i]

JNC NEXT ; IF array[i] > Smallest goto NEXT

MOV AL, AH ; ELSE AL = new Smallest

NEXT:

LOOP L1 ; next loop

PUSH AX ; AL = Smallest

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SUB SP, 2 ; restore stack

END_PROC:

RET

My_PROC ENDP

end start

(c) Explain the following in the context of 8086 Microprocessor : (6 Marks)

(i) Physical address calculation in code and data segment

8086 has a concept of Memory Segmentation. It is a method where the whole memory is segmented (divided) into smaller parts called segments. These segments are

- Code Segment (CS)
- Stack Segment (SS)
- Data Segment (DS)
- Extra Segment (ES)

Each Segment has a corresponding 16-bit Segment Register which holds the Base Address (starting Address) of the Segment. At any given time, 8086 can address 16-bit x 64KB = 256 KB of memory chunk out of 1MB.

Assume that:-

8086 has 20bit address line. So the maximum value of address that can be addressed by 8086 is $2^{20} = 1\text{MB}$. So 8086 can address the locations ranging between 00000 H to FFFFF H. This 1MB memory is divided into 16 logical segments, each with a memory of 64KB.

To locate any address in the memory bank, it needs the Physical address of that memory location. It cannot get the 20-bit Physical address using the 8086 Address Line or 16-bit Segment Registers alone.

In order to access memory location, you cannot pass 20-bit address directly to the processor. You need to tell the 16-bit address with respect to the segment. This 16-bit address with respect to the part (segment of 64KB) of the memory bank is called the offset.

So, Physical Address = Base Address + Offset.

Suppose the Data Segment holds the Base Address as 1000h and the data you need is present in the 0020h memory location (Offset) of the Data Segment. The calculation of the actual address is done as follows.

1. Left shift the 16-bit address present in the segment register by 4-bits

0001 0000 0000 0000 (0000)

2. Add the 16-bit offset address to this shifted base address

0001 0000 0000 0000 0000

+ 0000 0000 0010 0000

0001 0000 0000 0010 0000

So the actual address turns out to be 10020h.

At any point of time we can change the base address of the segment registers and use the memory locations in those segments using the offset.

(ii) Interrupt vector table and its use

An 8086 is interrupted by some condition produced in the 8086 by the execution of an instruction. For example divide by zero : Program execution will automatically be interrupted if you attempt to divide an operand by zero.

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At the end of each instruction cycle 8086 Interrupts checks to see if there is any interrupt request. If so, 8086 responds to the interrupt by performing series of actions (Refer Fig. 9.1).

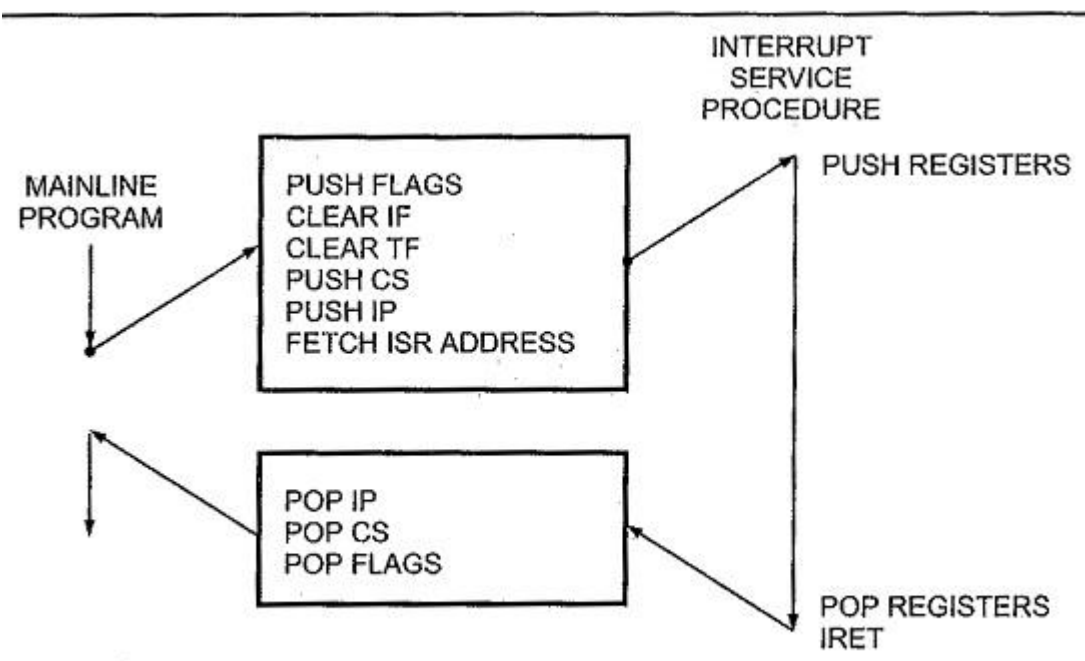
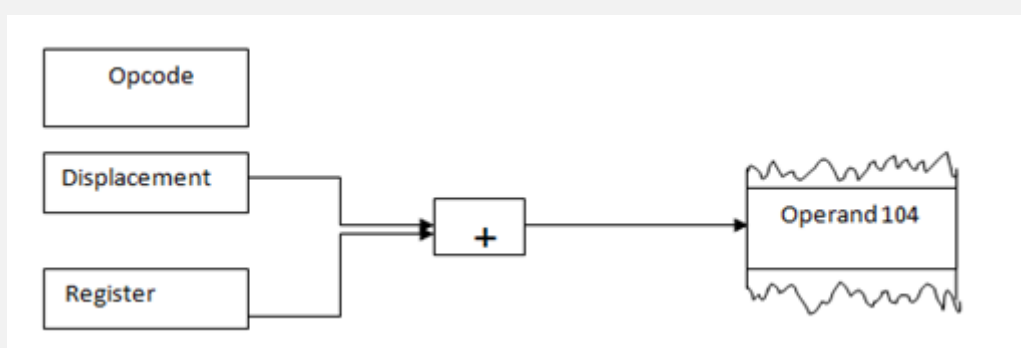


Fig. 9.1 8086 interrupt response

1. It decrements stack pointer by 2 and pushes the flag register on the stack..
2. It disables the INTR interrupt input by clearing the interrupt flag in the flag
3. It resets the trap flag in the flag register.
4. It decrements stack pointer by 2 and pushes the current code segment register contents on the stack.
5. It decrements stack pointer by 2 and pushes the current instruction pointer contents on the stack.
6. It does an indirect far jump at the start of the procedure by loading the CS and IP values for the start of the interrupt service routine (ISR).

(iii) Based Indexed addressing mode with the help of an example

Based Addressing Mode



In this addressing mode, the offset address of the operand is given by the sum of contents of the BX/BP registers and 8-bit/16-bit displacement.

Example: MOV DX, [BX+04],

ADD CL, [BX+08]