UNIVERSITY *of* LIMERICK

OLLSCOIL LUIMNIGH

COLLEGE *of* INFORMATICS *and* ELECTRONICS

Department of Computer Science
and Information Systems

End-of-Semester Assessment Paper

Academic Year:	2006/2007	Semester:	Autumn
Module Title:	Computer Organisation 1	Module Code:	CS4211
Duration of Exam:	2½ Hours	Percent of Total Marks:	80
Lecturer:	Dave Burns	Paper marked out of :	80

Instructions to Candidates:

Section 1. Answer all Multiple Choice questions . 10 Multiple Choice Questions on a separate sheet. All questions in Section 1 are compulsory. 2 marks for each question. Circle the answer that you think is appropriate. If you wish to change your answer, cross out the circled answer and circle your new choice.

Section 2. Attempt 3 of the 4 questions.

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Q1. Convert –27.625 to a 32-bit floating point binary representation for a computer. (6 marks)

Show the layout of a 16-bit integer initialised with the value 69. What is the effect of performing a left shift three times on the integer, followed by a negation? Express your answers in both binary and Hex. (4 marks)

A 32-bit word computer displays a memory address 0006ce28. How many words are in memory between this address and address 008084c? (4 marks)

Given that the hexadecimal representations for ASCII codes are 41 for A, 5A for Z, and 61 for a, 7A for z, describe how you could convert an upper-case character to a lower case using AND or OR together with a suitable value. (6 marks)

Section 2 continued

Q2.

a. Show, by means of a truth table, that xy'. (x + y + z) = x.y' (3 marks)

Simplify the following Boolean expressions:

i. ~ (X'.Y + X'.Y')
ii. AB + ABC + AB' + A'BC (4 marks)

b. By drawing up a truth table, show that the sum S from the Full Adder (that is, the sum of bits a, b and p, where p is the carry in from a previous addition), is given by:

S = p'(ab' + a'b) + p (ab + a'b') (6 marks)

By applying de Morgan's Law to the second term above, show that

S = p'(ab' + a'b) + p'. ~(ab' + a'b) (4 marks)

Given that Sum(1/2 Adder), the Sum for the Half Adder (for bits x and y) is x EXOR y, show that the Sum for the Full Adder can be written in terms of p and Sum(1/2 Adder). (3 marks)

3. Write brief notes on 4 of the following:

The program Process
LAN using Ethernet bus topology
Transformation of a high-level source program to an executable object program
RISC v CISC architecture
The layout of computer memory, including operating system, I/O, user area and system stack.

(20 marks)

4a. Describe the Instruction Fetch and Execute cycle, with reference to the assembly language instruction:

add x, y // Add the contents of memory location x to the contents of location y
(7 marks)

b. Show how the C++ instruction **S = a + b* (x – y) ;** could be implemented in a one-address assembly language using an accumulator. (6 marks)

c. Describe one of the Intel Processor range with regard to features such as registers, ALU, cache, and clock speed. (7 marks)