UNIVERSITY *of* LIMERICK

OLLSCOIL LUIMNIGH

COLLEGE *of* INFORMATICS *and* ELECTRONICS

Department of Computer Science
and Information Systems

End-of-Semester Assessment Paper

Academic Year:	2006/07	Semester:	Spring
Module Title:	Computer Organisation 2	Module Code:	CS4212
Duration of Exam:	2½ Hours	Percent of Total Marks:	80
Lecturer(s):	Dr M. Eaton	Paper marked out of :	80

Instructions to Candidates:

- Answer any FOUR questions
- All questions carry equal marks
- 20% midterm 80% this exam

Q1. a) Devise an instruction set for a simple hypothetical computer (SHC) which can load its accumulator from one of 100 available memory locations numbered 00-99, can store the contents of it's accumulator in any memory location, and can perform the operations of addition, subtraction and multiplication. Each memory location will be four decimal digits wide and it should also be possible to perform conditional and unconditional branching.

Give the opcode and mnemonic for each instruction and explain the overall operation of your computer.

8 Marks

b) Using the technique of self modifying code, write a program for your SHC to add together the contents of the thirty memory locations 00-29. The resulting sum should then be multiplied by the contents of memory location 30 to obtain the final result, which should be stored in location 31.

Ensure that your program is adequately commented throughout.

12 Marks

Q2. a) Briefly describe the ASM (Algorithmic State Machine) method for describing state machines

4 Marks

b) What is the function of an exitation table? Derive the J K flip-flop exitation table and explain the entries.

6 Marks

c) Design an ASM chart and state assignment for a decade counter.

4 Marks

d) Derive the individual J K input maps for this system.

6 Marks

Q3. a) Show how to construct a one bit ALU accepting 2 one bit inputs, A and B producing a one bit output, C, and performing the following functions:

Addition	AND
OR	NAND
XOR	NOT A
NOR	NOT B

16 Marks

b) Identify the logical unit and the decoder in the final circuit. Give an example of the circuit performing the XOR operation, showing the inputs and corresponding output values on your diagram.

4 Marks

Q4. a) What is a register? Describe the commonly used registers in a computer system.

6 Marks

b) Draw a flowchart illustrating the Fetch-Execute cycle of a CPU.

6 Marks

c) Demonstrate the operation of the Fetch-Execute cycle using as an example a simple 3-bus CPU with two general purpose registers (GPR'S).

8 Marks

Q5. a) What is cache memory? Explain the problem of cache consistency. What is the meaning of the terms 'hit ratio' and 'dirty bit'?

7 Marks

b) What is an interrupt? Explain the difference between internal, external, maskable and non-maskable interrupts.

7 Marks

b) "21st Century Technologies….will allow the possibility to create "artilects" (artificial intellects) with capacities many orders of magnitude above human levels. Humanity will have to decide whether artilects should be built. Humanity will probably be split on the issue. On the one hand building artilects is godlike, a magnificent endeavor, but risky. What if the artilects decide that humans are a pest?"

-Prof. Hugo de Garis, Former head: Brain Builder Group, Starlab, Brussels.

Do you consider the above opinions:- far fetched; frightening; a possibility? Elaborate.

6 Marks