

31	16	15	4	3	0
Timestamp [47:32]		Channel ID		Format bits	
Timestamp [31:16]		Timestamp [15:0]			
Index of Peakhigh value [15:0]		Peakhigh value [15:0]			
Information [7:0]		Accumulator sum of Gate 1 [23:0]			
"0000"	Accumulator sum of Gate 2 [27:0]				
"0000"	Accumulator sum of Gate 3 [27:0]				
"0000"	Accumulator sum of Gate 4 [27:0]				
"0000"	Accumulator sum of Gate 5 [27:0]				
"0000"	Accumulator sum of Gate 6 [27:0]				
"0000"	Accumulator sum of Gate 7 [27:0]				
"0000"	Accumulator sum of Gate 8 [27:0]				
"0000"	MAW maximum value [27:0]				
"0000"	MAW value before Trigger [27:0]				
"0000"	MAW value after/with Trigger [27:0]				
Start Energy value (Energy value from first value of Trigger Gate)					
Max. Energy value (during Trigger Gate active)					

If Format bit 0 = 1

If Format bit 1 = 1

If Format bit 2 = 1

If Format bit 3 = 1

31-28	27	26	25-0
0xE	MAW Test Flag	Status Flag	number of raw samples (x 2 samples, 32-bit words)

ADC raw data if number of raw samples != 0x0	sample 2	sample 1
	sample 4	sample 3
MAW Test data	sample N	sample N-1

Information [7:0]
- bit 7: Overflow flag
- bit 6: Underflow flag
- bit 5: RePileup flag
- bit 4: Pileup flag
- bit 5-0: reserved

Status Flag
until ADC FPGA Versions V0125-0009/V0250-0009
Status Flag = RePileup or Pileup Flag

Status Flag			
from ADC FPGA Versions V0125-000A/V0250-000A			
Internal Trigger enabled	External Trigger enabled	Pileup Trigger enabled	Status Flag
1	x	x	RePileup or Pileup
0	1	x	Internal Trigger
0	0	1	1