
STM32
CubeMX

1. Description

1.1. Project

Project Name	raptor
Board Name	NUCLEO-H723ZG
Generated with:	STM32CubeMX 6.10.0
Date	02/29/2024

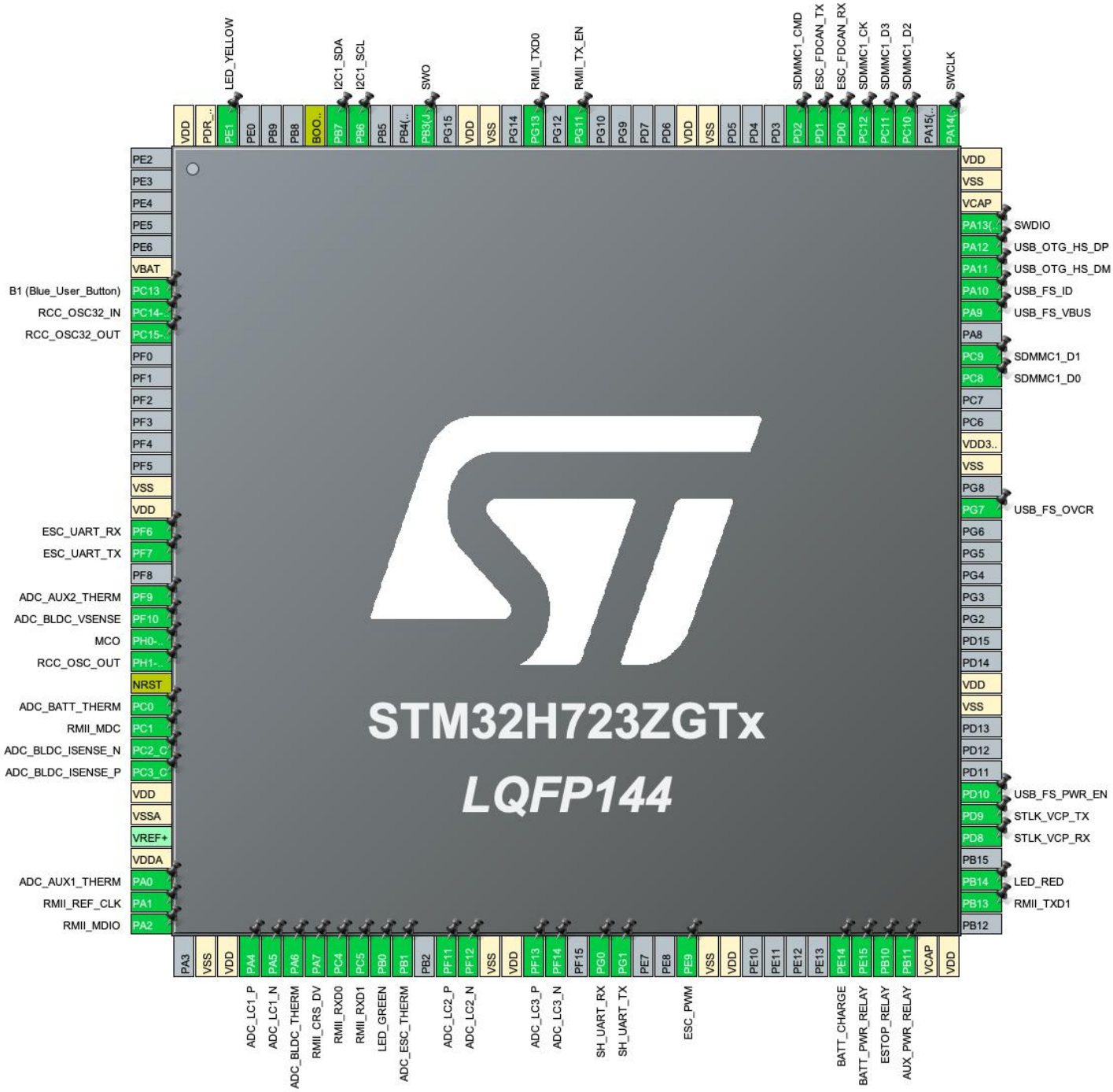
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H723/733
MCU name	STM32H723ZGTx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	Arm Cortex-M7

2. Pinout Configuration



3. Pins Configuration

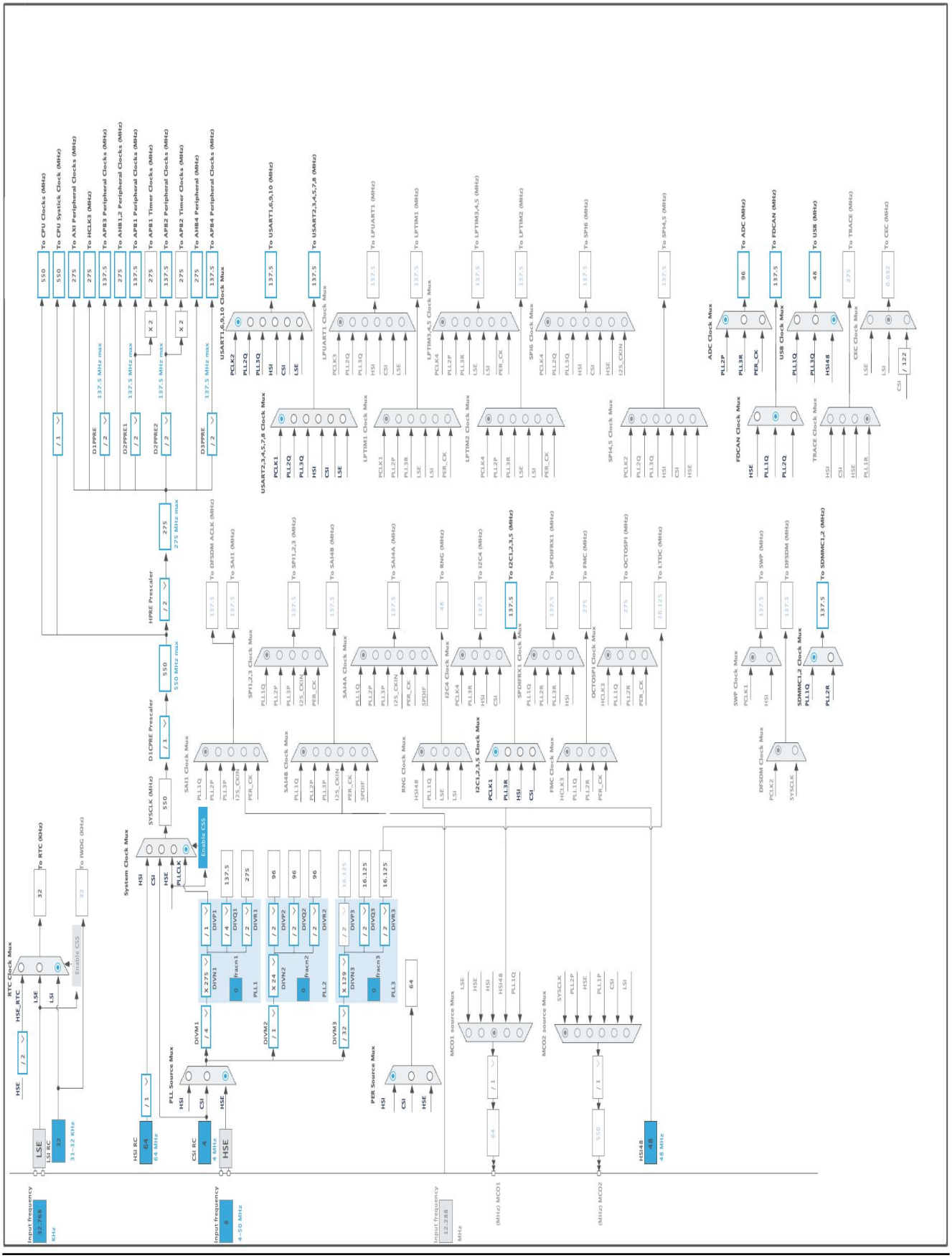
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
7	PC13 *	I/O	GPIO_Input	B1 (Blue_User_Button)
8	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
16	VSS	Power		
17	VDD	Power		
18	PF6	I/O	UART7_RX	ESC_UART_RX
19	PF7	I/O	UART7_TX	ESC_UART_TX
21	PF9	I/O	ADC3_INP2	ADC_AUX2_THERM
22	PF10	I/O	ADC3_INP6	ADC_BLDC_VSENSE
23	PH0-OSC_IN	I/O	RCC_OSC_IN	MCO
24	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
26	PC0	I/O	ADC1_INP10	ADC_BATT_THERM
27	PC1	I/O	ETH_MDC	RMII_MDC
28	PC2_C	I/O	ADC3_INN1	ADC_BLDC_ISENSE_N
29	PC3_C	I/O	ADC3_INP1	ADC_BLDC_ISENSE_P
30	VDD	Power		
31	VSSA	Power		
33	VDDA	Power		
34	PA0	I/O	ADC1_INP16	ADC_AUX1_THERM
35	PA1	I/O	ETH_REF_CLK	RMII_REF_CLK
36	PA2	I/O	ETH_MDIO	RMII_MDIO
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	ADC1_INP18	ADC_LC1_P
41	PA5	I/O	ADC1_INN18	ADC_LC1_N
42	PA6	I/O	ADC1_INP3	ADC_BLDC_THERM
43	PA7	I/O	ETH_CRS_DV	RMII_CRS_DV
44	PC4	I/O	ETH_RXD0	RMII_RXD0
45	PC5	I/O	ETH_RXD1	RMII_RXD1
46	PB0 *	I/O	GPIO_Output	LED_GREEN
47	PB1	I/O	ADC1_INP5	ADC_ESC_THERM
49	PF11	I/O	ADC1_INP2	ADC_LC2_P
50	PF12	I/O	ADC1_INN2	ADC_LC2_N
51	VSS	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
52	VDD	Power		
53	PF13	I/O	ADC2_INP2	ADC_LC3_P
54	PF14	I/O	ADC2_INN2	ADC_LC3_N
56	PG0	I/O	UART9_RX	SH_UART_RX
57	PG1	I/O	UART9_TX	SH_UART_TX
60	PE9	I/O	TIM1_CH1	ESC_PWM
61	VSS	Power		
62	VDD	Power		
67	PE14 *	I/O	GPIO_Output	BATT_CHARGE
68	PE15 *	I/O	GPIO_Output	BATT_PWR_RELAY
69	PB10 *	I/O	GPIO_Output	ESTOP_RELAY
70	PB11 *	I/O	GPIO_Output	AUX_PWR_RELAY
71	VCAP	Power		
72	VDD	Power		
74	PB13	I/O	ETH_TXD1	RMII_TXD1
75	PB14 *	I/O	GPIO_Output	LED_RED
77	PD8	I/O	USART3_TX	STLK_VCP_RX
78	PD9	I/O	USART3_RX	STLK_VCP_TX
79	PD10 *	I/O	GPIO_Output	USB_FS_PWR_EN
83	VSS	Power		
84	VDD	Power		
92	PG7	I/O	GPIO_EXTI7	USB_FS_OVCR
94	VSS	Power		
95	VDD33USB	Power		
98	PC8	I/O	SDMMC1_D0	
99	PC9	I/O	SDMMC1_D1	
101	PA9	I/O	USB_OTG_HS_VBUS	USB_FS_VBUS
102	PA10	I/O	USB_OTG_HS_ID	USB_FS_ID
103	PA11	I/O	USB_OTG_HS_DM	
104	PA12	I/O	USB_OTG_HS_DP	
105	PA13(JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	SWDIO
106	VCAP	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14(JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	SWCLK
111	PC10	I/O	SDMMC1_D2	
112	PC11	I/O	SDMMC1_D3	
113	PC12	I/O	SDMMC1_CK	
114	PD0	I/O	FDCAN1_RX	ESC_FDCAN_RX

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
115	PD1	I/O	FDCAN1_TX	ESC_FDCAN_TX
116	PD2	I/O	SDMMC1_CMD	
120	VSS	Power		
121	VDD	Power		
126	PG11	I/O	ETH_TX_EN	RMII_TX_EN
128	PG13	I/O	ETH_TXD0	RMII_TXD0
130	VSS	Power		
131	VDD	Power		
133	PB3(JTDO/TRACESWO)	I/O	DEBUG_JTDO-SWO	SWO
136	PB6	I/O	I2C1_SCL	
137	PB7	I/O	I2C1_SDA	
138	BOOT0	Boot		
142	PE1 *	I/O	GPIO_Output	LED_YELLOW
143	PDR_ON	Power		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	raptor
Project Folder	/Users/christiansargusingh/Projects/dronectl/raptor/cube
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.11.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_ETH_Init	ETH
4	MX_FDCAN1_Init	FDCAN1
5	MX_I2C1_Init	I2C1
6	MX_SDMMC1_SD_Init	SDMMC1
7	MX_TIM1_Init	TIM1
8	MX_UART7_Init	UART7
9	MX_UART9_Init	UART9
10	MX_USART3_UART_Init	USART3
11	MX_USB_OTG_HS_USB_Init	USB_OTG_HS

Rank	Function Name	Peripheral Instance Name
12	MX_ADC1_Init	ADC1
13	MX_ADC2_Init	ADC2
14	MX_ADC3_Init	ADC3
15	MX_RTC_Init	RTC

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32H7
Line	STM32H723/733
MCU	STM32H723ZGTx
Datasheet	DS13313_Rev1

1.2. Parameter Selection

Temperature	25
Vdd	3.0

1.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

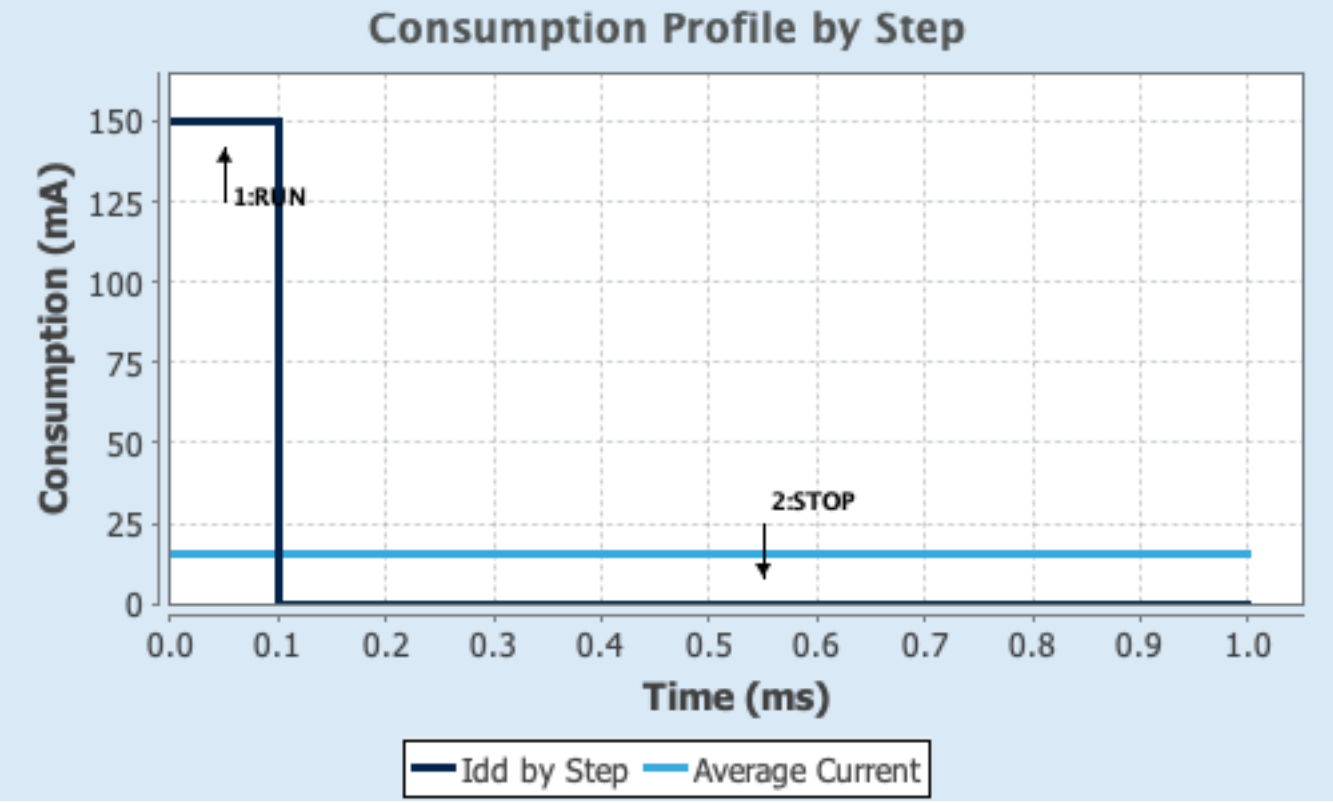
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0: Scale0/Boost	SVOS5: System-Scale5
D1 Mode	DRUN	DSTANDBY
D2 Mode	DRUN	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	SRAM1/FlashMode-ON/Cache	NA
CPU Frequency	550 MHz	0 Hz
Clock Configuration	HSE BYP PLL	ALL_CLOCKS_OFF
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	150 mA	94.5 µA
Duration	0.1 ms	0.9 ms
DMIPS	1177.0	0.0
Ta Max	105.2	124.99
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	15.09 mA
Battery Life	1 day, 17 hours	Average DMIPS	1177.0 DMIPS

1.6. Chart


Consumption Profile by Step
Consumption (mA)
150
125
100
75
50
25
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

2. Peripherals and Middlewares Configuration

2.1. ADC1

IN2: IN2 Differential

IN3: IN3 Single-ended

IN5: IN5 Single-ended

IN10: IN10 Single-ended

IN16: IN16 Single-ended

IN18: IN18 Differential

2.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Left Bit Shift	No bit shift
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 2
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset Signed Saturation	Disable

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

2.2. ADC2

IN2: IN2 Differential

2.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Left Bit Shift	No bit shift
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 2
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset Signed Saturation	Disable

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

2.3. ADC3
IN1: IN1 Differential
IN2: IN2 Single-ended
mode: IN6

2.3.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 12-bit resolution
Scan Conversion Mode	Disabled
Data Alignment	Right alignment
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Left Bit Shift	No bit shift
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Sampling Mode	Normal
Rank	1
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset
Offset Sign	Offset Sign Negative

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

2.4. DEBUG

Debug: Trace Asynchronous Sw

2.5. ETH

Mode: RMII

2.5.1. Parameter Settings:

General : Ethernet Configuration:

Warning	The ETH can work only when RAM is pointing at 0x24000000
Ethernet MAC Address	00:80:E1:00:00:00
Tx Descriptor Length	4
First Tx Descriptor Address	**0x30000200 ***
Rx Descriptor Length	4
First Rx Descriptor Address	**0x30000000 ***
Rx Buffers Length	1524

2.6. FDCAN1

mode: Activated

2.6.1. Parameter Settings:

Basic Parameters:

Frame Format	Classic mode
Mode	Normal mode
Auto Retransmission	Disable
Transmit Pause	Disable
Protocol Exception	Disable
Nominal Sync Jump Width	1
Data Prescaler	1
Data Sync Jump Width	1
Data Time Seg1	1
Data Time Seg2	1
Message Ram Offset	0
Std Filters Nbr	0
Ext Filters Nbr	0

Rx Fifo0 Elmts Nbr	0
Rx Fifo0 Elmt Size	8 bytes data field
Rx Fifo1 Elmts Nbr	0
Rx Fifo1 Elmt Size	8 bytes data field
Rx Buffers Nbr	0
Rx Buffer Size	8 bytes data field
Tx Events Nbr	0
Tx Buffers Nbr	0
Tx Fifo Queue Elmts Nbr	0
Tx Fifo Queue Mode	FIFO mode
Tx Elmt Size	8 bytes data field

Clock Calibration Unit:

Clock Calibration	Disable

Bit Timings Parameters:

Nominal Prescaler	16
Nominal Time Quantum	**116.36363636363636 ***
Nominal Time Seg1	2
Nominal Time Seg2	2
Nominal Time for one Bit	**581 ***
Nominal Baud Rate	**1718750 ***

2.7. I2C1

I2C: I2C

2.7.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x60404E72 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled

Primary slave address	0

2.8. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

2.8.1. Parameter Settings:

Power Parameters:

SupplySource	PWR_LDO_SUPPLY
Power Regulator Voltage Scale	Power Regulator Voltage Scale 0

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	64

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	3 WS (4 CPU cycle)

PLL range Parameters:

PLL1 input frequency range	Between 2 and 4 MHz
PLL2 input frequency range	Between 8 and 16 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	Wide VCO range

2.9. RTC

mode: Activate Clock Source

2.9.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

2.10. SDMMC1

Mode: SD 4 bits Wide bus

2.10.1. Parameter Settings:

SDMMC parameters:

Clock transition on which the bit capture is made	Rising transition
SDMMC Clock output enable when the bus is idle	Disable the power save for the clock
SDMMC hardware flow control	The hardware control flow is disabled
SDMMC clock divide factor	0
Is external transceiver present ?	no

2.11. SYS

Timebase Source: TIM2

2.12. TIM1

Channel1: PWM Generation CH1

2.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable

BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

2.13. UART7

Mode: Asynchronous

2.13.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

2.14. UART9

Mode: Asynchronous

2.14.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

2.15. USART3

Mode: Asynchronous

2.15.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

2.16. USB_OTG_HS

Internal FS Phy: OTG/Dual_Role_Device

Activate_VBUS: Activate-VBUS

2.17. FREERTOS

Interface: CMSIS_V2

2.17.1. Config parameters:

API:

FreeRTOS API	CMSIS v2

Versions:

FreeRTOS version	10.3.1

CMSIS-RTOS version	2.00

MPU/FPU:

ENABLE_MPU	Disabled
ENABLE_FPU	Disabled

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	56
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Enabled
USE_COUNTING_SEMAPHORES	Enabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Disabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Enabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Enabled

TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	256

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

CMSIS-RTOS V2 flags:

USE_OS2_THREAD_SUSPEND_RESUME	Enabled
USE_OS2_THREAD_ENUMERATE	Enabled
USE_OS2_EVENTFLAGS_FROM_ISR	Enabled
USE_OS2_THREAD_FLAGS	Enabled
USE_OS2_TIMER	Enabled
USE_OS2_MUTEX	Enabled

2.17.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Enabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Enabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Enabled
xTaskGetCurrentTaskHandle	Enabled
eTaskGetState	Enabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Enabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

2.17.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT	**Enabled ***

Project settings (see parameter description first):

Use FW pack heap file	Enabled

*** User modified value**

3. System Configuration

3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_INP10	Analog mode	No pull-up and no pull-down	n/a	ADC_BATT_THERM
	PA0	ADC1_INP16	Analog mode	No pull-up and no pull-down	n/a	ADC_AUX1_THERM
	PA4	ADC1_INP18	Analog mode	No pull-up and no pull-down	n/a	ADC_LC1_P
	PA5	ADC1_INN18	Analog mode	No pull-up and no pull-down	n/a	ADC_LC1_N
	PA6	ADC1_INP3	Analog mode	No pull-up and no pull-down	n/a	ADC_BLDC_THERM
	PB1	ADC1_INP5	Analog mode	No pull-up and no pull-down	n/a	ADC_ESC_THERM
	PF11	ADC1_INP2	Analog mode	No pull-up and no pull-down	n/a	ADC_LC2_P
	PF12	ADC1_INN2	Analog mode	No pull-up and no pull-down	n/a	ADC_LC2_N
ADC2	PF13	ADC2_INP2	Analog mode	No pull-up and no pull-down	n/a	ADC_LC3_P
	PF14	ADC2_INN2	Analog mode	No pull-up and no pull-down	n/a	ADC_LC3_N
ADC3	PF9	ADC3_INP2	Analog mode	No pull-up and no pull-down	n/a	ADC_AUX2_THERM
	PF10	ADC3_INP6	Analog mode	No pull-up and no pull-down	n/a	ADC_BLDC_VSENSE
	PC2_C	ADC3_INN1	Analog mode	No pull-up and no pull-down	n/a	ADC_BLDC_ISENSE_N
	PC3_C	ADC3_INP1	Analog mode	No pull-up and no pull-down	n/a	ADC_BLDC_ISENSE_P
DEBUG	PA13(JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	SWDIO
	PA14(JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	SWCLK
	PB3(JTDO/TRACESWO)	DEBUG_JTDO-SWO	n/a	n/a	n/a	SWO
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	Low	RMII_MDC
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	RMII_REF_CLK
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	Low	RMII_MDIO
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	Low	RMII_CRS_DV
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low	RMII_RXD0
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low	RMII_RXD1
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low	RMII_TXD1
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	Low	RMII_TX_EN
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low	RMII_TXD0
FDCAN1	PD0	FDCAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	ESC_FDCAN_RX
	PD1	FDCAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	ESC_FDCAN_TX
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PB7	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	MCO
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SDMMC1	PC8	SDMMC1_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC9	SDMMC1_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC10	SDMMC1_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SDMMC1_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SDMMC1_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDMMC1_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
TIM1	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	ESC_PWM
UART7	PF6	UART7_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	ESC_UART_RX
	PF7	UART7_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	ESC_UART_TX
UART9	PG0	UART9_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	SH_UART_RX
	PG1	UART9_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	SH_UART_TX
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	STLK_VCP_RX
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	STLK_VCP_TX
USB_OTG_HS	PA9	USB_OTG_HS_VBUS	Input mode	No pull-up and no pull-down	n/a	USB_FS_VBUS
	PA10	USB_OTG_HS_ID	Alternate Function Push Pull	No pull-up and no pull-down	Low	USB_FS_ID
	PA11	USB_OTG_HS_DM	n/a	n/a	n/a	
	PA12	USB_OTG_HS_DP	n/a	n/a	n/a	
GPIO	PC13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	B1 (Blue_User_Button)
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_GREEN
	PE14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BATT_CHARGE
	PE15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BATT_PWR_RELAY
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ESTOP_RELAY
	PB11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	AUX_PWR_RELAY
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_RED
	PD10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_FS_PWR_EN
	PG7	GPIO_EXTI7	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	USB_FS_OVCR
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_YELLOW

3.2. DMA configuration

nothing configured in DMA service

3.3. BDMA configuration

nothing configured in DMA service

3.4. MDMA configuration

nothing configured in DMA service

3.5. NVIC configuration

3.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
TIM2 global interrupt	true	15	0
PVD/AVD through EXTI Line detection Interrupt	unused		
Tamper and TimeStamp interrupts through the EXTI line	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
FDCAN1 interrupt 0	unused		
FDCAN1 interrupt 1	unused		
EXTI line[9:5] interrupts	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
USART3 global interrupt	unused		
SDMMC1 global interrupt	unused		
Ethernet global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 86	unused		
FDCAN calibration unit interrupt	unused		
FPU global interrupt	unused		
UART7 global interrupt	unused		
HSEM1 global interrupt	unused		
ADC3 global interrupt	unused		
UART9 global interrupt	unused		

3.5.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
TIM2 global interrupt	false	true	true

*** User modified value**

4. System Views

4.1. Category view

4.1.1. Current

5. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32h7_bsdl.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip
System View Description	https://www.st.com/resource/en/svd/stm32h7-svd.zip
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h7_series_product_overview.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h72x-3x_line_product-overview.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf
Brochures	https://www.st.com/resource/en/brochure/brstm32h7.pdf
Brochures	https://www.st.com/resource/en/brochure/brstm32h7vl.pdf
Brochures	https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32nucleo.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32trust.pdf
Application Notes	https://www.st.com/resource/en/application_note/an1181-electrostatic-discharge-sensitivity-measurement-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2606-stm32-

	microcontroller-system-memory-boot-mode-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2639-soldering-recommendations-and-package-information-for-leadfree-ecopack-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2867-oscillator-design-guide-for-stm8afals-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3126-audio-and-waveform-generation-using-the-dac-in-stm32-products-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3155-usart-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3156-usb-dfu-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4013-stm32-crossseries-timer-overview-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4221-i2c-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4229-how-to-implement-a-vocoder-solution-using-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4277-using-stm32-device-pwm-shutdown-features-for-motor-control-and-digital-power-conversion-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4286-spi-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4566-extending-the-dac-performance-of-stm32-microcontrollers-stmicroelectronics.pdf
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Application Notes	https://www.st.com/resource/en/application_note/an4655-virtually-increasing-the-number-of-serial-communication-peripherals-in-stm32-applications-stmicroelectronics.pdf

Application Notes	https://www.st.com/resource/en/application_note/an4750-handling-of-soft-errors-in-stm32-applications-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4759-using-the-hardware-realtime-clock-rtc-and-the-tamper-management-unit-tamp-with-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4776-generalpurpose-timer-cookbook-for-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4803-highspeed-si-simulations-using-ibis-and-boardlevel-simulations-using-hyperlynx-si-on-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4839-level-1-cache-on-stm32f7-series-and-stm32h7-series-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4861-lcdtft-display-controller-ltdc-on-stm32-mcus-stmicroelectronics.pdf
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Application Notes	https://www.st.com/resource/en/application_note/an5020-digital-camera-interface-dcmi-on-stm32-mcus-stmicroelectronics.pdf
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Application Notes	https://www.st.com/resource/en/application_note/an5033-stm32cube-mcu-package-examples-for-stm32h7-series-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5036-thermal-management-guidelines-for-stm32-applications-stmicroelectronics.pdf
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	audio-stream-with-the-stm32f4f7h7-series-stmicroelectronics.pdf
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Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an4841-digital-signal-processing-for-stm32-microcontrollers-using-cmsis-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an4891-stm32h72x-stm32h73x-and-singlecore-stm32h74x75x-system-architecture-and-performance-stmicroelectronics.pdf
Application Notes for related Tools	https://www.st.com/resource/en/application_note/an5001-stm32cube-expansion-package-for-stm32h7-series-mdma-stmicroelectronics.pdf

& Software	
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5014-stm32h7x3-smart-power-management-expansion-package-for-stm32cube-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5033-stm32cube-mcu-package-examples-for-stm32h7-series-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5054-secure-programming-using-stm32cubeprogrammer-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5056-integration-guide-for-the-xcubesbsfu-stm32cube-expansion-package-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5360-getting-started-with-projects-based-on-the-stm32mp1-series-in-stm32cubeide-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5361-getting-started-with-projects-based-on-dualcore-stm32h7-microcontrollers-in-stm32cubeide-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5394-getting-started-with-projects-based-on-the-stm32l5-series-in-stm32cubeide-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5418-how-to-build-a-simple-usbpd-sink-application-with-stm32cubemx-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5426-migrating-graphics-middleware-projects-from-stm32cubemx-540-to-stm32cubemx-550-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5534-stm32h735gdk-firmware-upgrade-for-atbased-emw3080-wifi-module-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5564-getting-started-with-projects-based-on-dualcore-stm32wl-microcontrollers-in-stm32cubeide-stmicroelectronics.pdf

Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an4865-lowpower-timer-lptim-applicative-use-cases-on-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5698-adapting-the-xcubestl-functional-safety-package-for-stm32-iec-61508-compliant-to-other-safety-standards-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5731-stm32cubemx-and-stm32cubeide-threadsafe-solution-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5450-stm32h7a37b3-lines-and-stm32h7b0-value-line-smart-power-management-expansion-package-for-stm32cube-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an4502-stm32-smbuspmbus-expansion-package-for-stm32cube-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5952-how-to-use-cmake-in-stm32cubeide-stmicroelectronics.pdf
Design Notes & Tips	https://www.st.com/resource/en/design_tip/dt0117-microphone-array-beamforming-in-the-pcm-and-pdm-domain-stmicroelectronics.pdf
Errata Sheets	https://www.st.com/resource/en/errata_sheet/es0491-stm32h72xx73xx-device-errata-stmicroelectronics.pdf
Datasheet	https://www.st.com/resource/en/datasheet/dm00701028.pdf
Programming Manuals	https://www.st.com/resource/en/programming_manual/pm0253-stm32f7-series-and-stm32h7-series-cortexm7-processor-programming-manual-stmicroelectronics.pdf
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Technical Notes & Articles	https://www.st.com/resource/en/technical_note/tn1163-description-of-wlcsp-for-microcontrollers-and-recommendations-for-its-use-stmicroelectronics.pdf
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